**MOSFET Lab – Scaling**

**(** <http://nanohub.org/tools/mosfet> )

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**Problem Background**

You are head of a semiconductor company involved in fabricating chips. To be competitive you need to scale the MOSFET channel length every year according to the following table.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Time** | **Year 1** | **Year 2** | **Year 3** | **Year 4** | **Year 5** |
| **Channel Length** | **100 nm** |  **75 nm** |  **50 nm** |  **30 nm** |  **15 nm** |

 Your process engineering team has developed the capability to fabricate **Bulk** MOSFET, Ultra thin body **(UTB)** Silicon on Insulator (SOI) MOSFET and Double Gate **(DG)** MOSFET with increasing order of complexity.

**tox=2 nm**

 Bulk mosfet

**tc=20 nm**

**tox=1 nm**

**tc=10 nm**

 Ultra thin body (UTB) Silicon on Insulator (SOI) mosfet

**BOX**

**tox=1 nm**

**tox=1 nm**

**tc=10 nm**

 Double Gate MOSFET.

Use the following specifications for all the three types,

Channel doping (uniform doping) =1018 /cm3

Source/Drain doping (uniform doping) =2x1020 /cm3

Drain bias, Vd=0.8V

T=300K

For the devices and the chip to behave faithfully it is important that drain induced barrier lowering (DIBL) is controlled. DIBL should be below 100 mV/dec for the chip to perform well.(You may need not worry about Ion/Ioff ratio for now.

Q1) As the head of the company you need to decide which process technology (Bulk/UTB/DG) will be able to deliver the chip performance for each year with minimum complexity. (You need to design for NMOS only).

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| --- | --- | --- | --- | --- | --- |
| **Time** | **Year 1** | **Year 2** | **Year 3** | **Year 4** | **Year 5** |
| **Channel Length** | **100 nm** | **75 nm** | **50 nm** | **30 nm** | **15 nm** |
| **Process Technology** | **?** | **?** | **?** | **?** | **?** |

 Q2) Do you have a solution for Year 5 (L=15nm). If you could scale SiO2 thickness till tox=0.2 nm can you still be competitive.