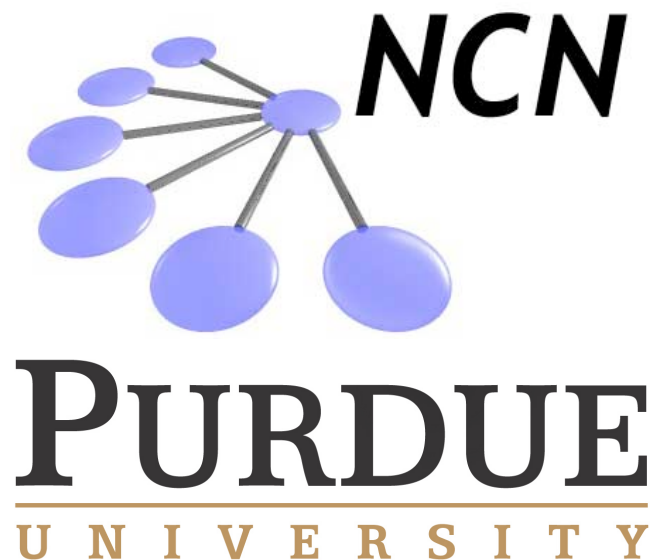


Network for Computational Nanotechnology (NCN)

UC Berkeley, Univ. of Illinois, Norfolk State, Northwestern, Purdue, UTEP

First-Time User Guide to OMEN Nanowire**



**Sung Geun Kim*, Saumitra R. Mehrotra,
Ben Haley, Mathieu Luisier, Gerhard Klimeck**
Network for Computational Nanotechnology (NCN)
Electrical and Computer Engineering

*kim568@purdue.edu

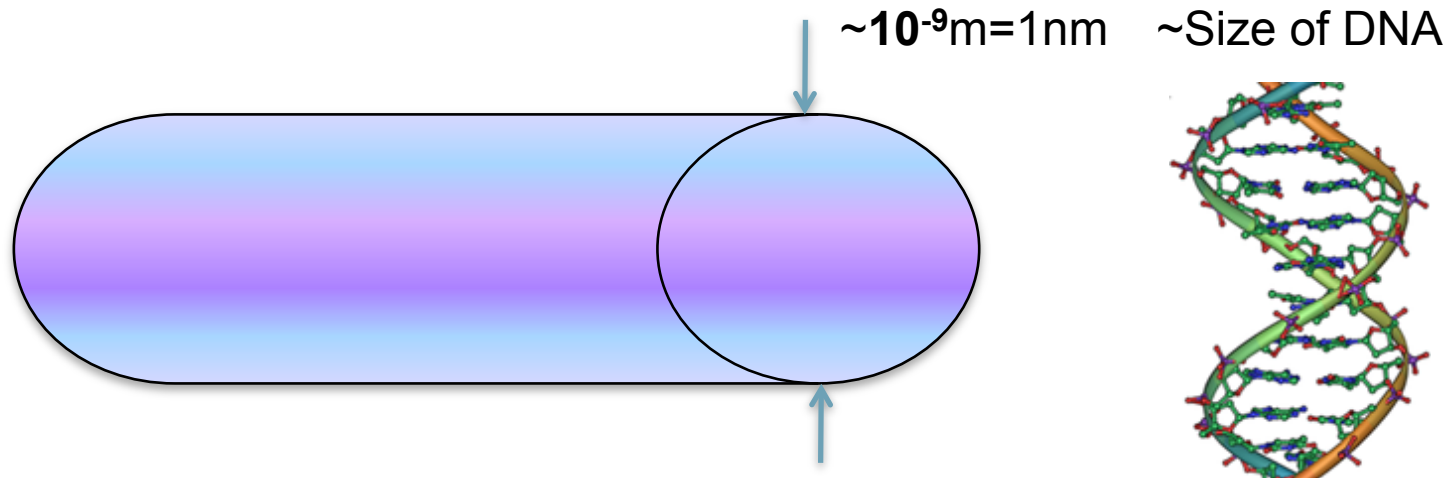
** <https://nanohub.org/resources/5359>

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Introduction: What is a Nanowire?

nanowire: wire-like structure with diameter or lateral dimension of nanometer(10^{-9}m)



<http://en.wikipedia.org/wiki/DNA>

→ Various material systems can be used to fabricate nanowires.
For example: silver, gold, copper, ..., etc. (metal)
Si, Ge, GaAs, GaN, ..., etc. (semiconductor)

What is a Nanowire?

Application of nanowires

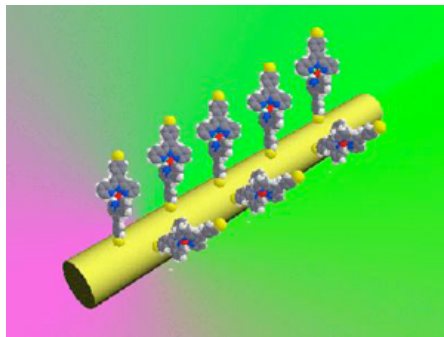


Fig. 1 **Nanowire memory cell

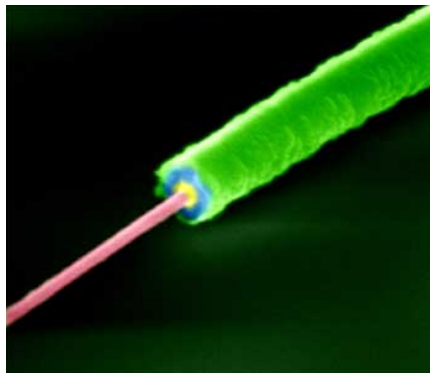


Fig. 2 ***Nanowire LED

B. Tian, Lieber Group, Harvard University

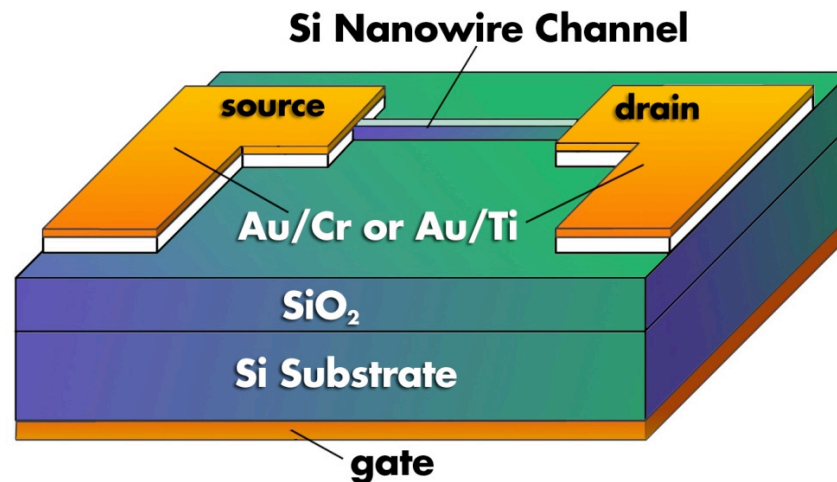


Fig. 3 Nanowire FET

National Institute of Standards and Technology

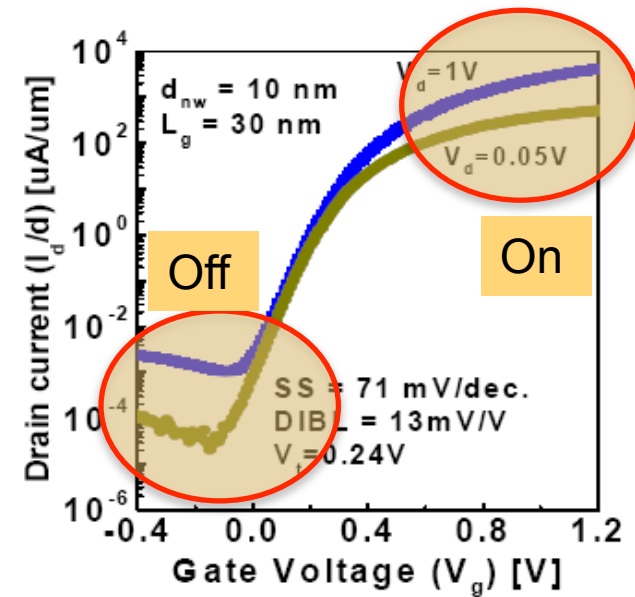
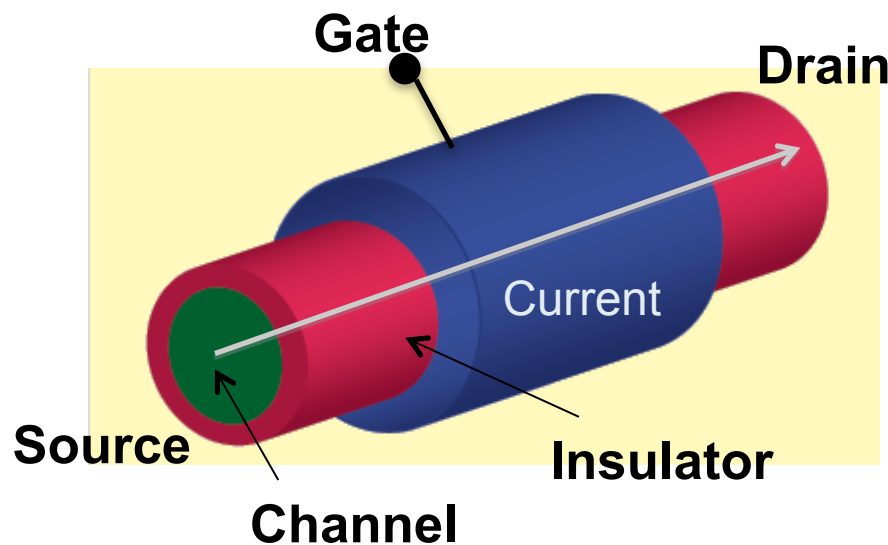
Fig 1. http://www.eurekalert.org/pub_releases/2004-04/uosc-spn042004.php

Fig 2. <http://www.spectrum.ieee.org/oct07/5642>

Fig 3. http://www.nist.gov/public_affairs/techbeat/tb2005_0630.htm#transistors

What is a Nanowire FET?

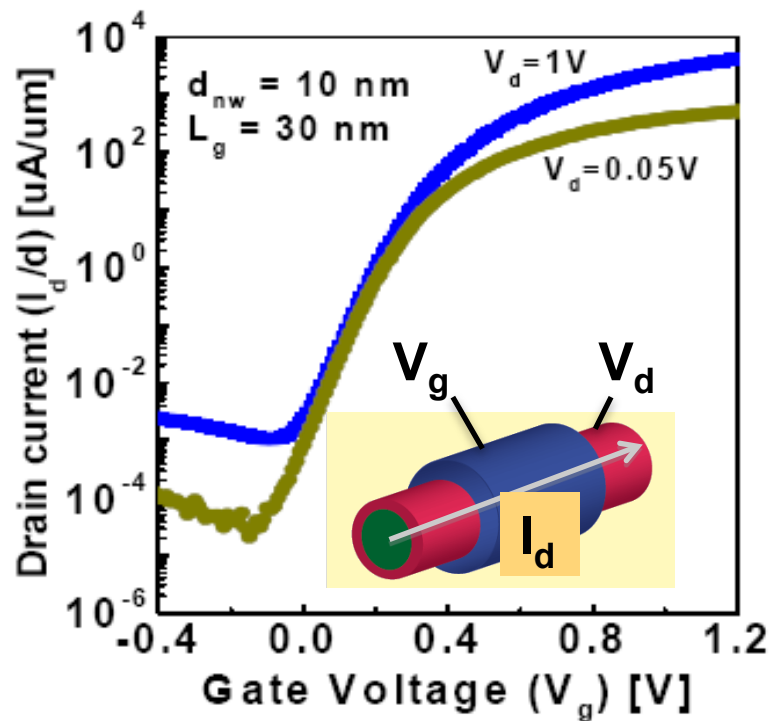
nanowire FET: field effect transistor(FET) using nanowire



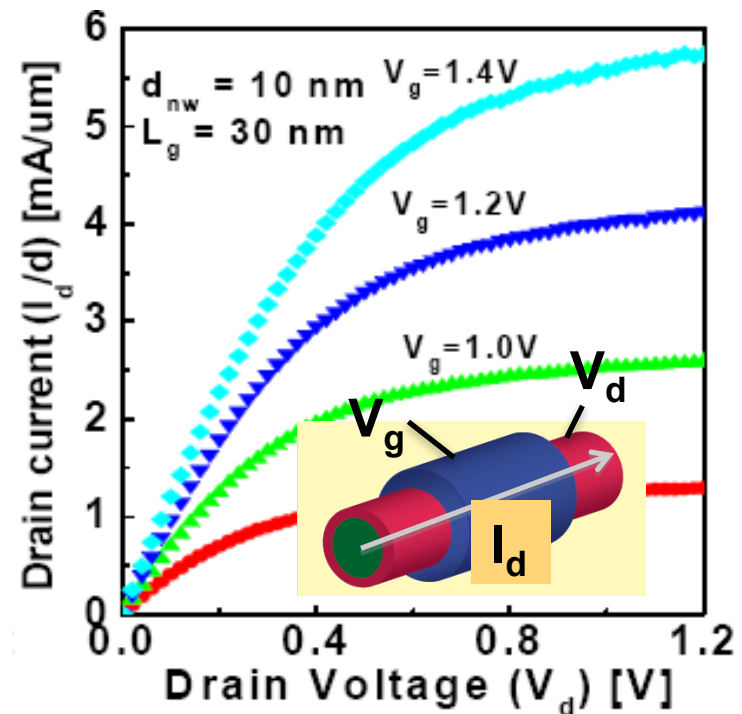
- » The current from the source to the drain is turned on and off by the voltage applied to the gate.
- » Because the gate in nanowires is surrounding the channel, it can control the electrostatics of the channel more efficiently than the conventional MOSFET.

What Can Be Measured in a Nanowire FET?

IV Characteristics^[1](I_d - V_g , I_d - V_d)



(a) I_d - V_g



(b) I_d - V_d

[1] Sung Dae Suk, et. al., IEDM, 2005, "High Performance 5nm radius Twin Silicon Nanowire MOSFET(TSNWFET) : Fabrication on Bulk Si Wafer, Characteristics, and Reliability

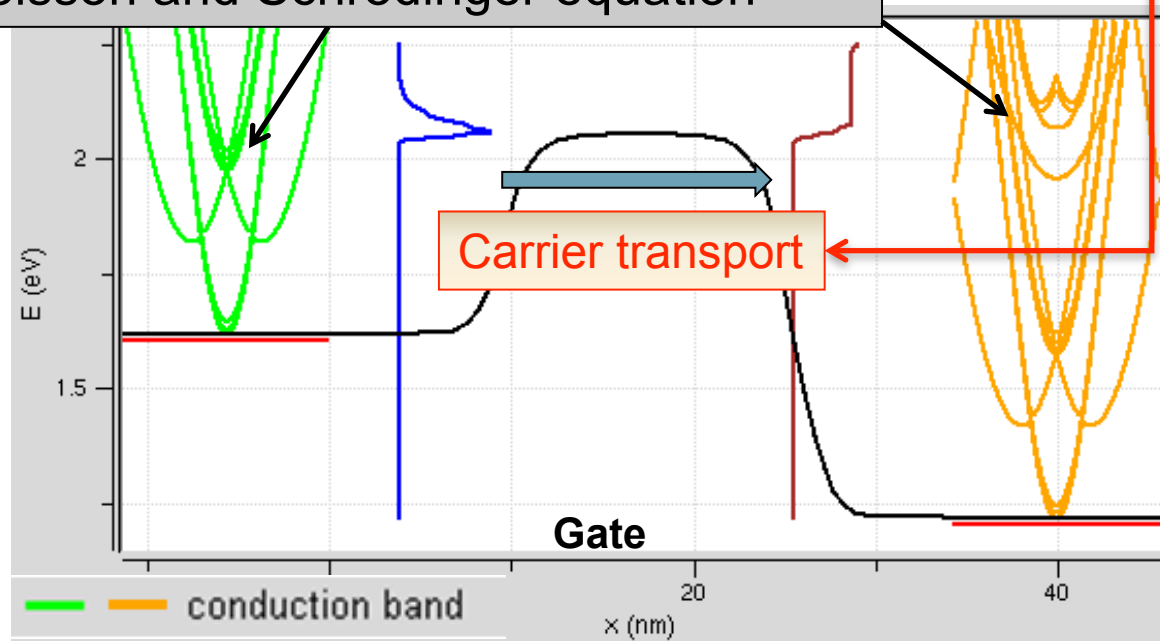
What is OMEN?

OMEN^[3,4] : atomistic full-band quantum transport simulator

Atomistic description of bandstructure
– sp³d⁵s* tight binding model
+3D Poisson and Schrodinger equation ^[3,4]

Wave Function Approach^[3,4]

Source



Drain

Carrier transport

[3] Mahieu Luisier, et. al., Physical Review B, 2006

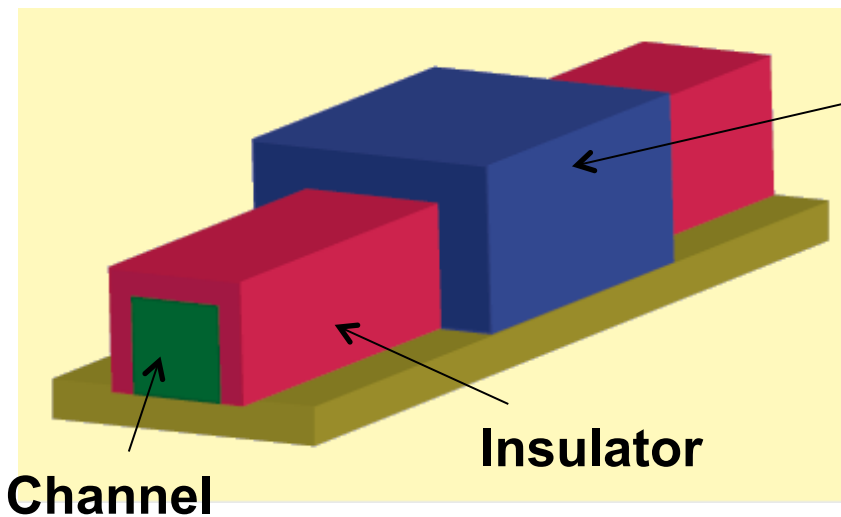
[4] <http://cobweb.ecn.purdue.edu/~gekco/omen/index.html>

What Can Be Simulated by OMEN Nanowire?

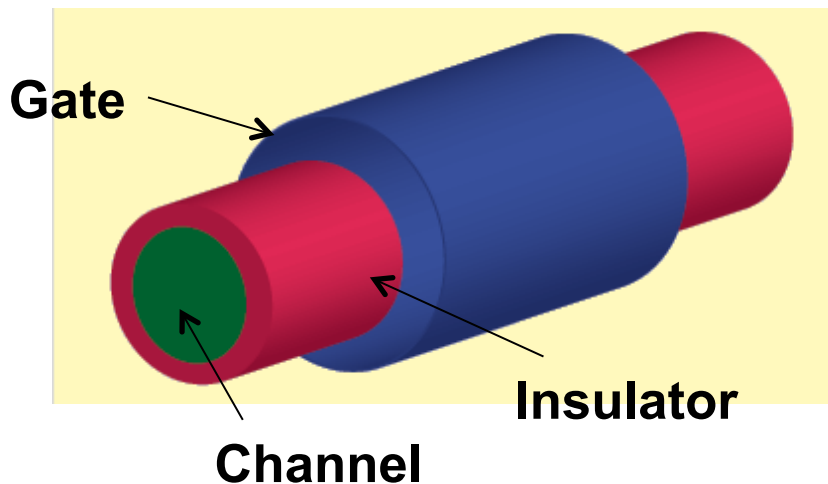
Device Type

OMEN Nanowire can simulate nanowire FETs of different types. You can choose between a rectangular nanowire and a circular nanowire.

Rectangular Nanowire



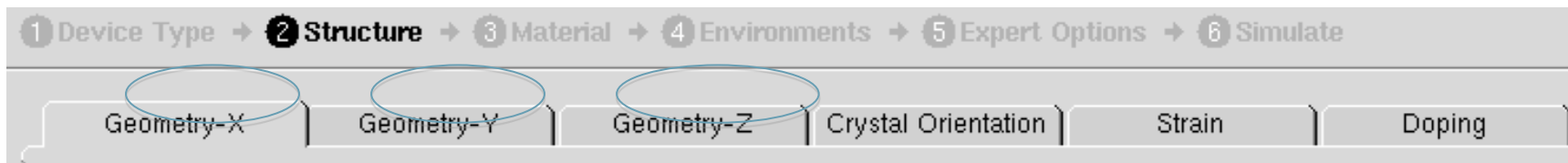
Circular Nanowire



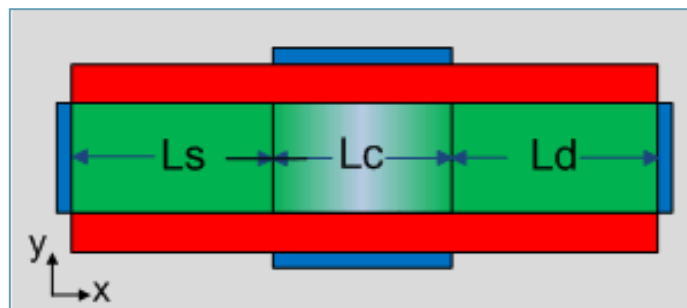
What Can Be Simulated by OMEN Nanowire?

Device Structure - Geometry

Nanowire FETs of various sizes

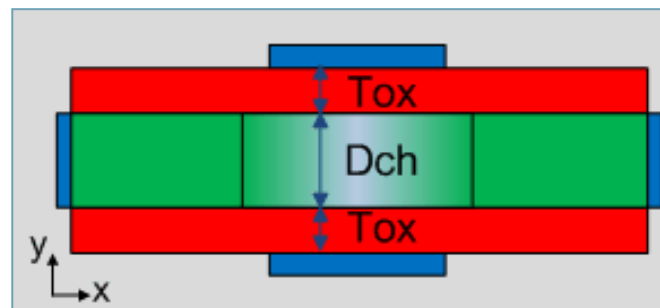


Geometry-X



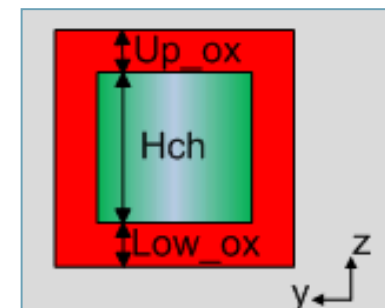
Channel length - L_c : **15nm**
Source length - L_s : **10nm**
Drain length - L_d : **10nm**

Geometry-Y



Diameter - D_{ch} : **3nm**
Oxide thickness - T_{ox} : **1nm**

Geometry-Z

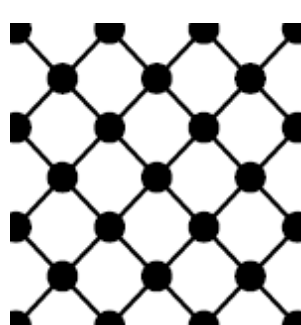
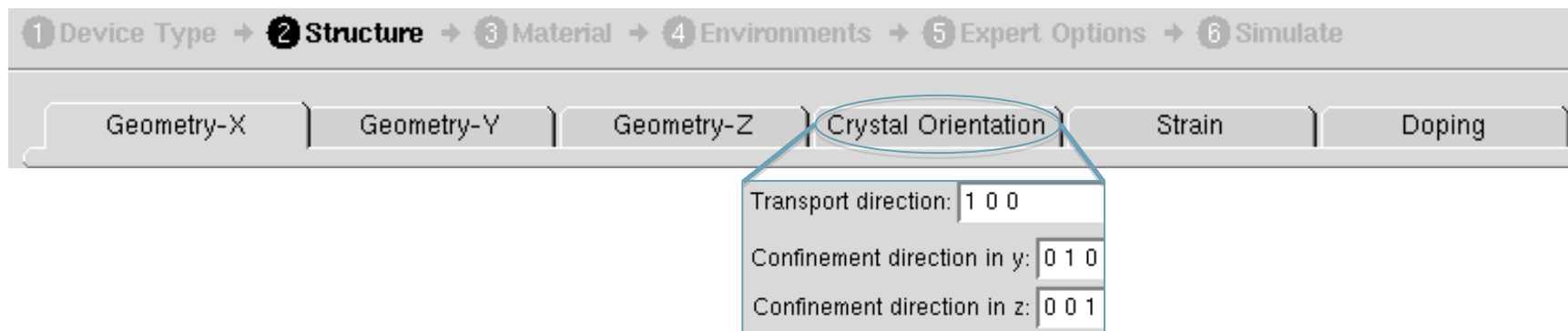


Channel height - H_{ch} : **2nm**
Upper oxide thickness - Up_{ox} : **1nm**
Lower oxide thickness - Low_{ox} : **1nm**

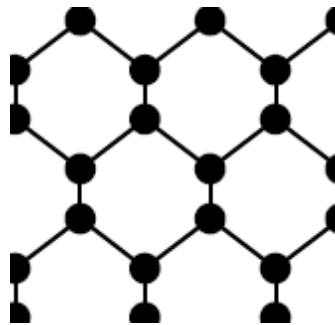
What Can Be Simulated by OMEN Nanowire?

Device Structure – Crystal Orientation

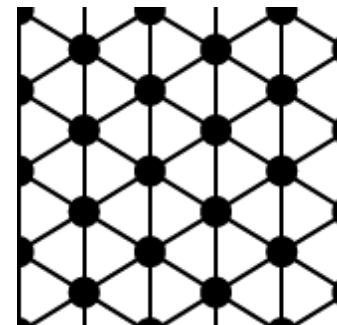
Nanowire FETs of different crystal orientation



(a) [100]



(b) [110]



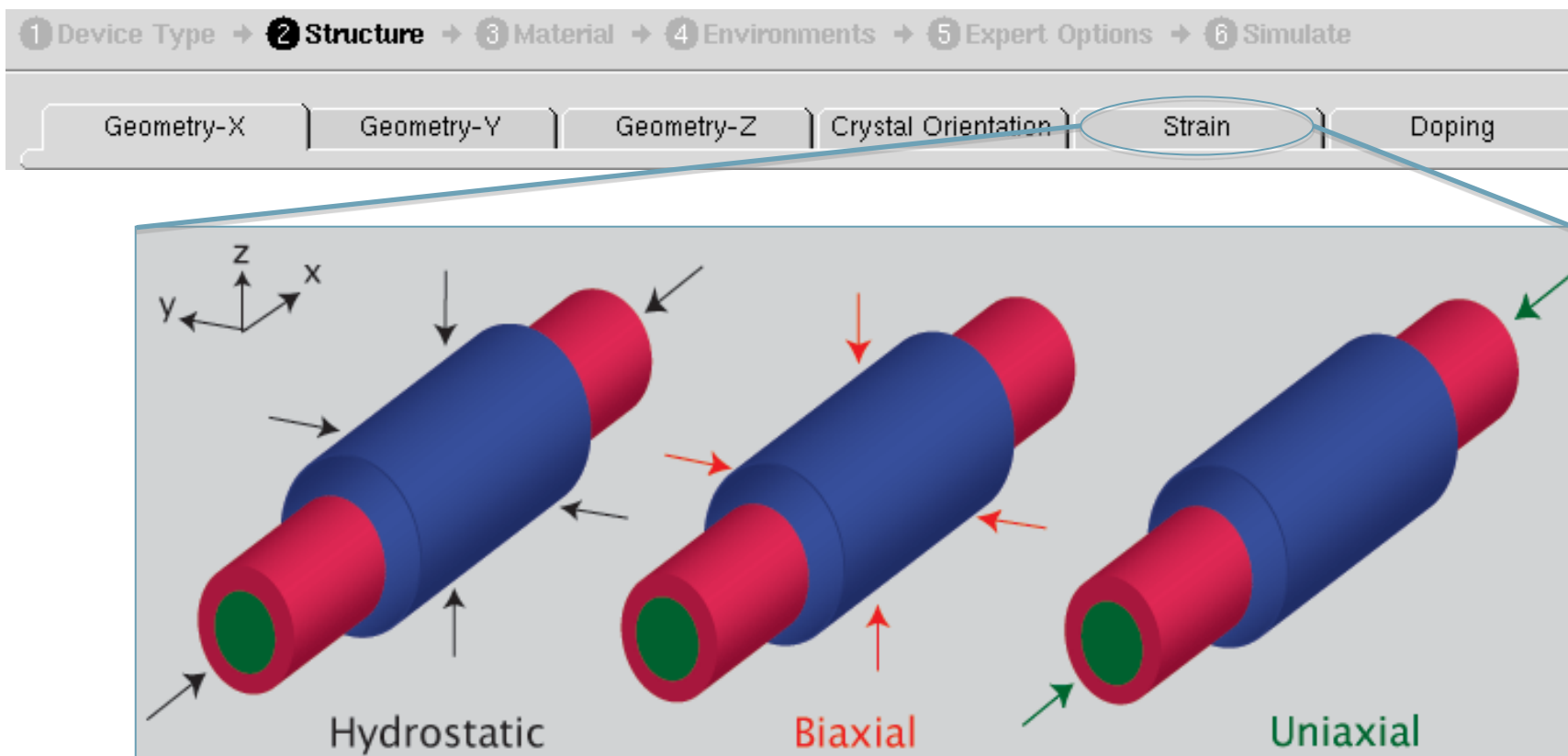
(c) [111]

cross-section of the nanowire with transport direction^[3] (a) [100], (b) [110], (c) [111]

What Can Be Simulated by OMEN Nanowire?

Device Structure - Strain

Nanowire FETs with strain



What Can Be Simulated by OMEN Nanowire?

Material/Environment

OMEN Nanowire can simulate nanowire FETs of different material and environment parameters.

1 Device Type → 2 Structure → 3 Material → 4 Environments → 5 Expert Options → 6 Simulate

Gate
Insulator
Channel

Gate bias | Drain bias | Source bias | Temperature | Plot options for bias

Channel material: Si

Channel material characteristics

Dielectric constant of channel:	11.9
Affinity of channel material:	4.05eV
Dielectric constant of insulator:	3.9
Gate contact work function:	4.25eV

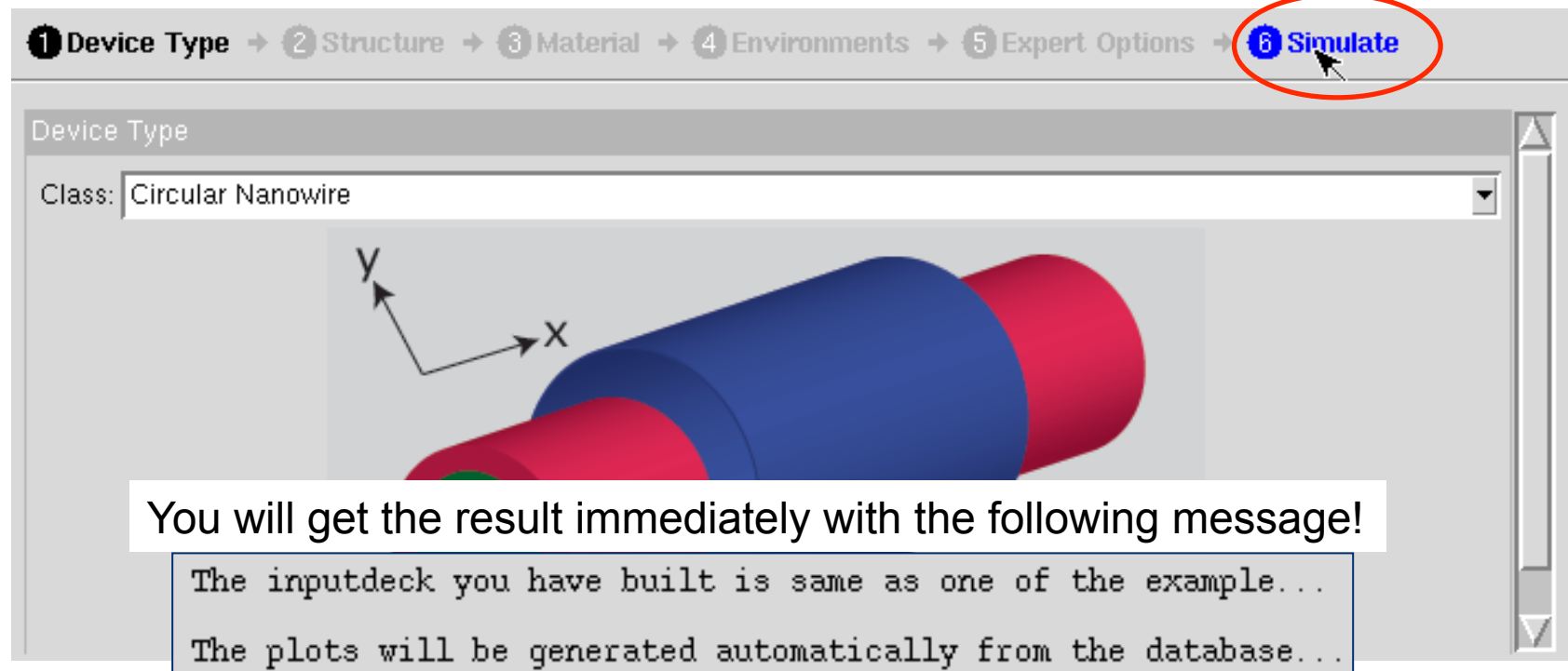
Minimum bias: $-1\frac{1}{2}$ 0V

Maximum bias: $-1\frac{1}{2}$ 0.6V

Number of bias points: 13

Diagram showing a nanowire FET structure with a coordinate system (x, y) and gate voltages V_g .

What If You Just Hit “Simulate”?

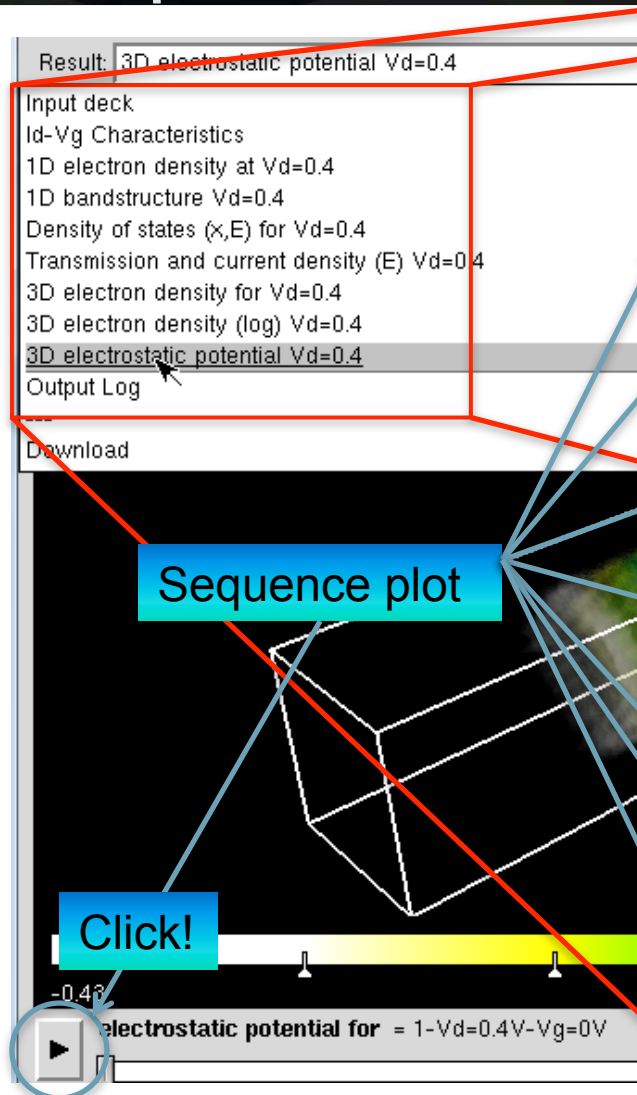


- To submit a new simulation, change other input parameters such as the structure, material, environment parameters. The estimated walltime/memory usage[5] to run the simulation will post after “Simulate” is clicked.

[5]

http://cobweb.ecn.purdue.edu/~gekco/students/SungGeunKim/SungGeunKim_OMENNanowire_time_table.html

Outputs

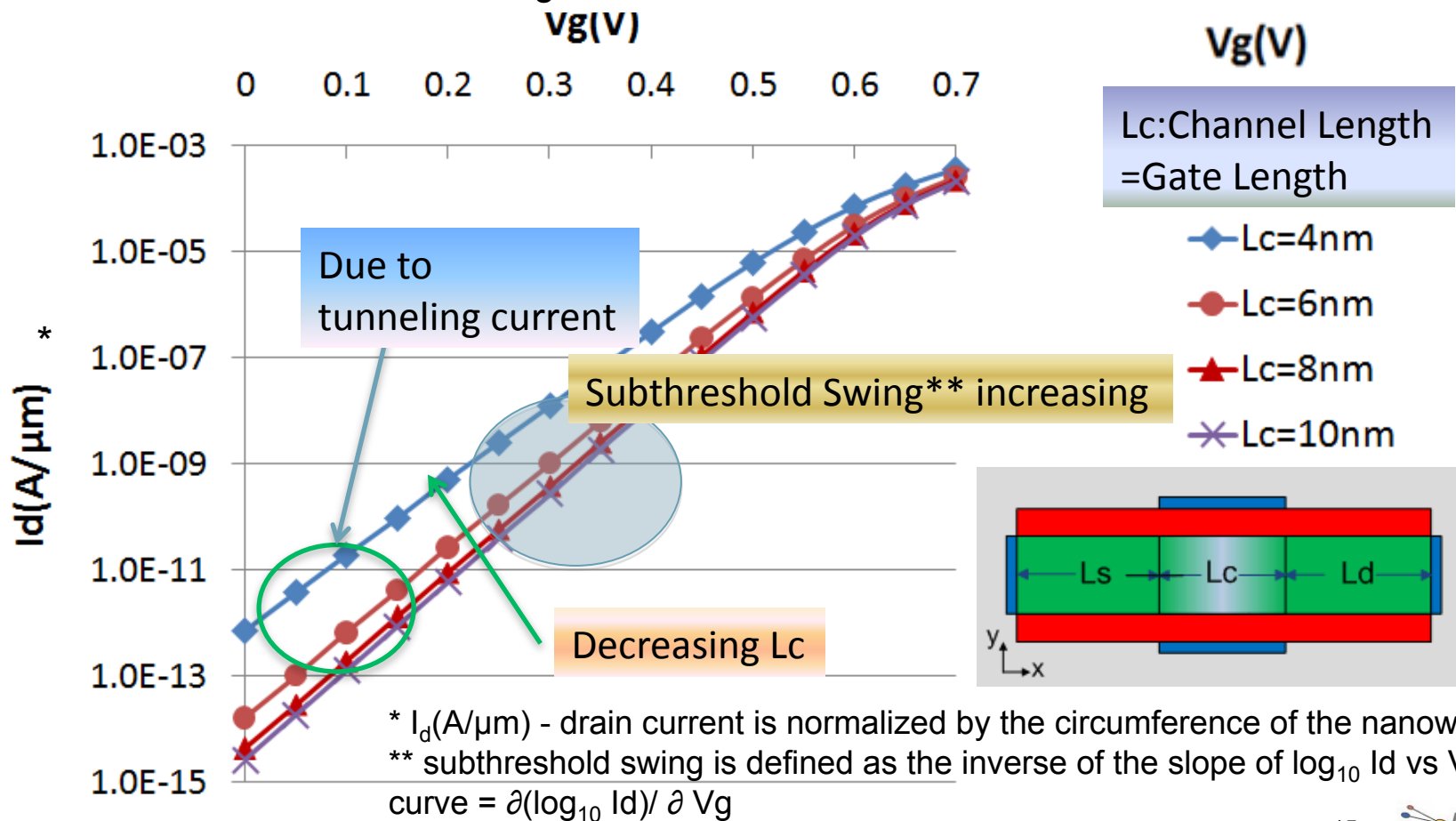


- [Inputdeck] : Input parameters translated to the format that can be used for job submission to OMEN
- [Id-Vg Characteristics] : Id-Vg curve (Id-Vd curve can be chosen to be shown in the environment input option)
- [1D electron density] : 1D electron density (/cm³) to the transport direction
- [1D bandstructure] : 1D bandstructure/Fermi levels in the contacts/transmission coefficient/current density/conduction band edge through the nanowire
- [Density of states (x,E)] : 2D density of states as function of transport direction x and energy E
- [Transmission and current density] : Transmission coefficient and the current density(=Transmission*(f_L-f_R) f_L/f_R:fermi function at the left and right contact)
- [3D electron density]
- [3D electron density(log)] : log scale of 3D electron density
- [3D electrostatic potential]
- [Output Log] : includes all the messages posted on the screen after you click "Simulate" and the output/error messages from the OMEN simulator

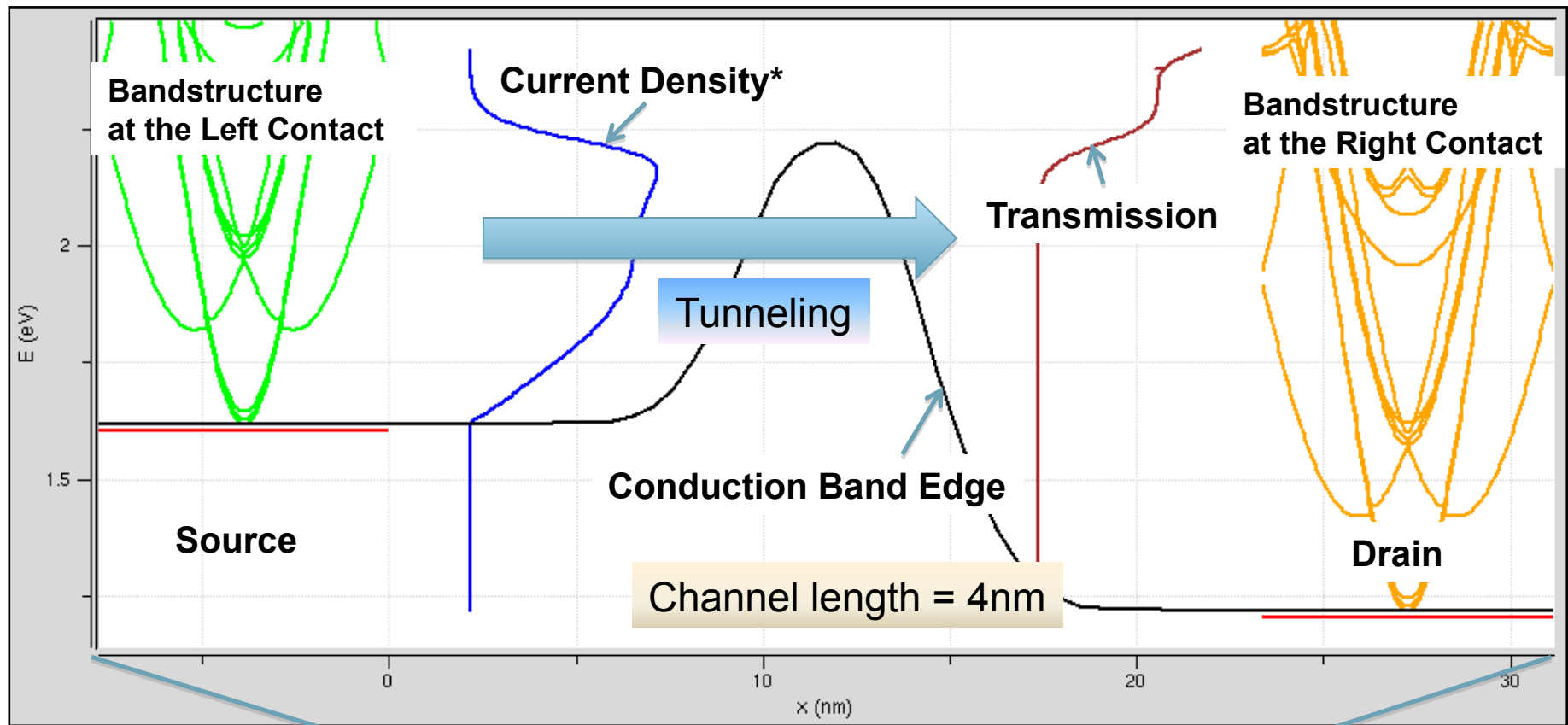
Example: What if the length of the channel is changed?

IV Characteristics

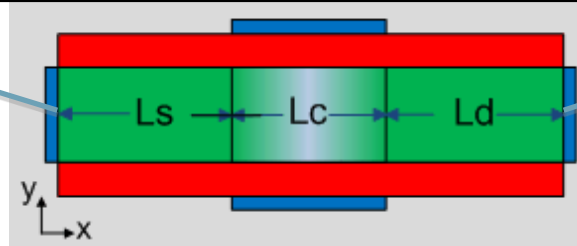
The drain current and subthreshold swing** at small V_g increases due to the tunneling current and as the channel length decreases.



Example: What Happens at a Small Channel Length? (bandstructure)



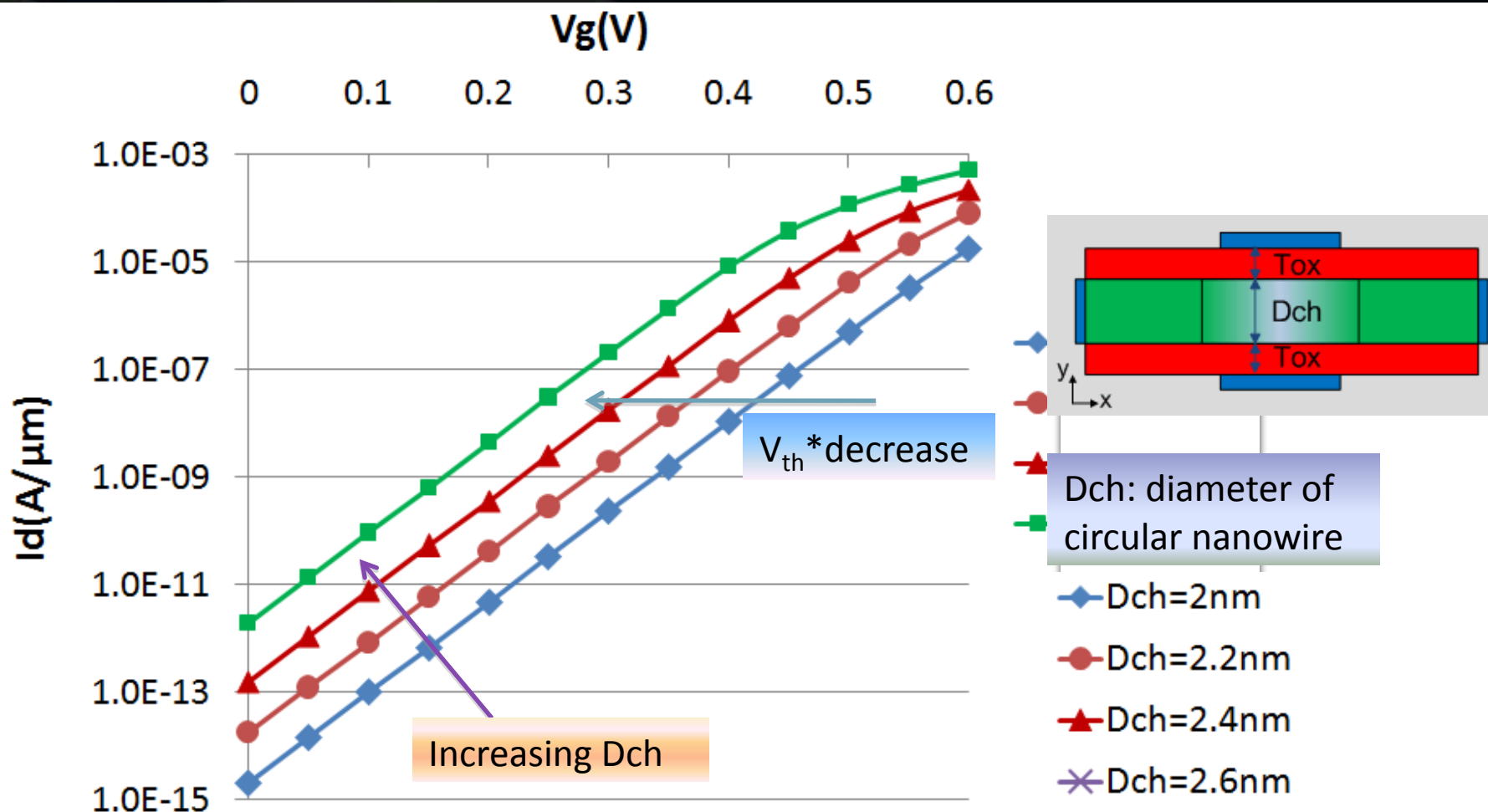
$$V_g = 0V, V_d = 0.4V$$



*Current Density
= Transmission * ($f_L - f_R$)

f_L : left contact fermi function
 f_R : right contact fermi function

Example: What if the Nanowire Diameter is Changed? (IV Characteristics)

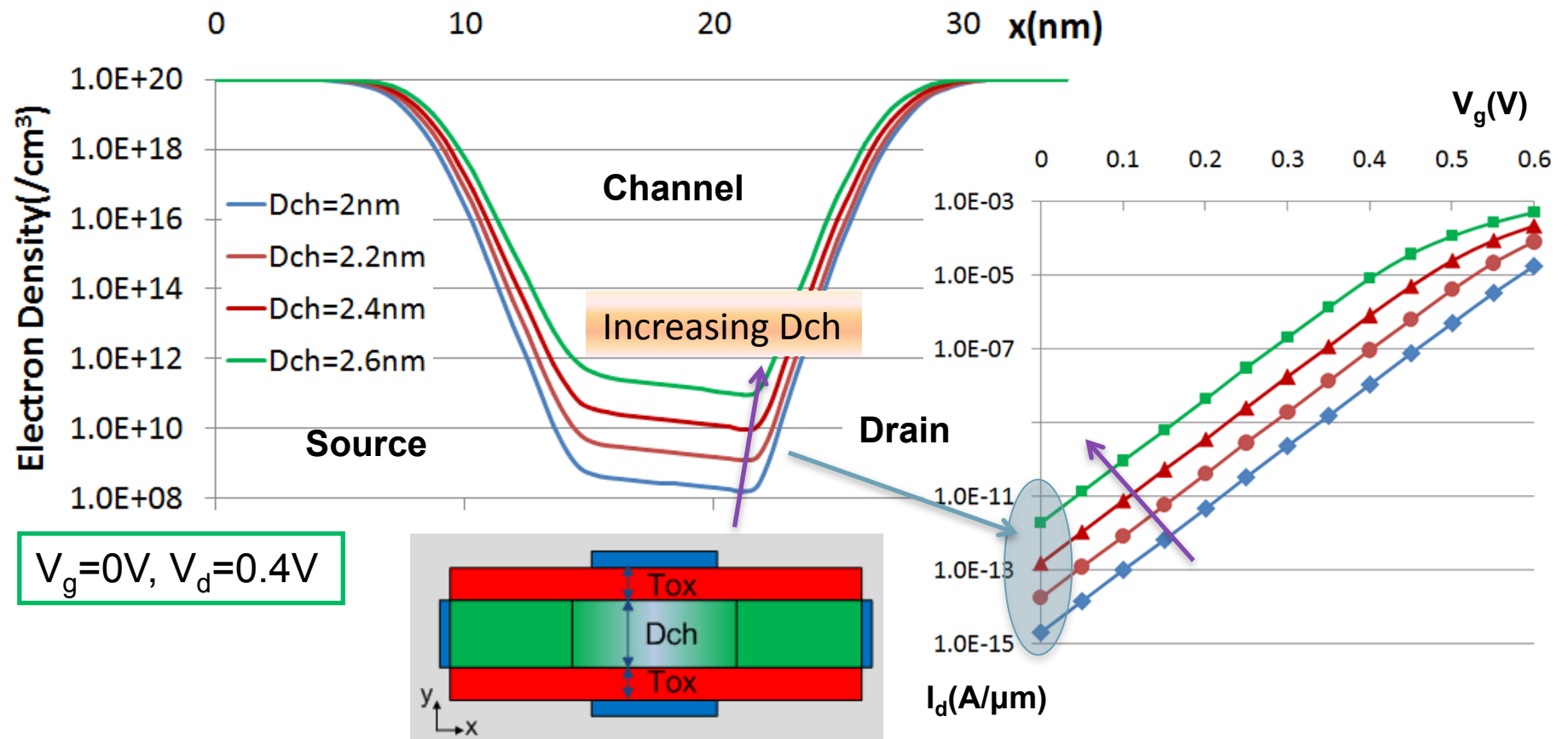


* V_{th} can be defined in many ways. Here we define it as a voltage where the drain current becomes larger than certain value ($10^{-7}\text{A}/\mu\text{m}$)

Example: What happens in the channel?

Electron density in the channel increases as the diameter of the nanowire increases.

→ Drain current increases at large diameter nanowire



Limitations of the OMEN Nanowire Tool

- Cross section of nanowire cannot be larger than $3 \times 3 \text{ nm}^2$ or smaller than $1.5 \times 1.5 \text{ nm}^2$
- Length of gate should be less than 60 nm
- You can not choose which server or the number of CPUs* in that server to use
- Simulation may not be converged at high V_g (e.g. larger than 0.7V) when the potential barrier is about the same as the conduction band edge of the source side^[6]

*The number of CPUs is estimated by the OMEN Nanowire according to the time table^[5] database and as based on the cross section and gate length of the nanowire that user inputs.

[6] <https://nanohub.org/resources/6315>

On-demand Simulation

- The number of CPUs for which OMEN Nanowire can submit a job, in order to end the simulation in 4 hours* in a steale cluster, is less than 256.
- If your simulation needs more than 256 CPUs, the simulation will be aborted and the following message will appear:

```
The number of CPUs required to fullfill the simulation is more than 256  
Please reduce the size of nanowire structure or reduce the number of bias points
```

- If you want to simulate structure that uses more than 256 CPUs, or if you want to simulate with a different material system than what is now provided in OMEN Nanowire, you may submit a request for a device that can manage such a job. Contact the developer team by email (kim568@purdue.edu) or by webpage (<https://nanohub.org/resources/5359/questions>).

*This is the walltime limit in steale cluster

References

- Experimental Study on Nanowire FET
- [1] Sung Dae Suk, et. al., IEDM, 2005, "High Performance 5nm radius Twin Silicon Nanowire MOSFET(TSNWFET) : Fabrication on Bulk Si Wafer, Characteristics, and Reliability
- Physics of Nanowire FET
- [2] Wang, Jing (2006), "Device Physics and Simulation of Silicon Nanowire Transistors,"
<http://nanohub.org/resources/1313>
- OMEN
- [3] Mahieu Luisier, et. al., "Atomistic simulation of nanowires in the sp³d⁵s* tight-binding formalism : From boundary conditions to strain calculations", Physical Review B,2006
- [4] <http://cobweb.ecn.purdue.edu/~gekco/omen/index.html>
- Time/memory estimation in OMEN Nanowire
- [5] http://cobweb.ecn.purdue.edu/~gekco/students/SungGeunKim/SungGeunKim_OMENNanowire_time_table.html
- The Limitation of the OMEN Nanowire at high gate voltage
- [6] OMEN Nanowire Supporting Document : Limitation of the Tool at Large Gate Voltage
- <https://nanohub.org/resources/6315>