First-Time User Guide to 
MOSFET V1.2.2

Saumitra Mehrotra*, Ben Haley, Gerhard Klimeck
Network for Computational Nanotechnology (NCN)
Electrical and Computer Engineering

*http://nanohub.org/resources/mosfet
smehrotr@purdue.edu
Table of Contents

• Introduction
  » What is a MOSFET? ................................................................. 3
  » What is a SOI-MOSFET? ............................................................ 4

• What Can Be Simulated by the MOSFET Tool? ............................ 5

• What if You Just Hit “Simulate”? ............................................. 10

• Some Examples
  » What if the Channel Length is Changed? ................................ 11
  » SOI versus Bulk MOSFET ...................................................... 12

• Tool Limitations and General Comments ................................ 13

• References .............................................................................. 14
metal–oxide–semiconductor field-effect transistor: (MOSFET, MOS-FET, or MOS FET) is a device used to amplify or switch electronic signals.

- Gate: Polysilicon or Metal (eV)
- Oxide: SiO$_2$ used as the dielectric (nm)
- Channel: n-type doped semiconductor for PMOS and p-type doped for NMOS
- Source/Drain: Heavily doped regions in contact with channel
- Substrate: Base semiconductor material
What is a SOI MOSFET?

(Silicon on Insulator) metal–oxide–semiconductor field-effect transistor (SOI) MOSFET: semiconductor device formed above an insulator

Advantages
- Better gate control* over thinner channel
- Reduces short channel effects*

Disadvantages
- Increases parasitic resistance*
- Quantization effects come in leading to increasing (threshold voltage) $V_t$

*Refer [1] https://nanohub.org/resources/5085 for detailed description of working of a MOSFET.
What Can Be Simulated by the MOSFET Tool?

MOSFET simulation with different geometry types

SOI nMOS & pMOS

Bulk nMOS & pMOS

Structural Properties

Device Type: SOI n-type

Doping Profile

MOSFET n-type

MOSFET p-type

Source/Drain: SOI n-type

Channel Length: 50nm

Channel Nodes: 20

Oxide Thickness: 2nm

Oxide Nodes: 5

Junction Depth: 15nm

Junction Nodes: 20

Buried Oxide Thickness: 100nm

Buried Oxide Nodes: 20

Device Width: 1000nm
What Can Be Simulated by the MOSFET Tool?

- Design different MOSFET structures

More nodes: higher accuracy but more compute time

3 different doping profiles to simulate real devices:
- Uniform
- Gaussian S/D
- Gaussian S/D + Halo

Modern MOSFET structure.[2]

What Can Be Simulated by the MOSFET Tool?

- CONMOB: Ionized Impurity scattering
- FLDMOB: Velocity Saturation model
- GATMOB: Gate-field mobility model

Refer [3] below to know more about the models.


Set material parameters and model

- No poly depletion included in simulations
- Bandgap, dielectric constant, and barrier height can be tuned to simulate another materials

<table>
<thead>
<tr>
<th>Structural Properties</th>
<th>Model</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Temperature:</td>
<td>300K</td>
<td></td>
</tr>
<tr>
<td>Gate Electrode:</td>
<td>n+ poly silicon</td>
<td></td>
</tr>
<tr>
<td>Gate Electrode Workfunction:</td>
<td>0eV</td>
<td></td>
</tr>
</tbody>
</table>

Silicon parameters

- Silicon Bandgap at 300K: 1.12eV
- Silicon Dielectric Constant: 11.8

Oxide Parameters

- Oxide Barrier Height at 300K: 3.4eV
- Oxide Dielectric Constant: 3.9
- Oxide Fixed Charge Density (me/m^2): 0

- CONMOB: yes
- FLDMOB: yes
- GATMOB: yes
- IMPACT Ionization: no
- Bipolar Carriers: no
What Can Be Simulated by in the MOSFET Tool?

- Both \(I_d-V_g\) and \(I_d-V_d\) curves can be simulated during the same run.
- Keep number of bias points at 0.1 V spacing for better convergence.
What Can Be Simulated by the MOSFET Tool?

In 2D, 1D (along x) and 1D (along y):
- Doping profile (/cm³)
- Potential profile (V)
- Electron density (/cm³)
- Hole density (/cm³)
- Electric field (V/cm)
- Quasi-Fermi level (eV)

Output Characteristics:
- \( I_d - V_{g} \) & \( I_d - V_{d} \)
Default setting simulates Id-Vg characteristics for N-type MOSFET:

Channel length, \( L = 100\, \text{nm} \)

Oxide thickness, \( T_{ox} = 2\, \text{nm} \)

Channel doping, \( N_{ch} = 1 \times 10^{18}/\text{cm}^3 \)

DIBL \( \approx 38.2\, \text{mV/V} \)

SS \( \approx 80\, \text{mV/dec} \)

\( I_{on}/I_{off} \approx 4.8 \times 10^3 \)

Id-Vg simulated are at

\( V_d = 0.05\, \text{V (low)} \) & \( V_d = 1.5\, \text{V (high)} \)

Long channel device behavior
Example: What if the Channel Length is Changed?

Id-Vg comparison between MOSFET with Lc=50nm & Lc=100nm

Severe short channel effects [3] at Lc=50nm. Vd=1.5V (red) & Vd=0.05 (blue)

• High OFF state current*
• High DIBL*
• High Subthreshold slope*

*Please refer to reference [3] for more information about short channel effects in MOSFETS

DIBL: Drain Induced Barrier Lowering

https://nanohub.org/resources/5085

Barrier lowered for Lc=50nm
Example: SOI versus Bulk MOSFET

Id-Vg comparison between bulk and SOI MOSFET with $L_c=50$nm

Improved short channel effects [3] for SOI-MOS (10 nm body thickness) over bulk-MOS at $L_c=50$nm.

- Lower $I_{off}$
- Lower DIBL
- Lower subthreshold slope

Please refer [3] for more information about Short Channel Effects in MOSFETS

https://nanohub.org/resources/5085

<table>
<thead>
<tr>
<th>SS (mV/dec)</th>
<th>SOI</th>
<th>Bulk</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>113</td>
<td>162</td>
</tr>
</tbody>
</table>
Tool Limitations and General Comments

- No polydepletion effects are included in the simulations.
- Quantum effects are not present in the simulations.
  > This is important for SOI simulation with very thin (<5nm) body thickness
- Few bias points during the large bias sweep (Vg or Vd sweep) might lead to non-convergence.
- Take note of the location of 1D output plots while running the simulation (i.e. output profile should lie in the desired region of interest).

Please use the following link to submit any issues/comment:
• https://nanohub.org/resources/3/reviews?action=addreview#reviewform

If you reference this work in a publication, please cite as follows:
• Matteo Mannino; Shaikh S. Ahmed; Gerhard Klimeck; Dragica Vasileska; Xufeng Wang; Himadri Pal (2006), "MOSFet," DOI: 10254/nanohub-r452.7.
[1] MOSFET OPERATION DESCRIPTION: https://nanohub.org/resources/5085

