Technology Trends as Viewed in 2011

Scaling the Conventional Transistors

Future Nanoelectronic Devices

Nobel Prizes in Electron Devices

- **1956 – The Transistor**
  William Shockley, John Bardeen, and Walter Brattain
- **1973 – Tunneling Diode**
  Leo Esaki, Ivar Giaever
  – Josephson Junction
  Brian David Josephson
- **2000 – Integrated Circuit**
  Jack Kilby
  – Semiconductor Heterojunction Devices
  Zohres Alferov and Herbert Kroemer
- **2007 – Giant Magnetoresistive Effect (GMR)**
  Albert Fert and Peter Grunberg
- **2009 – Charge Coupled Devices**
  George Smith and Willard Boyle
  – Fiber Optic Technology
  Charles Kao By

Technology Trends: Scaling

Downsizing of the components has been the driving force for circuit evolution:

1900	1950	1960	1970	2000
VT	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm

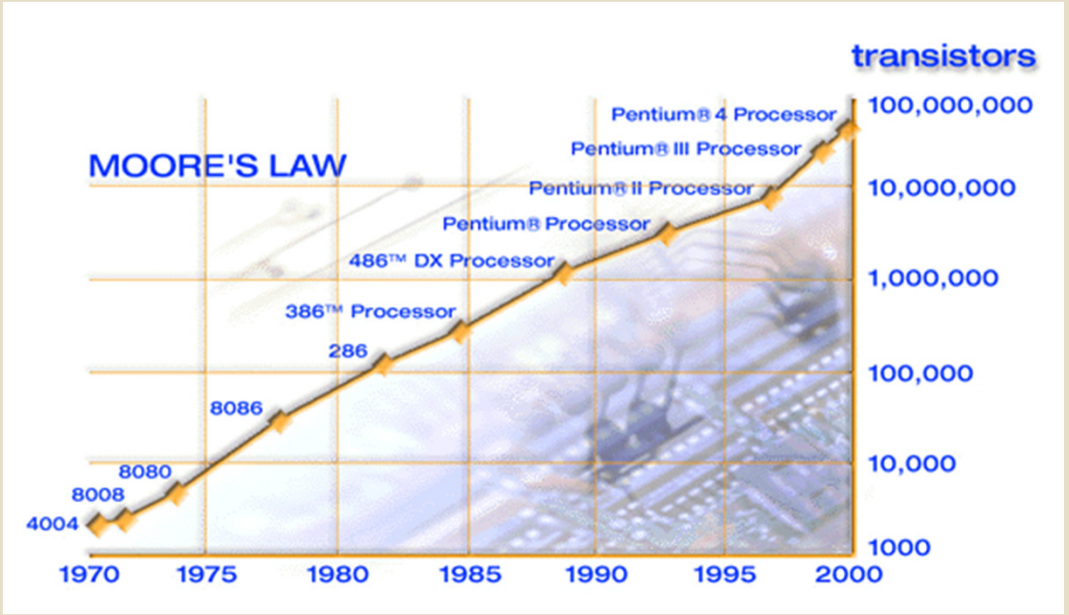
In 100 years, the size reduced by one million times.

We have never experienced such a tremendous reduction of devices in human history.

Transistor Scaling: Moore's Law

Gordon Moore

"*every 1.5 years complexity doubles*"



Technology Trends: Scaling

- Downsizing:
  - Reduce Capacitance
    - Reduce switching time of MOSFET
    - Increase clock frequency
      - Increase Circuit operation Speed
  - Increase number of transistors
    - Parallel processing
      - Increase Circuit operation Speed

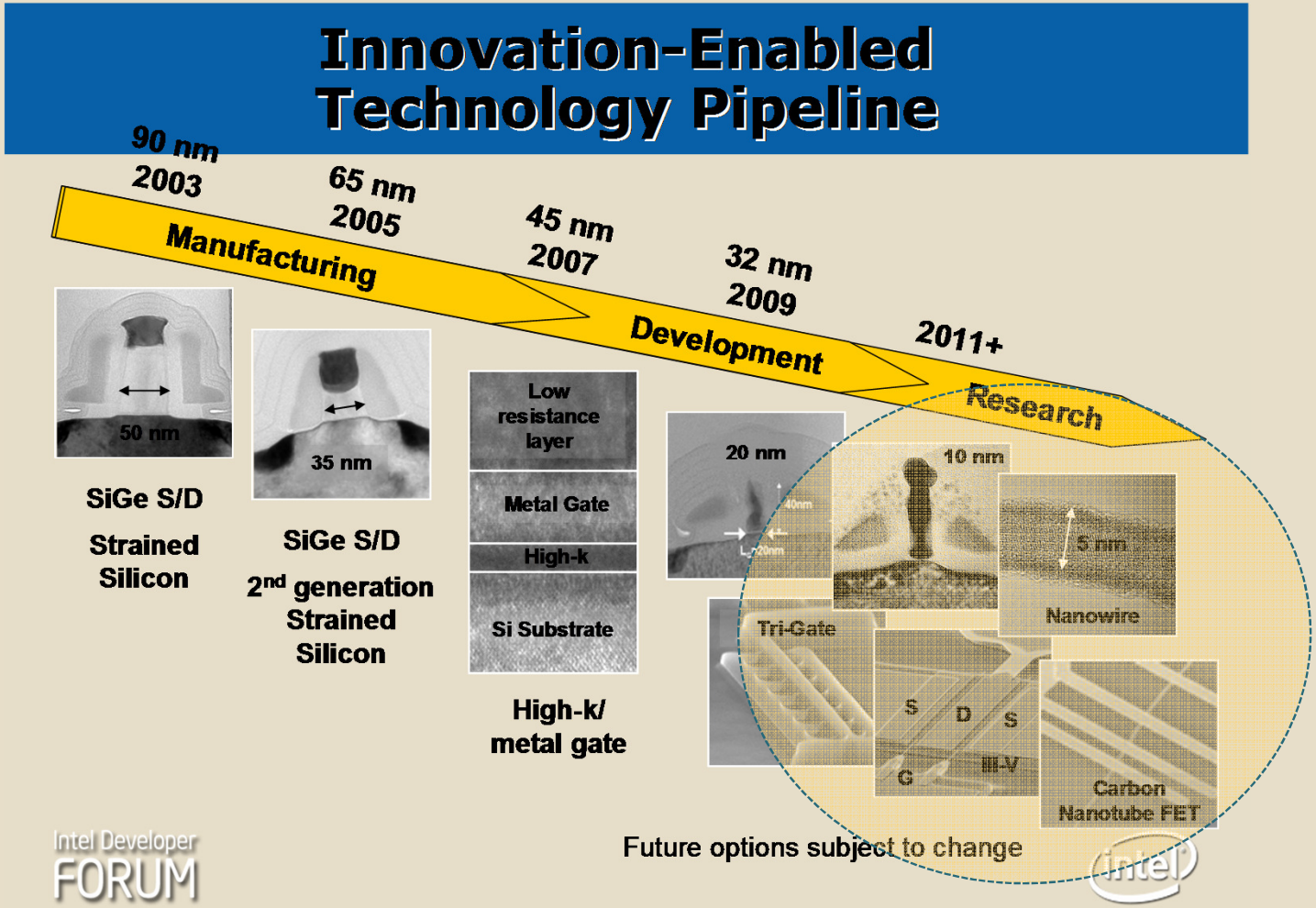
Downsizing contributes to the performance increase in two ways.

Thus, downsizing of Si devices is the most important and critical issue.

Technology trends: Constant Field Scaling

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area → $W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$ → $KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d$ → $KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor → **In the past, $\alpha>1$ for most cases**
Integration (# of Tr)	N	α/K^2	N → α/K^2 **$= 1/K^2$, when $\alpha=1$**
Power per chip	P	α	$fNCV^2/2$ → $K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ **$= 1$, when $\alpha=1$**

Scaling of Today's Devices



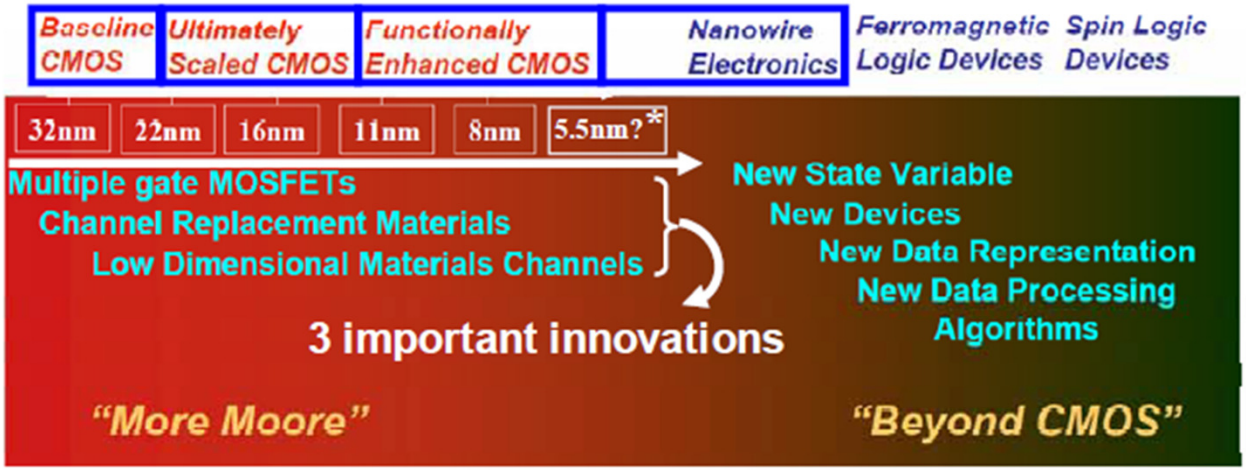
Future Device Technologies: … More Moore

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Three important technologies

1. High-k/metal gate stack with <0.5nm EOT, Silcide S/D
2. Si Nanowire MOSFETs
3. Alternative channel MOSFETs (III-V, Ge), maybe nanowire

- Other Beyond CMOS devices are still in the cloud.

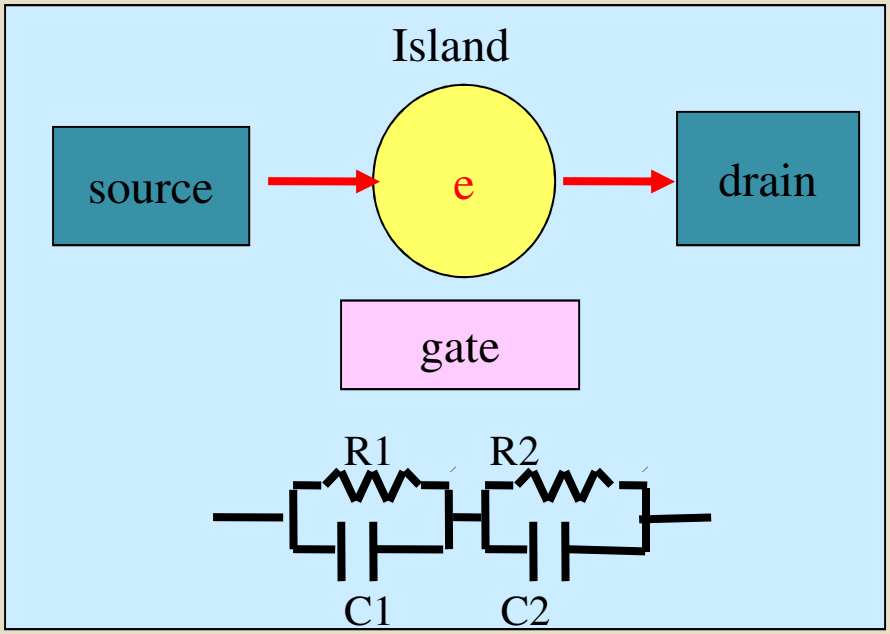


ITRS figure edited by Iwai

More than Moore …

- 1969 Lambe and Jaklevic: Charge quantization in a small box
- 1987 Averin and Likharev Single Charge Transfer, Single Electron Transistor at very low temperatures
- 1991 Fulton (Bell Labs) Single Charge Sensing Structure
- 1993 Nakazato and Ahmed, Dresselhaus and Likharev
  Single Electron Memory Prototype
- 1994 Many groups from Hitachi, IBM, Minesota, etc.
  Single Electron Memory at Room Temperature Using Quantum Dots
- 1996 Yano (Hitachi Central Lab)
  First Single Electron Memory Array, 64 bits.
- 1998 Yano (Hitachi Central Lab)
  First ULSI Single Electron Memory Prototype. 128 Mbits.
- 1999 Nakazato (Hitachi Cambridge) and Ahmed (Cavendish Lab)
  Announce Manufacturable Device for Next Generation Memory.

Coulomb Blockade Effect



Coulomb Blockade Effect

Quantum tunneling of electron between source and drain can be blocked If the charging energy

$E_c = e^2/2C >> kT$

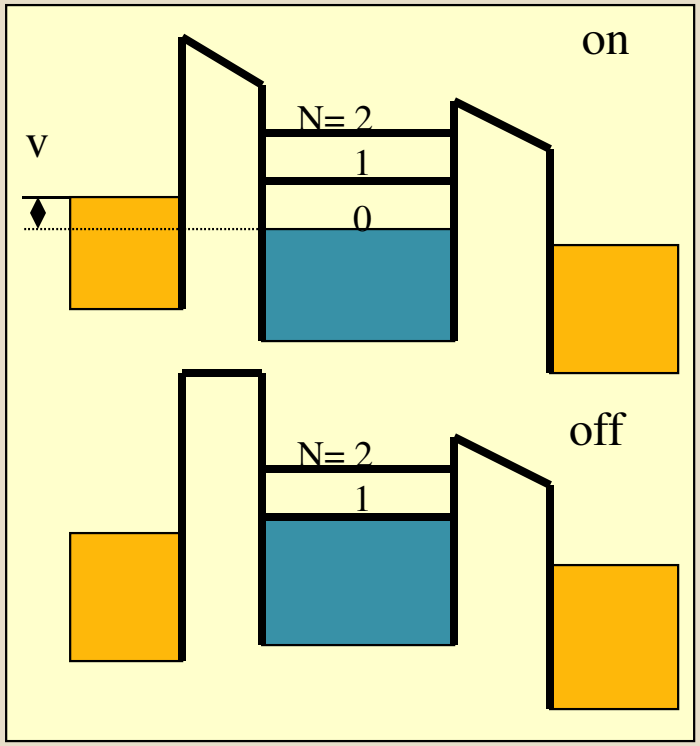
$\Delta E = eV - E_c < 0$: blocked

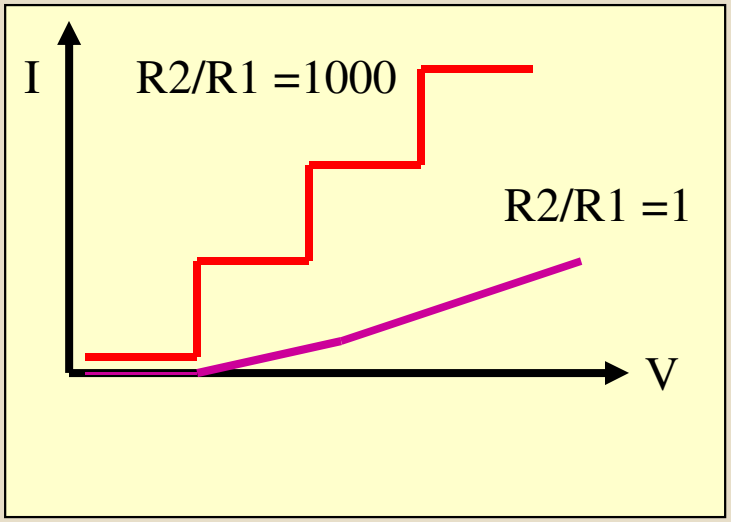
$2E_c = e^2/(C_1+C_2)$

Coulomb Staircase

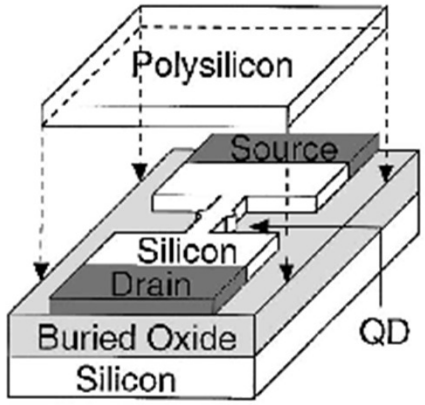
- Asymmetric junction $(R2>>R1)$
- Current steps at $e/2C_2 + n(e/C_2)$

Coulomb Blockade Effect – Cont'd

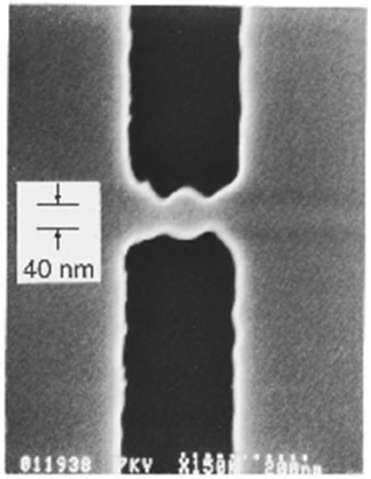




SET at 100 K



[a]



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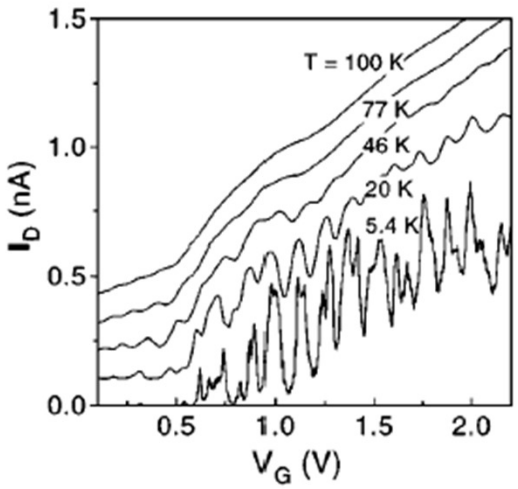


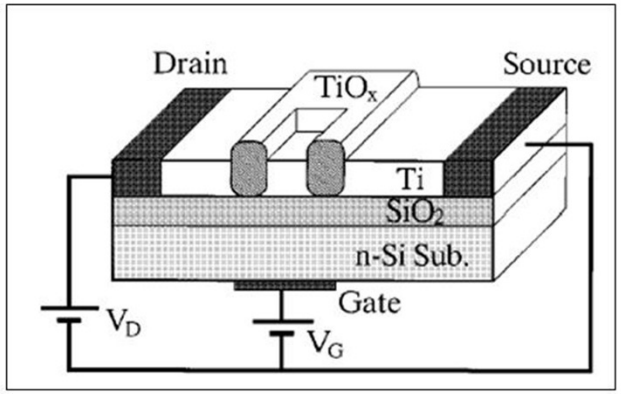
FIG. 2. The drain current I_D vs the gate voltage V_G of a Si QDT with 20 nm dot at different temperatures up to 100 K (curves are displaced for clarity). The V_{DS} was kept at 50 μV to prevent the drain bias from broadening the oscillations at 5.4 K significantly.

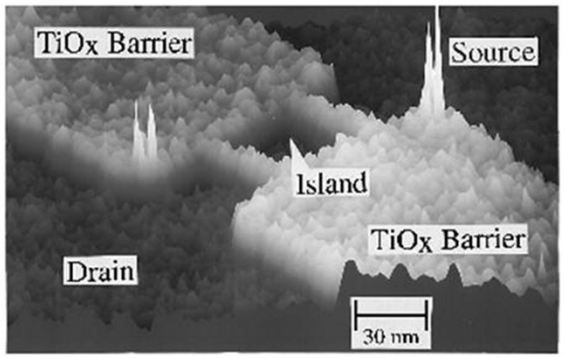
Si dot with 20nm diameter : energy spacing = 40meV

Current oscillation due to the interference between different modes of quantum waves in a cavity

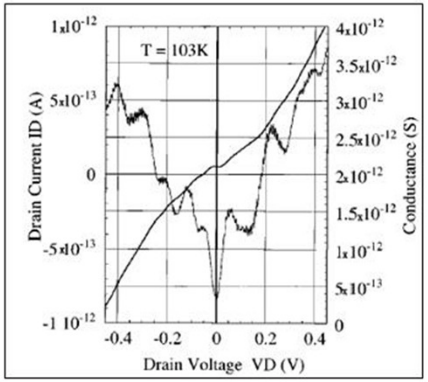
S.Y. Chou et al., Appl. Phys. Lett 67, 938 (1995)

SET Operation at 300K

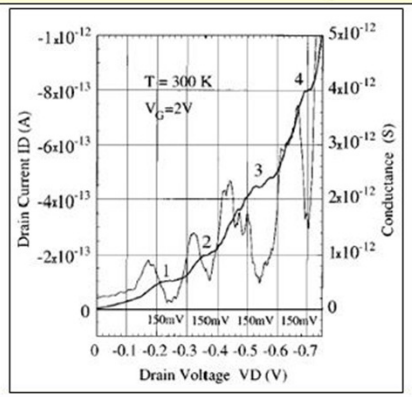




K. Matsumoto et al., Appl. Phys. Lett. 68, 34 (1996)

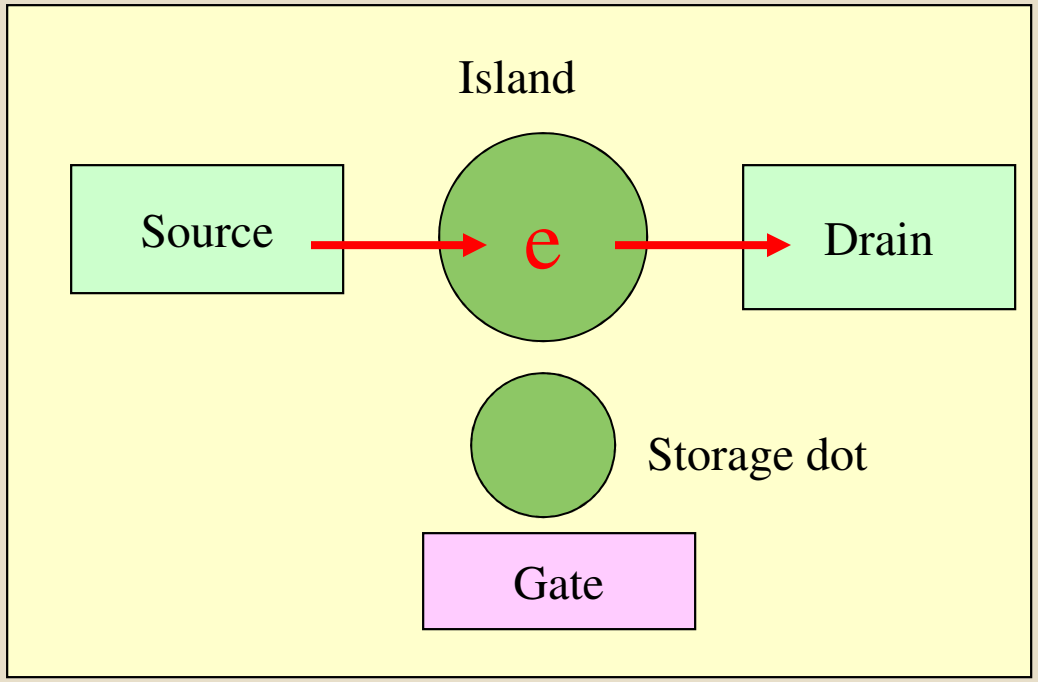


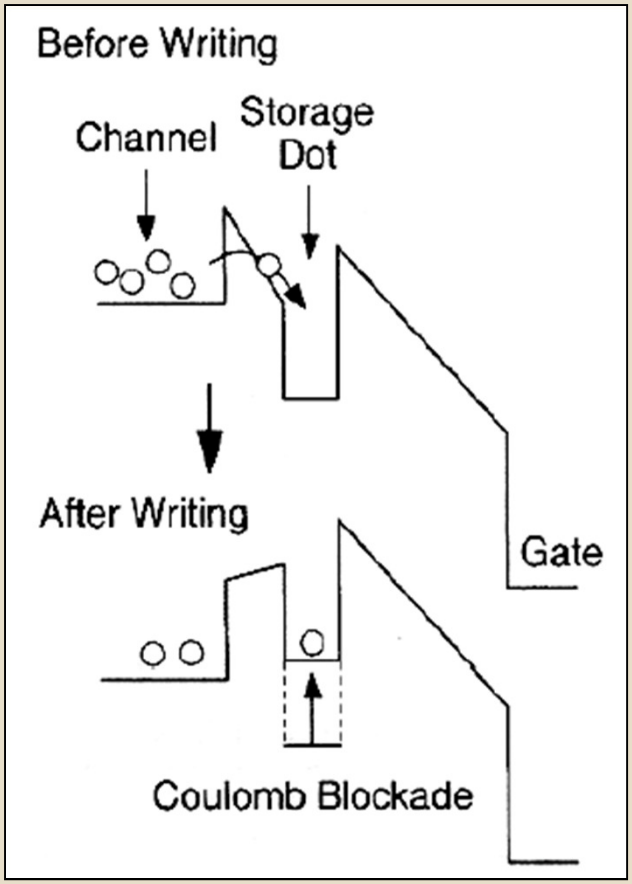
Unclear coulomb staircase due to the symmetric size of the tunnel juncton



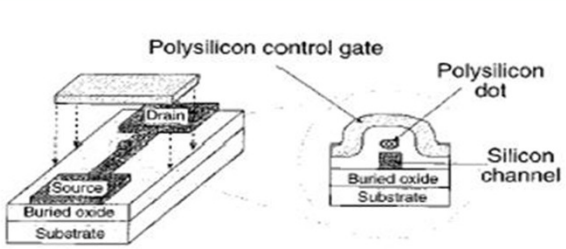
Coulomb staircase with periods of 150mV

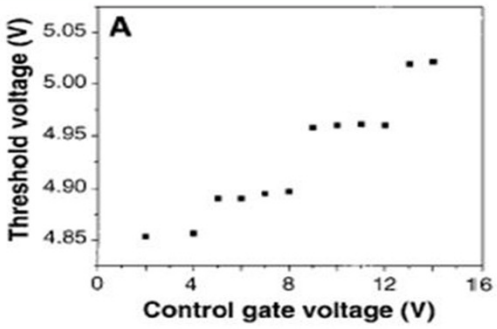
Single Electron Memory

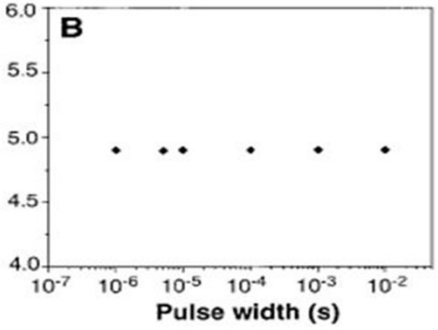


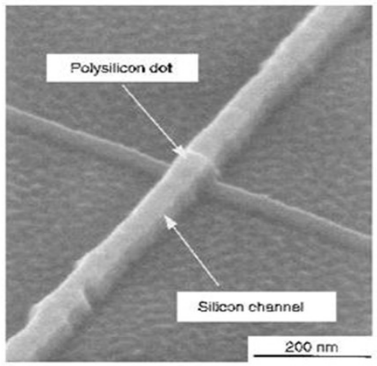


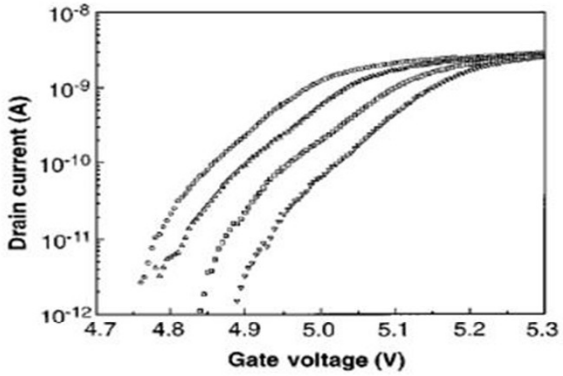
Single Electron Memory - Demonstration

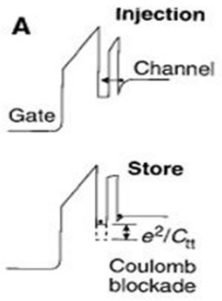


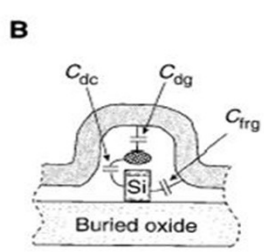








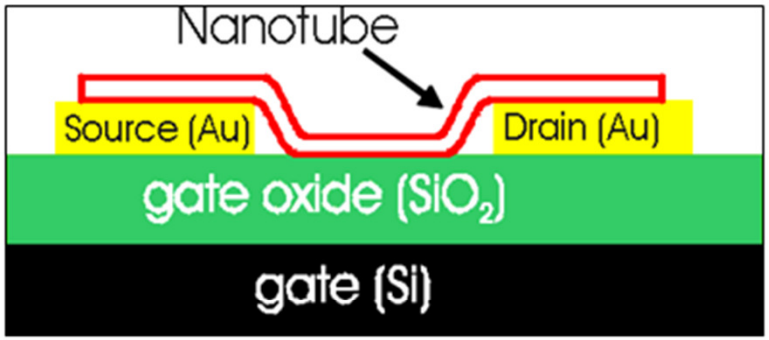


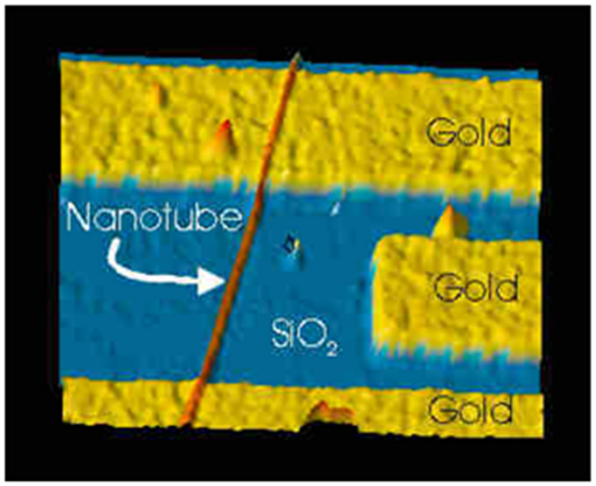


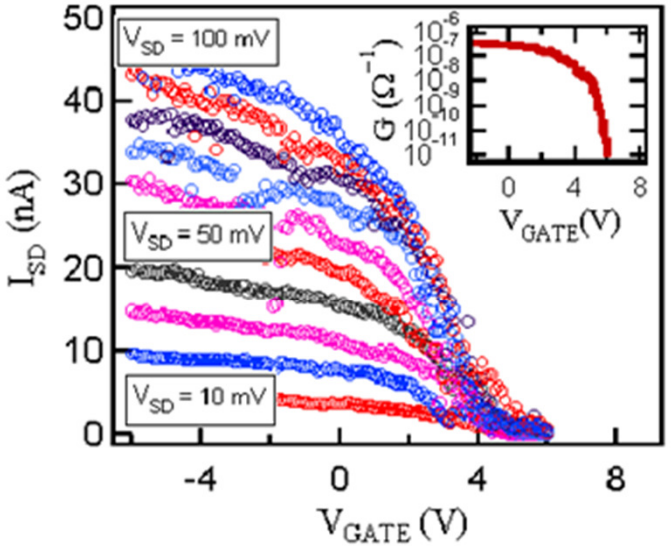
- Discrete shift in the threshold voltage
- Staircase relation between the charging voltage and the shift
- Self-limiting charging process

L. Guo, E. Leobandung, S.Y. Chu, Science 275, 649 (1997)

Nanotube Single Electron Transistor



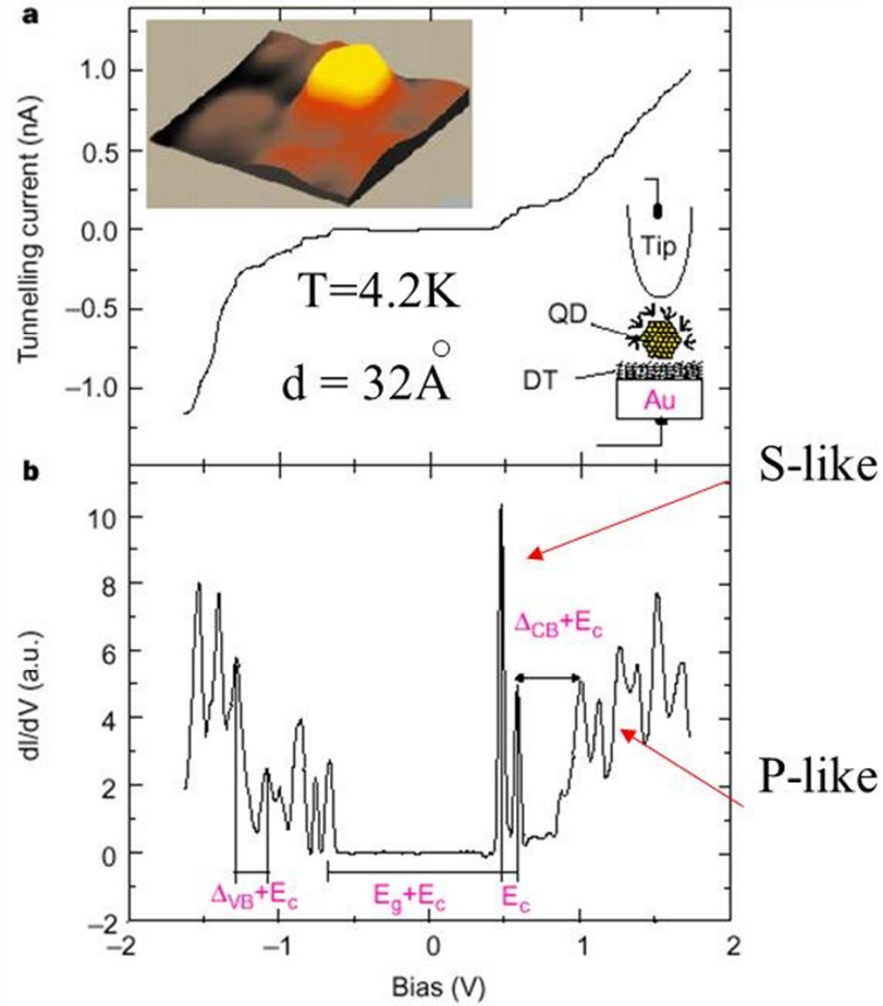


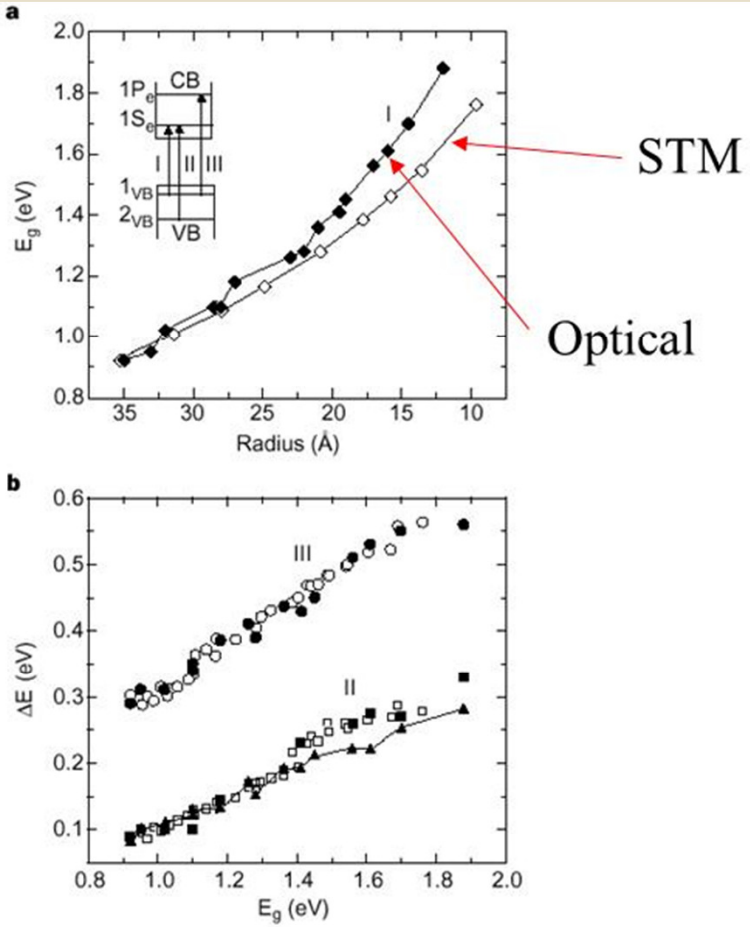


The amount of current (I_{SD}) flowing through the nanotube channel can be varied by a factor of 100,000 by changing the voltage applied to a gate (V_G),

P. Avouris et al. ,Appl. Phys. Lett, 73, 2447 (1998)

Tunneling Spectroscopy of InAs Quantum Dots

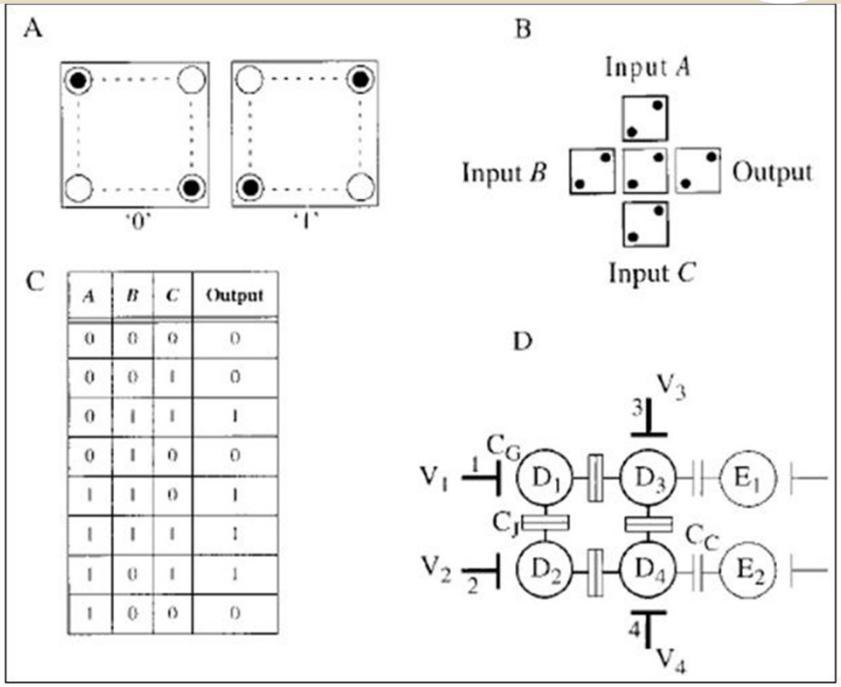




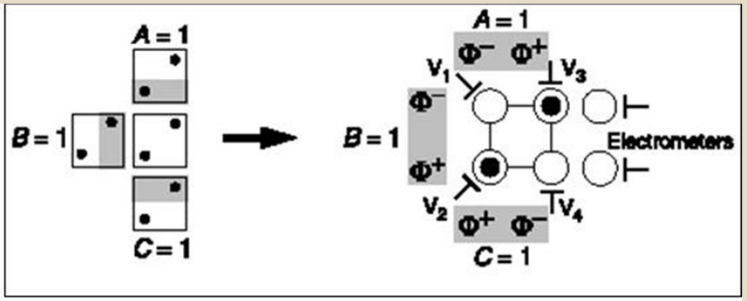
Ec=0.11 eV: single electron charging energy
Eg=1.02 eV: nanocrystal band gap

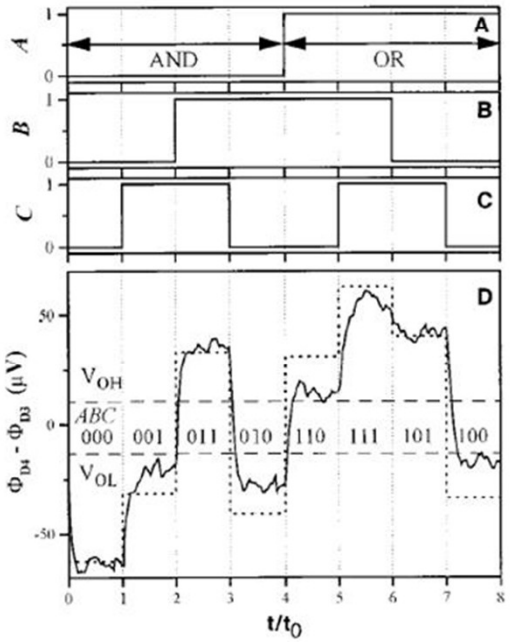
U. Banin et al, Nature, 400, 926 (2000)

Quantum Dot Cellular Automata



A	B	C	Output
0	0	0	0
0	0	1	0
0	1	1	1
0	1	0	0
1	1	0	1
1	1	1	1
1	0	1	1
1	0	0	0



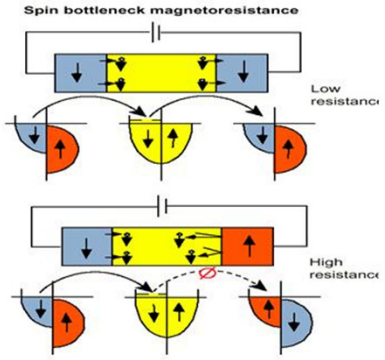


- Wireless interconnection
- Communicate by the electric fields of electrons

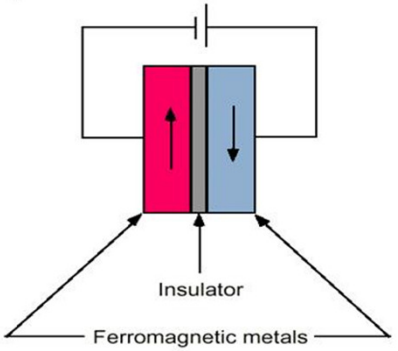
I. Amlani et al., Science, 284, 289 (1999).

Magnetic Random Access Memory (MRAM)

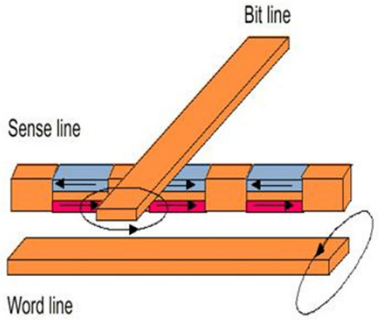
G.A. Prinz, *Science* 282, 1660 (1998)



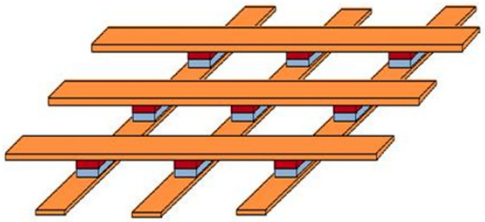
Spin-polarized transport



Magnetic Tunnel Junction(MTJ)



RAM that is constructed of GMR elements



RAM that is constructed of magnetic tunnel junction

Nanowire Transistor

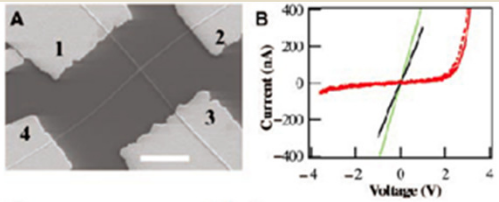


Fig. 1. Crossed SiNW junctions. **(A)** Typical FESEM image of a crossed SiNW junction with Al/Au contacts. The scale bar is 2 μm. The diameters of the NWs used in these studies ranged from 20 to 50 nm. **(B** through **D)** *I-V* behavior of *p-n*, *p-p*, and *n-n* junctions, respectively. The black and green curves correspond to the *I-V* behavior of individual *p-* and *n*-type SiNWs, respectively. The red curves represent *I-V* behavior of junctions. (B) The red curves correspond to four-terminal *I-V* through the *p-n* junction; the current values are multiplied by 10. The solid line corresponds to voltage drop measured between leads 3 and 4, and the dashed line to voltage between 3 and 2. (C and D) The red curves are two-terminal *I-V* through *p-p* and *n-n* junctions, respectively. The solid lines correspond to data from contacts 1-2, and the dashed lines correspond to data from the other three pairs (that is, 1 and 4, 2 and 3, and 3 and 4).

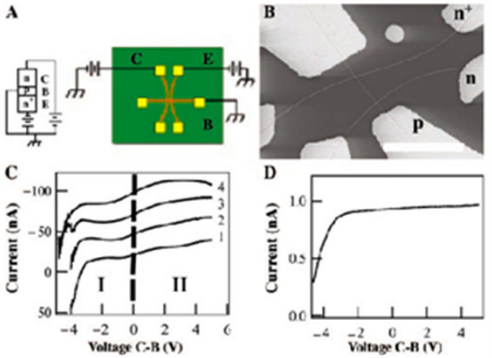
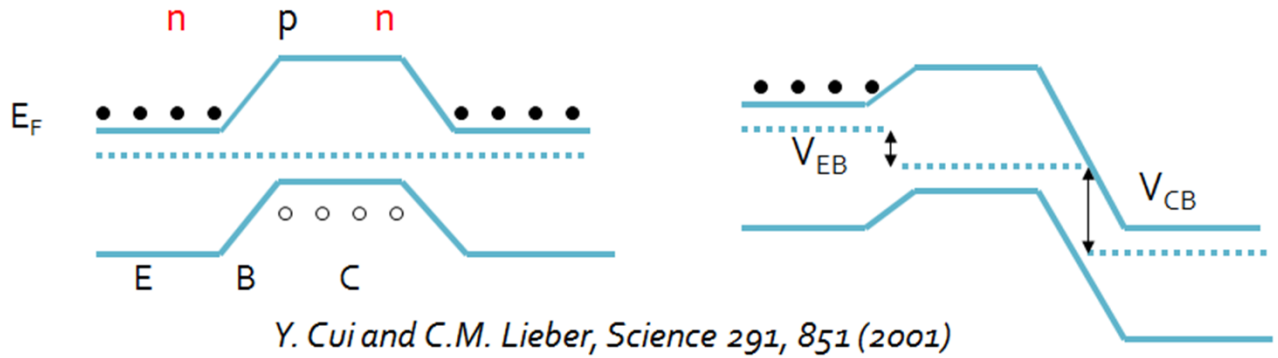


Fig. 2. Shown are n^+-*p*-*n* SiNW bipolar transistors. **(A)** Schematics illustrating the common base configuration of an n^+-*p*-*n* bipolar transistor (*19*) and the corresponding structure built from crossed SiNWs (right). The n^+-, *p*-, and *n*-type SiNWs function as emitter, base, and collector, respectively. **(B)** Typical FESEM image of SiNW bipolar transistor. The three wires labeled as n^+, *p*, and *n* were used as emitter, base, and collector, respectively. Scale bar, 5 μm. **(C)** Collector current versus collector-base voltage recorded on an n^+-*p*-*n* transistor with emitter and collector SiNWs 15 μm apart. Curves 1 to 4 correspond to the data recorded for emitter-base voltages of −1, −2, −3, −4 V, respectively. Regime I and II are separated by a dashed line, corresponding to saturation mode and active mode, respectively. **(D)**, The common base current gain versus collector-base voltage.

- Common base current gain: I_C/I_E=0.94
- Common emitter current gain: I_C/I_B=16



Y. Cui and C.M. Lieber, Science 291, 851 (2001)

Transistor Scaling: Beyond CMOS

Device	Operating Principle	Status	Advantages	Disadvantages
Resonant Tunneling Transistor	Quantum resonance in double barrier potential wells	Capable of large scale fabrication	Logic compression semiconductor based	Same scaling limitations as microelectronic transistor.
Single Electron Transistor	Coulomb Blockade in small quantum dots	Experimental only at very low temperatures	High gain. Similar in operation to FET	Low temperature. Difficult to control.
Quantum Dot Cell	Single electron confinement in arrays of Quantum dots	Quantum dots can be fabricated in the laboratory. Quantum dots are still theoretical.	Wireless. Low energy dissipation.	Difficult design rules. Susceptible to noise.
Molecular Shuttle Switch	Movement of a molecular "bead" between two stations on a switch molecule	Experimental, can only be switched chemically	Small, but robust. Assembly chemically.	Slow switching speed. How to interconnect?
Atom Relay	Vibrational movement of a single atom in and out of an atom wire	Theoretical	Very high speed. Sub-nanometer size.	Very low temperature. Very unreliable.
Refined Molecular Relay	Rotational movement of a group in and out of an atom wire	Theoretical	Sub-nanometer size. More reliable than atom relay.	How to fabricate? How to interconnect?