MOSFET: Series Resistance and Transistor Breakdown

Dragica Vasileska and Gerhard Klimeck

Login to nanoHUB.org and look for ABACUS. As part of the ABACUS tool-based curricula you will find the MOSFET Lab. Use the MOSFET Lab to simulate the device structure shown in the figure below. In your calculations use the appropriate model for low field mobility description in silicon inversion layers, Shockley-Read-Hall generation-recombination process (not that relevant for MOSFET operation), velocity saturation effect and impact ionization model due to Selberherr. The oxide thickness of the device being simulated equals 1.2 nm. For the substrate doping assume 5×10^{18} cm^{-3}. The junction depth is 0.36 nm and the total device depth, measured from the Si-SiO_2 interface, is 0.1 μm. For the doping of the source and drain regions assume, in one case (1) 10^{19} cm^{-3}, and in the second case (2) 10^{20} cm^{-3}. Vary the gate voltage from 1 V to 1.4 V, in 0.2 V increments. For each gate voltage value, do a drain voltage sweep from 0 V to 1.4 V. Perform the following set of simulation runs:

- Exclude the impact ionization process and use the two different values for the source and drain doping densities ((1) 10^{19} and (2) 10^{20} cm^{-3}). This will demonstrate the role of the series resistance effects on the device output characteristics. Also, discuss the role of the DIBL effect in the device output characteristics.

- Investigate the role of the impact ionization process on the device performance, by including the Selberherr's model for impact ionization. In these simulation runs assume that the doping of the source and drain regions equals 10^{20} cm^{-3}.