NCN Summer School: Nanoscale Transistors: July, 2012

Lecture 2:
IV Characteristics:
traditional approach

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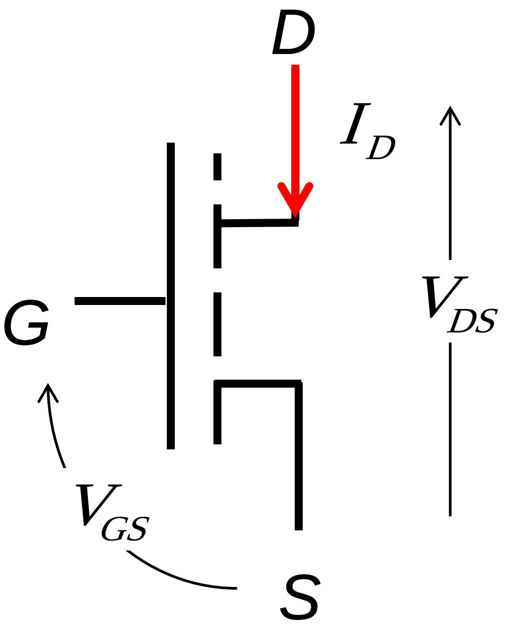
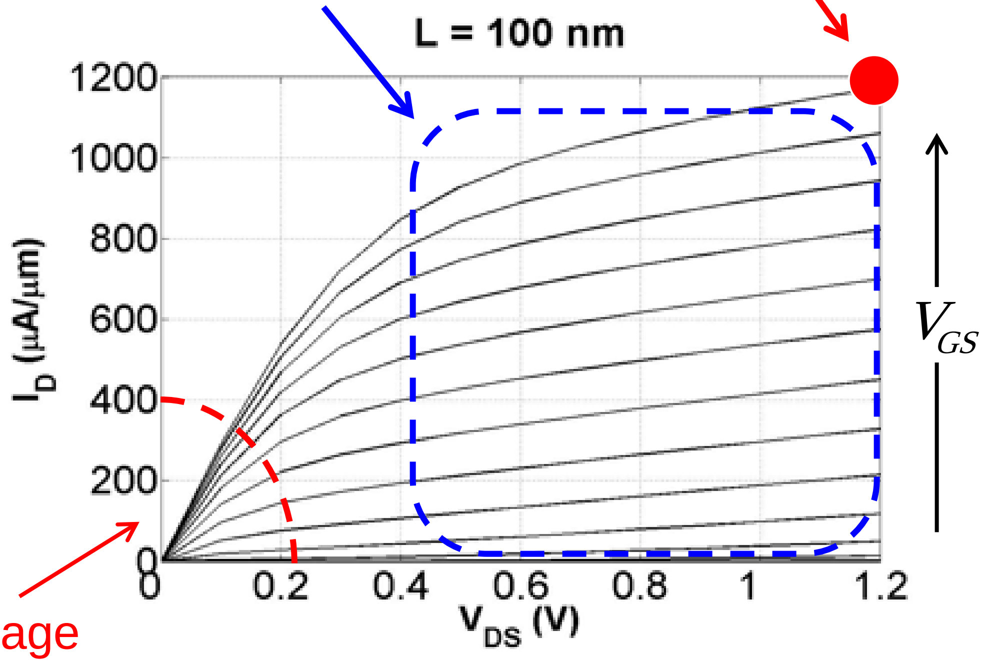
MOSFET IV characteristic

circuit symbol



gate-voltage controlled current source

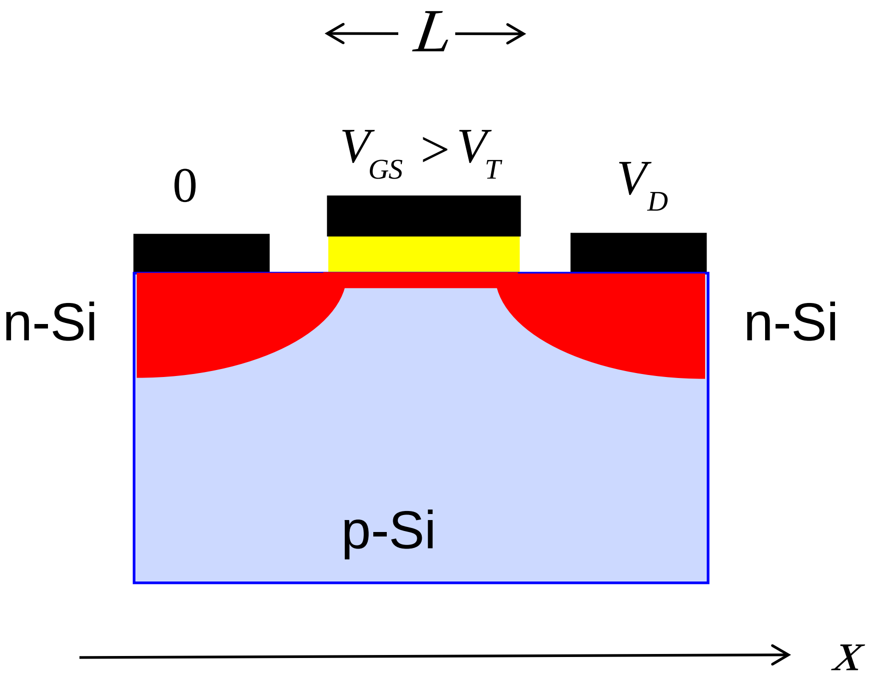
on-current



gate-voltage controlled resistor

(Courtesy, Shuji Ikeda, ATDF, Dec. 2007)

MOSFET IV



current is charge per unit time

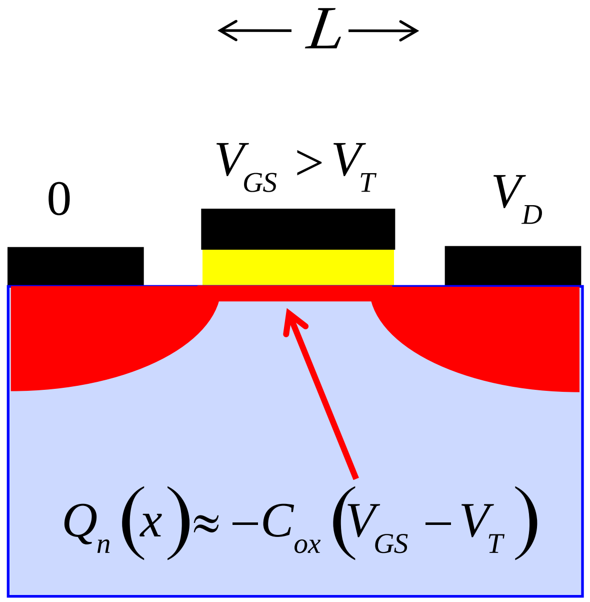
$$I_D = -WQ_n(x)\langle \upsilon_x(x)\rangle$$

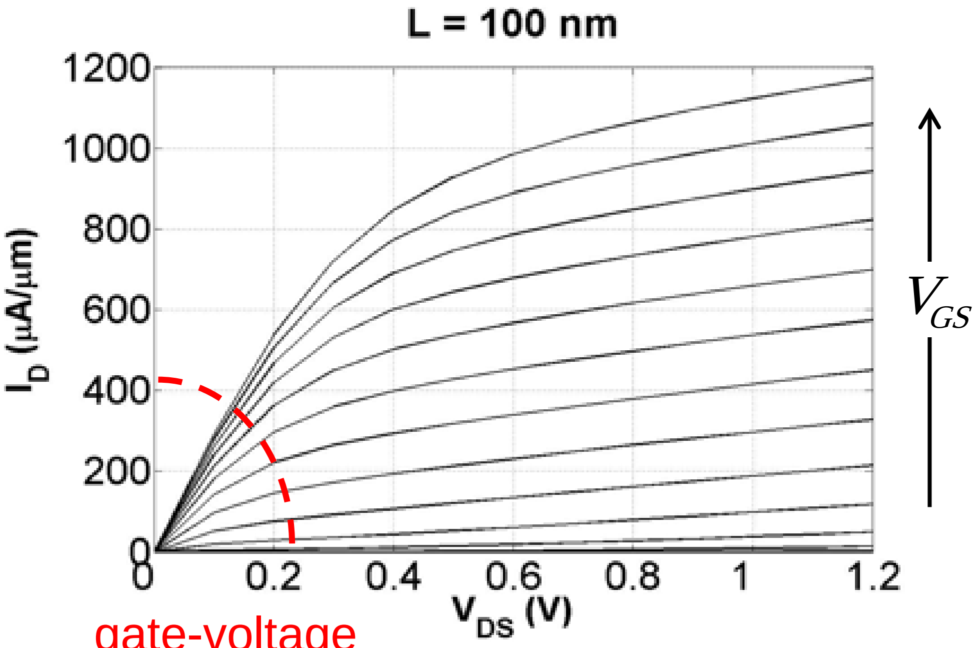
$$C \equiv \frac{Q}{V} \quad \mathrm{F}$$

MOS electrostatics

$$\begin{cases} Q_n \approx -C_{ox}\left(V_{GS} - V_T\right) & \mathrm{C/m^2} \\ Q_n \approx 0 & \left(V_{GS} < V_T\right) \\ C_{ox} = \dfrac{\kappa_{ox}\varepsilon_0}{t_{ox}} & \mathrm{F/cm^2} \end{cases}$$

MOSFET IV: low V_{DS}





gate-voltage controlled resistor

$$I_D = -W Q_n(x) \langle \upsilon_x(x) \rangle$$

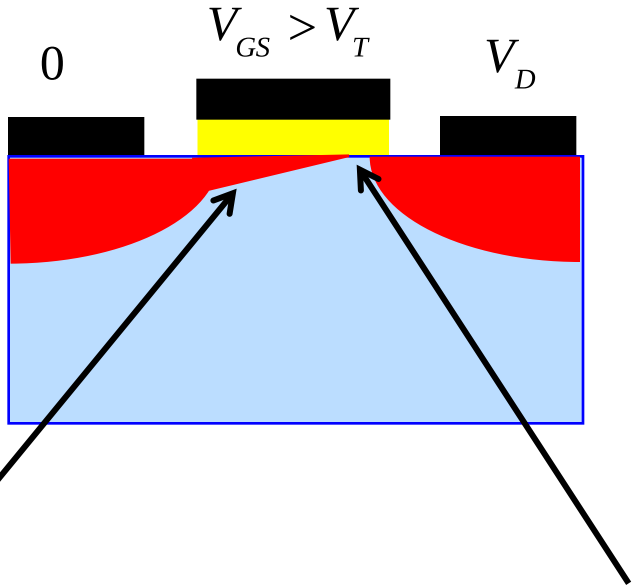
$$Q_n = -C_{ox}(V_{GS} - V_T)$$

$$\langle \upsilon(x) \rangle = -\mu_{eff} \mathcal{E}_x$$

$$\mathcal{E}_x = -V_{DS}/L$$

$$\boxed{I_D = \frac{W}{L} \mu_{eff} C_{ox} (V_{GS} - V_T) V_{DS}}$$

MOSFET IV: “pinch-off” at high V_{DS}



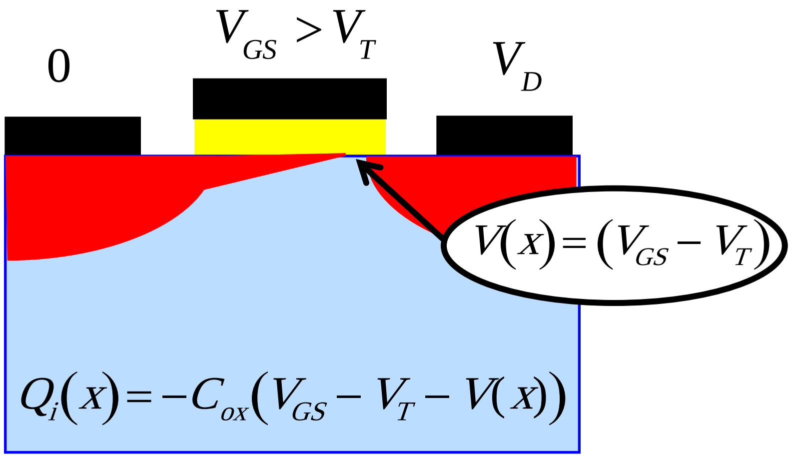
$$Q_n(x) = -C_{ox}\left(V_{GS} - V_T - V(x)\right)$$

$$V(x) = \left(V_{GS} - V_T\right)$$

$$Q_n(x) \approx 0$$

Note: thickness of channel illustrates the number of electrons – not the actual thickness.

MOSFET IV: high V_{DS}



$$V(x) = (V_{GS} - V_T)$$

$$Q_i(x) = -C_{ox}(V_{GS} - V_T - V(x))$$

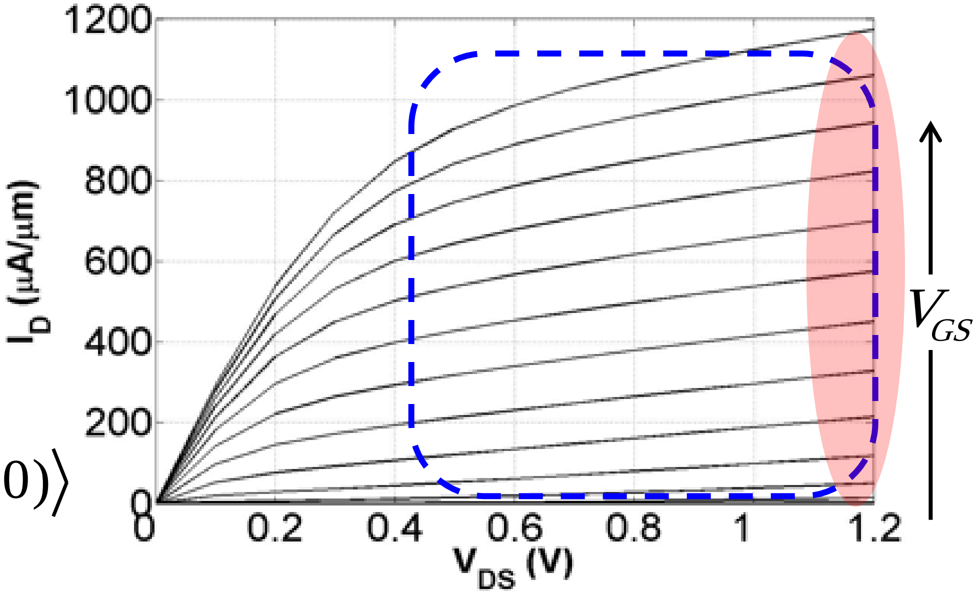
$$I_D = -WQ_i(x)\langle \upsilon_x(x)\rangle = WQ_i(0)\langle \upsilon_x(0)\rangle$$

$$Q_n(0) = -C_{ox}(V_{GS} - V_T)$$

$$\langle \upsilon(0)\rangle = -\mu_{eff}\mathcal{E}_x(0)$$

$$\mathcal{E}_x(0) \approx -(V_{GS} - V_T)/L$$

gate-voltage controlled current source



$$I_D = \frac{W}{2L}\mu_{eff}C_{ox}(V_{GS} - V_T)^2$$

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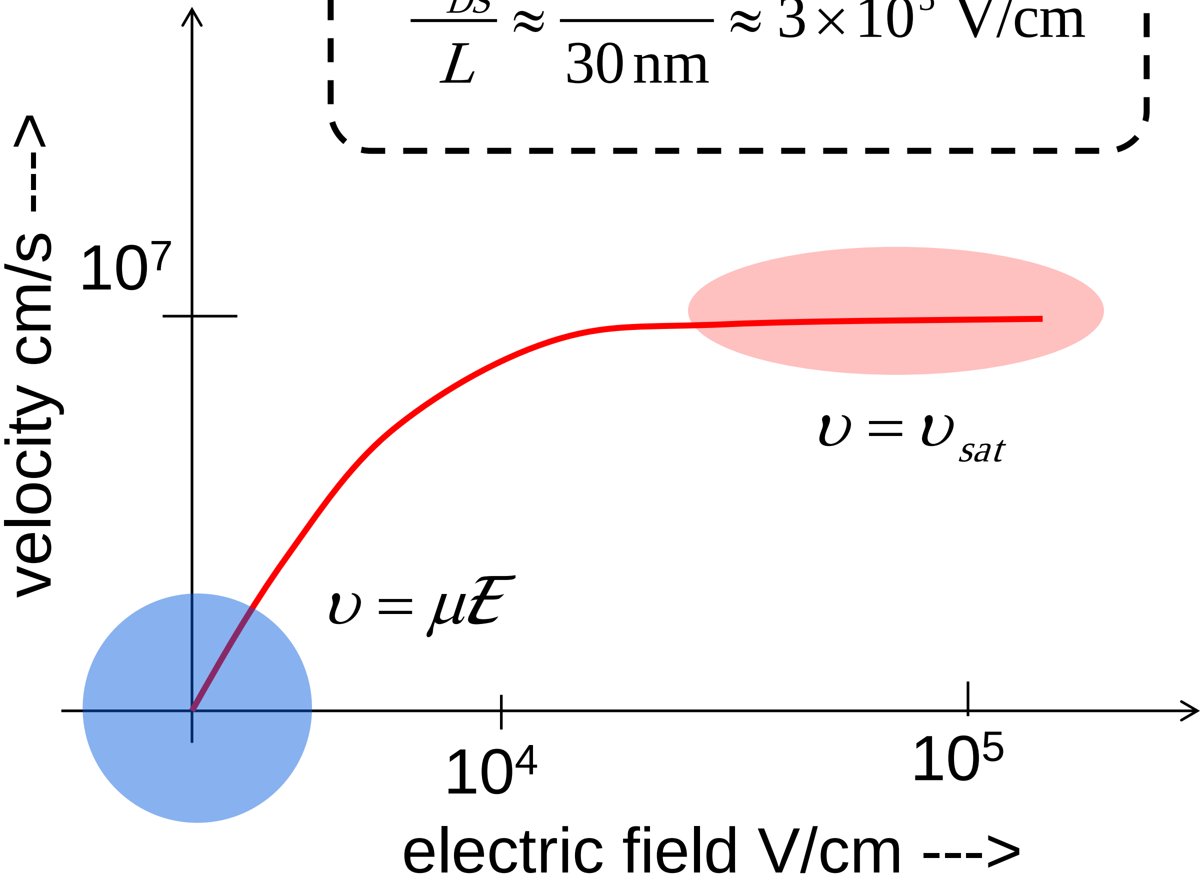
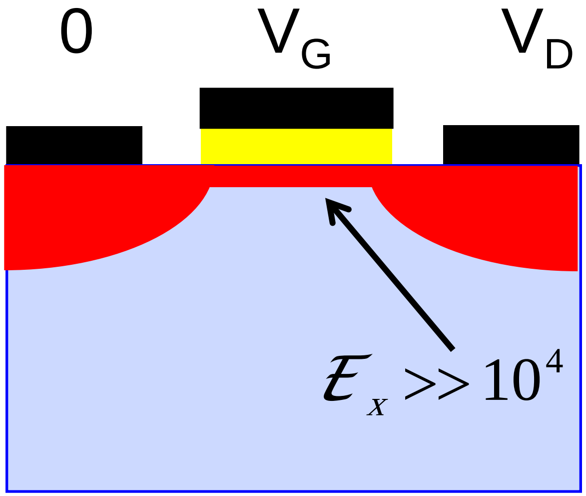
velocity saturation

$$\frac{V_{DS}}{L} \approx \frac{1.0\,\mathrm{V}}{30\,\mathrm{nm}} \approx 3 \times 10^{5}\ \mathrm{V/cm}$$



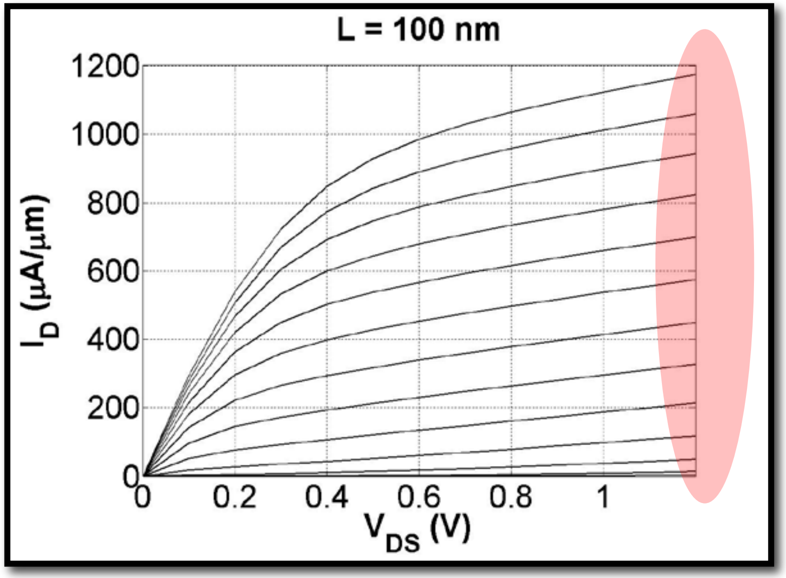
MOSFET IV: velocity saturation



$$I_D = -WQ_n(x)\langle\upsilon_x(x)\rangle$$

$$Q_n = -C_{ox}(V_{GS} - V_T)$$

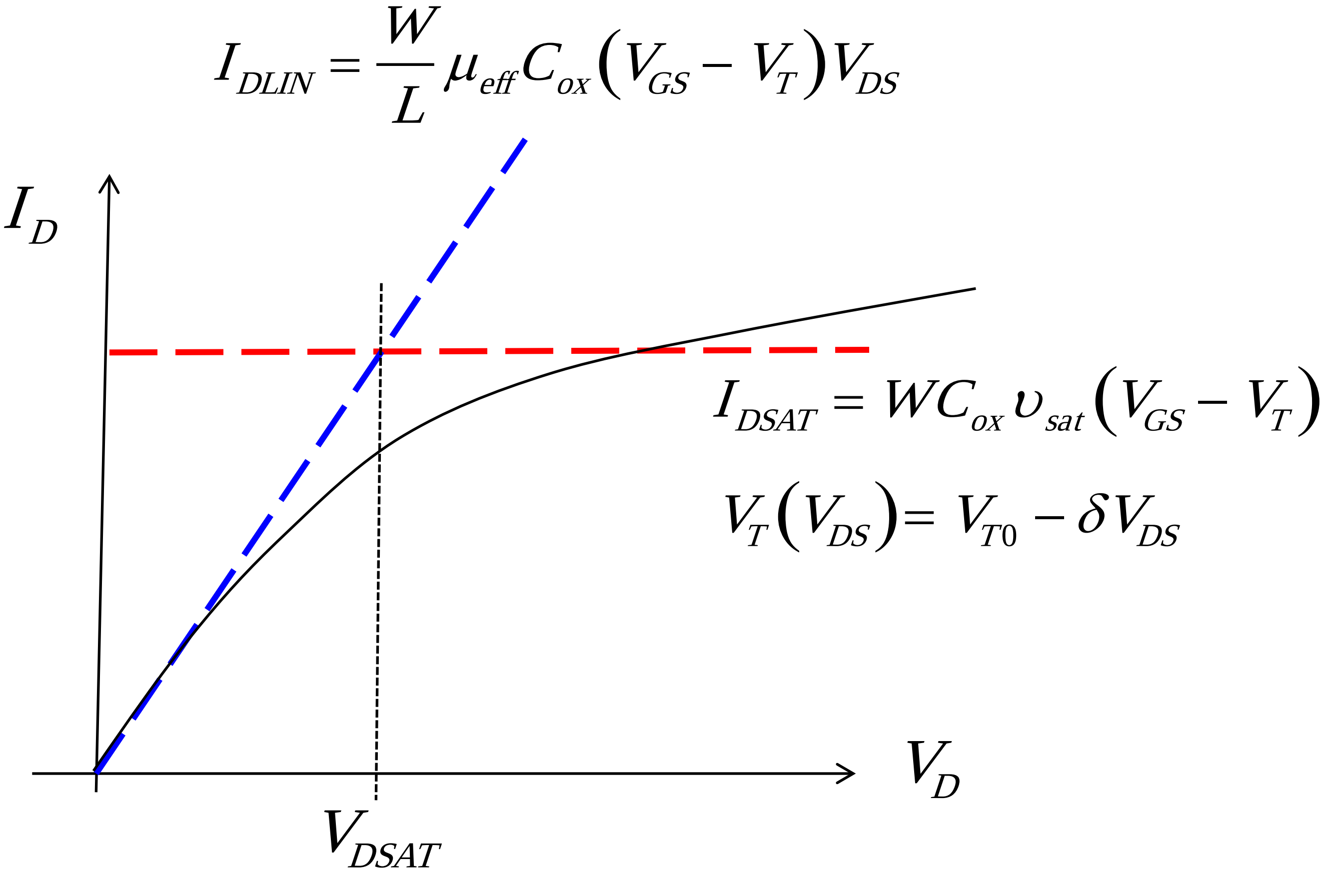
$$\langle\upsilon_x\rangle = \upsilon_{sat}$$



(Courtesy, Shuji Ikeda, ATDF, Dec. 2007)

$$\boxed{I_D = WC_{ox}\upsilon_{sat}(V_{GS} - V_T)}$$

MOSFET: IV (re-cap)



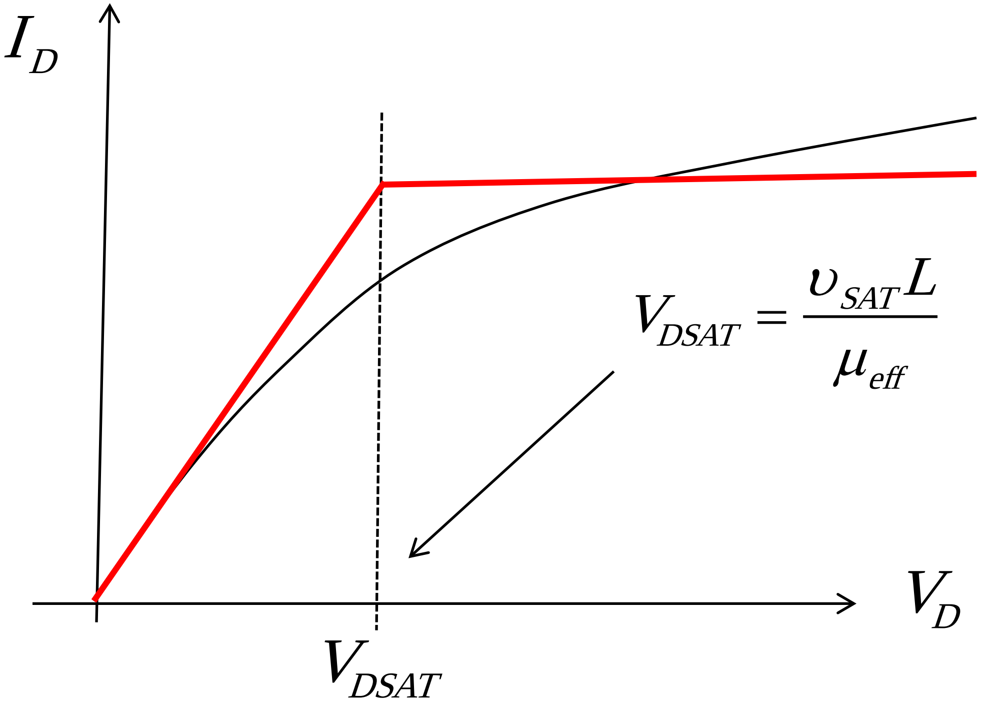
$$I_{DLIN} = \frac{W}{L}\mu_{eff}C_{ox}\left(V_{GS} - V_T\right)V_{DS}$$

$$I_{DSAT} = WC_{ox}\upsilon_{sat}\left(V_{GS} - V_T\right)$$

$$V_T\left(V_{DS}\right) = V_{T0} - \delta V_{DS}$$

We have developed a 2-piece approximation to the MOSFET IV characteristic.

2-piece model for $I_D(V_G, V_D)$



$$V_{DSAT} = \frac{\upsilon_{SAT} L}{\mu_{eff}}$$

$$V_D \leq V_{DSAT} : \; I_D = I_{DLIN}$$

$$V_D > V_{DSAT} : \; I_D = I_{DSAT}$$

$$I_{DLIN} = \frac{W}{L} \mu_{eff} C_{ox} \left(V_G - V_T \right) V_D$$

$$I_{DSAT} = W C_{ox} \upsilon_{sat} \left(V_G - V_T \right)$$

Can we do better?

model for $I_D(V_G, V_D)$

Small V_{DS}

Large V_{DS}

$$I_{DLIN} = \frac{W}{L}\mu_{eff} C_{ox}\left(V_G - V_T\right)V_D$$

$$I_{DSAT} = W C_{ox} \upsilon_{sat}\left(V_G - V_T\right)$$

$$I_{DLIN}/W = C_{ox}\left(V_G - V_T\right)\left(\mu_{eff}\frac{V_D}{L}\right)$$

$$I_{DSAT}/W = C_{ox}\left(V_G - V_T\right)\upsilon_{sat}$$

$$I_{DLIN}/W = Q_n\left(V_G\right)\left\langle \upsilon\left(V_D\right)\right\rangle$$

$$I_{DSAT}/W = Q_n\left(V_G\right)\left\langle \upsilon\left(V_D\right)\right\rangle$$

$$\left\langle \upsilon\left(V_D\right)\right\rangle = \left(\mu_{eff}\frac{V_D}{L}\right)$$

$$\left\langle \upsilon\left(V_D\right)\right\rangle = \upsilon_{SAT}$$

model for $I_D(V_G, V_D)$

$$I_D/W = Q_S(V_G)\langle \upsilon(V_D)\rangle$$

$$V_G \geq V_T: \quad Q_n(V_G) = -C_{ox}(V_G - V_T) \qquad V_D \leq V_{DSAT}: \langle \upsilon(V_D)\rangle = \left(\mu_{eff}\frac{V_D}{L}\right)$$

$$V_G < V_T: \quad Q_n(V_G) = 0 \qquad V_D > V_{DSAT}: \langle \upsilon(V_D)\rangle = \upsilon_{SAT}$$

If we can make the average velocity go smoothly from the low V_D to high V_D limits, then we will have a smooth model for $I_D(V_G, V_D)$.

empirical model for $I_D(V_G, V_D)$

$$\langle \upsilon(V_D) \rangle = F_{SAT}(V_D)\upsilon_{SAT}$$

$$F_{SAT}(V_D) \equiv \frac{V_D / V_{DSAT}}{\left[1 + \left(V_D / V_{DSAT}\right)^{\beta}\right]^{1/\beta}}$$

$$V_D << V_{DSAT} : F_{SAT}(V_D) \rightarrow \frac{V_D}{V_{DSAT}}$$

$$\langle \upsilon(V_D) \rangle \rightarrow \frac{V_D}{V_{DSAT}} \upsilon_{SAT}$$

$$\langle \upsilon(V_D) \rangle \rightarrow \frac{V_D}{\upsilon_{SAT} L / \mu_{eff}} \upsilon_{SAT}$$

$$\langle \upsilon(V_D) \rangle \rightarrow \mu_{eff} \frac{V_D}{L}$$ ✓

$$V_D >> V_{DSAT} : F_{SAT}(V_D) \rightarrow 1$$

$$\langle \upsilon(V_D) \rangle \rightarrow \upsilon_{SAT}$$ ✓

understanding the saturating function: $F_{SAT}(V_D)$

$$\frac{1}{\langle \upsilon(V_D)\rangle} = \frac{1}{\mu_{eff} V_D / L} + \frac{1}{\upsilon_{SAT}} \rightarrow \langle \upsilon(V_D)\rangle = \left[\frac{V_D/V_{DSAT}}{1+V_D/V_{DSAT}}\right]\upsilon_{SAT}$$

$$\langle \upsilon(V_D)\rangle = F_{SAT}(V_D)\upsilon_{SAT} \qquad F_{SAT}(V_D) = \frac{V_D/V_{DSAT}}{\left[1+(V_D/V_{DSAT})^{\beta}\right]^{1/\beta}}$$

The extra parameter, β, is empirically adjusted to fit the IV characteristic. Typically, $\beta \approx 1.6 - 1.8$

saturating function: $F_{SAT}(V_D)$

$$\langle \upsilon(V_D) \rangle = F_{SAT}(V_D)\,\upsilon_{SAT}$$

$$F_{SAT}(V_D) = \frac{V_D / V_{DSAT}}{\left[1 + \left(V_D / V_{DSAT}\right)^{\beta}\right]^{1/\beta}}$$

Although this is just an empirical method to produce smooth curve that properly goes between the small and large V_D limits, it works very well in practice, which suggests that it captures something important about MOSFETs.

level 0 “Virtual Source model”

1) $I_D/W = Q_n(V_G)\langle \upsilon(V_D)\rangle$

2) $V_{GS} \le V_T: \quad Q_n(V_{GS}) = 0$

$V_{GS} > V_T: \quad Q_n(V_{GS}) = C_{ox}(V_{GS} - V_T)$

3) $\langle \upsilon(V_D)\rangle = F_{SAT}(V_D)\upsilon_{SAT}$

4) $F_{SAT}(V_D) = \dfrac{V_D/V_{DSAT}}{\left[1+(V_D/V_{DSAT})^{\beta}\right]^{1/\beta}}$

5) $V_{DSAT} = \dfrac{\upsilon_{SAT}L}{\mu_{eff}}$

With this simple model, we can compute reasonable MOSFET IV characteristics, and the model can be extended step by step to make it more and more realistic.

There are only 5 device-specific input parameters to this model:

$$C_{ox}, V_{T,}\upsilon_{SAT}, \mu_{eff}, L$$

discussion

The model we have outlined is based on physics that is valid for long channel MOSFETs from the 1960’s, 70’s, and early 80’s. For nanotransistors, we need to make some changes. Surprisingly, the changes are minor:

1) The saturation velocity for high-field transport in bulk semiconductors is replaced by the so-called “injection velocity”.

2) The effective mobility for carriers in the inversion layer of a long channel MOSFET is replaced by the “apparent mobility”.

(Effects such as subthreshold conduction, DIBL, quantum capacitance also need to be considered.)

goals

Our goal is a simple, clear understanding of the physics of nanoscale MOSFETs along with a simple quantitative model (even if semi-empirical) to analyze and design nanotransistors.

references

For a discussion of velocity saturation in bulk semiconductors, see:

M. Lundstrom, “Electronic Transport in Semiconductors,” Lecture 36, Fall 2011. http://nanohub.org/resources/11872

The virtual source model is described in:

Ali Khakifirooz, Member, Osama M. Nayfeh, and Dimitri Antoniadis, “A Simple Semiempirical Short-Channel MOSFET Current–Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters, “ *IEEE Transactions on Electron Devices*, Vol. 56, pp. 1674-1680, 2009.