

#### ECE 595Z Digital VLSI Design Automation

#### Module 5 (Lectures 14-20): Multi-level Synthesis Lecture 18



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#### Lecture 17: Re-cap

- Can we go beyond the Algebraic Model?
- The algebraic model enables efficient (**fast**) transformations of a Boolean network
  - Collapsing/elimination, extraction/decomposition, substitution, ...
- However, it is limited in the **scope of optimization** since it does not take advantage of the unique properties of Boolean algebra.

## Lecture #17: Re-cap

- Boolean Division
  - Boolean division and factoring are much harder than algebraic counterparts
  - Number of Boolean divisors/factors can be very large
  - Boolean division can be indirectly performed using 2-level minimization
- Boolean Optimization Using Implicit Don't Cares
  - Implicit don't cares are introduced due to the network itself
  - We saw how to derive don't cares at a node's inputs by looking at it's fanin nodes
  - A node can be simplified using its implicit don't cares

## Informal Introduction to DCs: Example



- Look at "impossible" values of a, b, X
- Project to the inputs of the node f
- Use projected DCs to simplify node f



possible?

abX

000

001

010

011

100

101

110

111

• What if we know even more about the network?





- Let's add information about the nodes "after" f
- When does the output of f actually "matter" to the primary output Z?







 Can we simplify f further now using ALL the don't cares we have identified?





- What happened?
  - f and Y were redundant due to the context imposed by the Boolean network!



# Summary : Implicit Don't Cares

- Arise due to constraints imposed by the Boolean network on each of it's nodes
- Satisfiability don't cares
  - Caused due to combinations of input values to a node that can never occur
- Observability don't cares
  - Caused due to input combinations that make the node's output un-observable at the circuit's primary outputs

# Satisfiability Don't Cares

- Given a Boolean network with n primary inputs and k nodes
- The "state" of the circuit is the set of values on all inputs and node outputs
  - $v \in B^{n+k}$
  - However, not all points in  $B^{n+k}$  are feasible
    - Only B<sup>n</sup> are feasible (input values fully determine circuit state)
  - The remaining points are called Satisfiability Don't Cares (SDCs)



# Satisfiability Don't Cares

- Finding the SDCs of a Boolean network
  - For each node, list inconsistent assignments of inputs and outputs
    - Example: y<sub>i</sub> = ab
    - $SDC_i = y_i'ab + y_ia' + y_ib'$
  - SDC =  $U_i$  SDC<sub>i</sub> for i ∈ all nodes in the network
  - Not specific to a node
- The set of all SDCs is <u>huge</u> for practical sized networks



## **Observability Don't Cares**

- Some terminology
- Given a node i in a Boolean network
  - Let  $y_i$  be a literal representing the output of node i
  - Let g<sub>i</sub> be the **local function** at node i, *i.e.*, the node output expressed in terms of the node inputs
  - Let G<sub>i</sub> be the global function at node i, *i.e.*, the node output in terms of the circuit's primary inputs



## **Observability Don't Cares**

- Remember Co-factors?
  - Here's a chance to apply them!
- Let  $PO_j$ ,  $j \in \{1 \dots m\}$  be the primary outputs
- For input values where
   (G<sub>POj</sub>)<sub>yi</sub> = (G<sub>POj</sub>)<sub>yi</sub>, the node
   output is not observable at
   PO<sub>j</sub>
  - This is an observability don't care for node i w.r.t PO<sub>i</sub>
- The ODC for node i is given by

$$- \text{ ODC}_{i} = \bigcap_{j} ((G_{PO_{j}})_{y_{i}} = (G_{PO_{j}})_{y_{i}})$$



## **Optimization Using Implicit Don't Cares**

- General idea: Use two-level minimization for the SOP expressions in each node of the network
  - Boolean division
  - Node simplification

# **Boolean Division using DCs**

- For a given node in a Boolean network
  - g<sub>i</sub>: local function at the node
  - SDC and ODC<sub>i</sub> (in terms of all the variables of the network)
- Think of all nodes as functions of all the variables (not just the local inputs)
- Perform two-level minimization using SDC  $\cup$  ODC<sub>i</sub> as the don't care set
- Net effect of this is simultaneous Boolean division of  $g_i$  by all other nodes in the network
- **PROBLEM**: This can introduce combinational cycles into the network!
  - Solution: When optimizing node i, do not include SDC<sub>i</sub> and SDCs of all the nodes in the transitive fanout of node i



# Node Simplification using DCs

- Again, use two-level minimization using SDC and ODC
  - To perform (local) node optimization, DCs need to be specified only in terms of the node's inputs
  - However, SDC and  $ODC_i$  are in terms of ALL variables in the network!
    - Need to eliminate variables other than node inputs
- **Question**: Which operations (that we learned in class) have the effect of eliminating a variable from a function?
  - Answers: \_\_\_\_\_
- **Question**: Which one should we use here?
  - Answer: \_\_\_\_\_

## Quantification

- Two more functions of Shannon cofactors
  - $f_{x_i}$ .  $f_{x_i'} = 1$  specifies when f = 1 independent of the value of  $x_i$ 
    - $f(x_1 \dots x_{i-1}, \mathbf{x_i} = \mathbf{1}, x_{i+1} \dots x_n) = \mathbf{1} \text{ AND}$  $f(x_1 \dots x_{i-1}, \mathbf{x_i} = \mathbf{0}, x_{i+1} \dots x_n) = \mathbf{1}$

$$\forall x(f) = f_x \cdot f_{x'}$$

- Called Universal quantification or Consensus
- $f_x + f_{x'} = 1$  specifies when f = 1 for at least one value of  $x_i$

$$f(x_1 \dots x_{i-1}, x_i = 1, x_{i+1} \dots x_n) = 1 \text{ OR}$$

$$f(x_1 \dots x_{i-1}, \mathbf{x_i} = \mathbf{0}, x_{i+1} \dots x_n) = 1$$

 $\exists x(f) = f_x + f_{x'}$ 

 Called Existential quantification or Smoothing

#### Node Simplification using DCs: Example

- Example
  - SDC<sub>X</sub> = Xa' + Xb' + X'ab
    - Eliminating a from SDC<sub>X</sub>:
  - SDC<sub>Y</sub> = Yb'c' + Y'b + Y'c
    - Eliminating c from SDC<sub>Y</sub>:

DCs used to simplify node f :



## **Practical Considerations**

- Computing and representing the entire set of SDCs and ODCs can be very slow and require a lot of memory
  - Even using implicit representations like BDDs
- In practice
  - Do not attempt to compute the complete DC set.
    - Look at a limited size "environment" of the node
  - Use "filters" to only compute relevant DCs.



#### Further Reading : Don't Cares

- De Micheli, Chapter 8.4.1
- Hachtel & Somenzi, Chapter 11.3

- NOTE: De Micheli uses the term "Controllability Don't Cares" for SDCs
  - Strictly speaking, CDCs = SDCs U
    Explicit don't cares specified on primary inputs

#### **Prime and Irredundant Networks**

- Recall that each node in the Boolean network is represented by an SOP expression or a cover
- The node is **locally prime and irredundant (PI)** if no literal or cube can be deleted from the SOP expression without changing the local function
- The node is **prime and irredundant w.r.t. the entire network** if no literal or cube can be deleted from the SOP expression without changing the global function for some primary output
- Question: Which of the above two conditions is stricter?
- A **Boolean network is prime and irredundant** if each node is PI w.r.t. the network

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#### **Prime and Irredundant Networks**

• Example



Are g1, g2, and g3 locally prime and irredundant?

Are g1, g2, and g3 prime and irredundant w.r.t. the network?

#### **Prime and Irredundant Networks**

- **Theorem**: If the SOP expression for a node g<sub>i</sub> in a Boolean network is made prime and irredundant using SDC and ODC<sub>i</sub>, then it is prime and irredundant w.r.t. the network
- Prime and irredundant networks are desirable for multiple reasons

# Multi-level Minimization and Testability

- Recall that we would like to test fabricated instances for manufacturing defects
  - Need to generate test vectors
  - Commonly used: Stuck-at fault model



• **Theorem**: A prime and irredundant Boolean network is 100% testable for single stuck-at faults at all node inputs and outputs

- Test vector exists to detect each stuck-at fault

• **Theorem**: Algebraic transformations preserve single stuck-at fault testability (and the test set!)

# Other Approaches to Boolean Optimization

- Perturbation
  - Change the local function at a node from g<sub>i</sub> to h<sub>i</sub>
    - OK if  $g_i \bigoplus h_i \subseteq (SDC \cup ODC_i)$
- Redundancy Addition and Removal
  - Identify redundant s-at faults
  - Simplify circuit by propagating "constant" values
  - Add redundant connections to create new opportunities
    - Use don't cares to ensure that added connections do not change a function at the primary outputs



