Quick Start for the nanoHUB VS Tool: MIT Virtual-Source Tool
http://nanohub.org/resources/vsmod

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The MIT Virtual-Source tool on nanoHUB.org implements the MIT virtual source transistor model [1]. This document is a quick guide to the tool.

1. **MIT VS Model: Input Parameters**
2. **List of Examples**

1. MIT VS Model: Input Parameters

For a basic description of the MIT VS Model, see [1]. The model has subsequently evolved a bit and now has some features not described in [1].

The input parameters for the VS model are listed below. Different notation for these parameters is used in different papers and by different authors. The particular form used in the MIT Virtual-Source tool is consistent with the online course, Nanoscale Transistors, by M.S. Lundstrom (https://nanohub.org/groups/u).

Parameters:

L_E	The effective channel length, L_E, is determined from $L_E = L_G - 2 \times L_{ov}$, where L_G is the physical gate length and L_{OV} is the overlap length. If L_{OV} is not given, it is usually chosen to be $0.15 \times L_G$ for Si MOSFETs.
C_{INV}	The gate-to-channel capacitance per unit area under strong inversion (at $V_{GS} = V_{DD}$) in micro Farad $/\text{cm}^2$.
I_{SUB}	The subthreshold current at a specific bias point (V_{GS}, V_{DS}). Typically $V_{GS} = 0$ V and $V_{DS} = 0.05$V. The threshold voltage, V_T, can be calculated from $I_{SUB}(V_{GS}, V_{DS})$.
$V_{GS}(I_{SUB})$	Gate voltage at which I_{SUB} is measured.
$V_{DS}(I_{SUB})$	Drain voltage at which I_{SUB} is measured.

DIBL	The drain-induced barrier lowering in mV/V (in principle, DIBL depends on V_{DS}, this dependency is ignored in this tool). Note also that $V_T = V_{T0} - DIBL \times V_{DS}$, so from I_{SUB} and DIBL, we can also determine V_{TO}.
S_1	Value of the subthreshold swing in mV/decade at V_{DS1}.
$V_{DS}(S_1)$	Drain voltage at which S_1 is measured.
S_2	Value of the subthreshold swing in mV/decade at V_{DS2}.
$V_{DS}(S_2)$	Drain voltage at which S_2 is measured.

Typically $V_{DS}(S_1)$ = 0.05 V and $V_{DS}(S_2) = V_{DD}$. The subthreshold swing is related to a voltage divider parameter, *m*, according to

$$S = 2.3m\frac{k_B T_L}{q} .$$

The parameter, *m*, can be voltage dependent. It is modeled as

$$m = m_0 - \frac{dm}{dV_{DS}} V_{DS} .$$

The two parameters, m_0, and dm/dV_{DS}, are determined from the two values of *S*.

R_{SD}	The sum of the gate voltage independent source and drain series resistances, $R_{SD} = R_S + R_D$, in Ω-um.
μ_{app}	The so-called "apparent" mobility in cm^2/V–s, which includes the effects of the real inversion layer mobility, μ_{eff}, and the so-called ballistic mobility, μ_B, according to $\frac{1}{\mu_{app}} = \frac{1}{\mu_{eff}} = \frac{1}{\mu_B}$.
VS_Velocity	The average carrier velocity at the virtual source.
β	Parameter in the "saturation function" that controls the transition from linear to saturation regions of operation. Typically, $\beta = 1.8$ for N-FETs and $\beta = 1.4$ for P-FETs.

T	The environmental temperature. Usually T is set to be room temperature 300 K.
α	Parameter in the "inversion transition function" that controls the transition of the surface potential between weak and strong inversion regions of operation. Typically, $\alpha = 3.5$ works well for both N-FETs and P-FETs. This parameter is often fixed and not taken as an adjustable parameter.

2. List of Examples

Several examples of parameter sets for bulk and SOI silicon MOSFETs are listed below, along with references that describe these devices. Moreover, one example of experimental data sets for bulk silicon MOSFET is also included here.

Ex. 1: 65 nm NFET (ref. [1])

L_E (nm)	25
C_{INV} (uF/cm2)	1.83
I_{SUB} (nA/um)	4.46
V_{GS} (ISUB) (V)	0
V_{DS} (ISUB) (V)	0.05
DIBL (V/V)	0.12
S_1 (mV/dec)	100
V_{DS} (S_1) (V)	0.05
S_2 (mV/dec)	100
V_{DS} (S_2) (V)	1.2
R_{SD} (Ω-um)	150
u_{APP} (cm^2/V–s)	250
VS_Velocity ($1e^6$ cm/s)	14
β	1.8
T (K)	300
α	3.5

Ex. 2: 65 nm PFET (ref. [1])

L_E (nm)	25
C_{INV} (uF/cm2)	1.7
I_{SUB} (nA/um)	1.56
V_{GS} (ISUB) (V)	0
V_{DS} (ISUB) (V)	-0.05
DIBL (V/V)	0.155
S_1 (mV/dec)	95
V_{DS} (S_1) (V)	-0.05

$S2$ (mV/dec)	95
V_{DS} ($S2$) (V)	-1.2
R_{SD} (Ω-um)	260
u_{APP} ($cm^2/V-s$)	140
VS_Velocity ($1e^6$ cm/s)	8.5
β	1.8
T (K)	300
α	3.5

Ex. 3: 32 nm NFET (ref. [1])

L_E (nm)	22
C_{INV} (uF/cm2)	2.65
I_{SUB} (nA/um)	9.89
V_{GS} (ISUB) (V)	0
V_{DS} (ISUB) (V)	0.05
DIBL (V/V)	0.13
$S1$ (mV/dec)	98
V_{DS} ($S1$) (V)	0.05
$S2$ (mV/dec)	98
V_{DS} ($S2$) (V)	1.2
R_{SD} (Ω-um)	160
u_{APP} ($cm^2/V-s$)	250
VS_Velocity ($1e^6$ cm/s)	13.5
β	1.8
T (K)	300
α	3.5

Ex. 4: 32 nm PFET (ref. [1])

L_E (nm)	22
C_{INV} (uF/cm2)	2.6
I_{SUB} (nA/um)	3.13
V_{GS} (ISUB) (V)	0
V_{DS} (ISUB) (V)	-0.05
DIBL (V/V)	0.145
$S1$ (mV/dec)	95
V_{DS} ($S1$) (V)	-0.05
$S2$ (mV/dec)	95
V_{DS} ($S2$) (V)	-1.2
R_{SD} (Ω-um)	160
u_{APP} ($cm^2/V-s$)	210
VS_Velocity ($1e^6$ cm/s)	10.3
β	1.7
T (K)	300
α	3.5

Ex. 5: 30 nm ETSOI (refs. [2], [3])

L_E (nm)	30
C_{INV} (uF/cm2)	2
I_{SUB} (nA/um)	2.12
V_{GS} (ISUB) (V)	-0.5
V_{DS} (ISUB) (V)	0.05
DIBL (V/V)	0.06
S_1 (mV/dec)	75.2
V_{DS} (S_1) (V)	0.05
S_2 (mV/dec)	100
V_{DS} (S_2) (V)	1.2
R_{SD} (Ω-um)	260
u_{APP} (cm^2/V–s)	220
VS_Velocity ($1e^6$ cm/s)	8.2
β	1.9
T (K)	300
α	3.5

Ex. 6: 60 nm bulk NFET

The I-V data is supplied and can be fit with the VS model.

References:

[1] Ali Khakifirooz, Member, IEEE, Osama M. Nayfeh, Member, IEEE, and Dimitri Antoniadis, "A Simple Semiempirical Short-Channel MOSFET Current–Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters, *IEEE Trans. Electron Dev*., **56**, 1674, 2009.

[2] A . Majumdar, Z. Ren, S. J. Koester, and W. Haensch, "Undoped-body, extremely-thin SOI MOSFETs with back gates," *IEEE Trans. on Electron Devices*, **56**, pp. 2270-2276, 2009.

[3] A. Majumdar, X. Wang, A. Kumar, J. R. Holt, D. Dobuzinsky, R. Venigalla, C. Ouyang, S. J. Koester, and W. Haensch, "Gate length and performance scaling of undoped-body, extremely thin SOI MOSFETs," *IEEE Electron Device Lett.,* **30**, pp. 413-415, 2009.