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ECE695: Reliability Physics of Nano-Transistors

Lecture 15: Off-state HCI degradation

Muhammad Ashraful Alam
alam@purdue.edu

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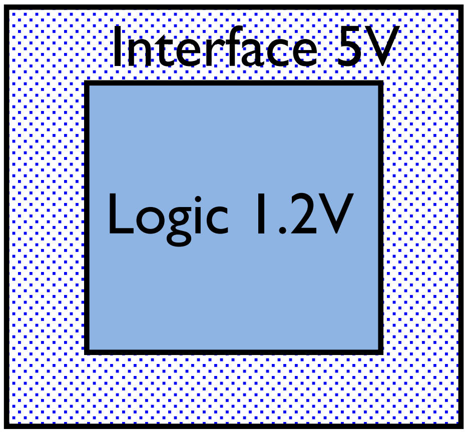
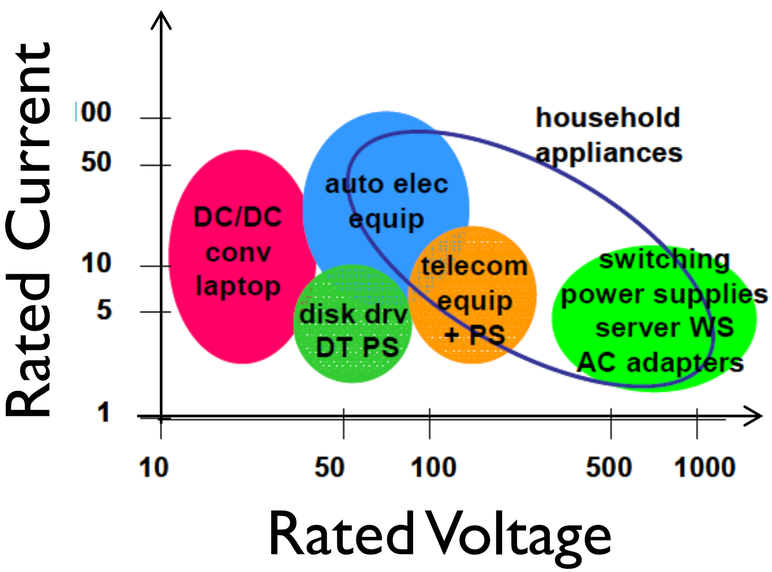
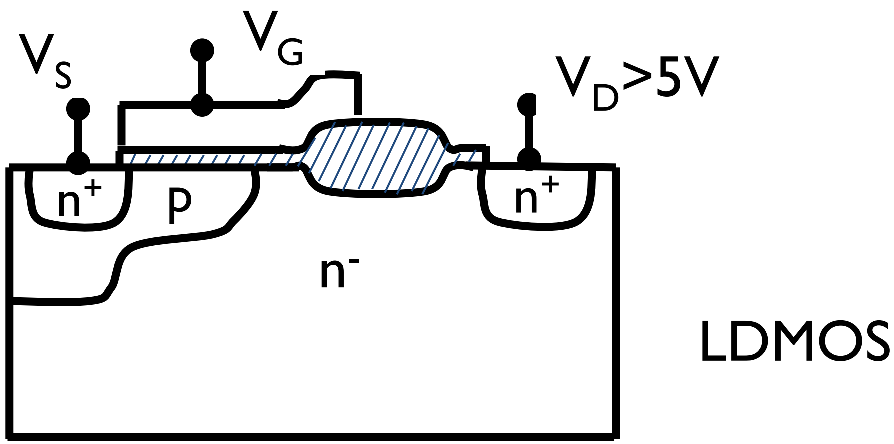
Outline

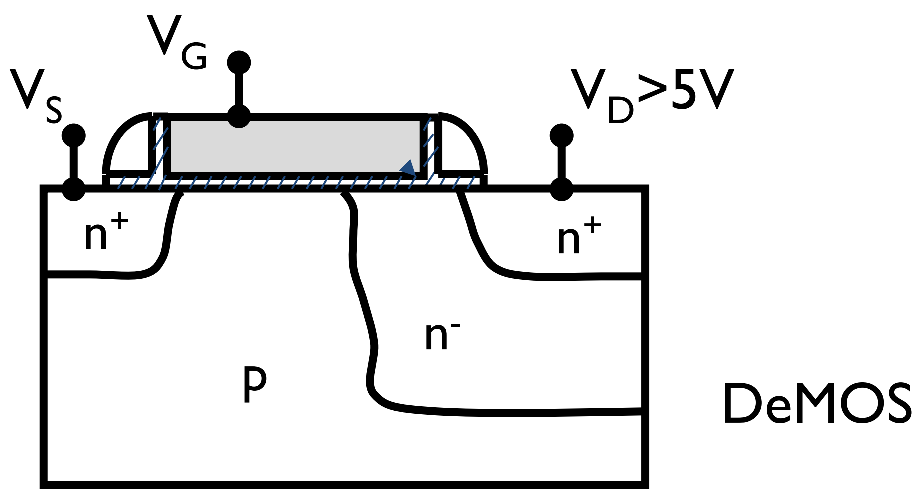
1. ON vs. OFF State HCI Degradation
2. Origin of hot carriers at off-state
3. SiH vs. SiO – who is getting broken?
4. Voltage acceleration factors by scaling
5. Conclusions

HCI degradation in non-logic transistors



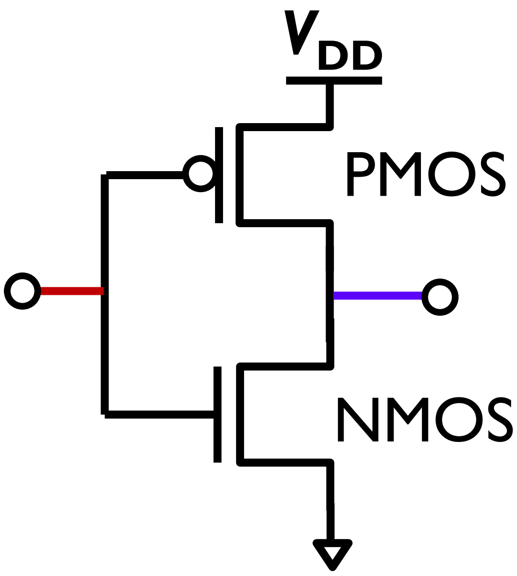


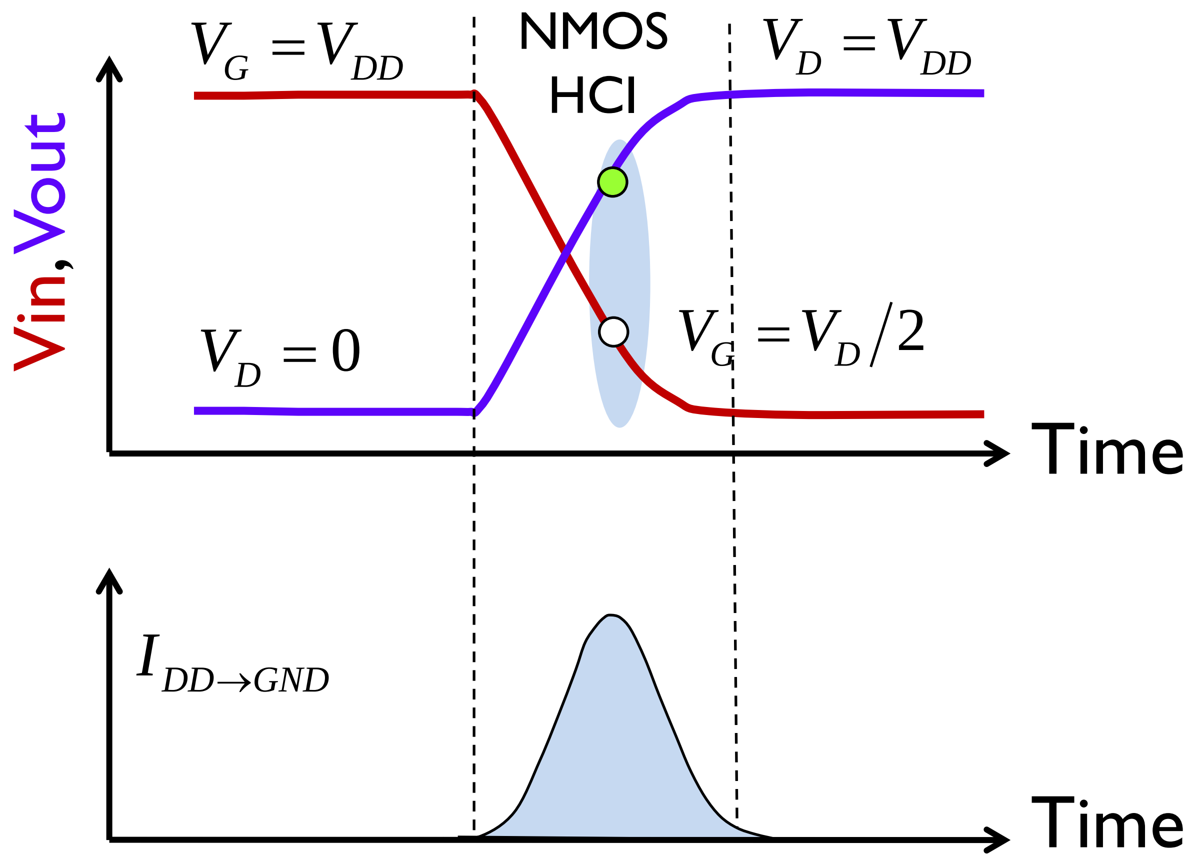




P. Hower et al., IEDM 2010, 13.1.1

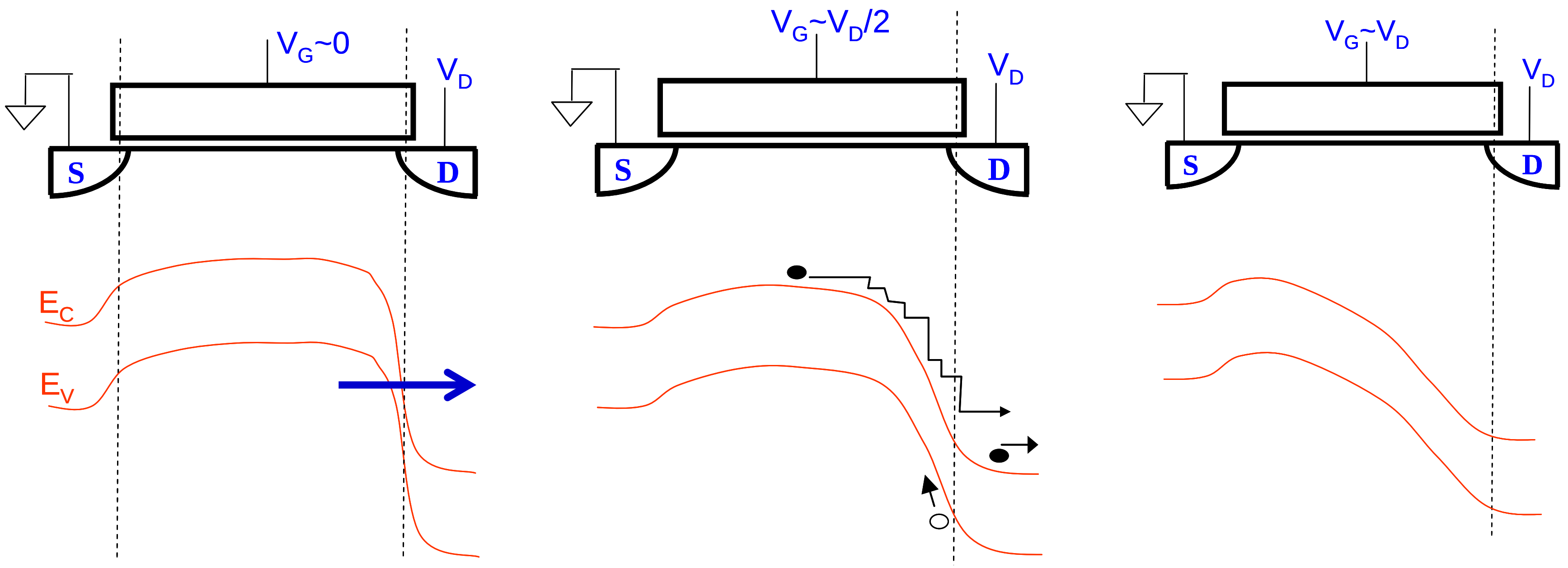
Classical HCI … only ON state?!





True only for logic transistor, at relatively low operating voltage

OFF state HCI is possible, if …



… large band-to-band tunneling at high VD

OR as parasitic degradation in accelerated tests of logic transistors

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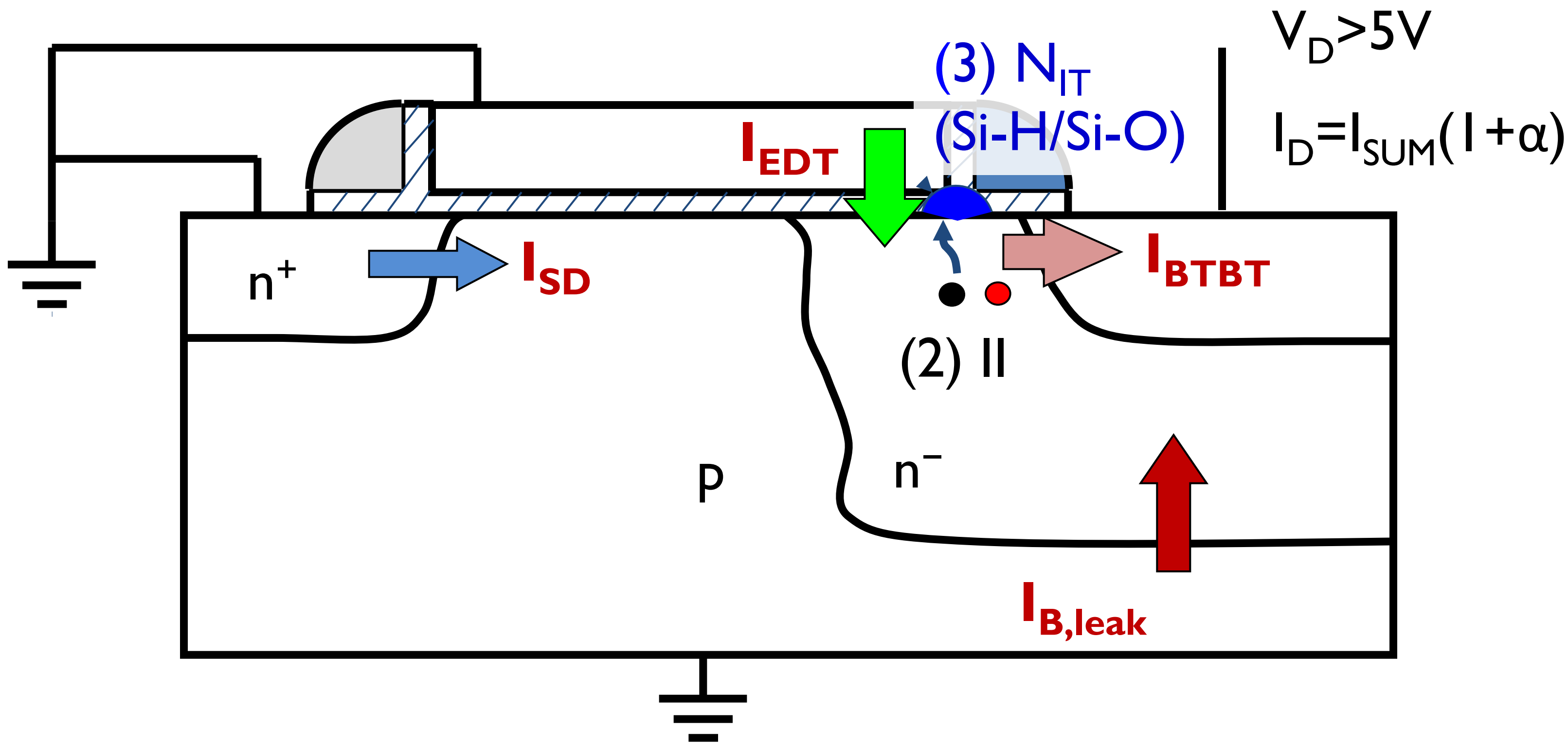
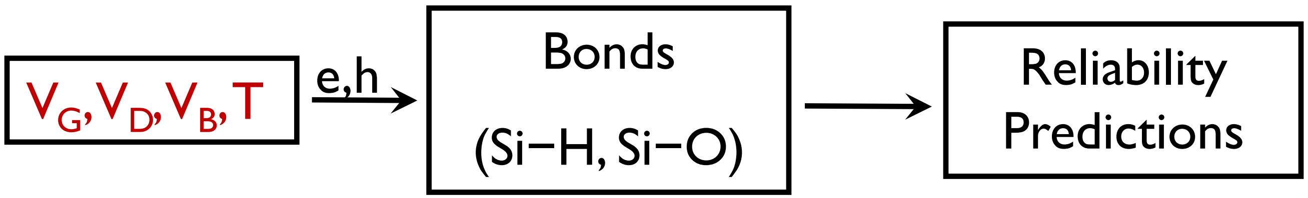
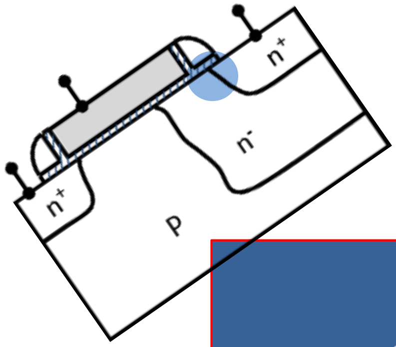
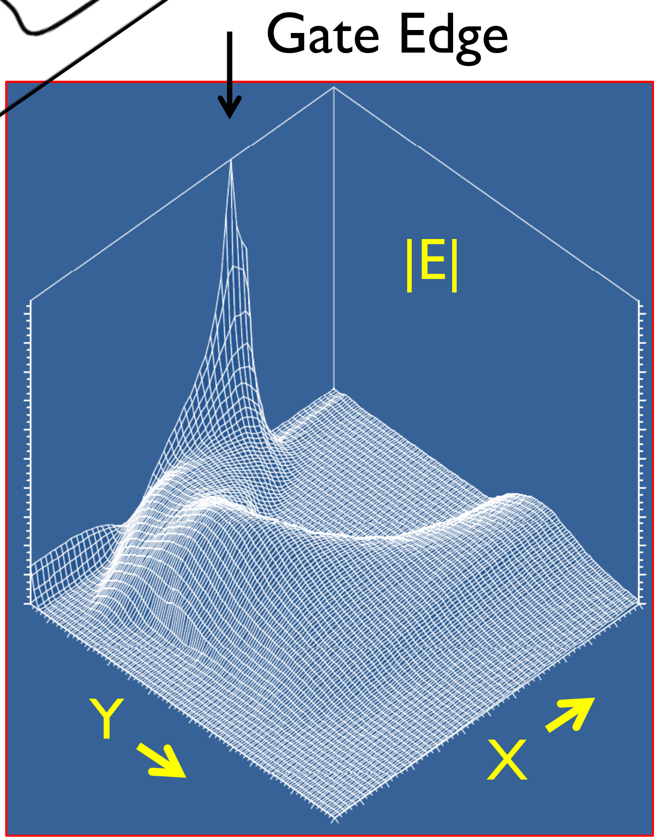
Many have moties, but who did it?!

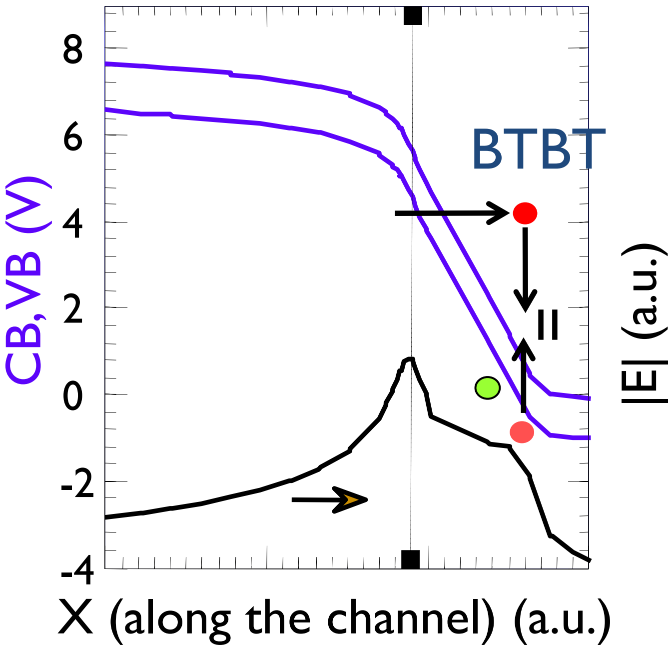






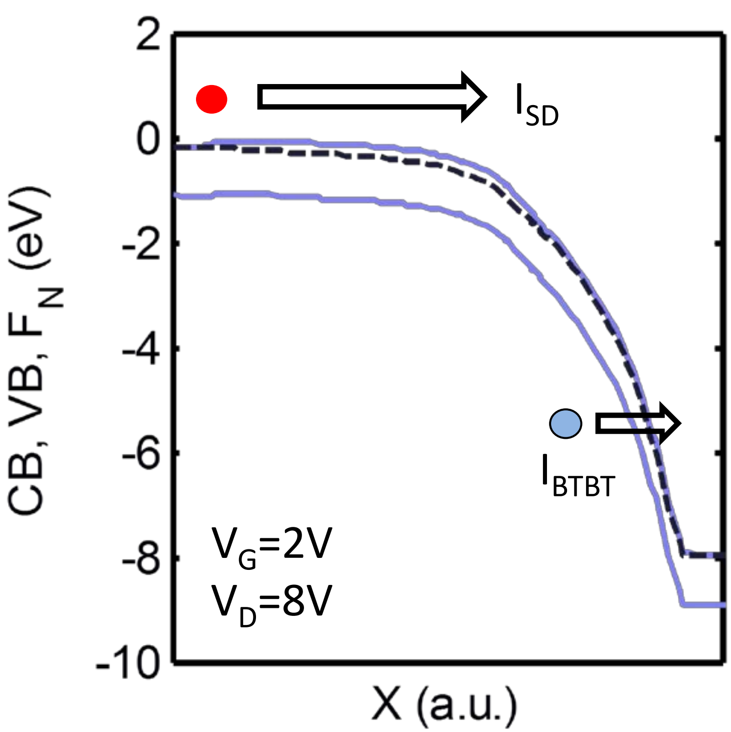
Degradation mechanism

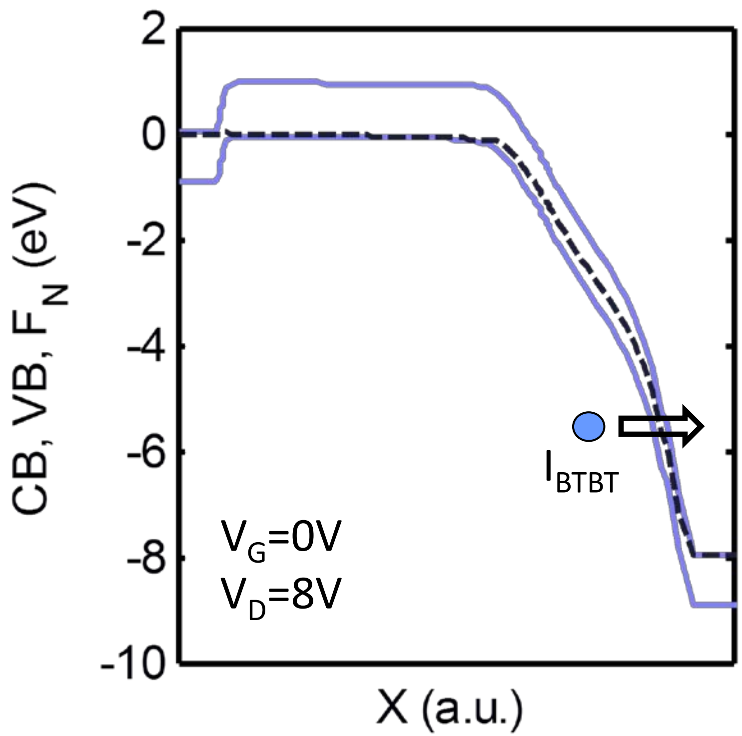




Electric field peaks at the surface leading to BTBT & Impact ionization

Drain Current at ON/OFF-state stress

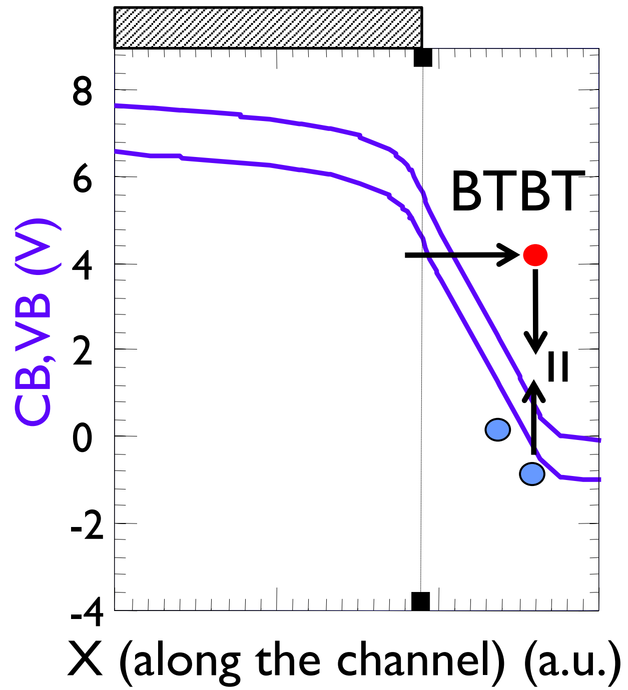


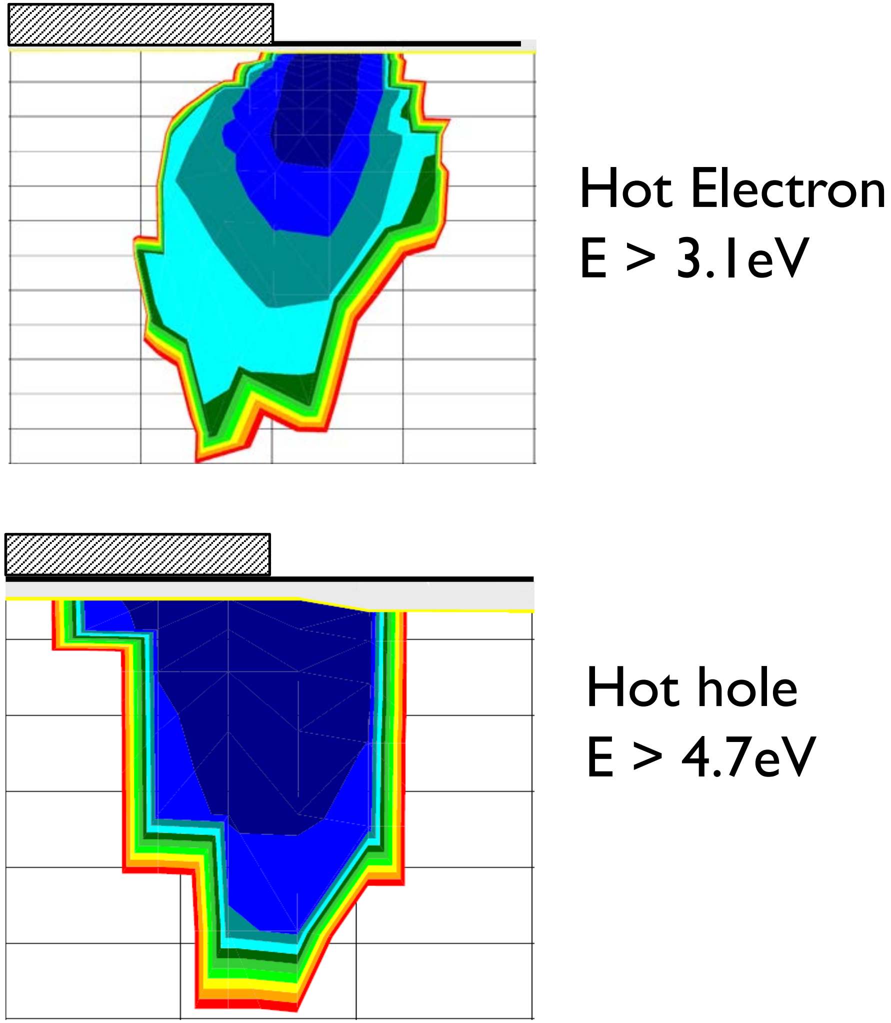


Channel inversion current is dominant in ON-State

Band-to-band tunneling current is dominant in OFF-State

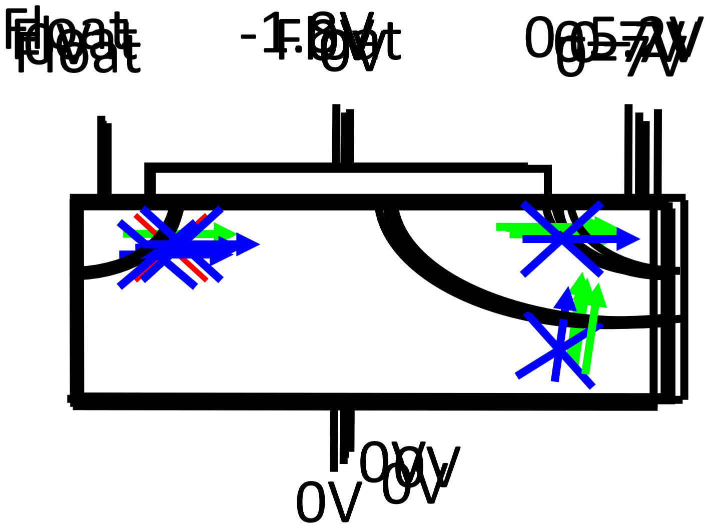
Heating of electrons generated by BTBT



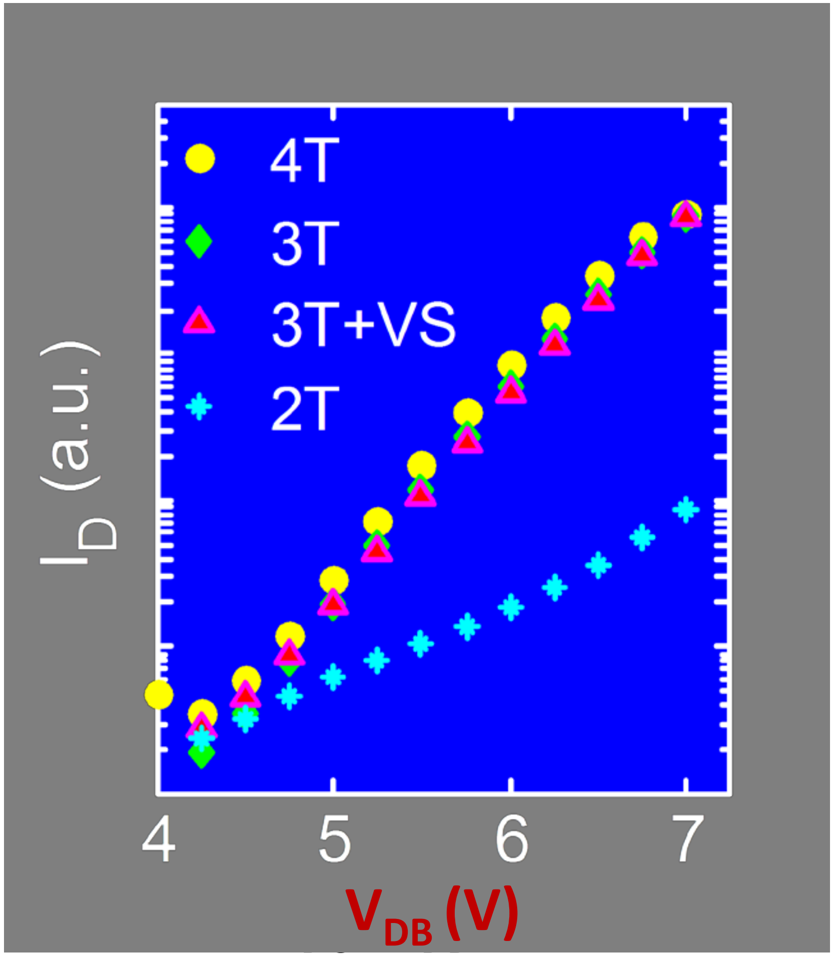


Impact Ionization of BTBT current generate hot carriers

Current components in DeNMOS



3 Terminal + Voltage Splitting



Surface BTBT is the dominant current component!

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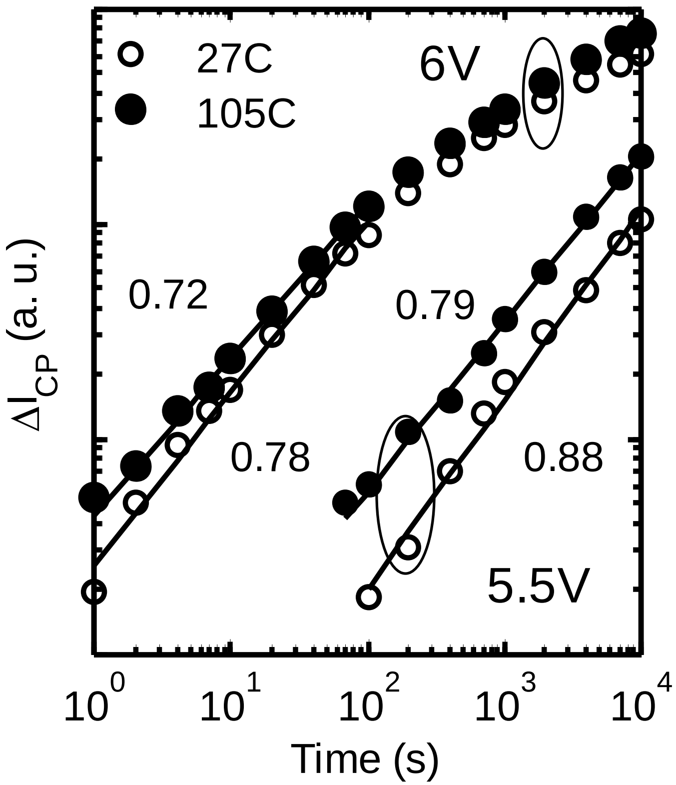
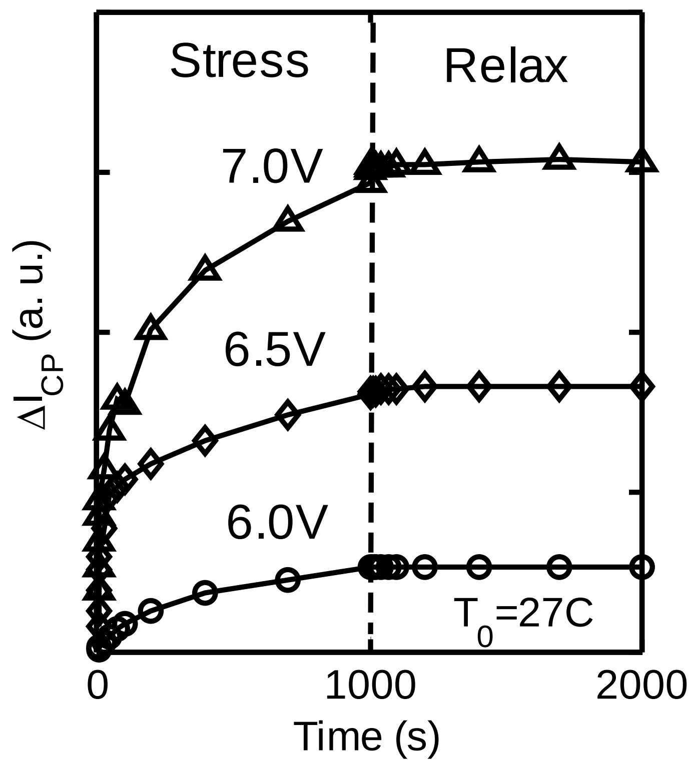
Generation & recovery of N_{OT} in Off-state



Higher time exponents

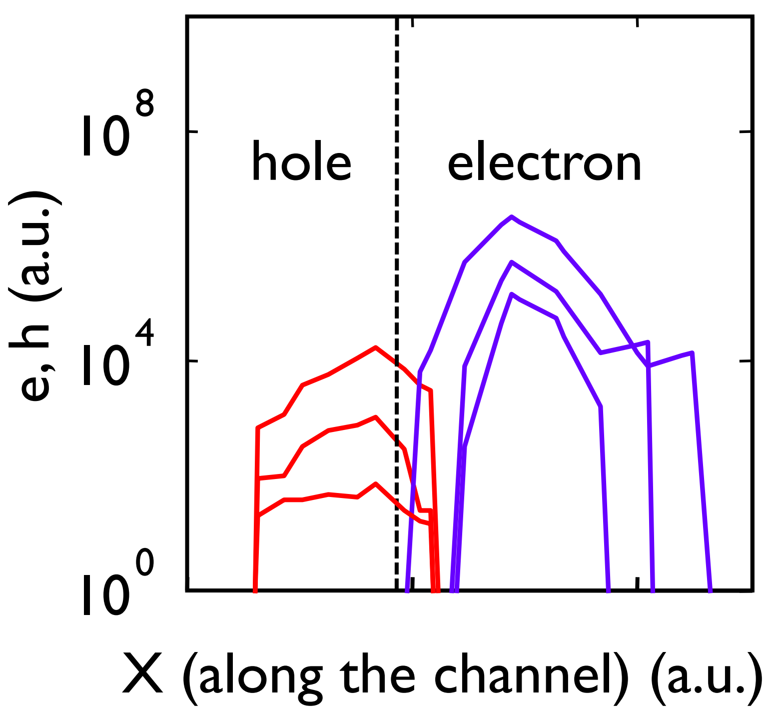


No recovery

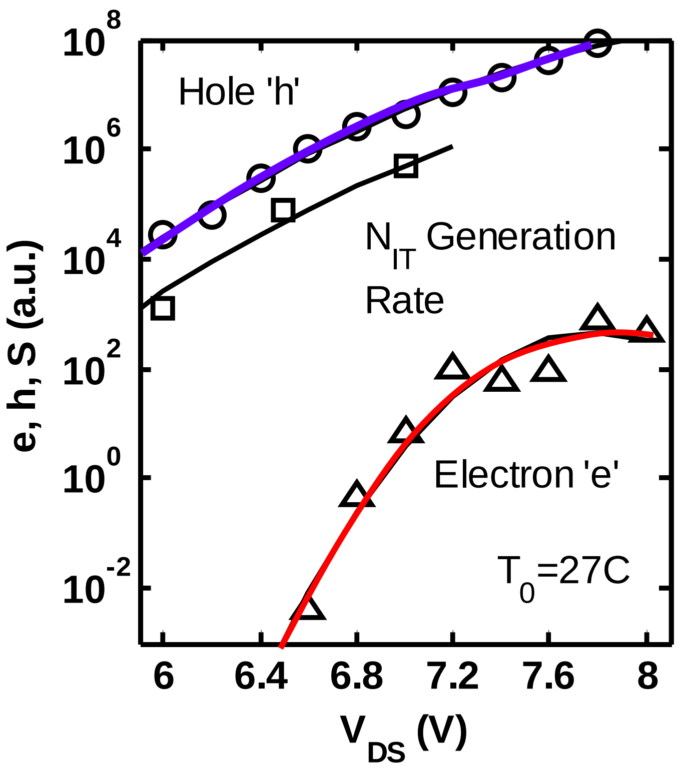
Most of the bonds broken are Si-O …

N_{IT} correlation with hot holes

Monte Carlo simulation



D. Varghese, EDL, Vol. 26, p. 572, 2006



Damage primarily due to broken Si-O bonds

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4. A scaling theory of Voltage acceleration
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Recall: Voltage dependent constant t_0

$$N_{IT}^{SiH} = \left(\frac{k_F\left(V_G, V_D\right) N_0}{k_R} \right)^m \times t^n \equiv \left(\frac{t}{t_0(V_G, V_D)} \right)^n = f_{HCI}\left(\frac{t}{t_0(V_G, V_D)} \right)$$

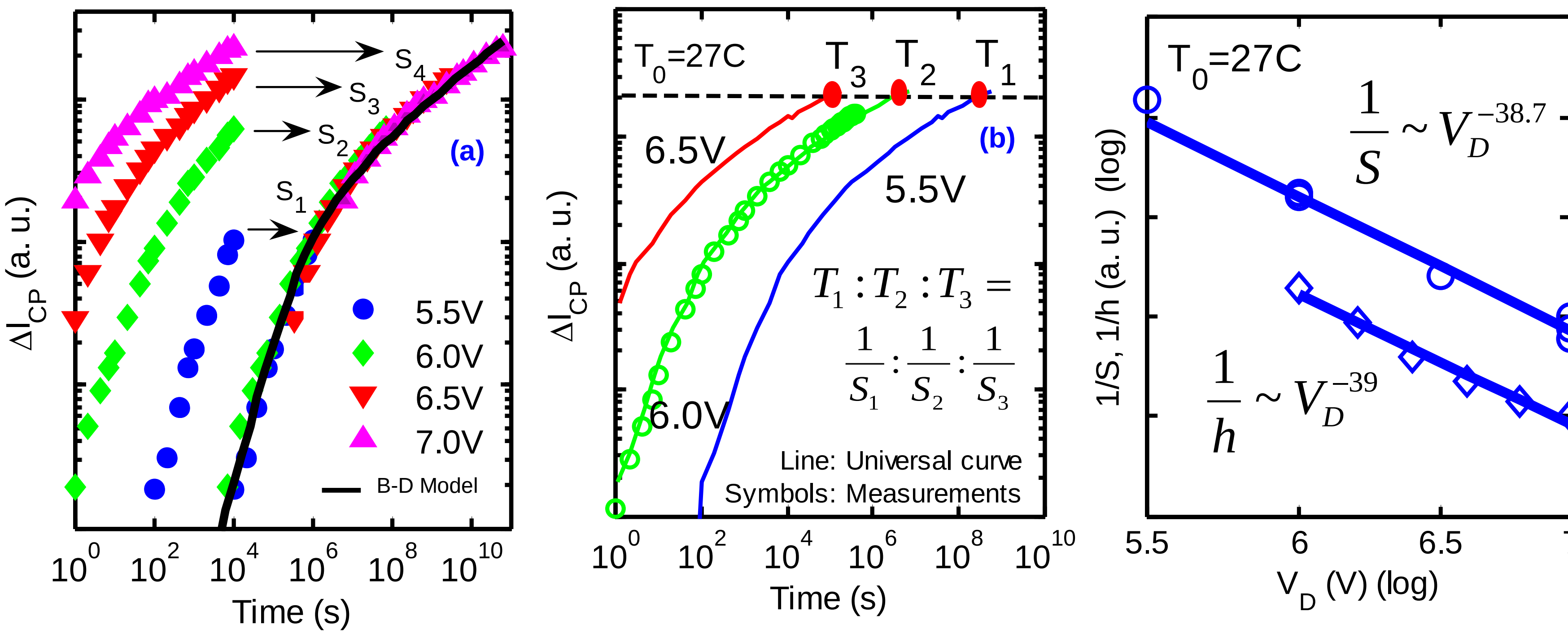
$$N_{IT}^{SiO} = \sum_E g\left(E\right)\left[1 + e^{-k_F\left(V_G, V_D\right)t}\right] dE \equiv f_{SiO}\left(\frac{t}{t_0\left(V_G, V_D\right)} \right)$$

$$t_0^{-1}(V_G, V_D) = I_G = k \frac{I_D}{W_{eff}} \left[\frac{I_{sub}}{I_d} \right]^{\Phi_e/\Phi i}$$

Scaling function describes SiO and SiH bond dissociation

Universal Degradation

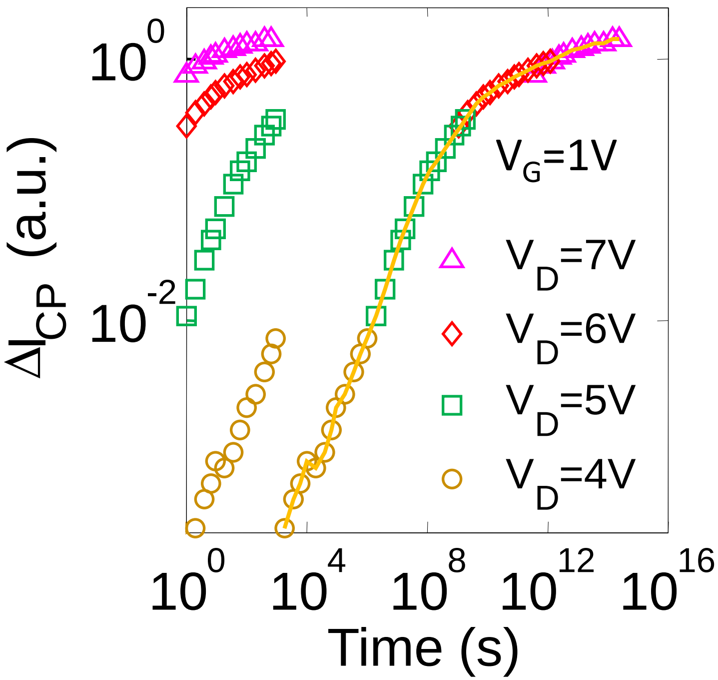
Varghese, IRPS, 2008.

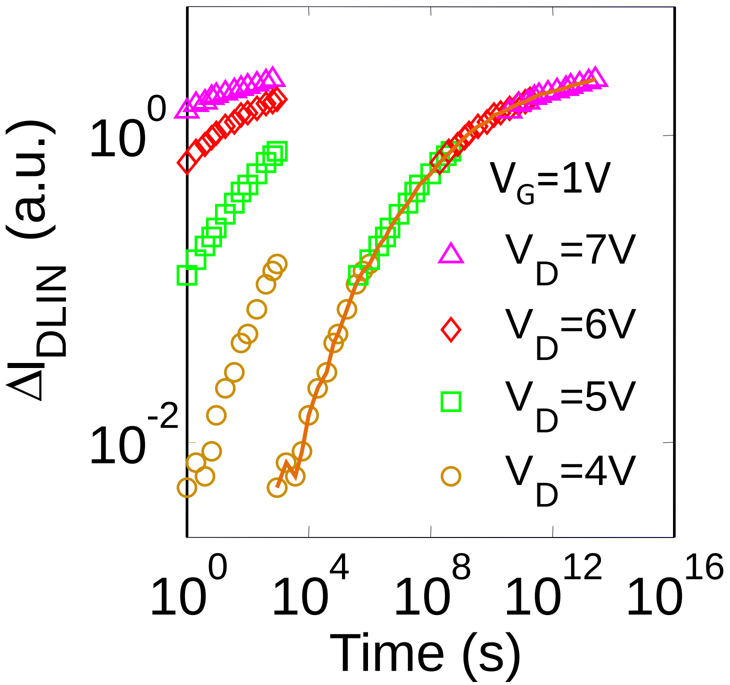


Outline

1. ON vs. OFF State HCI Degradation
2. Origin of hot carriers at off-state
3. SiH vs. SiO – who is getting broken?
4. A scaling theory of Voltage acceleration (for all technologies)
5. Conclusions

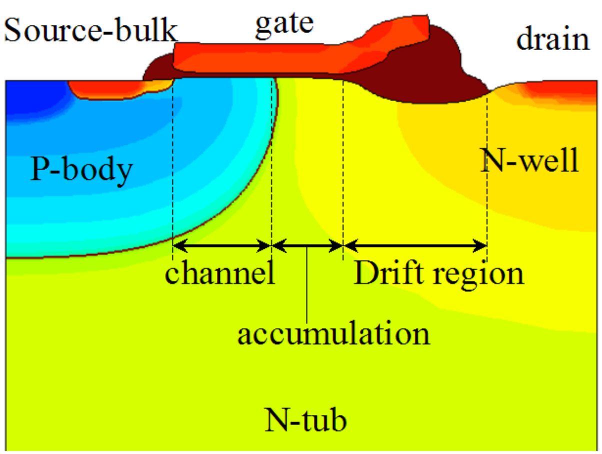
ON-state HCI in DeMOS transistors

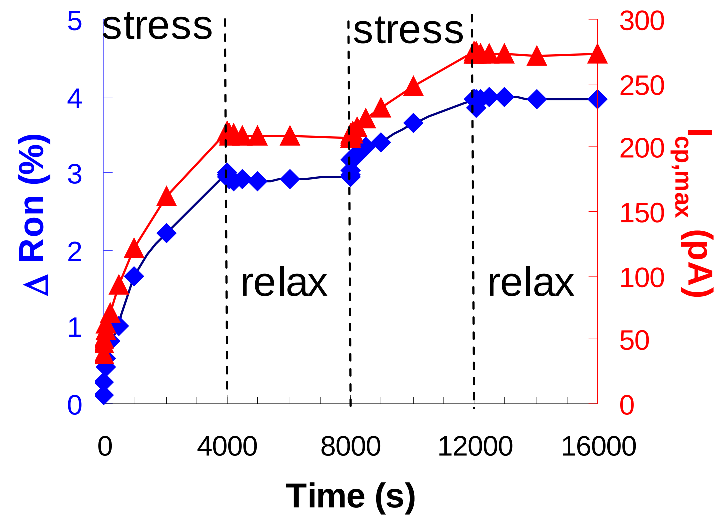


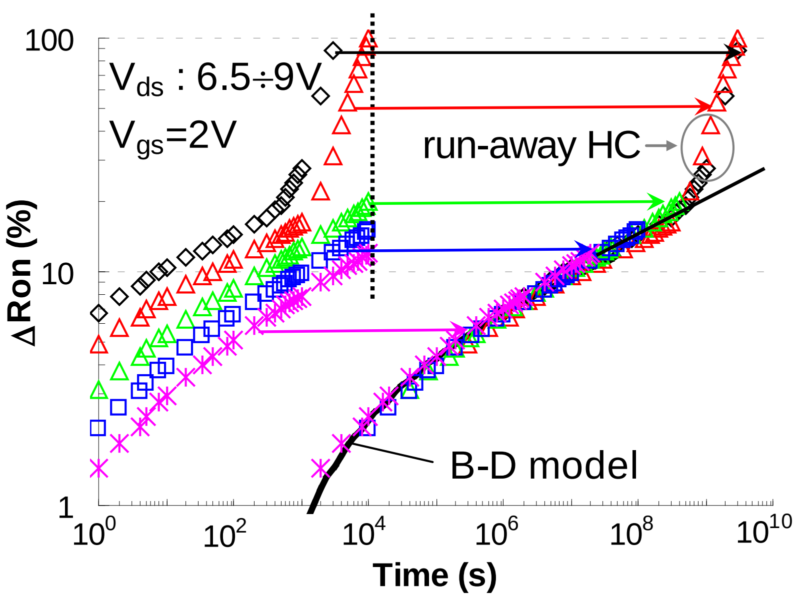


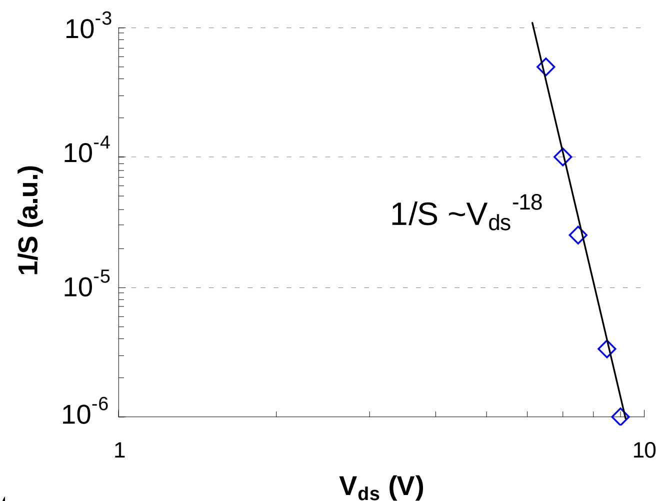
- Dominant current component changes from BTBT to I_{SD}
- Resultant degradation is universal for V_G =1V & 2V

LDMOS: SiO bonds and universality

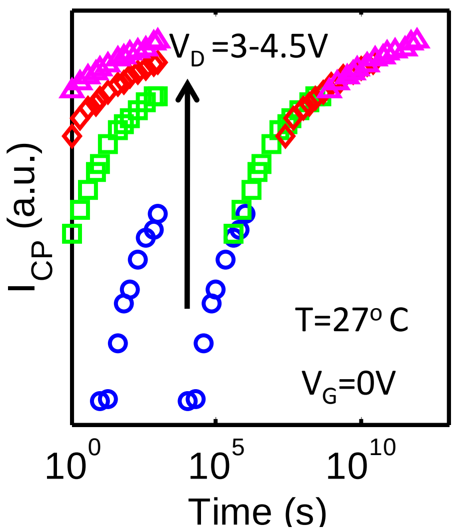


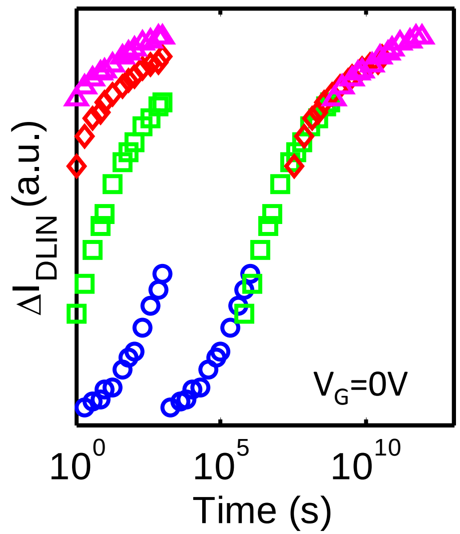


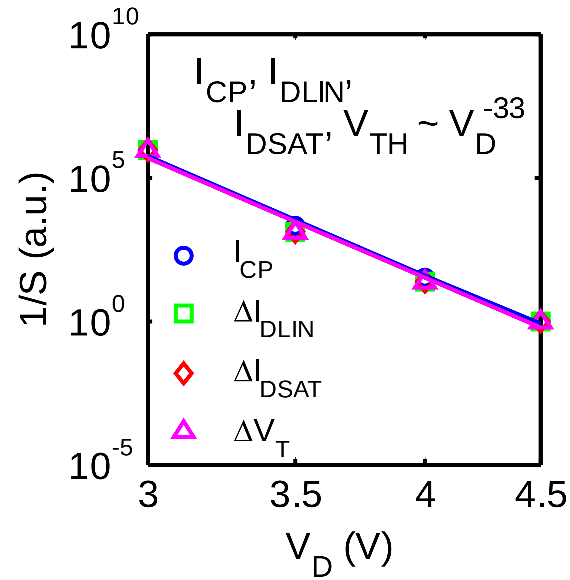


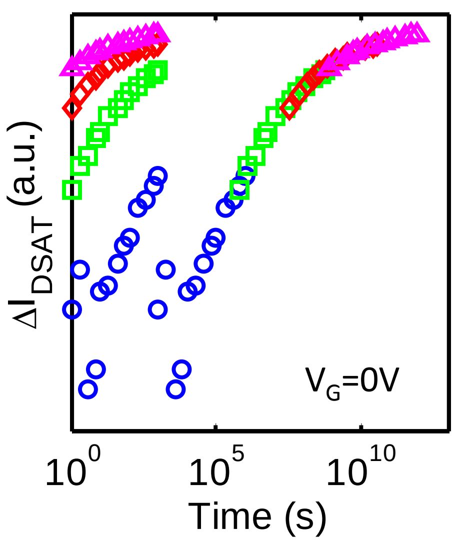


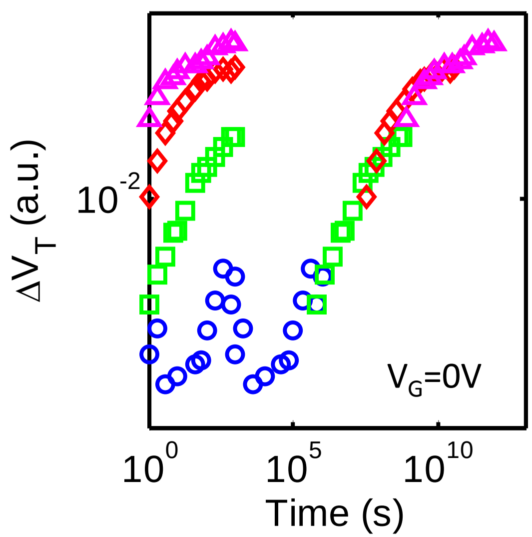
OFF-state HCI in **logic** transistors





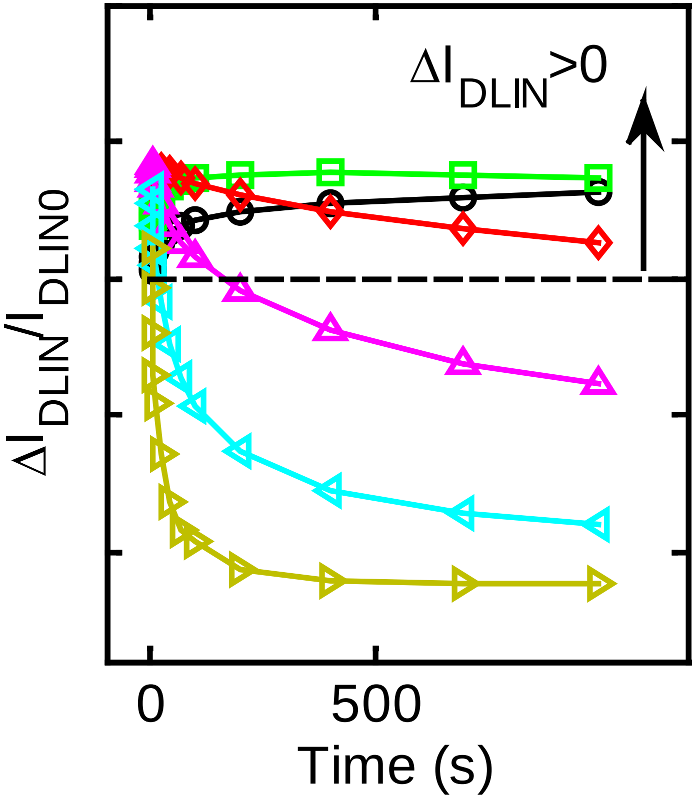


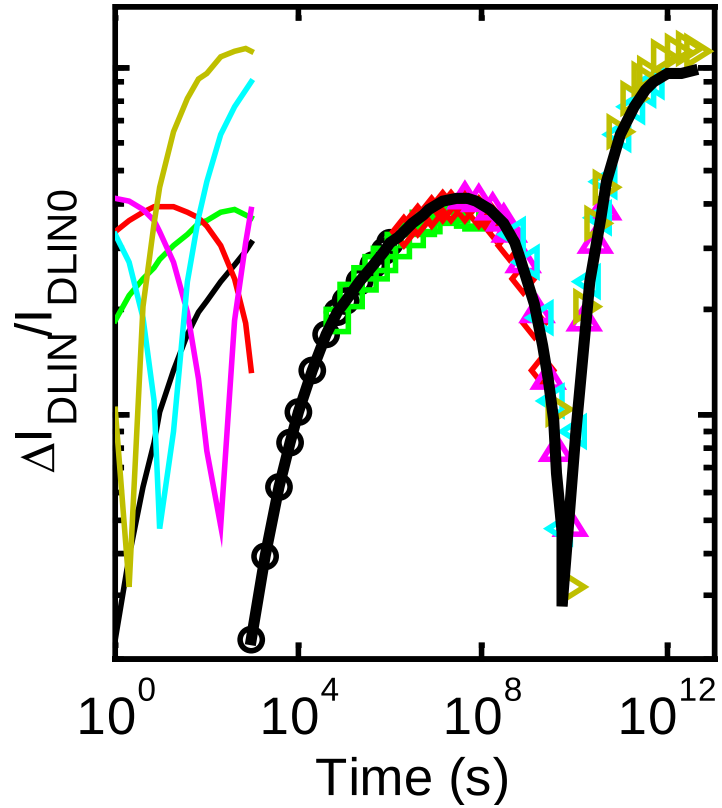




Logic transistors also show I_{DSAT} and V_{TH} degradation in addition to CP and I_{DLIN} degradation

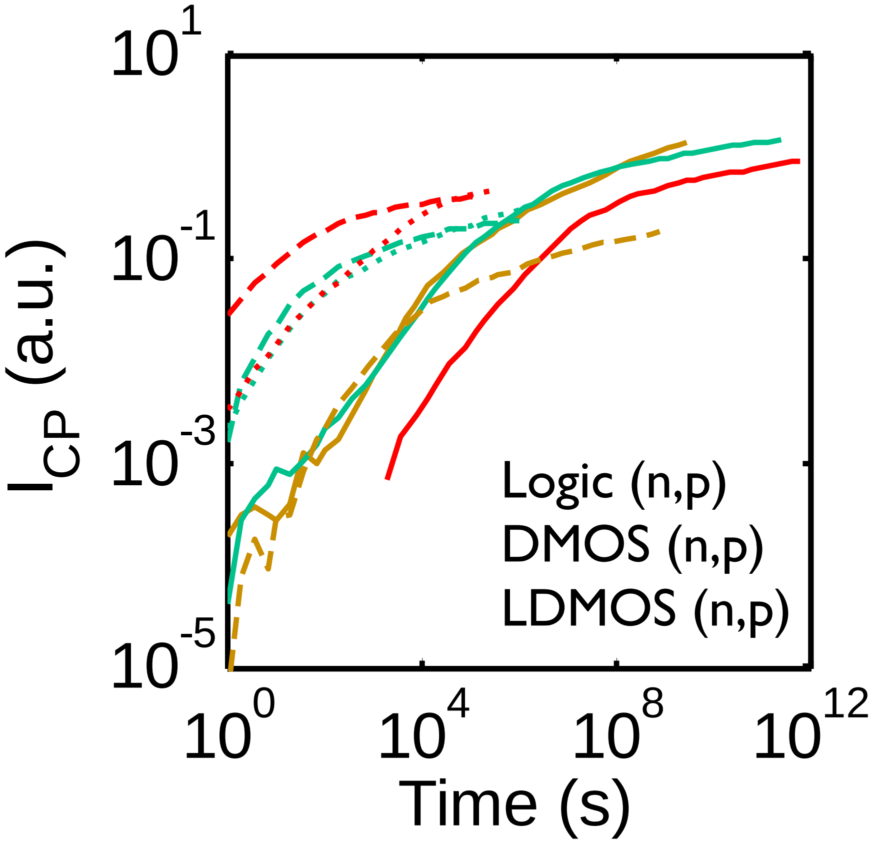
Universality of DePMOS degradation

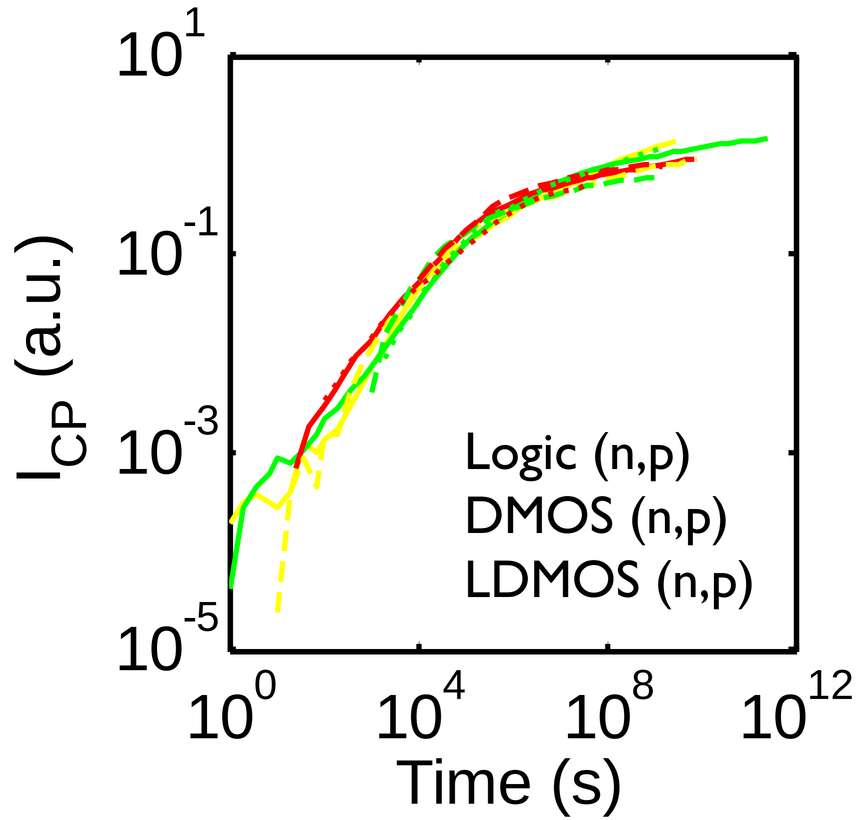




- I_{DLIN} for PMOS first increases, and then reduces
- Degradation curves still exhibit a universal behavior! Initially dominated by acceptor like traps, then donor traps

Universal HCI degradation across technologies





Wide range of devices and bias conditions show robust universality

Conclusions

- Off-state degradation in drain extended devices are driven hot carriers generated by Band-to-band tunneling and Impact ionization
- Bulk damage and parametric degradation in both NMOS and PMOS devices show similar universal behavior.
- The substrate current-based model involves a special form of scaling theory.
- The scaling function applies only when there is a dominant degradation mode. Mixed mode degradation needs to isolated in individual components, before scaling theory can be applied.

References

- An excellent review of the application of semiconductor devices in power electronics is discussed by Hower, IEDM 2010, 13.1.1.
- The long term saturation of HCI degradation is discussed in many paper, including A. Raychaudhuri, *et al.*, TED, 43(7), p. 1114, 1996 ; Vei-Han Chan *et al.*, TED, 42(5), p. 957, 1995; D. S. Ang *et al.*, TED, 45(1), p. 149, 1998
- The scaling theory is developed by Dhanoop Varghese and M. Alam see 2010 Ph.D. thesis by D. Varghese, Purdue University. Also see the 2012 IRPS Tutorial by D. Varghese. Variants of the scaling theory can be found in many other papers.
- For work on LDMOS transistors, read the papers by P. Moens. He has done extensive work on this topic.

Self Test Review questions

1. Why is BTBT tunneling important for OFF-state HCI, but nor for ON-state HCI?
2. What type of bond dissociation dominated DeMOS degradation? Provide two supporting arguments.
3. Will universality hold of SiH and SiO bond dissociation occur in equal proportion?
4. Do you expect NBTI to be described by universal voltage and temperature scaling? What if electron/hole trapping is present?
5. Support the argument that scaling hypothesis is theory-agnostic, and therefore once empirically demonstrated, is more powerful.