ECE695: Reliability Physics of Nano-Transistors
Lecture 21: Introduction to Dielectric Breakdown

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Outline

1. Basic features of gate dielectric breakdown
2. Physical characterization of breakdown spot
3. Time-dependent defect generation
4. Conclusions
## Topic map

<table>
<thead>
<tr>
<th>Intro</th>
<th>Model of reliability</th>
<th>Fish in a river</th>
<th>Accelerated tests</th>
</tr>
</thead>
<tbody>
<tr>
<td>Defects</td>
<td>Euler/Maxwell Relationship</td>
<td>Point defects</td>
<td>Log-t charging</td>
</tr>
<tr>
<td>NBTI</td>
<td>Trapping and Observations</td>
<td>Stress Exponent</td>
<td>Relaxation, f, duty cycle</td>
</tr>
<tr>
<td>HCI</td>
<td>Basics, Time dep.</td>
<td>Field</td>
<td>Temp.</td>
</tr>
<tr>
<td>Charac.</td>
<td>Charge-based</td>
<td>Flux-based</td>
<td>Spin-based</td>
</tr>
<tr>
<td>Radiation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Statistics</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Scaling and reliability: A short history

- **PMOS NBTI dominates**
- **TDDB increases due to $T_{OX}$ scaling, NBTI re-emerge due to increased fields**
- **HCl reduces due to $V_{DD}$ scaling, LDD structures**
- **NBTI reduces with NMOS transistors. HCl dominates due to high $V_{DD}$**
- **HCl remerges as an issue inspite of reduced $V_{DD}$**

<table>
<thead>
<tr>
<th>Year</th>
<th>Transistor Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>1970</td>
<td>10^2</td>
</tr>
<tr>
<td>1980</td>
<td>10^4</td>
</tr>
<tr>
<td>1990</td>
<td>10^8</td>
</tr>
<tr>
<td>2000</td>
<td>10^10</td>
</tr>
<tr>
<td>2010</td>
<td>10^12</td>
</tr>
</tbody>
</table>

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Gate dielectric breakdown is an issue for both NMOS and PMOS.
Time dependent dielectric breakdown


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Features: Breakdown can correlated or uncorrelated

**Correlated** breakdown in thick Insulators

**Uncorrelated** breakdown in thin insulators

Theory of partially correlated breakdown is important and contacts define everything.
Features: TDDB voltage (not field)-accelerated

- Nonlinear voltage dependence
- Highly accelerated voltage dependence

**Gate Current**

- $V_3 > V_2 > V_1$

**Breakdown**

- Empirical projection.

**Log (Time to breakdown)**

- $V_{op}$
- Years

- Days

Highly accelerated voltage dependence
Features: Failure times Weibull distributed

Breakdown

Gate current

Time

Average lifetime is not good enough ….

Features: Failure times Weibull distributed

Gate current

Time

Average lifetime is not good enough ….

Weibull distribution

$\ln(-\ln(1-F))$

$100/$million

VG1 > VG2 > VG3 VDD

$V_{G1} > V_{G2} > V_{G3} \quad V_{DD}$

log (TBD)

100/million

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Features: NMOS vs. PMOS Reliability

PMOS less reliable than NMOS, contacts defines everything!

Features: Soft vs. Hard breakdown

Breakdown could be hard or soft …
Features: BD softer at lower voltages

Features: PMOS with soft breakdown

![Graph showing oxide thickness vs. V_{op, V_{safe}} for PMOS and SBD thresholds.](graph.png)

- PMOS
- ITRS
- Multiple SBD
- SBD Threshold
- 1st SBD

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Features: Increase in Leakage Current

![Image of a circuit with thermal imaging]

Graph showing the relationship between I_DQ current at Vdd1 (mA) and Stress time (sec.).

- Vdd1 = 4.5V, 115°C, η(1)=0.8s
- Vdd1 = 4.3V, 113.7°C, η(1)=35s
- Vdd1 = 4.1V, 112.5°C, η(1)=400s

The graph indicates a decrease in I_DQ current at higher stress times and temperatures.
Outline

1. Basic features of gate dielectric breakdown
2. Physical characterization of breakdown spot
3. Time-dependent defect generation
4. Conclusions
Features: BD Induced Microstructure Damages

- Contact burnt out in various post breakdown samples.
- Note the associated substrate damages.
- Electrical measurement shows S/D short through channel.

BD Induced Microstructure Damages

- Sample with 20Å gate oxide and HBD at 100mA
- Total epitaxy of poly-Si gate with Si sub
- Severe Si substrate channel damages
- Electrical measurement shows S/D short through channel

Courtesy, Pey, Tutorial, 11th Workshop on Gate Oxide Technology, 2006.

Dielectric Breakdown induced Metal Migration

- Dielectric breakdown induced metal migration (DBIM) in various device dimension, process technologies, and stress conditions.

![Ti map](a)  
![Co map](b)  
![SiN map](c)

Courtesy, Pey, Tutorial, 11th Workshop on Gate Oxide Technology, 2006.
Features: Microstructure Damage

- Dielectric breakdown induced epitaxy (DBIE) in various device dimension, process technologies, and stress conditions.
- Device may still be functional.

*Courtesy, Pey, Tutorial, 11th Workshop on Gate Oxide Technology, 2006.*

*Tung et al., ULSI Semiconductor Technology Atlas, John Wiley and Sons, 2003.*
TEM image across transistor width

STI corner is not the BD location
Features: Hard vs. Soft breakdown

Region I: No Si epitaxy
- Functional
- 10nA, 100nA, 1µA, 10µA, 100µA

Region II: Si epitaxy
- Catastrophic failures
- 100nA, 10nA, 100µA

Region III: 25 & 33 Å Gox, 16 Å Gox

Pey et al., IEDM 2002.

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Outline

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Time exponent of degradation

- Does the time exponent remain constant with time?
- How does the time exponent change with bias?
Dissociation Barriers and its Distribution

Energy

Distance

E'(10.4 Gauss Doublet)
BD model anticipates time exponent

\[ \frac{dN_{IT}(t)}{dt} = k_f \left( N_0 - N_{IT}(t) \right) \]

\[ \frac{dN_{IT}(t)}{dt} = \int_{E_0-n\sigma}^{E_0+n\sigma} k_f(E)(g(E) - f(E,t))dE \]

\[ \sigma = 0.1 \]
\[ n = 3.38 \]

\[ g(E)/N_0 \text{ (eV}^{-1}) \]

\[ \Delta I_{CP} \text{ (a.u.)} \]

\[ E \text{ (eV)} \]

\[ \text{Time (s)} \]

Universal function obtained by CP/SILC

\[ N_{SiO} = \sum_E g(E) \left[ 1 + e^{-k_F(V_G,V_D)t} \right] dE = f_2 \left( \frac{t}{t_0} \right) \]
\[ \Delta I_G = \left( I_G - I_G(0) \right) / I_G(0) \text{ at } V_{\text{sense}}: \text{ depends on } T_{OX} \text{ and } V_{\text{sense}} \]

- Power-law: \( \Delta I_G \propto t^p \), \( p \) usually < 0.5 close to breakdown

- Find \( t^* \), time required to reach a given amount of \( \Delta I_G \)

Conclusions

- Dielectric breakdown has a long history and broad range of physical and technological implications.

- TDDB is important for thick and think dielectrics, but the physics of breakdown is very different.

- Measurement of TDDB at very low voltage has been difficult – therefore a theory of dielectric breakdown and accurate measurement techniques (SILC) are very important.

- For thin oxides, statistical distribution of failure time is a key feature of TDDB. Theory is essential here as well.
There have been considerable amount of work on gate dielectric breakdown. Here I refer to some of the work I have done – additional references can be found in the papers. You could get started by reading “A Future of Function or Failure?” M. A. Alam, Bonnie E. Weir, and P. Silverman, IEEE Circuits and Devices - The Electronics and Photonics Magazine 18(2), pp. 42-48, 2002.

Reviews can be found in ....


Modern theory of dielectric breakdown is discussed in ...


Theory of soft and hard breakdown are discussed in ...


TDDB Characterization techniques are discussed in ...


Review Questions

1. What is the name of the failure distribution that we expect for thin oxides?

2. For thin oxides, is PMOS or NMOS more of a concern in modern transistors?

3. What is DBIE? When does it occur? Can the transistor be still functional?

4. In what ways is TDDB compare with NBTI and HCI time-degradation? Explain.

5. Why do you suspect that hard breakdown destroys thick oxide, while in thin oxides breakdown can be soft?

6. What is stress-induced leakage current? What is ‘stress-induced’ about it?