



ECE695: Reliability Physics of Nano-Transistors
Lecture 21: Introduction to Dielectric Breakdown

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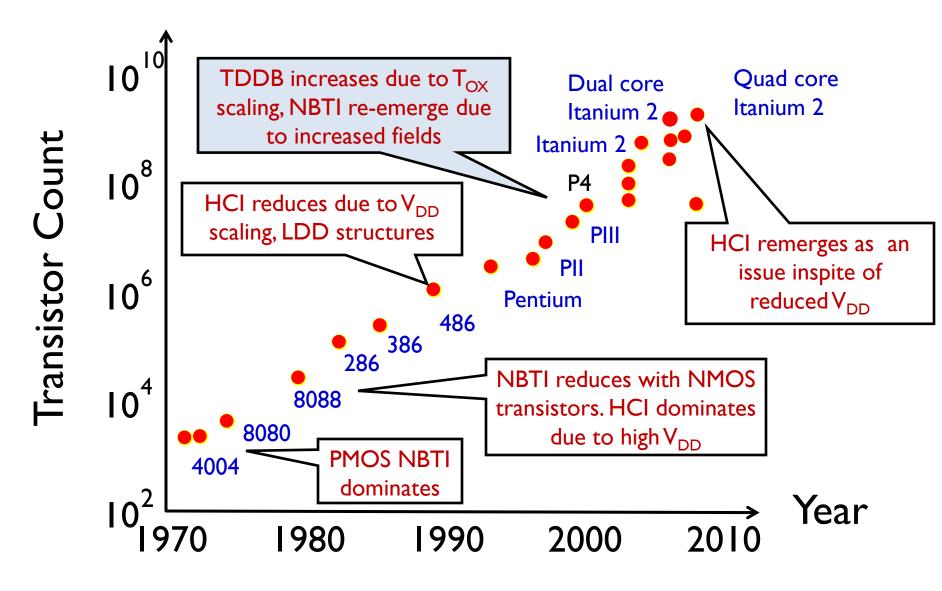
### **Outline**

- 1. Basic features of gate dielectric breakdown
- 2. Physical characterization of breakdown spot
- 3. Time-dependent defect generation
- 4. Conclusions

# Topic map

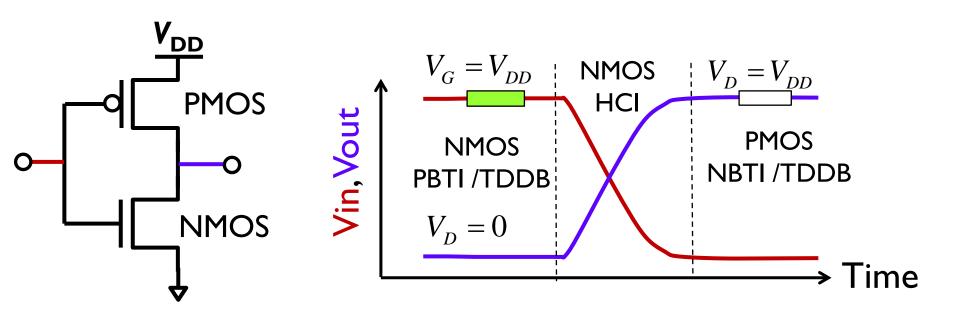
Intro	Model of reliability	Fish in a river	Accelerated tests		
Defects	Euler/Maxwell Relationship	Point defects	Log-t charging	I/f and RTN	
NBTI	Trapping and Observations	Stress Exponent	Relaxation, f, duty cycle	Field/Temp.	circuits
HCI	Basics,Time dep.	Field	Temp.	Off-state HCI	
Charac.	Charge-based	Flux- based	Spin-based	Relative merits	
TDDB	Basics, Time Dependence	Field dep. AHI	Asymmetry	Statistics: Cell Perc.	Meas. & Circuits
Radiation					
Statistics					

### Scaling and reliability: A short history



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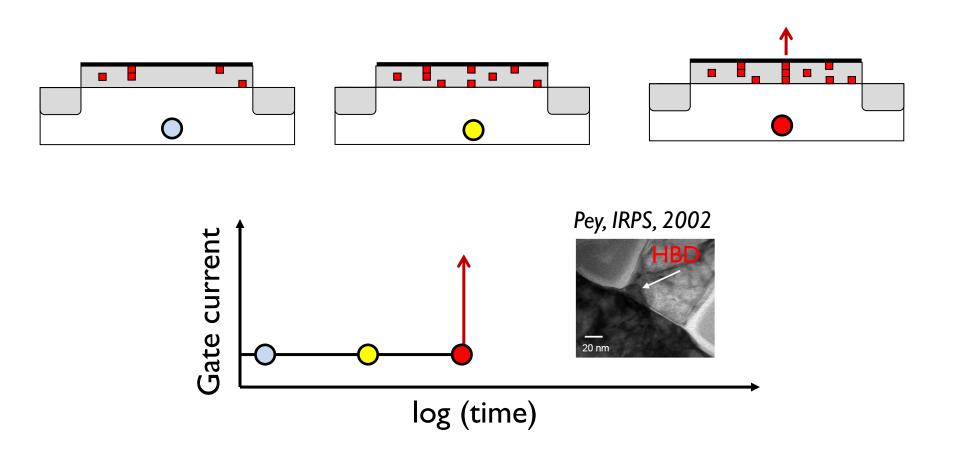
### Classical Gate Dielectric Breakdown



Gate dielectric breakdown is an issue for both NMOS and PMOS

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## Time dependent dielectric breakdown



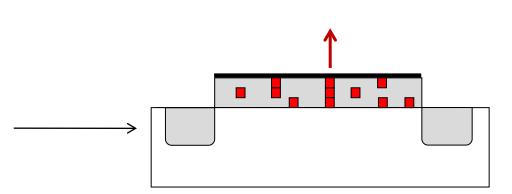
Alam, IRPS, 2000; Alam, ECS, 2000; Stathis, IBM J. Res/Dev, 46, 2002.

### Features: Breakdown can correlated or uncorrelated

Correlated breakdown in thick Insulators

Uncorrelated breakdown
In thin insulators

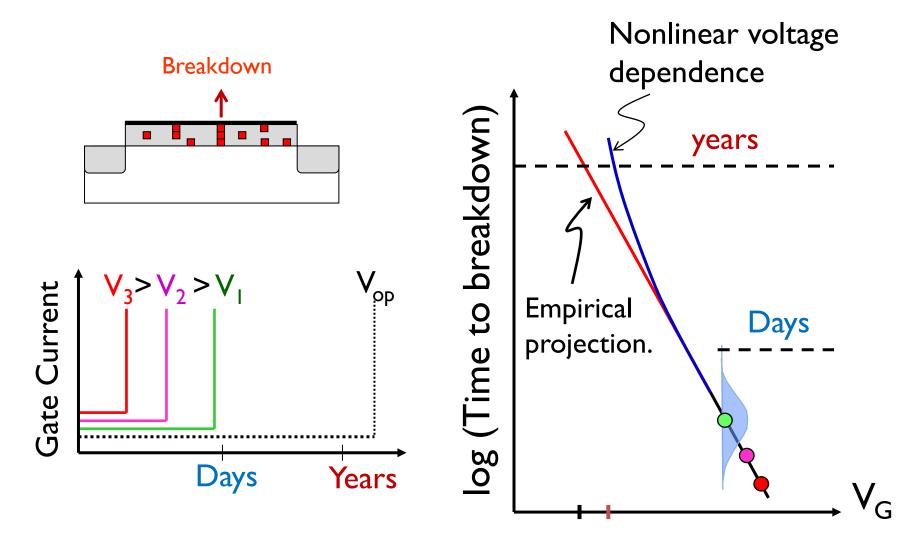




Theory of partially correlated breakdown is important and contacts define everything.

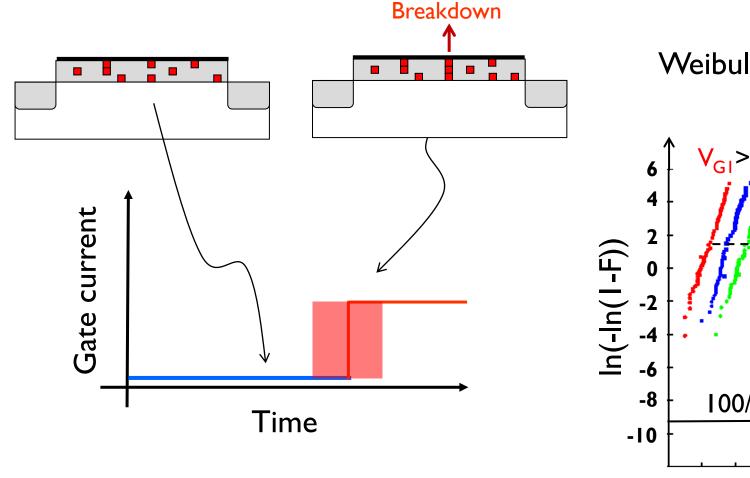
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### Features: TDDB voltage (not field)-accelerated



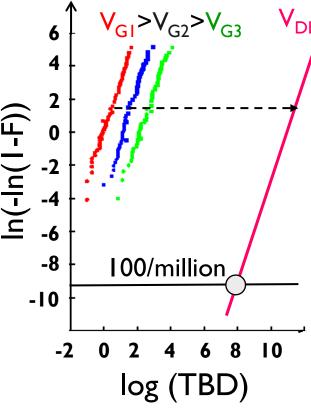
Highly accelerated voltage dependence

### Features: Failure times Weibull distributed

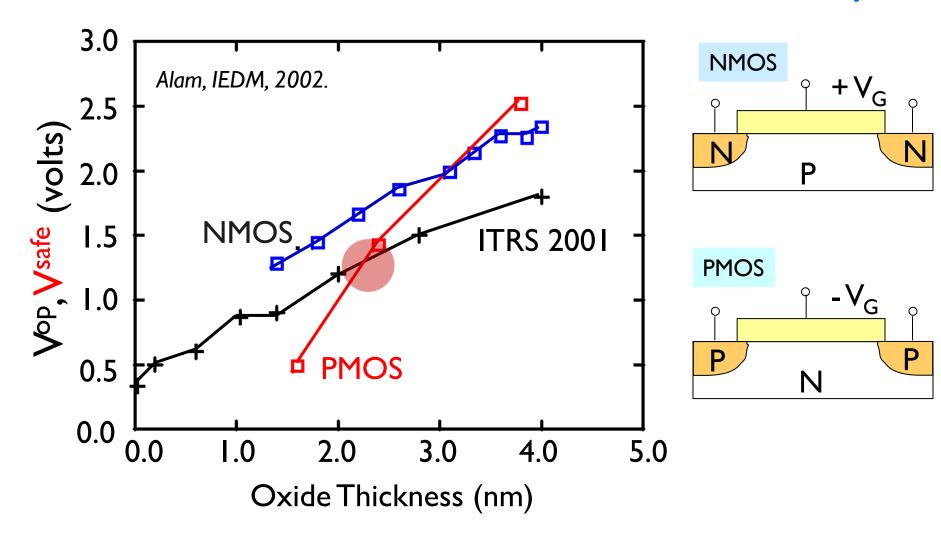


Average lifetime is not good enough ....

Weibull distribution

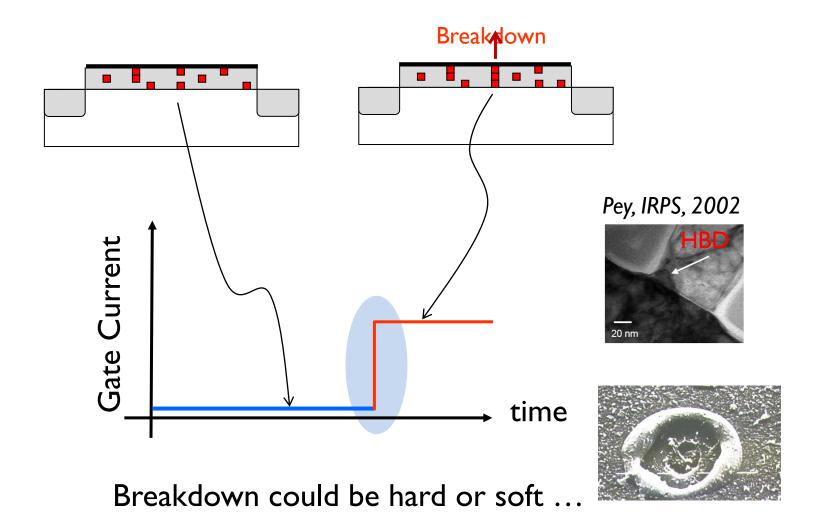


## Features: NMOS vs. PMOS Reliability



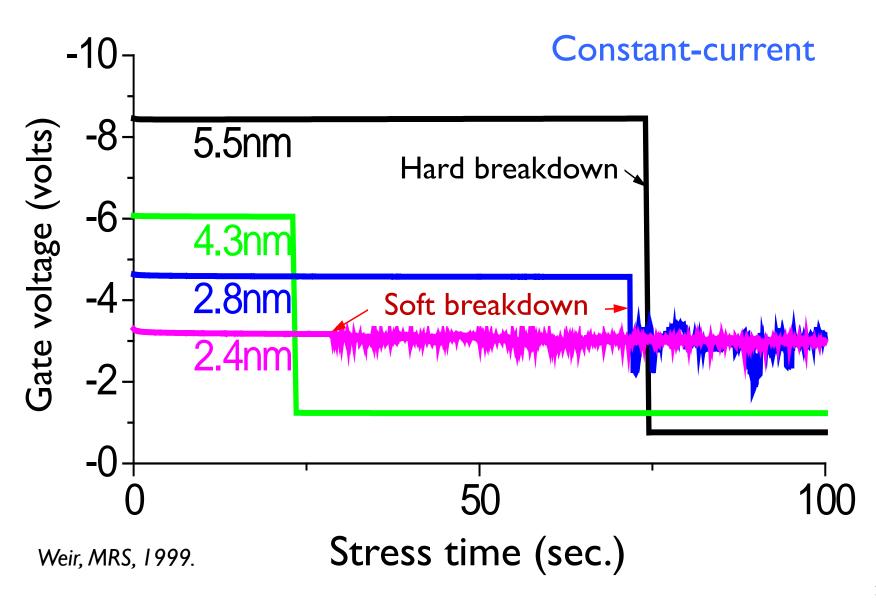
PMOS less reliable than NMOS, contacts defines everything!

### Features: Soft vs. Hard breakdown

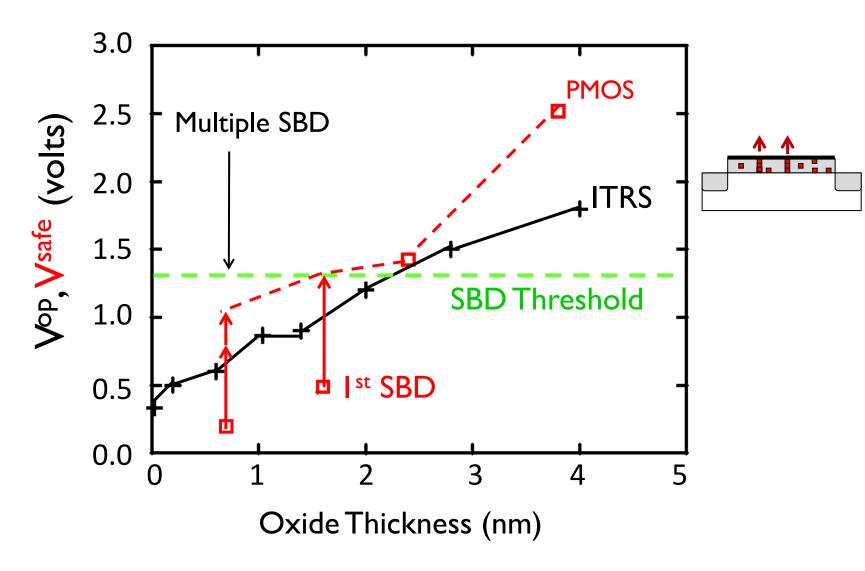


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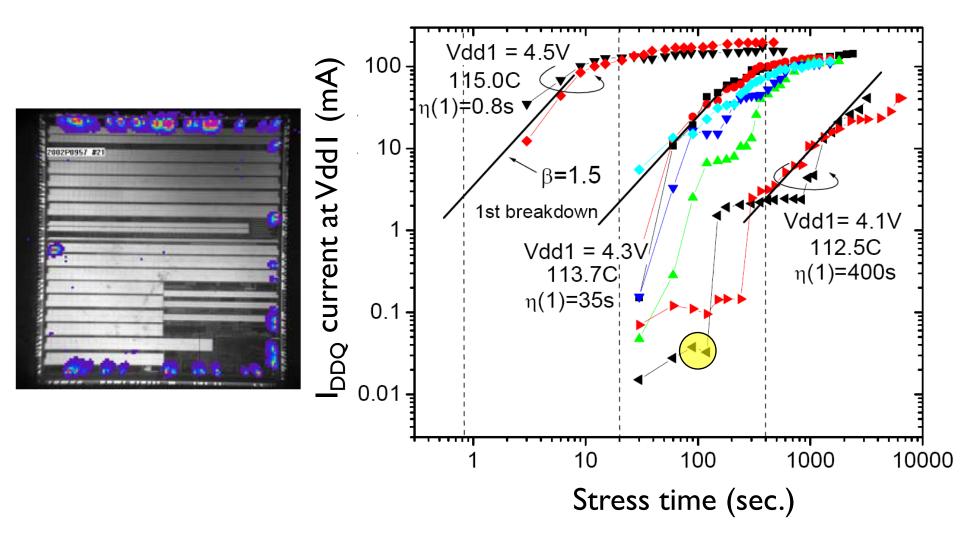
### Features: BD softer at lower voltages



### Features: PMOS with soft breakdown



# Features: Increase in Leakage Current



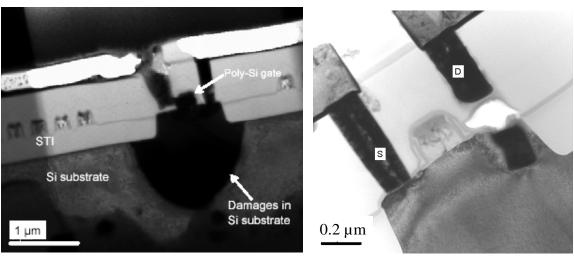
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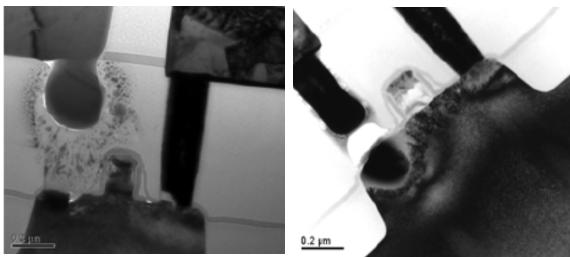
### **Outline**

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### Features: BD Induced Microstructure Damages

- Contact burnt out in various post breakdown samples.
- Note the associated substrate damages.
- Electrical measurement shows S/D short through channel.



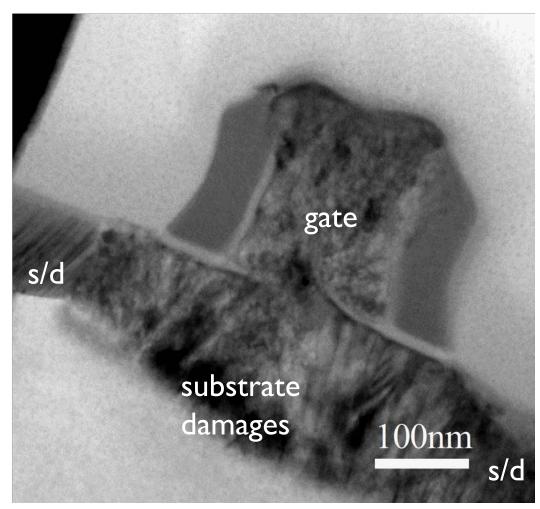


Tang et al., IEEE TDMR, 4(1), 2004; Pey et al., Microelectronics Rel., 43, 2003.

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## **BD Induced Microstructure Damages**

- Sample with 20Å gate oxide and HBD at I00mA
- Total epitaxy of poly-Si gate with Si sub
- Severe Si substrate channel damages
- Electrical measurement shows S/D short through channel



Tang et al., IEEE TDMR, 4(1), 2004.

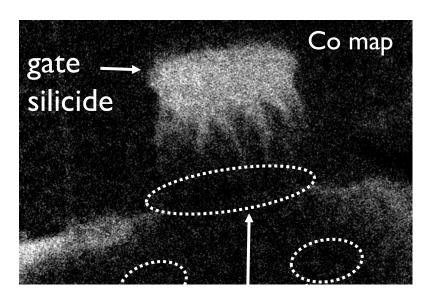
18

Courtesy, Pey, Tutorial, I I<sup>th</sup> Workshop on Gate Oxide Technology, 2006.

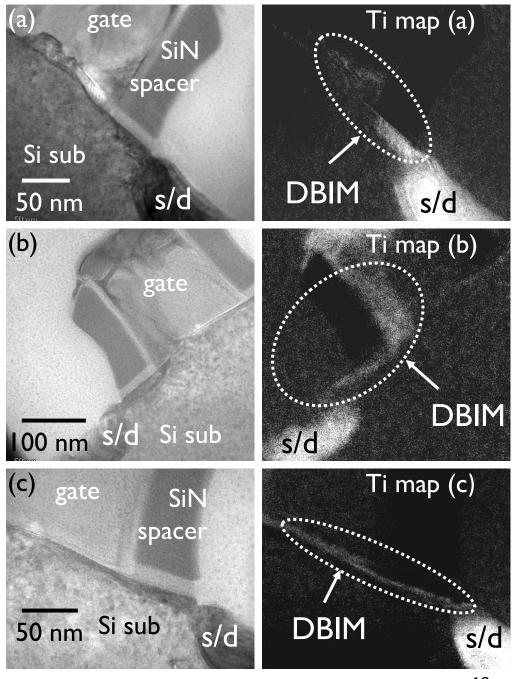
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# Dielectric Breakdown induced Metal Migration

Dielectric breakdown induced metal migration (DBIM) in various device dimension, process technologies, and stress conditions.



Courtesy, Pey, Tutorial, I I<sup>th</sup> Workshop on Gate Oxide Technology, 2006.



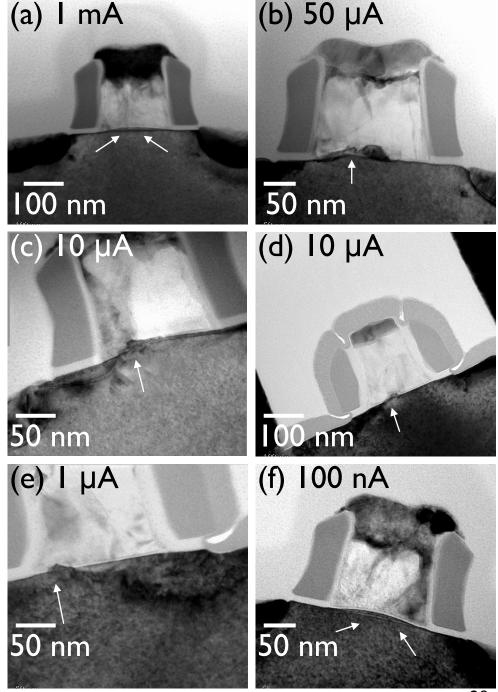
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# Features: Microstructure Damage

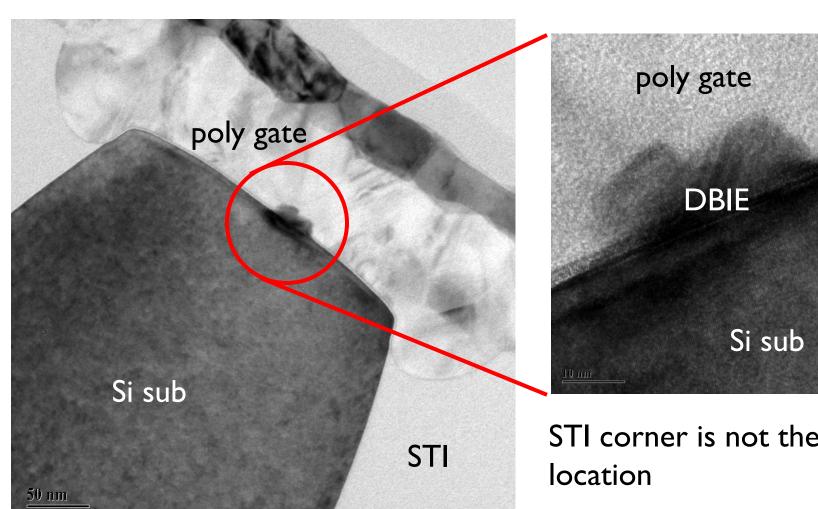
- Dielectric breakdown induced epitaxy (DBIE) in various device dimension, process technologies, and stress conditions.
- Device may still be functional.

Courtesy, Pey, Tutorial, I I<sup>th</sup> Workshop on Gate Oxide Technology, 2006.

Tung et al., ULSI Semiconductor Technology Atlas, John Wiley and Sons, 2003.



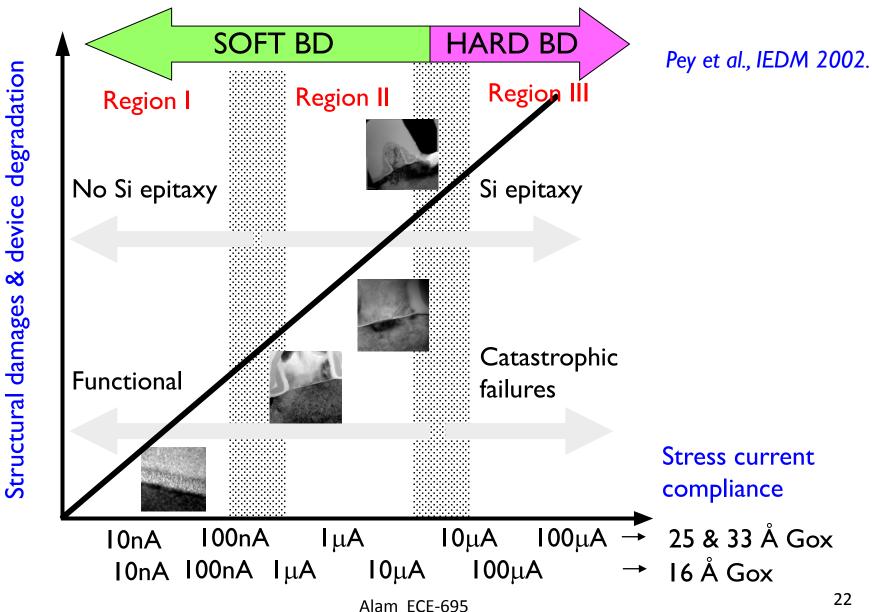
# TEM image across transistor width



STI corner is not the BD

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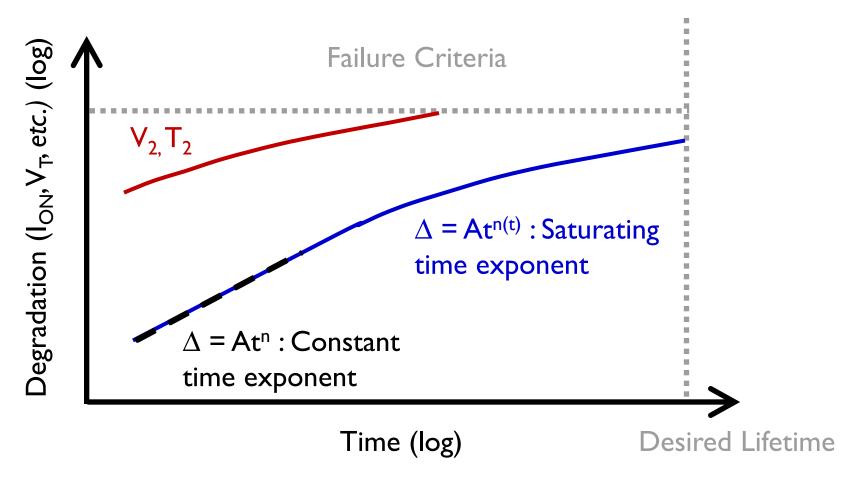
# Features: Hard vs. Soft breakdown



### **Outline**

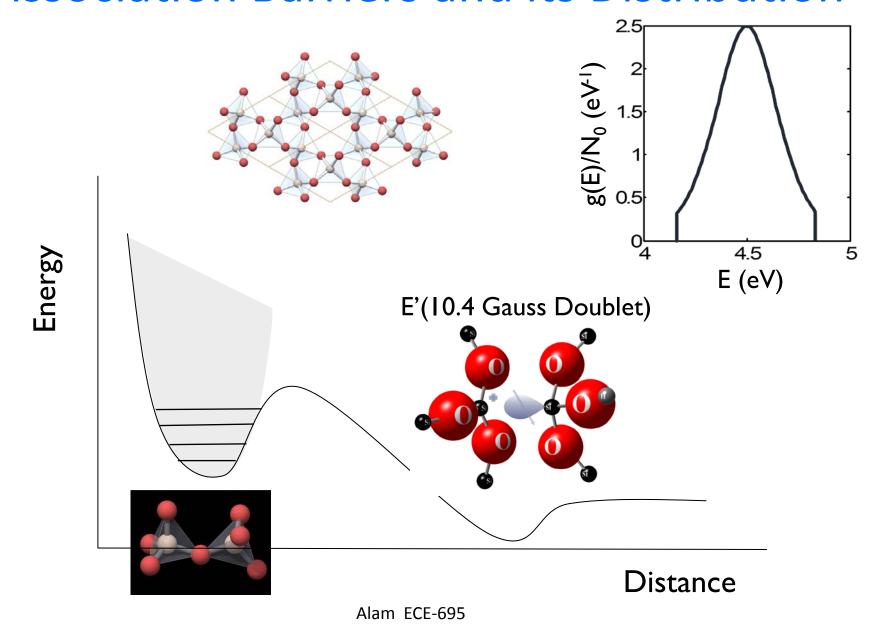
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# Time exponent of degradation



- Does the time exponent remain constant with time?
- How does the time exponent change with bias?

### Dissociation Barriers and its Distribution



# BD model anticipates time exponent

$$\frac{dN_{IT}(t)}{dt} = k_f \left( N_0 - N_{IT}(t) \right)$$

$$\frac{dN_{IT}(t)}{dt} = \int_{E_0 - n\sigma}^{E_0 + n\sigma} k_f(E) \left( g(E) - f(E, t) \right) dE$$

$$2.5 \quad \sigma = 0.1 \quad \text{in a } 3.38$$

$$2\sigma \quad \text{in a } 3.38$$

 $10^{0} \ 10^{2} \ 10^{4} \ 10^{6} \ 10^{8} \ 10^{10}$ 

Time (s)

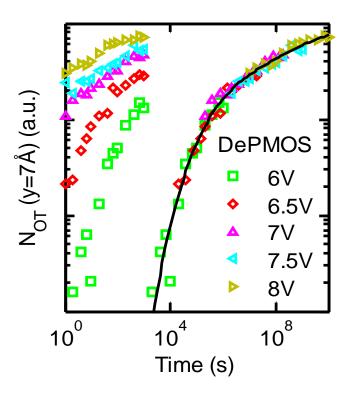
 $2n\sigma$ 

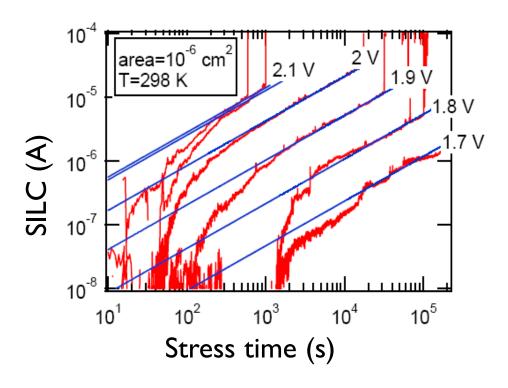
4.5

E (eV)

# Universal function obtained by CP/SILC

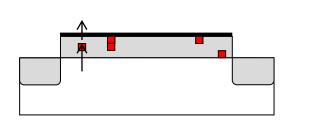
$$N_{SiO} = \sum_{E} g(E) \left[ 1 + e^{-k_F (V_G, V_D)t} \right] dE \equiv f_2 \left( \frac{t}{t_0} \right)$$

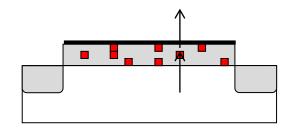




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# Measurement of trap generation by Stressinduced leakage current





- $\Box \Delta I_G = (I_G I_G(0)) / I_G(0)$  at  $V_{\text{sense}}$ : depends on  $T_{OX}$  and  $V_{\text{sense}}$
- $\Box$  Power-law:  $\Delta I_G \propto t^P$ , P usually < 0.5 close to breakdown
- $\Box$  Find t\*, time required to reach a given amount of  $\Delta I_G$

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### **Conclusions**

- Dielectric breakdown has a long history and broad range of physical and technological implications.
- TDDB is important for thick and think dielectrics, but the physics of breakdown is very different.
- Measurement of TDDB at very low voltage has been difficult therefore a theory of dielectric breakdown and accurate measurement techniques (SILC) are very important.
- ☐ For thin oxides, statistical distribution of failure time is a key feature of TDDB. Theory is essential here as well.

### References

There have been considerable amount of work on gate dielectric breakdown. Here I refer to some of the work I have done – additional references can be found in the papers. You could get started by reading "A Future of Function or Failure?" M.A.Alam, Bonnie E.Weir, and P. Silverman, IEEE Circuits and Devices - The Electronics and Photonics Magazine 18(2), pp. 42-48, 2002.

#### Reviews can be found in ....

"Gate Dielectric Breakdown in the Time-Scale of ESD Breakdown," (**Introductory Invited Paper**), B. Weir, C. Leung, P. Silverman, and M. Alam, Microelectronics Reliability, 45, pp. 427-436, 2005.

Modern theory of dielectric breakdown is discussed in ... "Gate dielectric breakdown: a focus on ESD protection," B. E. Weir, C.-C. Leung, P. J. Silverman, and M. Alam, Proc. of IRPS, pp. 399-404, 2004.

"Can an Accurate Anode Hole Injection Model Resolve the E vs. I/E controversy?" [Outstanding Paper Award] M. A. Alam, Jeff Bude, and A. Ghetti, Proceedings of International Reliability Physics Symposium, pp. 21-26, (2000).

"Anode Hole Generation Mechanisms," (Invited paper) A. Ghetti, M.A. Alam, and J. Bude, Microelectronics Reliability, 41(9), pp. 1347-1354, 2001.

#### Theory of soft and hard breakdown are discussed in ...

"Uncorrelated Breakdown of Silicon Integrated Circuits," M. A. Alam, R. K. Smith, B. E. Weir, and P. J. Silverman, Nature, 6914, p. 378, 2002.

"Uncorrelated Breakdown of Silicon Integrated Circuits," M. A. Alam, R. K. Smith, B. E. Weir, and P. J. Silverman, Nature, 6914, p. 378, 2002.

"A Study of Soft and Hard Breakdown: The Statistical Model," M. A. Alam, B. E. Weir, and P. J. Silverman, IEEE Transaction on Electron Devices, 49 (2), pp. 232-238, 2002. Also, see part 2 in TED, 49 (2), pp. 239-246, 2002. "A Phenomenological Theory of Correlated Multiple Soft Breakdown Events in Ultrathin Gate Dielectrics (, M. Alam and R. K. Smith, Proc. of International Reliability Physics Symposium, pp. 406-411, 2003.

### TDDB Characterization techniques are discussed in ...

"SILC as a Measure of Trap Generation and Predictor of TBD in Ultrathin Oxides", M. A. Alam, IEEE Transaction on Electron Devices, 49 (2), pp. 226-231, 2002.

"Theory of Current-Ratio Method for Oxide Reliability: Proposal and Validation of a New Class of Two-Dimensional Breakdown-Spot Characterization Techniques," M. Alam, D. Monroe, B. Weir, and P. Silverman, Proceedings of International Electron Device Meeting, 2005.

### **Review Questions**

- I. What is the name of the failure distribution that we expect for thin oxides?
- 2. For thin oxides, is PMOS or NMOS more of a concern in modern transistors?
- 3. What is DBIE? When does it occur? Can the transistor be still functional?
- 4. In what ways is TDDB compare with NBTI and HCI time-degradation? Explain.
- 5. Why do you suspect that hard breakdown destroys thick oxide, while in thin oxides breakdown can be soft?
- 6. What is stress-induced leakage current? What is 'stress-induced' about it?