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ECE695A: Reliability Physics of Nano-Transistors

Lecture 23: Characterization of Defects Responsible for TDDB

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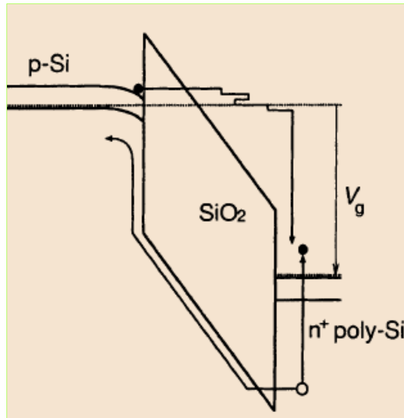
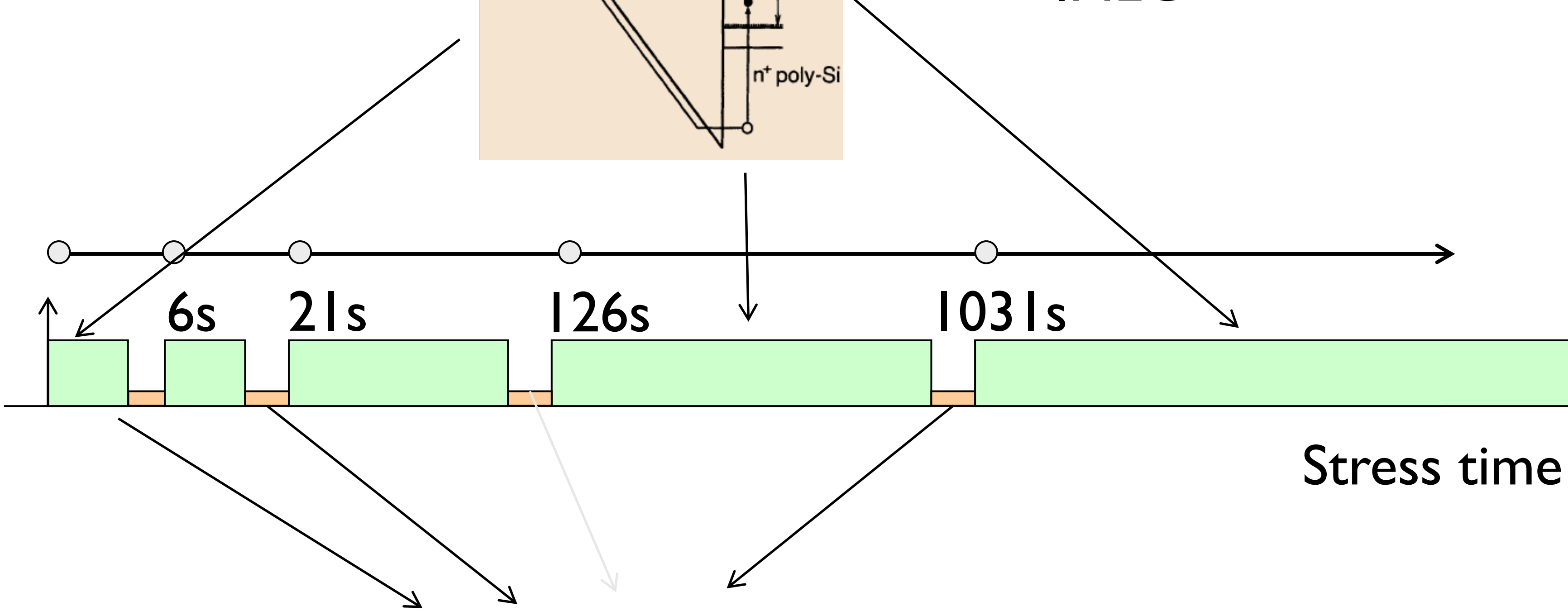
Measurement of bulk oxides



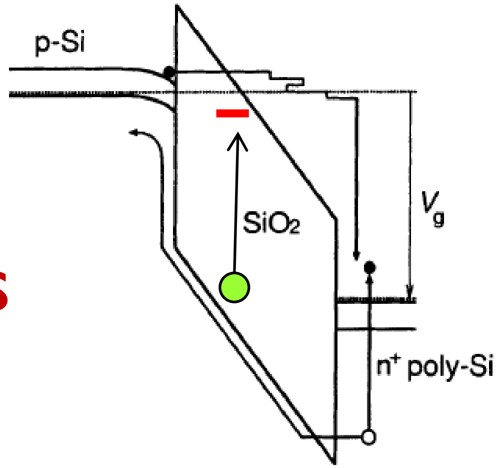
Robin Degraeve
Gido Groeseneken
IMEC



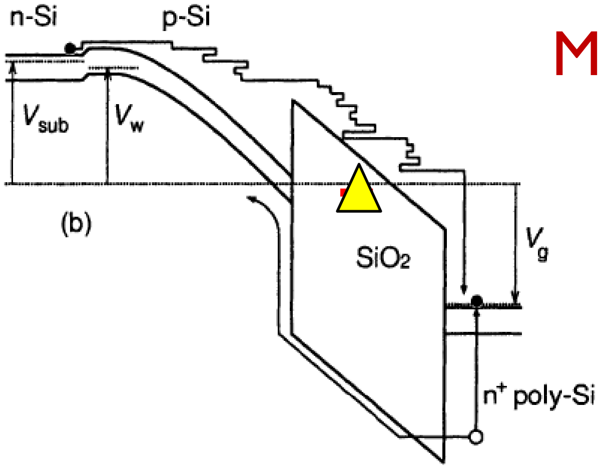
VT, SILC, QY, SDR, Idlin, DCIV, CP methods, …..

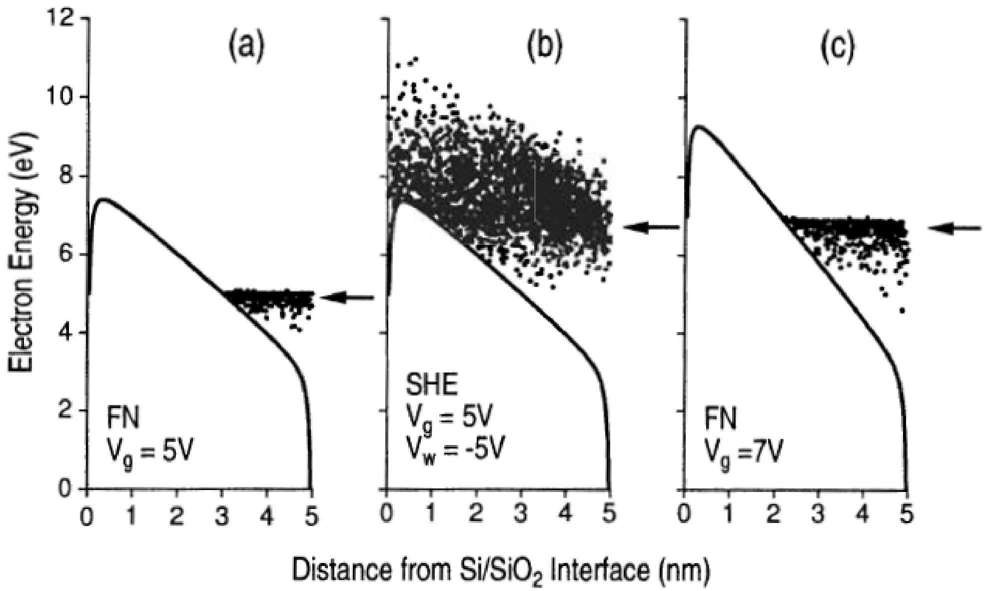
Measurement of bulk traps

Stress



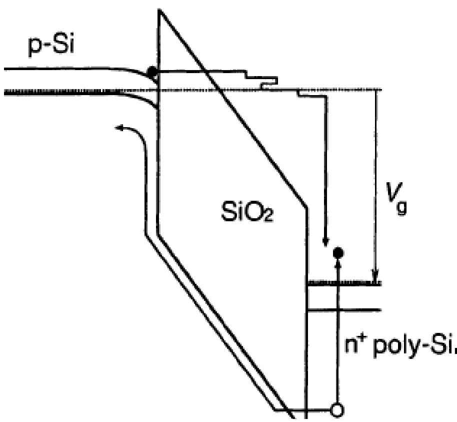
Meas

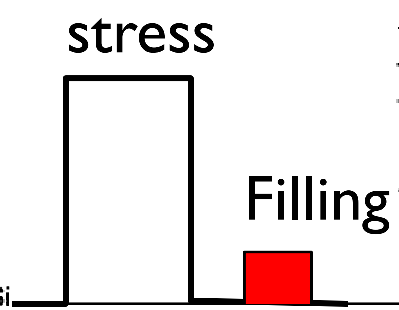


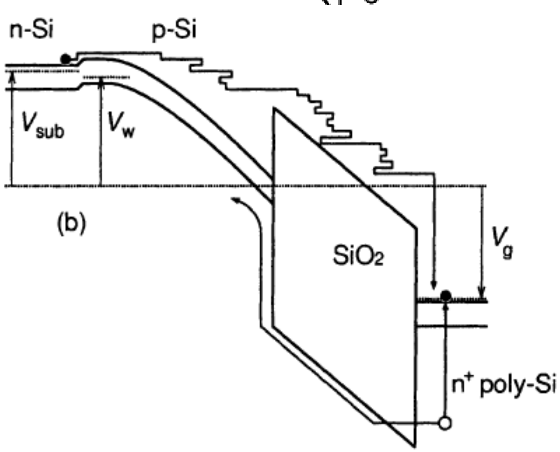


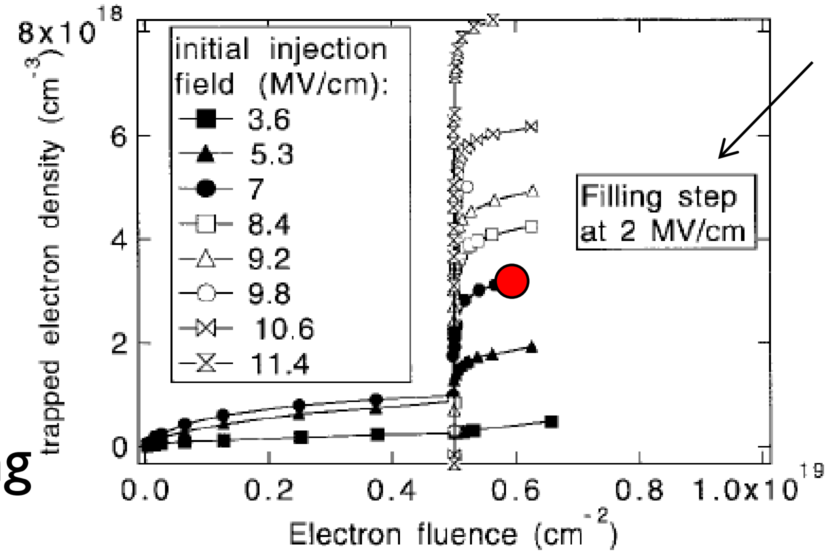
VT Method and Trap Coloring

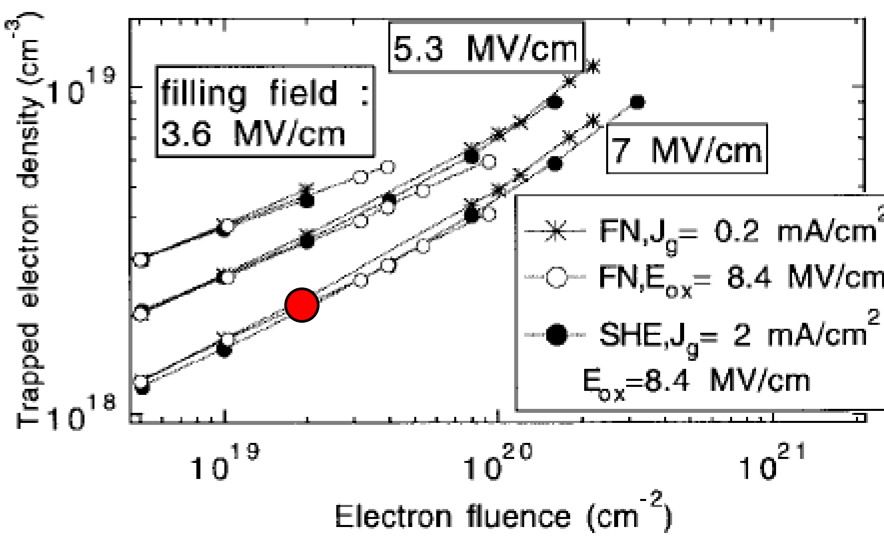
Fluence ~ time









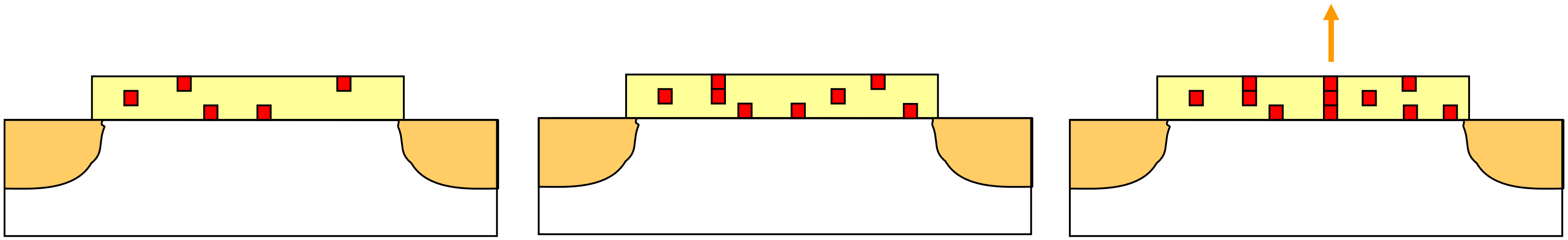


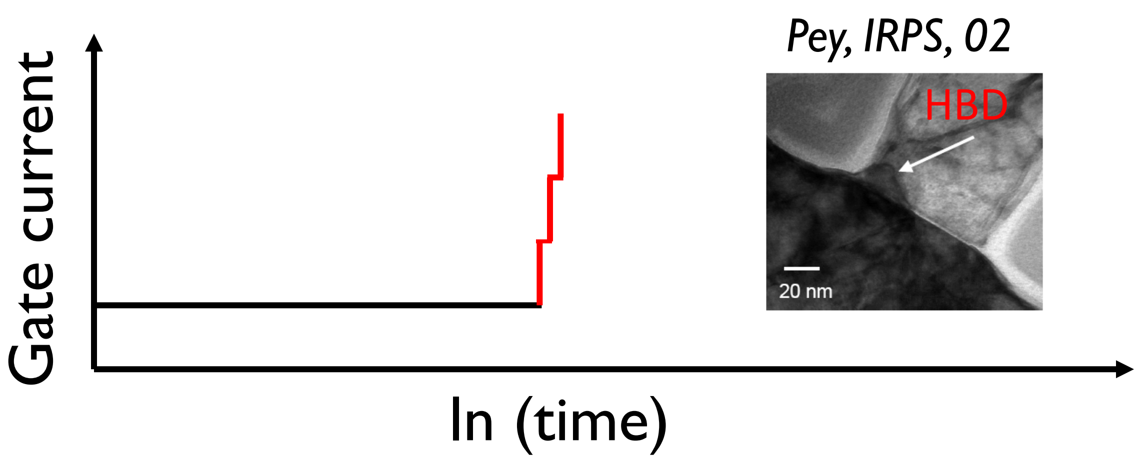
Degraeve, TED, 45(4), 904, 1998

Outline

1. Background: Measurement of bulk traps
2. Shift in Threshold Voltage and C-V Method
3. Stressed induced leakage current (SILC) method
4. Quantum Yield Experiments
5. Conclusions

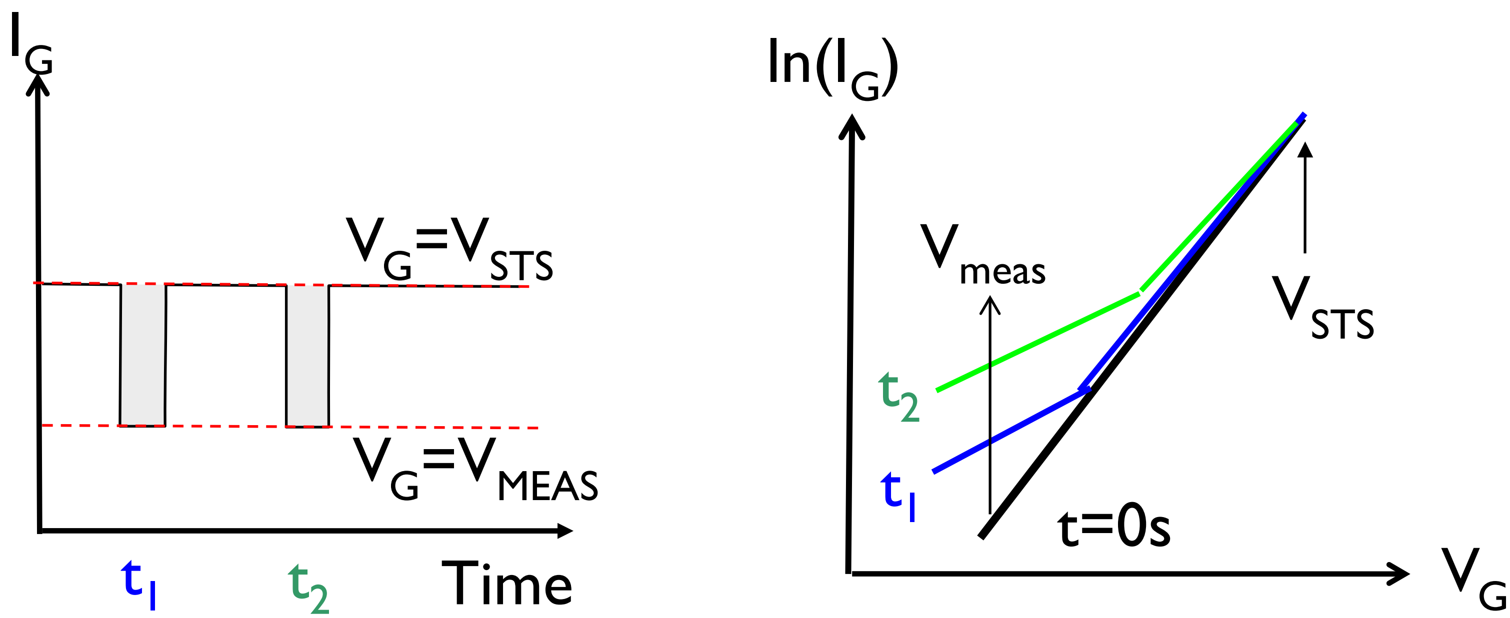
Gate Oxide Breakdown: SiO_2 on Planar Si





Alam, IRPS, 2000; ECS, 2000; Stathis, IBM J. Res/Dev, 46, 2002.

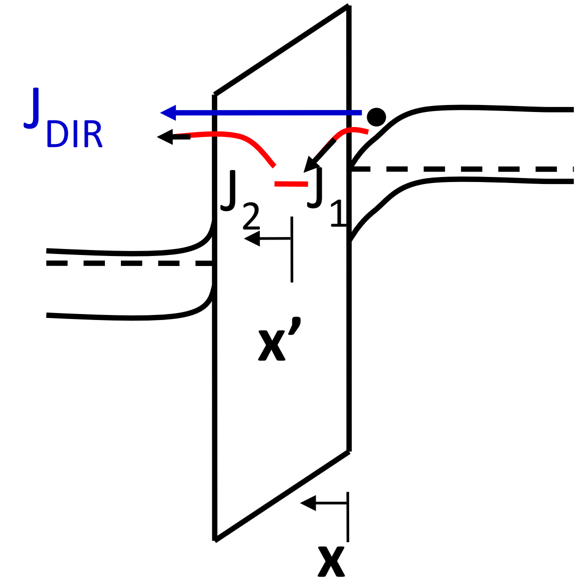
Stress Induced Leakage Current (SILC)



The low voltage leakage part is defined by half the slope of typical I_G-V_G curves !

Stress Induced Leakage Current (SILC)

$$J_{dir} = AP_{dir}\left[f_C(1 - f_A) - f_C(1 - f_A)\right]$$
$$= AP_{dir}\left(f_C - f_A \right)$$



$$J_1 = c\sigma N_{OT} P_1 \left[f_c(1 - f_T) - f_T(1 - f_C)\right]$$

$$J_1 = c\sigma N_{OT} P_1 \left(f_C - f_T \right)$$

$$J_2 = c\sigma N_{OT} P_2 \left(f_T - f_A \right)$$

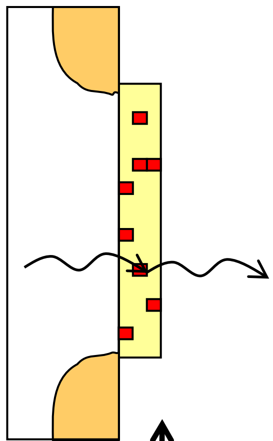
$$J_{SILC} = c\sigma N_{OT} \frac{P_1 P_2}{P_1 + P_2}\left(f_C - f_A \right)$$

$$P(x) \sim e^{-\int_0^x k(x)dx}$$

Stress Induced Leakage Current (SILC)

$$J_{dir} = AP_{dir}\left(f_C - f_A\right) \qquad J_{SILC} = c\sigma N_{OT}\frac{P_1 P_2}{P_1 + P_2}\left(f_C - f_A\right)$$

$$\sim c\sigma N_{OT} P\left(f_C - f_A\right)$$

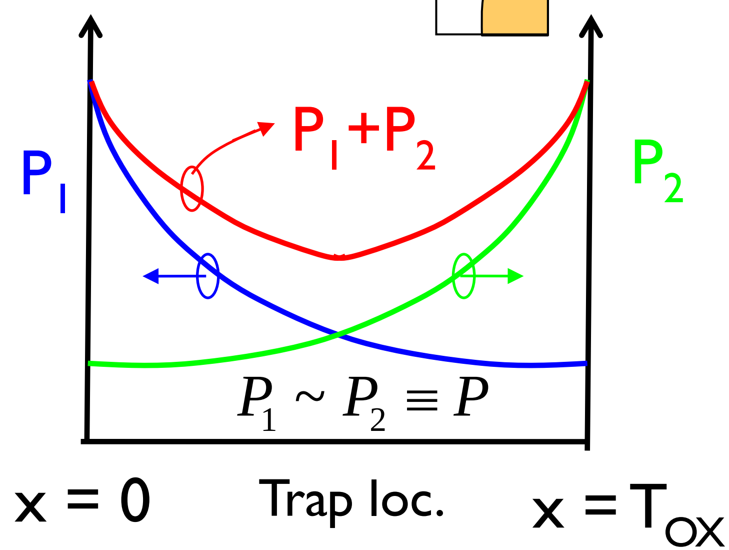


$$P_{DIR} \propto \exp\left(-\int_0^{T_{ox}} k(x)dx\right)$$

$$= \exp\left(-\int_0^{\xi T_{ox}} k(x)dx\right) \times \exp\left(-\int_0^{\xi' T_{ox}} k(x')dx'\right)$$

$$\frac{P_1 P_2}{P_1 + P_2} = \frac{\exp\left(-\int_0^{\xi T_{ox}} k(x)dx\right) \times \exp\left(-\int_0^{\xi' T_{ox}} k(x')dx'\right)}{\exp\left(-\int_0^{\xi T_{ox}} k(x)dx\right) + \exp\left(-\int_0^{\xi' T_{ox}} k(x')dx'\right)}$$

$$= P_{dir} \times \left[\exp\left(-\int_0^{\xi T_{ox}} k(x)dx\right) + \exp\left(-\int_0^{\xi' T_{ox}} k(x')dx'\right)\right]^{-1}$$



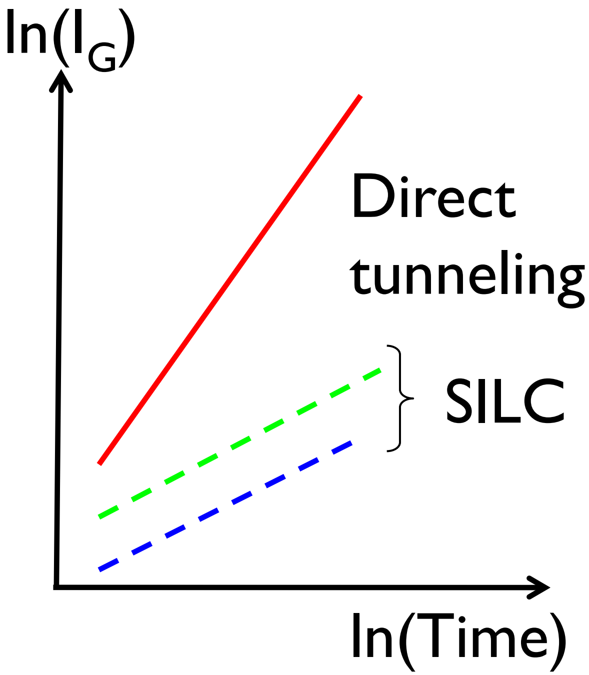
Stress Induced Leakage Current (SILC)

$$J_{SILC} = \frac{c\sigma N_{OT} P}{2}\left(f_C - f_A\right)$$

$$J_{DIR} = AP^2\left(f_c - f_a\right)$$

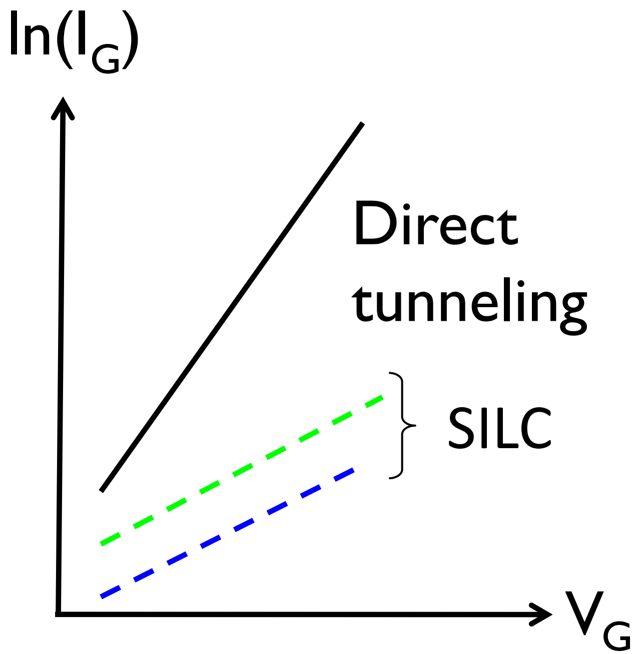
$$J_{SILC} = \frac{c\sigma N_{OT}}{2}\sqrt{\frac{\left(f_C - f_A\right)}{A}}\sqrt{J_{DIR}}$$

$$\ln\left(J_{SILC}\right) = \ln\left(\frac{c\sigma N_{OT}(t)}{2}\sqrt{\frac{\left(f_C - f_A\right)}{A}}\right) + \frac{1}{2}\ln\left(J_{DIR}\right)$$

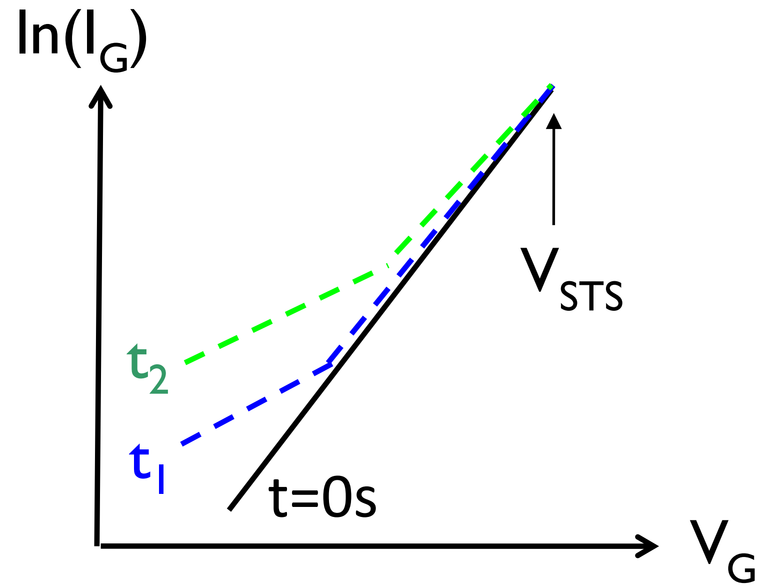


Stress induced leakage current has half the slope of direct tunneling current

I_G-V_G Slope of SILC vs. Direct Tunneling

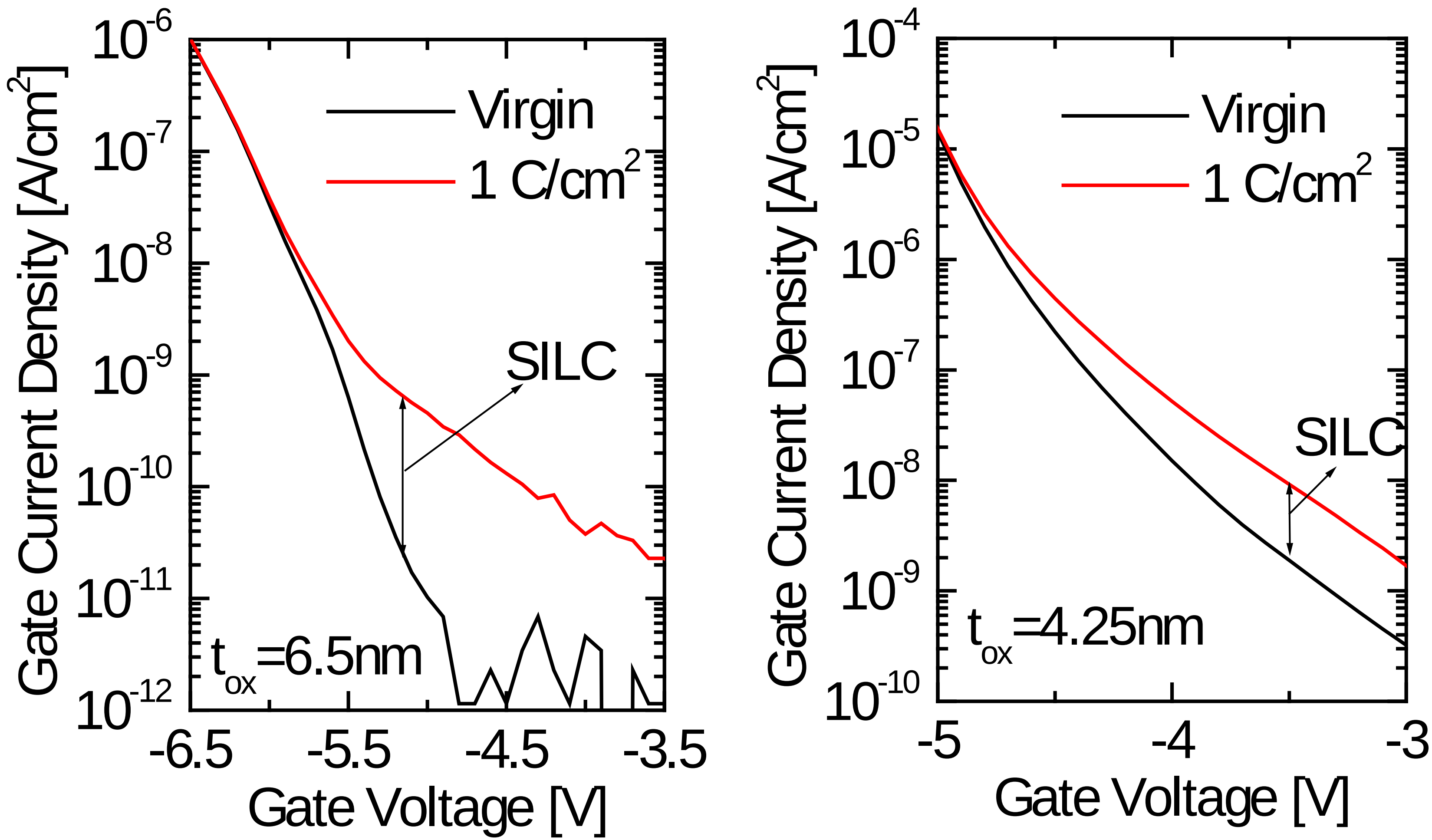


Individual current components

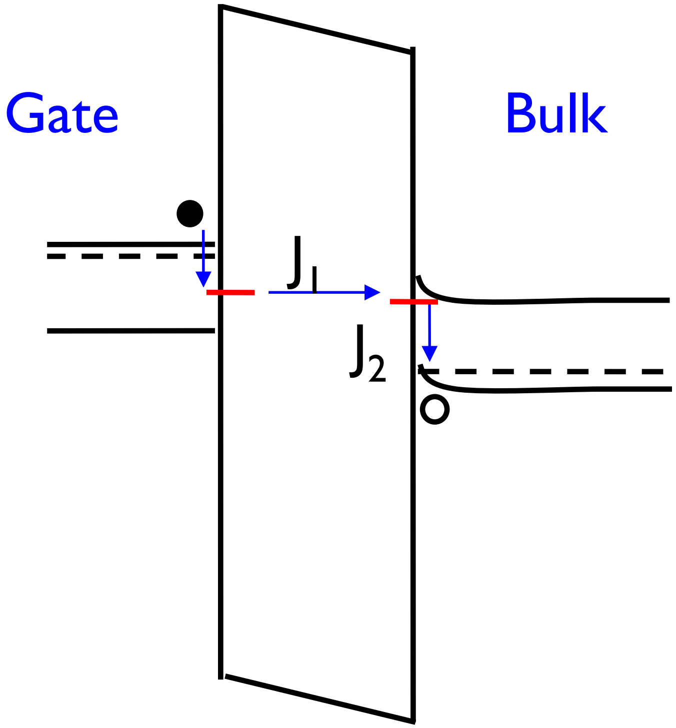


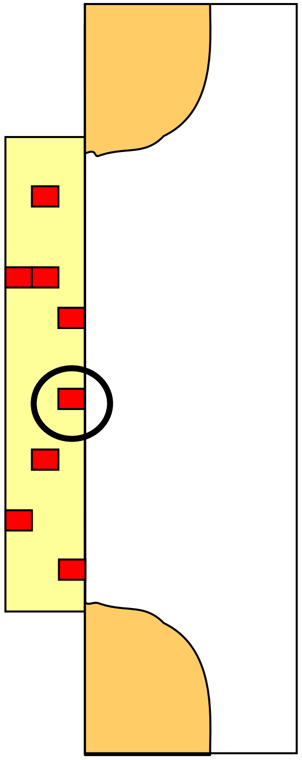
Total current

Native Traps: VG Dependence



Low Voltage Stress Induced Leakage (LV-SILC)

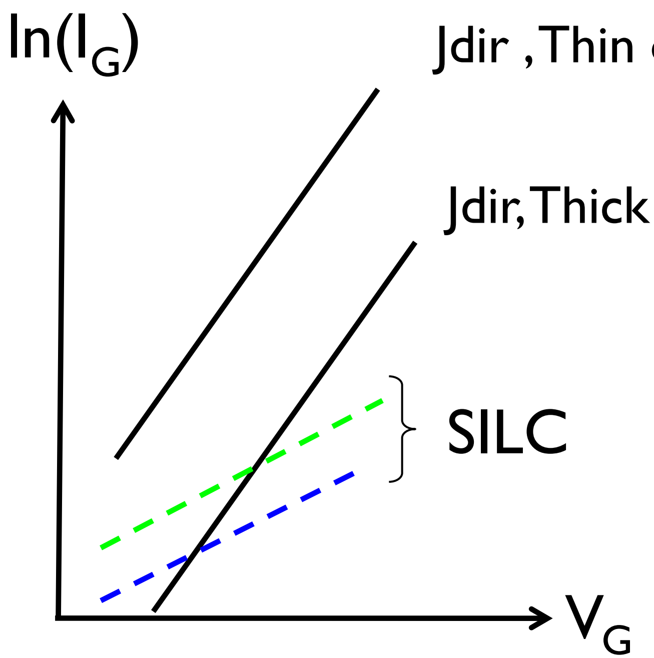




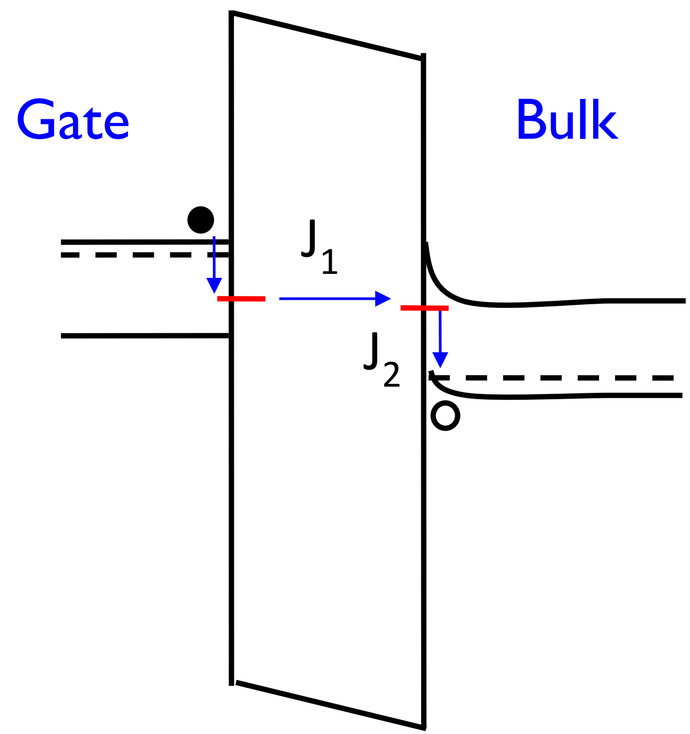
$$J_1 = c\sigma N_{OT} P_{DIR} \left(f_C - f_T \right)$$

$$J_2 = \frac{N_{OT} f_T}{\tau_R}(1 - f_A)$$

Classical SILC and low-voltage SILC

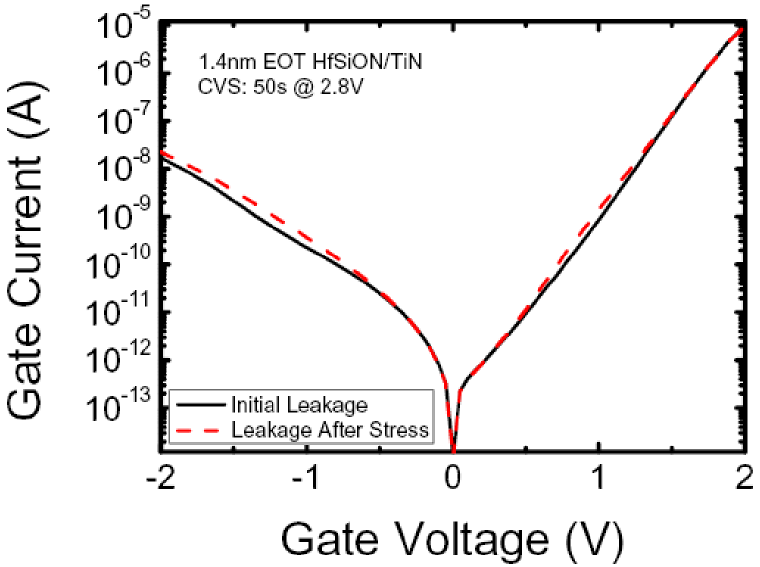


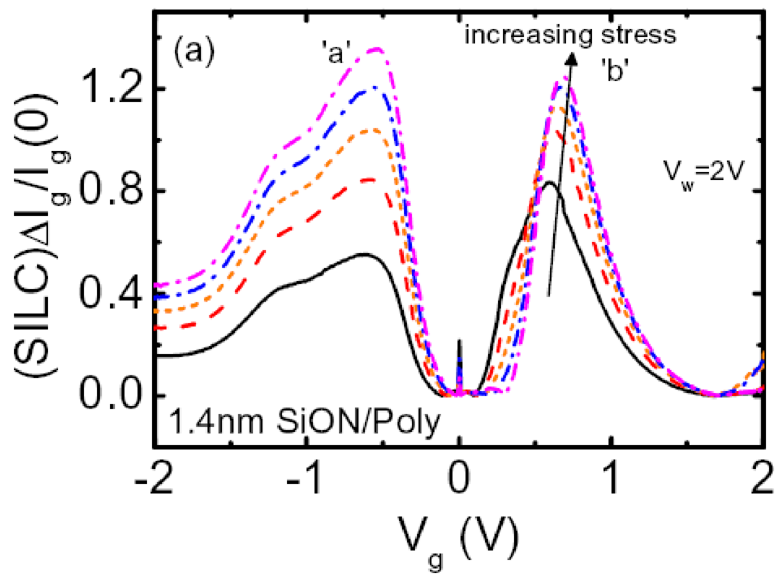
In very thin oxides, classical SILC may always be undetectable



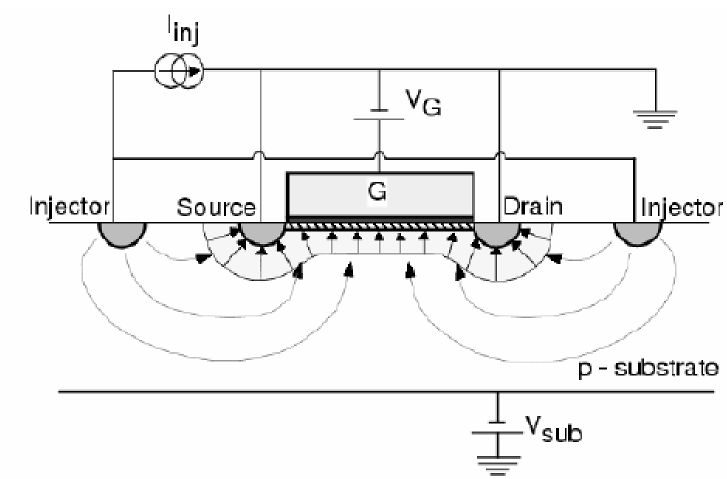
Bias it so that J_{dir} is suppressed

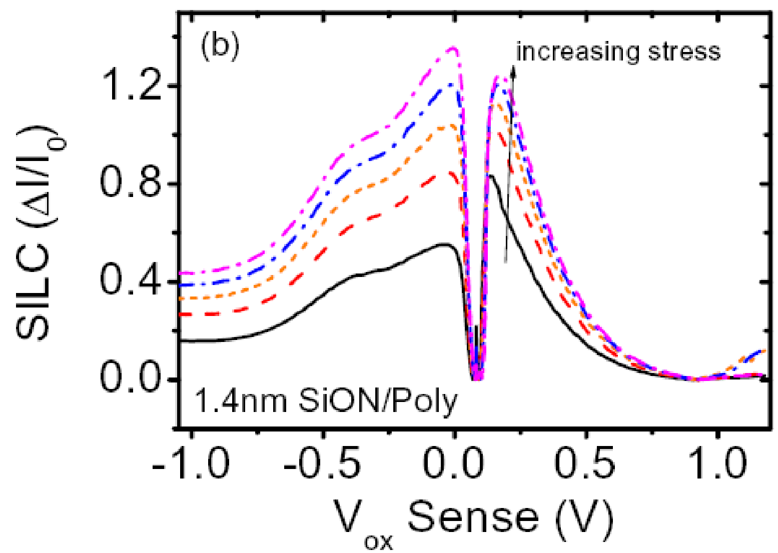
Low-voltage SILC (LV-SILC)



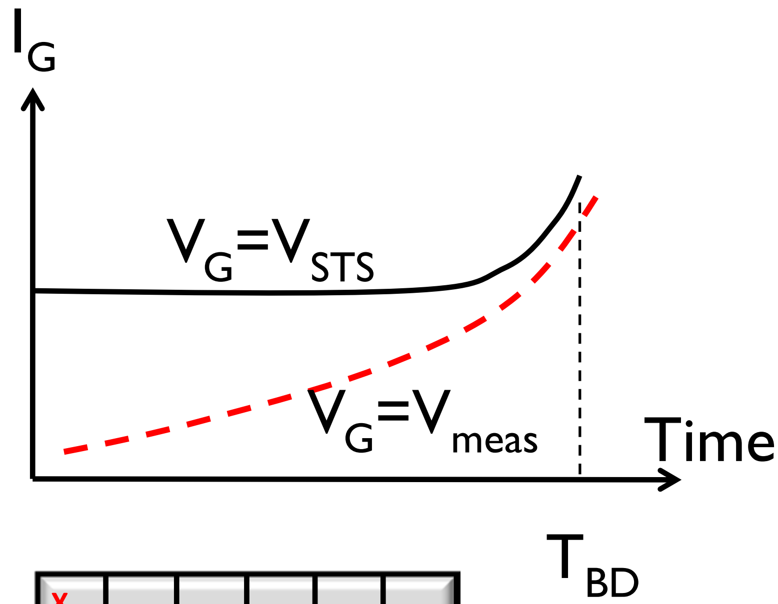


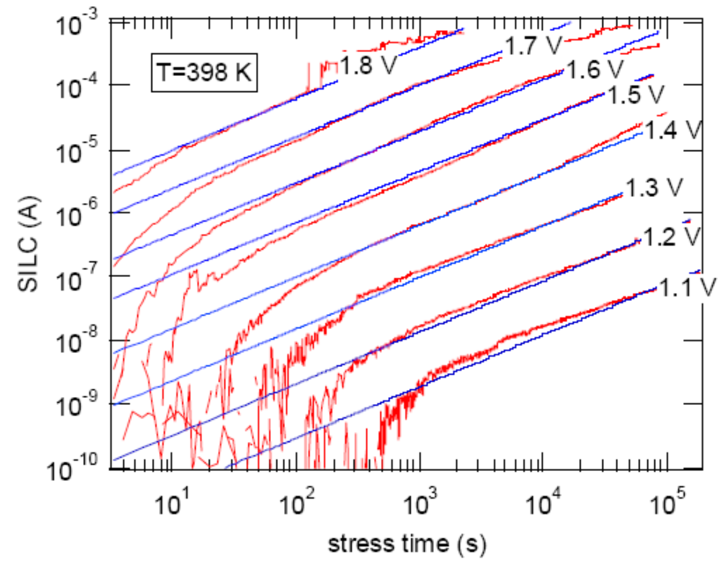
O'Conner et al., IRPS, 2008.

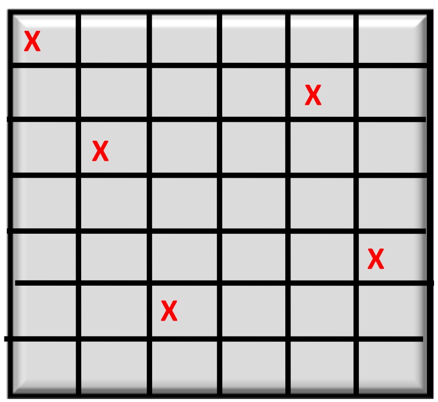


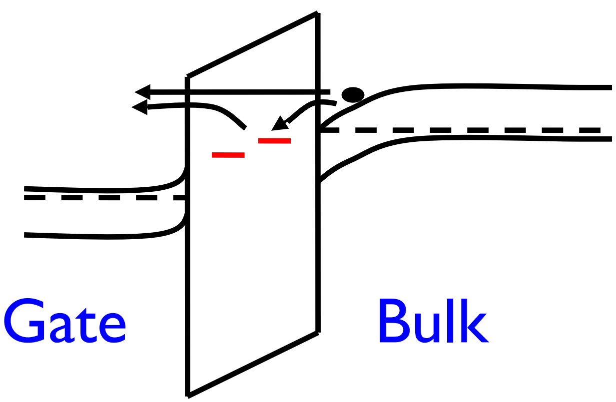


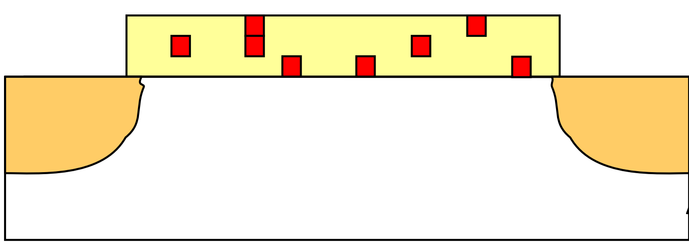
Gate Leakage at Low Voltages (SILC)





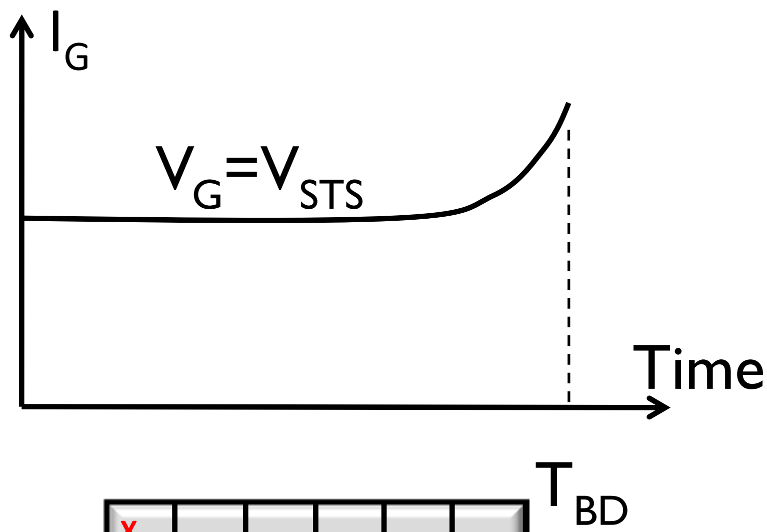


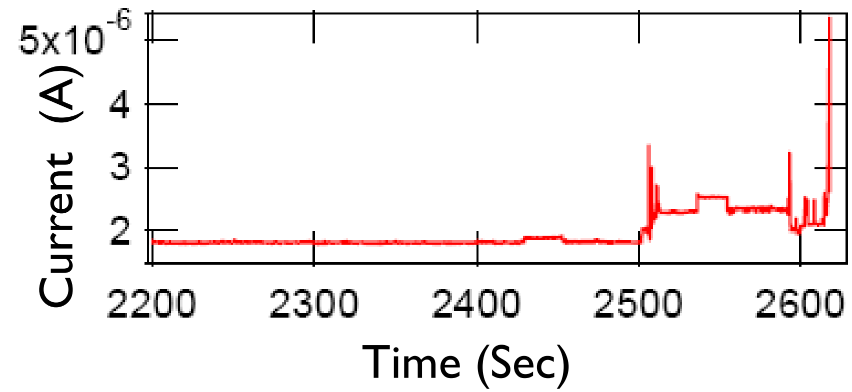


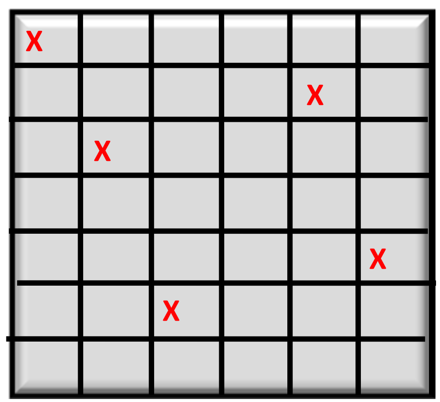


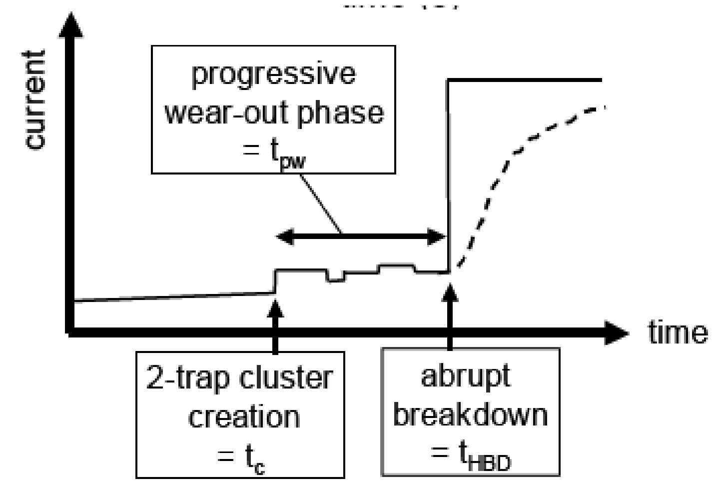
Degraeve, IRPS, 2005.

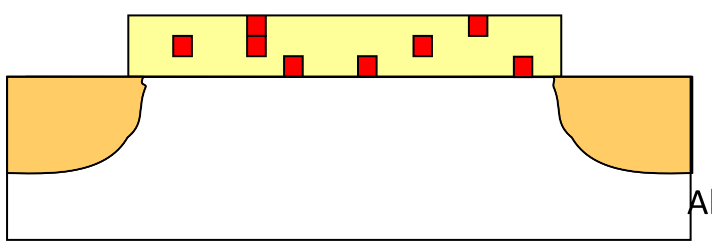
Gate Leakage Fluctuation at Breakdown





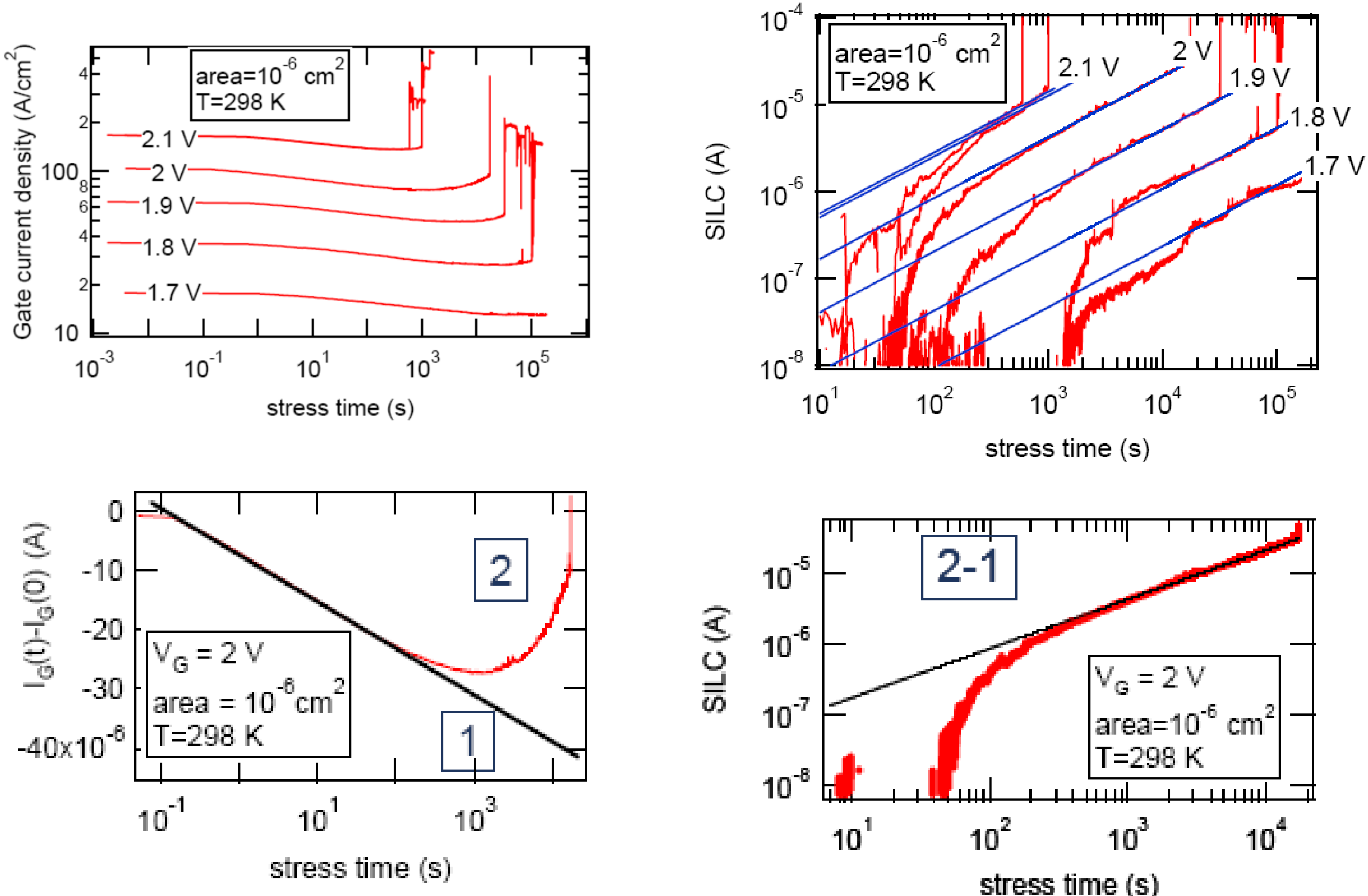






Degraeve, IRPS, 2005.

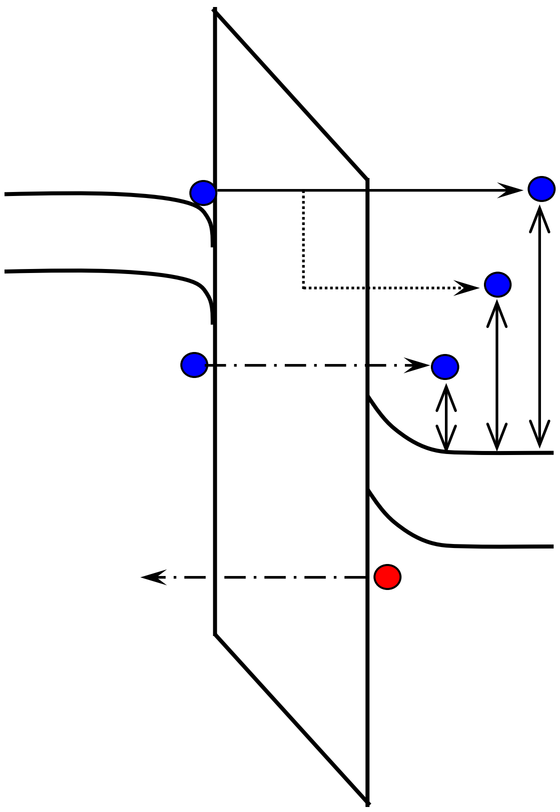
Precaution: log-t Trapping must be subtracted



Outline

1. Background: Measurement of bulk traps
2. Shift in Threshold Voltage and C-V Method
3. Stressed induced leakage current (SILC) method
4. Quantum Yield Experiments
5. Conclusions

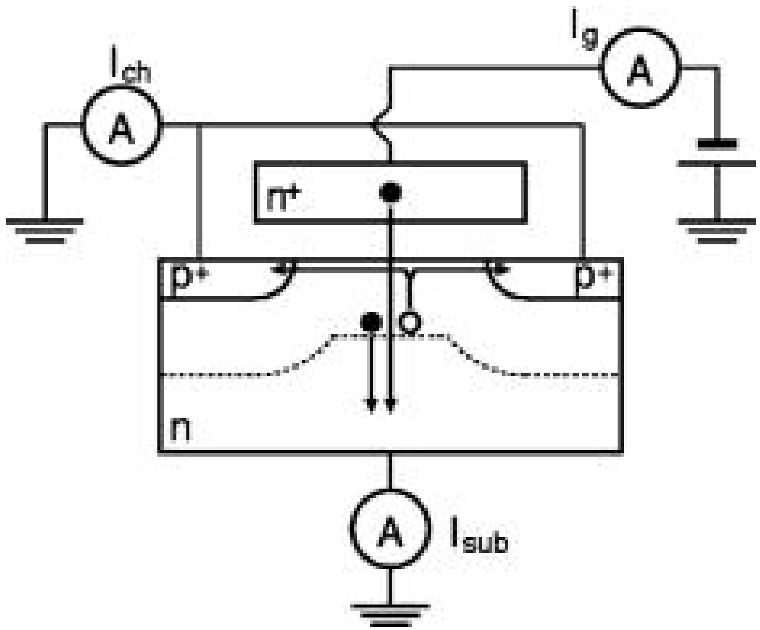
What is the energy of injected electrons?

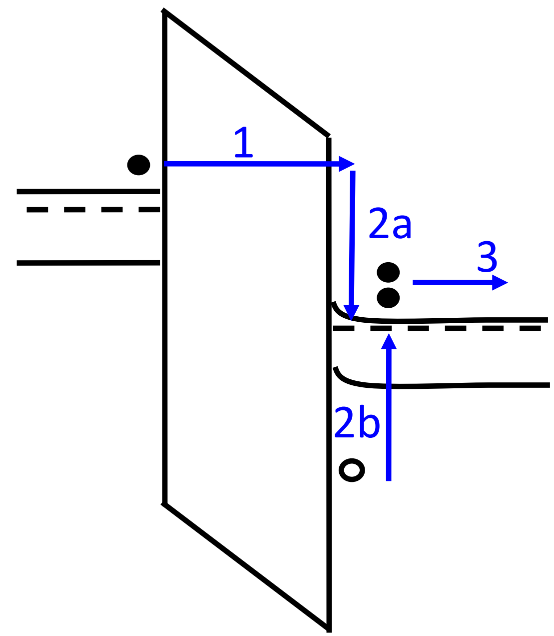


Kamakura, JAP, 88(10), 2000.

- Reliability depends on the energy of injected carriers
- Many tunneling components with different energy characteristics

Quantum yield by carrier separation



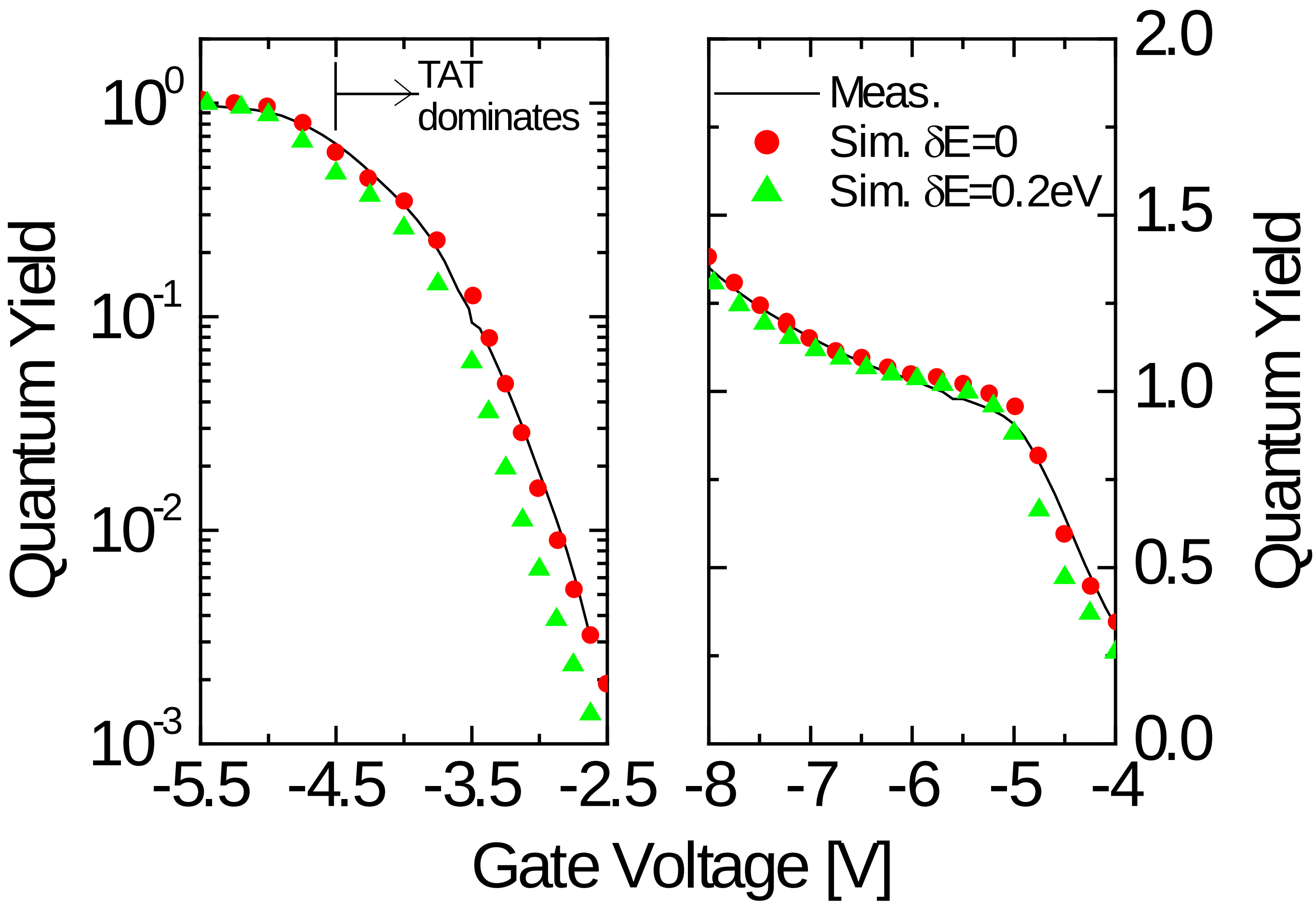


SILC: Inelastic → *Takagi et al., T-ED, 46, 1999, p. 335.*

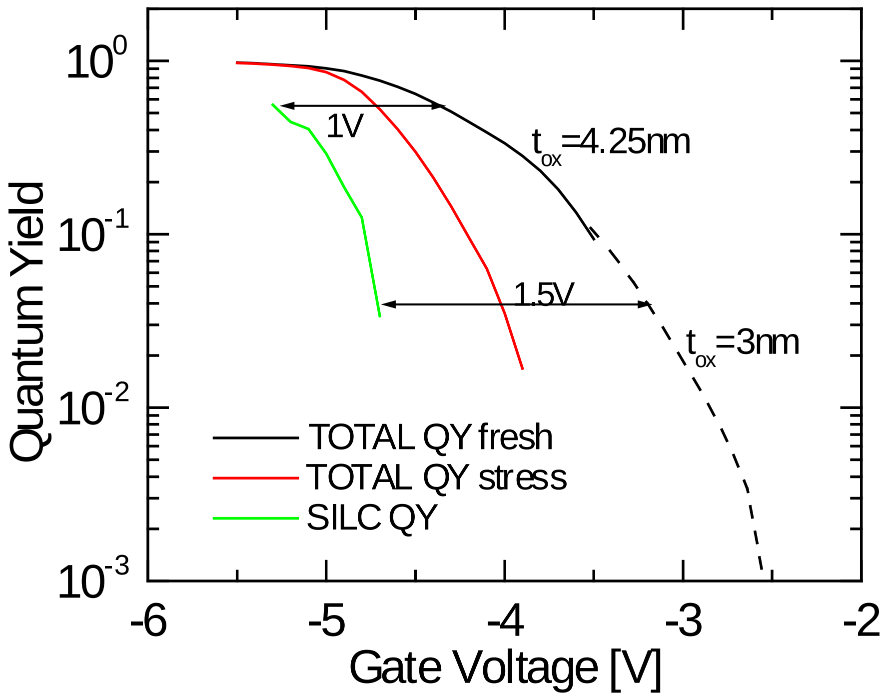
Elastic → *Ricco' et al., T-ED 45, 1999, p. 1554.*

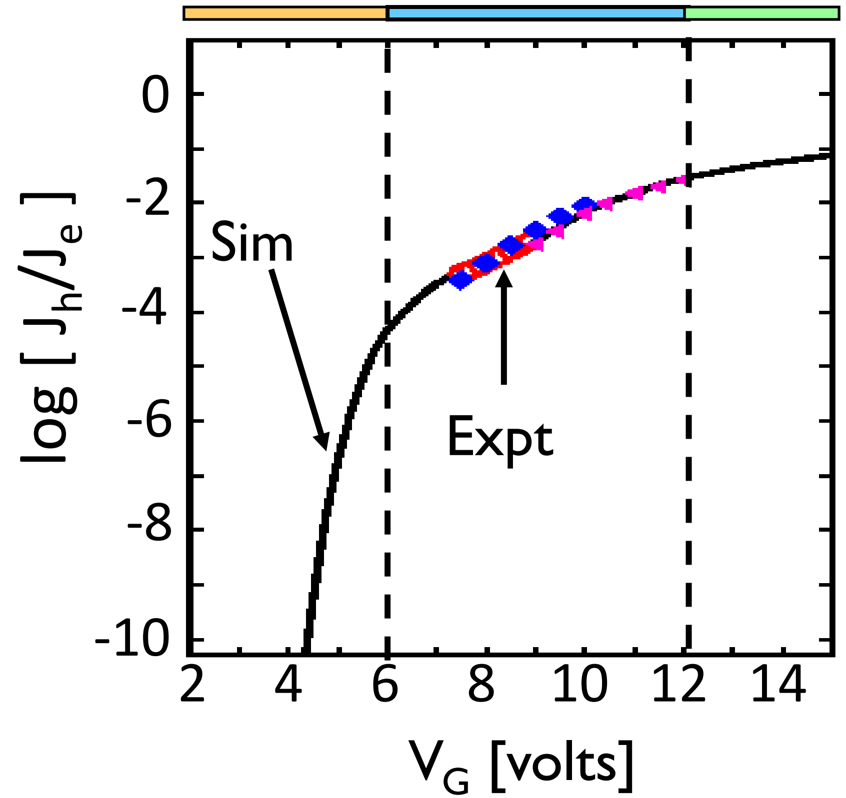
$$QY = \frac{I_{S/D}}{I_G}$$

QY in unstressed Devices



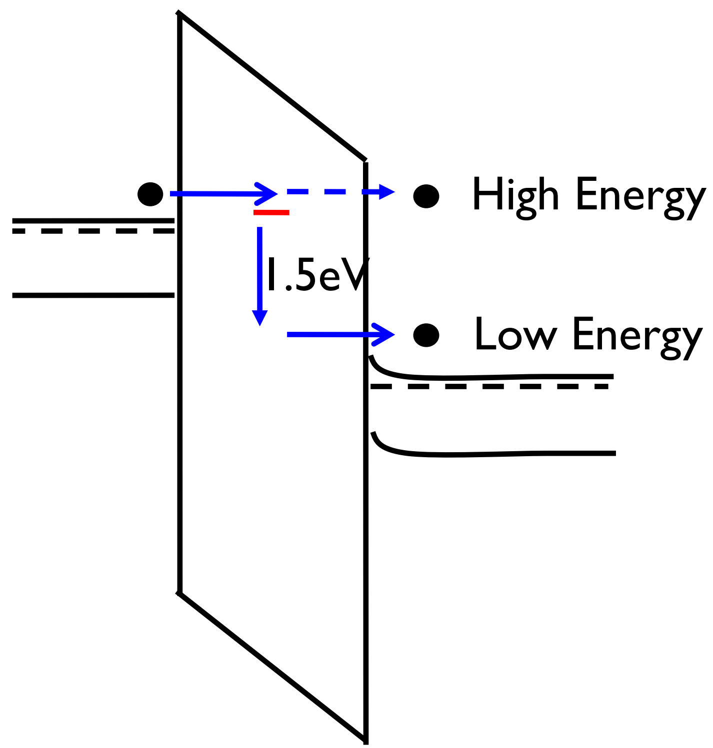
QY in Stressed Devices





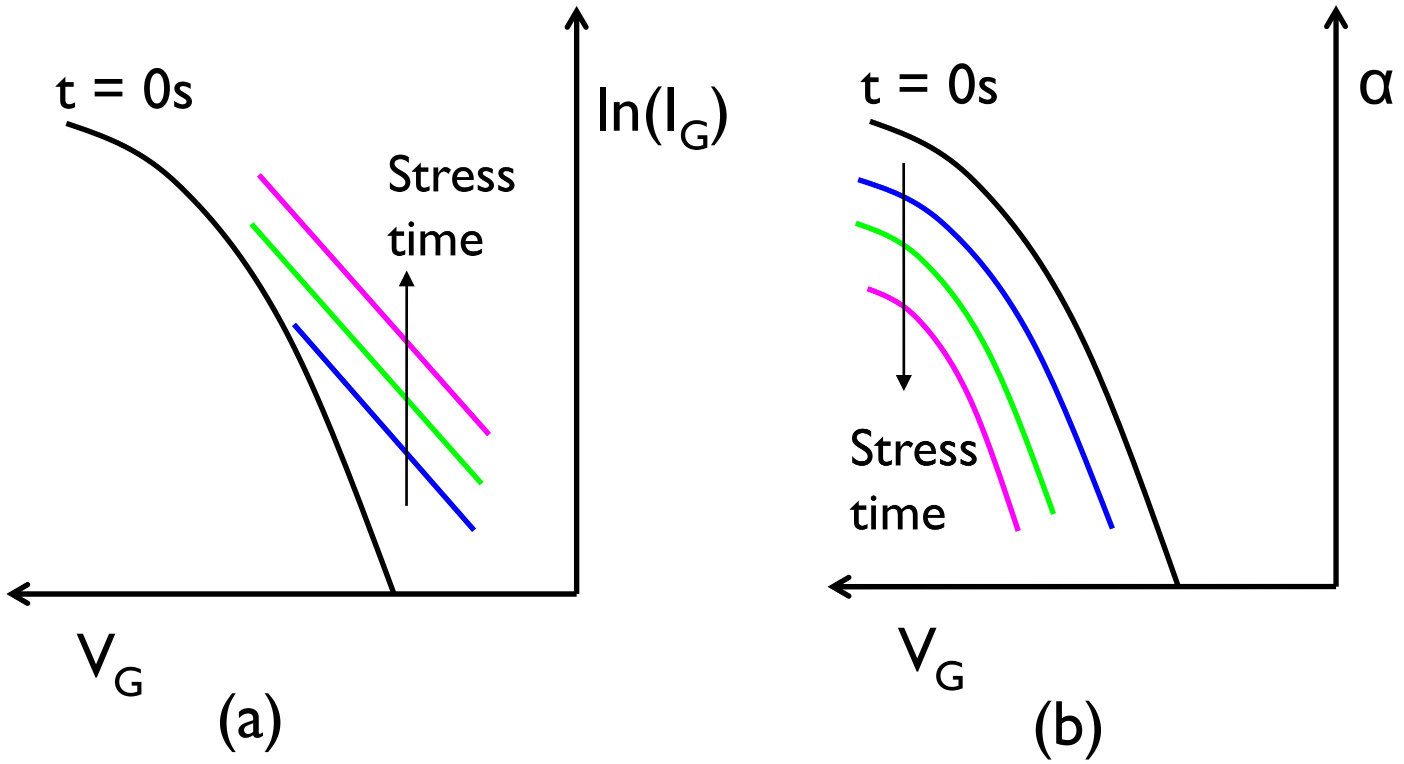
Ref. Koabashi, Analytical formulation of QY.

Inelastic energy spectroscopy by QY



Apparently there is a structural relaxation for oxide defects …

Correlated SILC and QY …



Conclusions

1. Bulk traps require new measurement techniques – such as pulse CV, SILC, and Quantum yield experiments.

2. Classical SILC probe mid-thickness taps (in thick oxides); LV-SILC appropriate probes surface states, in thin oxides).

3. Quantum Yield experiments show that native traps are elastic, while stress-induced traps are inelastic.

4. Low-frequency CP can be correlated to SILC and QY experiments for a comprehensive analysis.

References

Measurements theories are discussed in

- "SILC as a Measure of Trap Generation and Predictor of TBD in Ultrathin Oxides", M. A. Alam, IEEE Transaction on Electron Devices, 49 (2), pp. 226-231, 2002.
- The SILC characterization technique is discussed in detail by R. Degraeve et al., IRPS Proc. 2005. "Degradation and Breakdown of 0.9 EOT gate dielectric". A similar paper is published in Microelectronics Reliability, 80, 440, 2005.
- LV-SILC is discussed by A. Ghetti, Proc. of IEDM, 22.3, 2000. "TBD Prediction from Measurement at Low field and Room temperature using a new Estimator".
- S. Takagi discusses inelastic defects by QY experiments in Proc. of IEDM, 13.2, 323, 1996 (Experimental Evidence of Inelastic Tunneling and a new I-V model for Stress induced leakage current)
- "Theory of Current-Ratio Method for Oxide Reliability: Proposal and Validation of a New Class of Two-Dimensional Breakdown-Spot Characterization Techniques," M. Alam, D. Monroe, B. Weir, and P. Silverman, Proceedings of International Electron Device Meeting, 2005.
- 2D BD-position also discussed in detail in "Exploratory analysis of the breakdown spots spatial distribution in metal gate/high-K/III–V stacks using functional summary statistics" by E. Miranda, E. O'Connor, P.K. Hurley. Microelectronics Reliability, 50, 1294, 2010.

Review Questions

G1: Can you use charge pumping method to determine bulk trap density?

G2: What method would you use if you want to determine defect close to the middle of the oxide?

G3: Define Quantum yield. How does quantum yield change with electron energy?

G4: Can you think of similar use of QY in HCI measurement? Explain.

G5: QY experiments used gate injection technique. Can you use substrate injection?

G6: There is a striking similarity between SILC and SRH in terms of the position of the traps. Can you say what the similarity is?

G7: What is the difference between SILC and LV-SILC ? Why do we use LV-SILC?