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ECE695: Reliability Physics of Nano-Transistors
Lecture 27: Correlated TDDB in Off-State HCI

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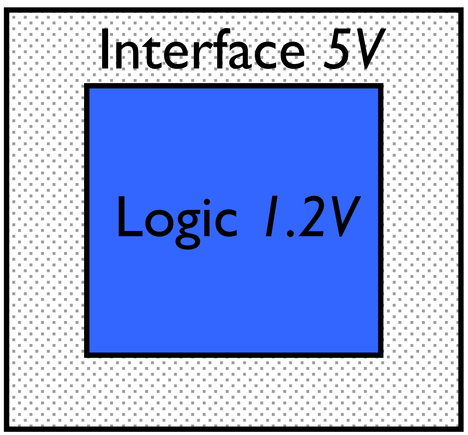
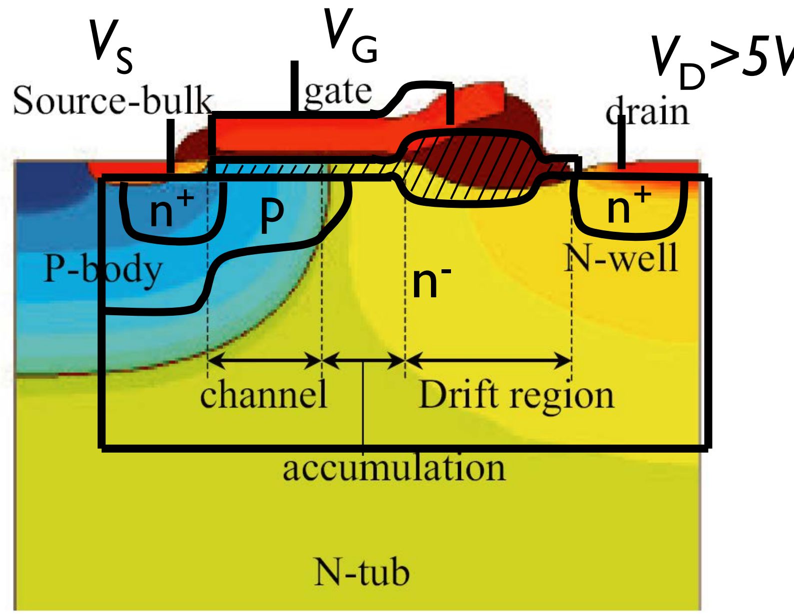
Outline

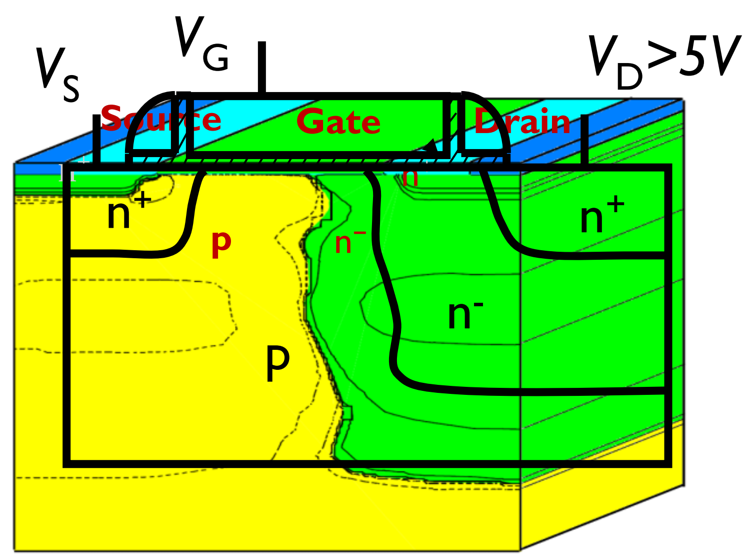
1. Recall: ON vs. OFF State HCI Degradation
2. SiH vs. SiO bonds and theory of universal scaling
3. Dielectric Breakdown during HCI
4. Conclusions

Recall: HCI degradation in non-logic transistors



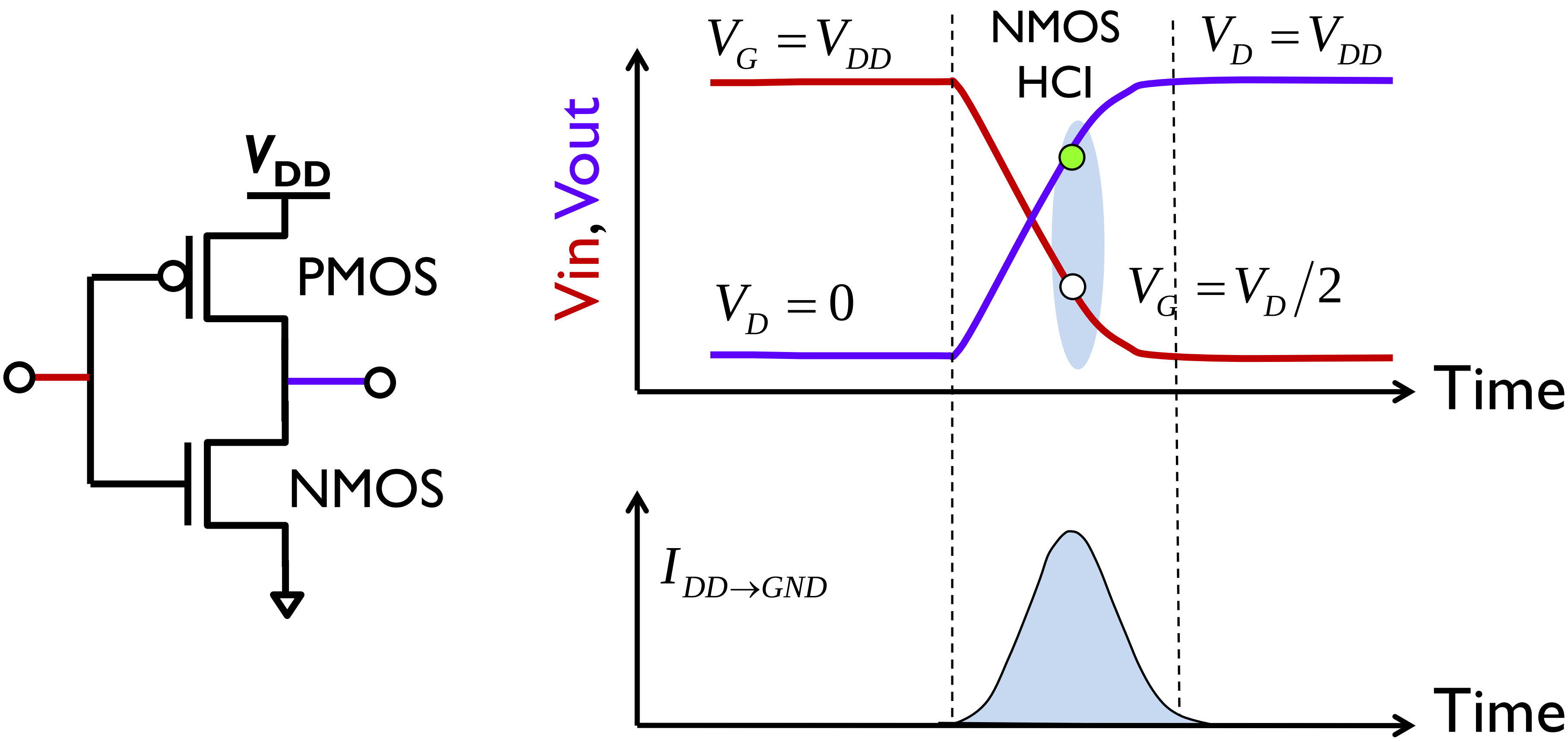


LDMOS



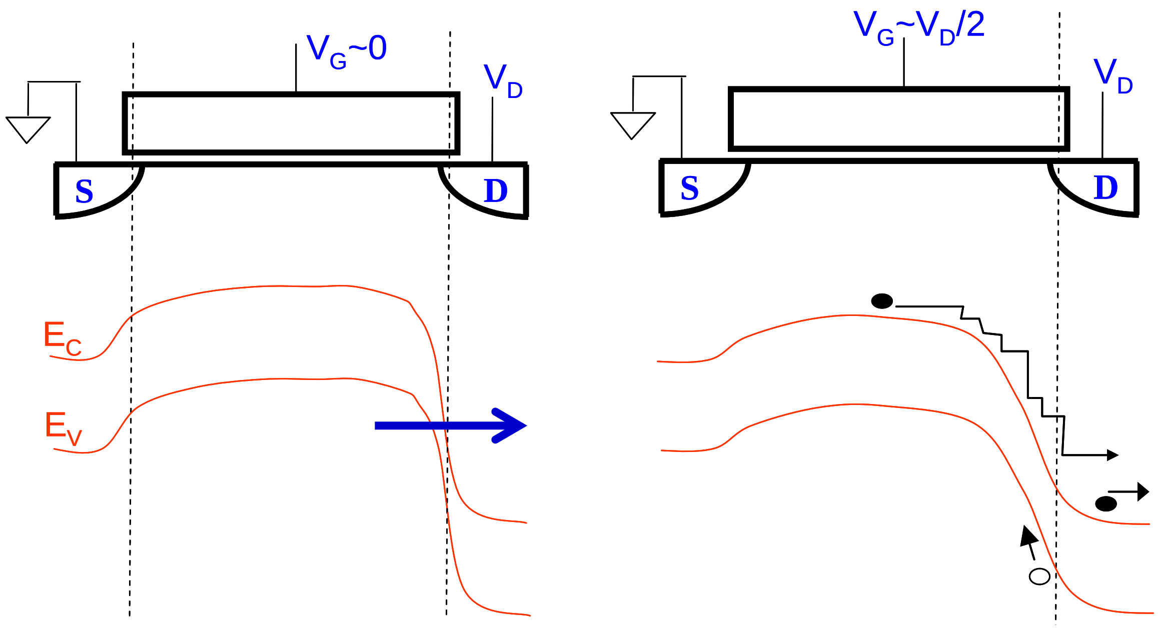
DeMOS

Classical HCI … only ON state?!



True only for logic transistor, at relatively low operating voltage

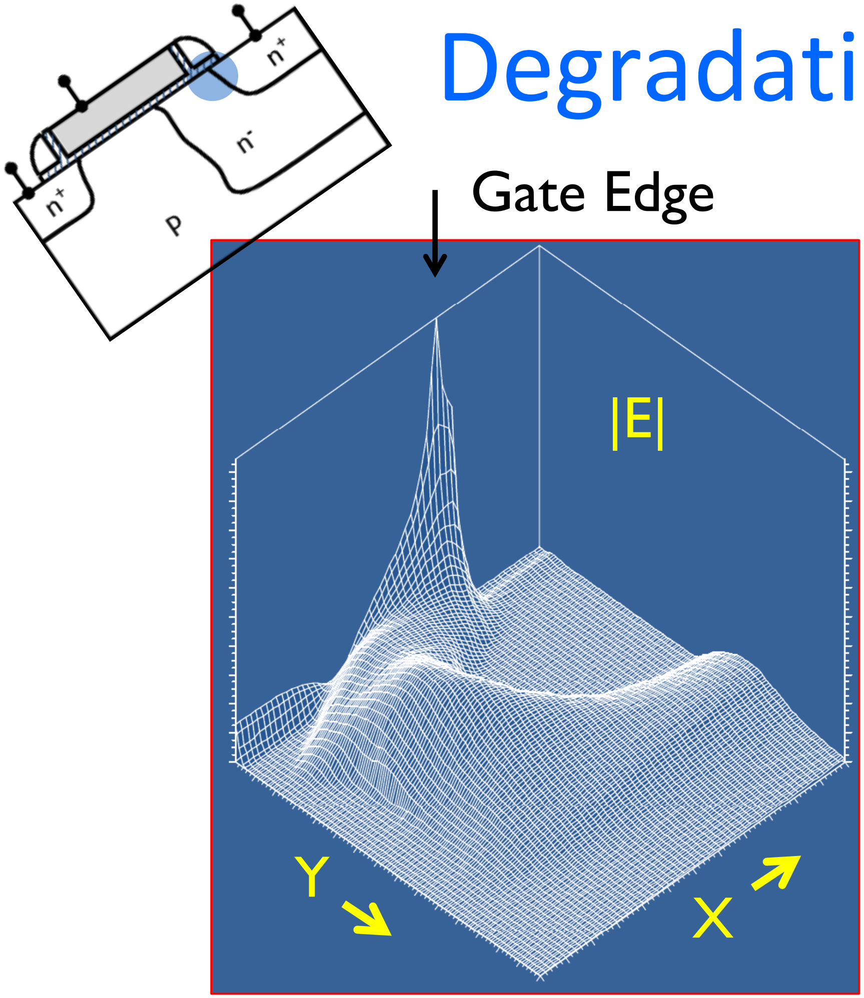
Recall: OFF state HCI is possible, if …

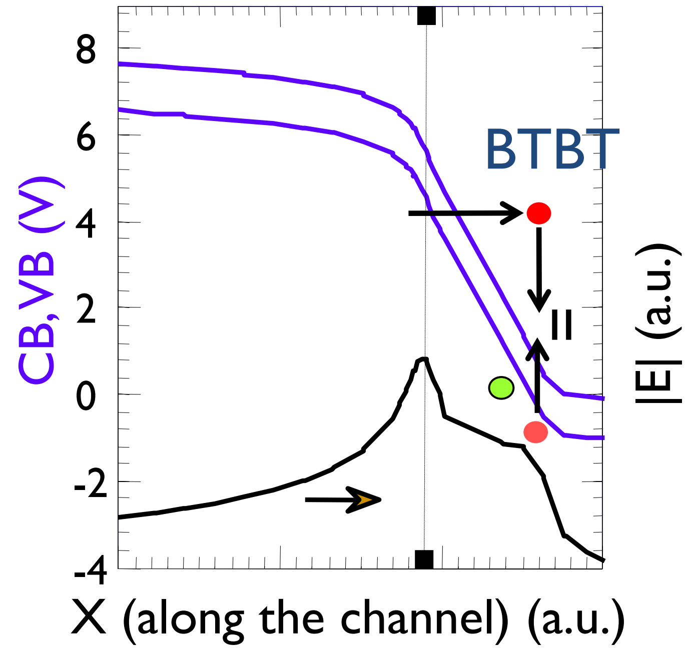


… large band-to-band tunneling at high VD

OR as parasitic degradation in accelerated tests of logic transistors

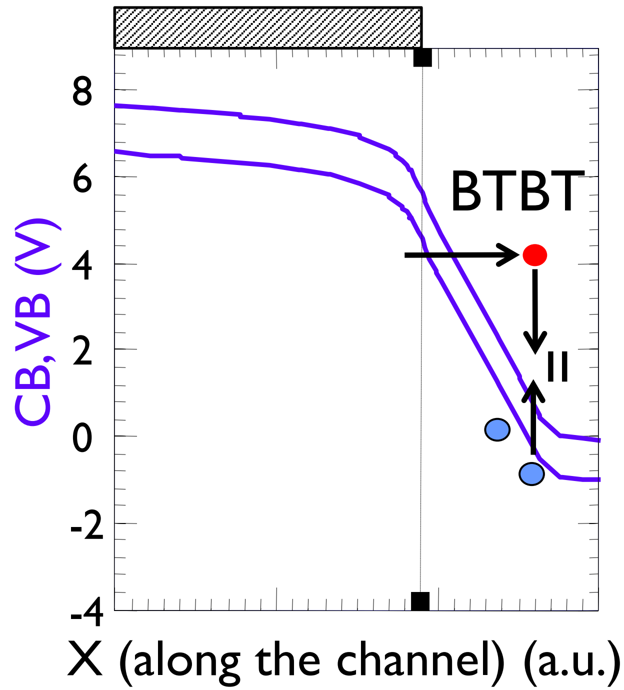
Degradation mechanism

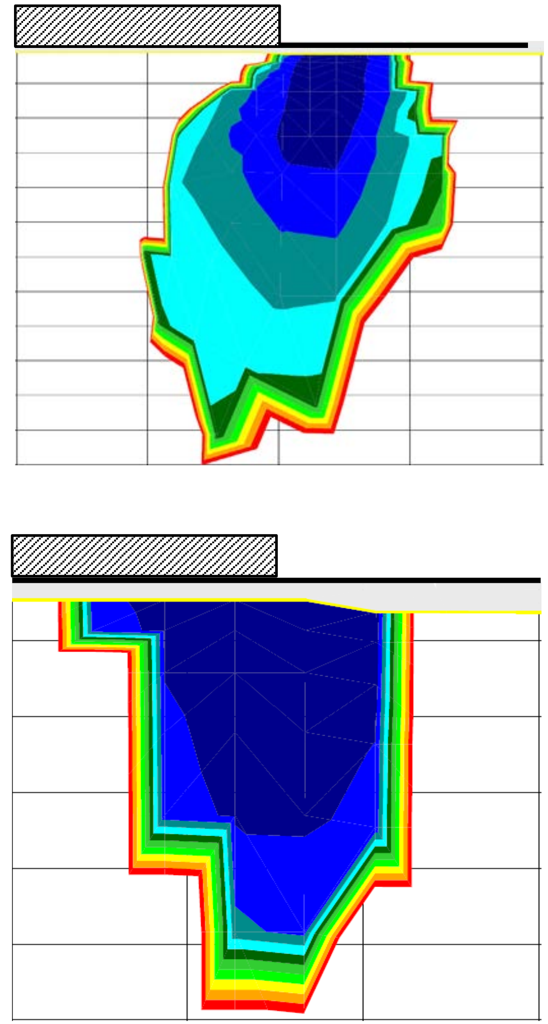




Electric field peaks at the surface leading to BTBT & Impact ionization

Heating of electrons generated by BTBT





Hot Electron
E > 3.1eV

Hot hole
E > 4.7eV

Impact Ionization of BTBT current generate hot carriers

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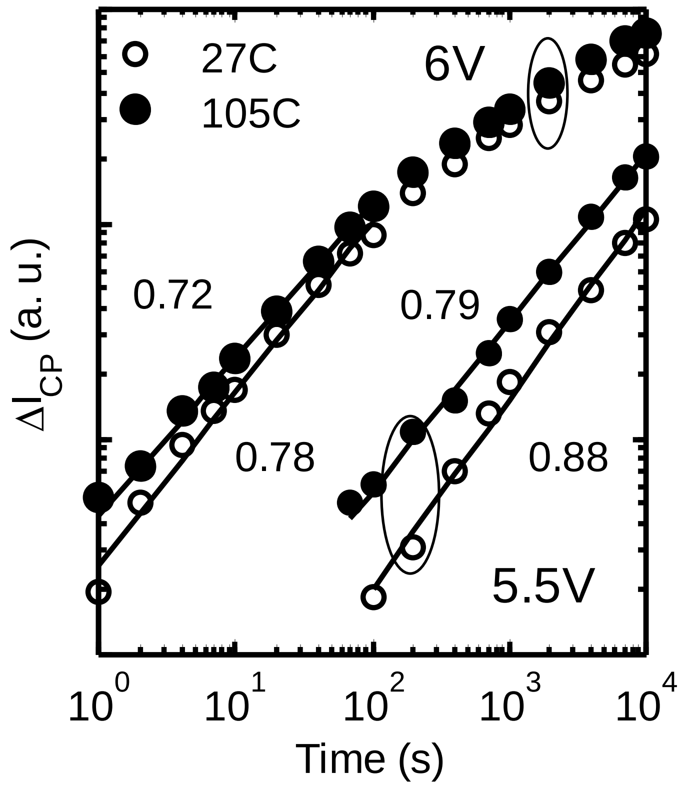
1. ON vs. OFF State HCI Degradation

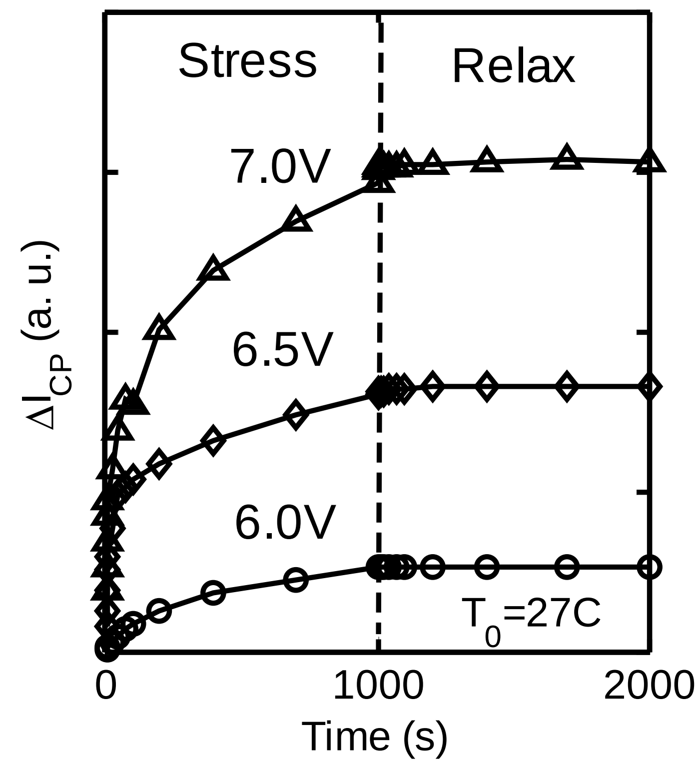
2. SiH vs. SiO bonds and theory of universal scaling

3. HCI by TDDB: Puzzle of the Weibull slope

4. Conclusions

Generation & recovery of N_{OT} in Off-state



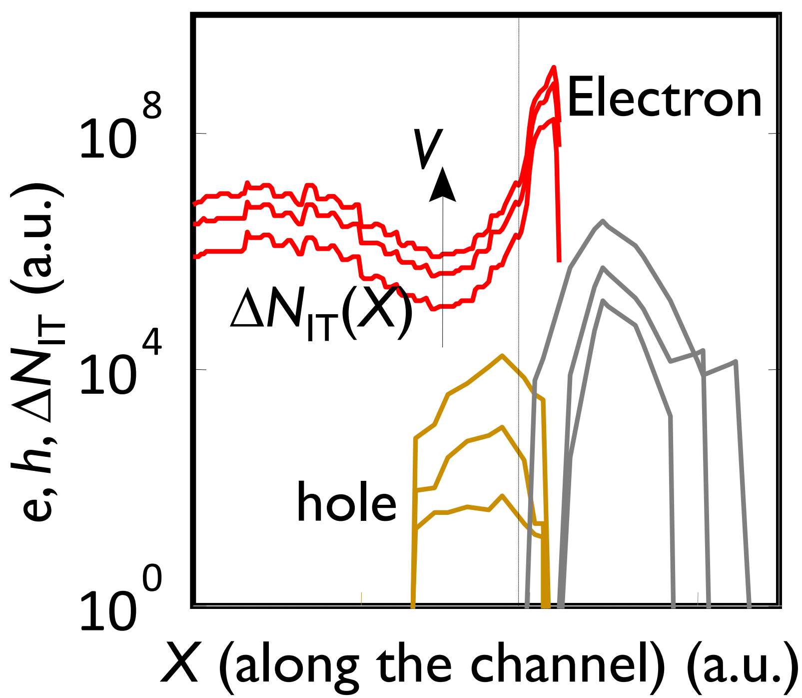


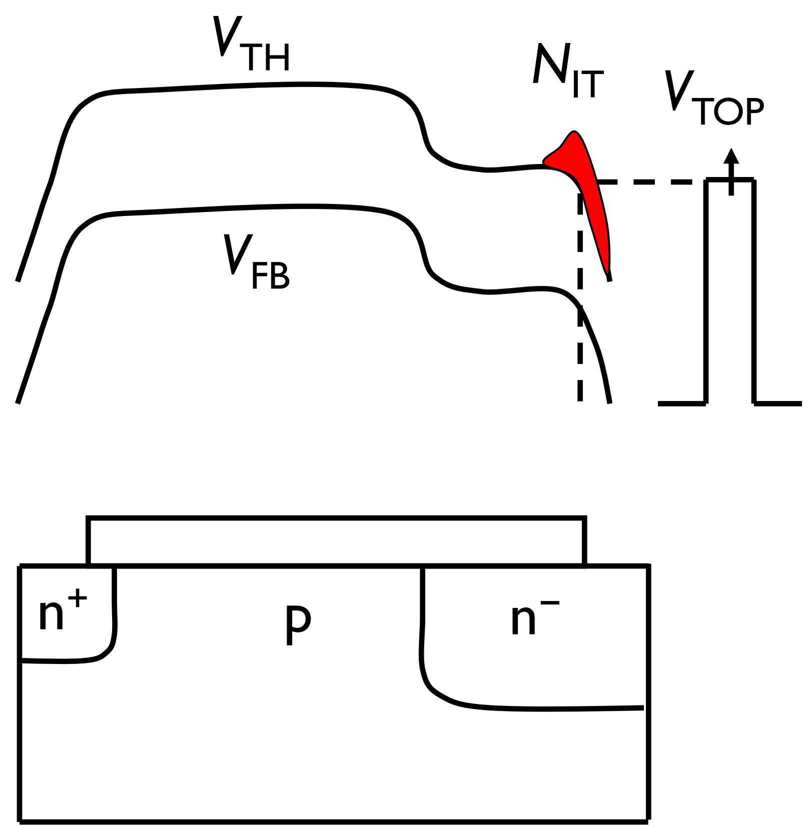
Higher time exponents

No recovery

Most of the bonds broken are Si-O …

Correlation of hot hole and N_{IT}





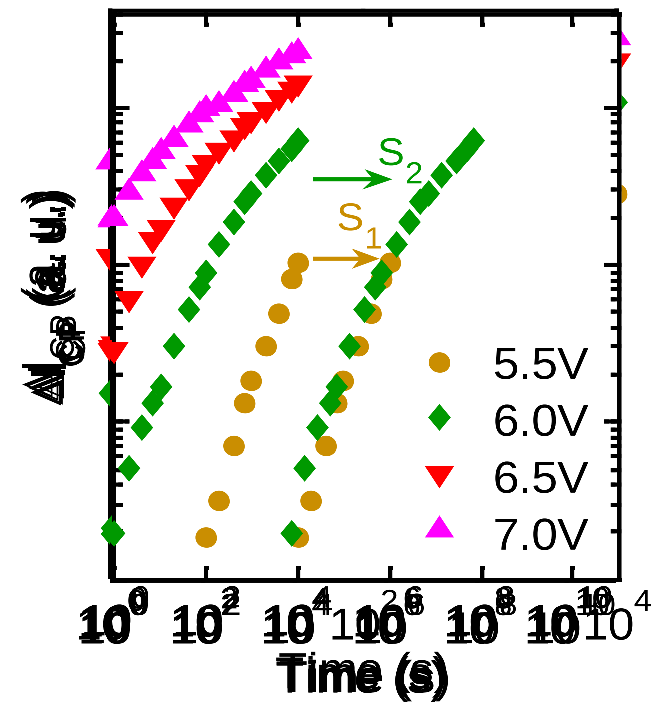
Lateral profiling of N_{IT} correlates well with hot carrier profile by SMC

Recall: voltage dependent constant t_0

$$N_{IT}^{SiH} = \left(\frac{k_F(V_G, V_D)N_0}{k_R}\right)^{\alpha} t^n \equiv \left(\frac{t}{t_0}\right)^n = f_1\left(\frac{t}{t_0}\right)$$

$$N_{IT}^{SiO} = \sum_{\mathcal{E}} g(\mathcal{E})\left[1 + e^{-k_F(V_G, V_D)t}\right] d\mathcal{E} \equiv f_2\left(\frac{t}{t_0}\right)$$

$$t_0^{-1}(V_G, V_D) = I_G = k\frac{I_D}{W_{eff}}\left[\frac{I_{sub}}{I_D}\right]^{\Phi_{ii}/\Phi_i}$$



How to determine t_0 …

$$t^*/t_0(V_G, V_D) = f^{-1}(N_{IT}^*) = \text{const.}$$

$$t_0(V_G, V_D) \propto t^*(V_G, V_D)$$

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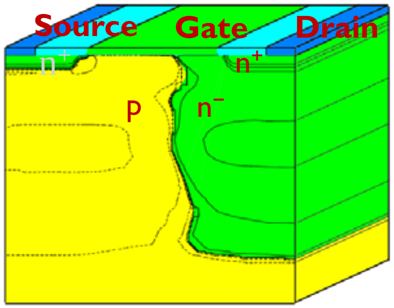
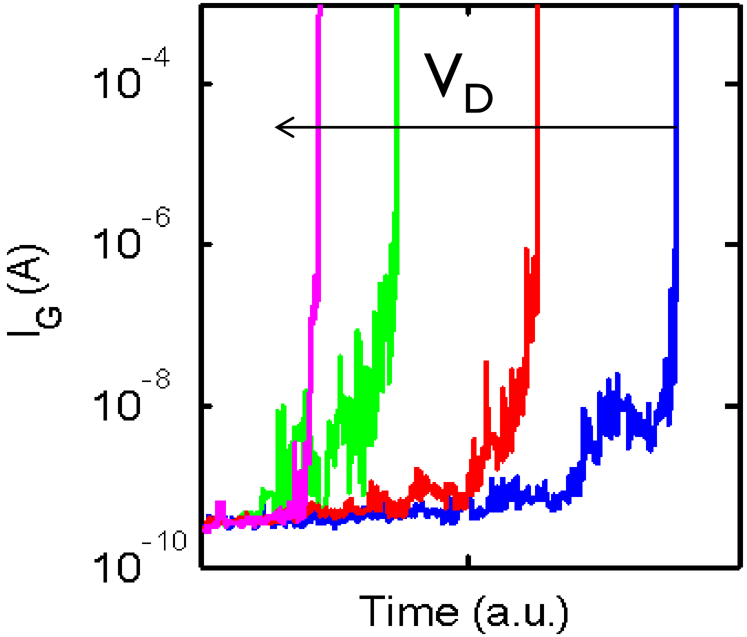
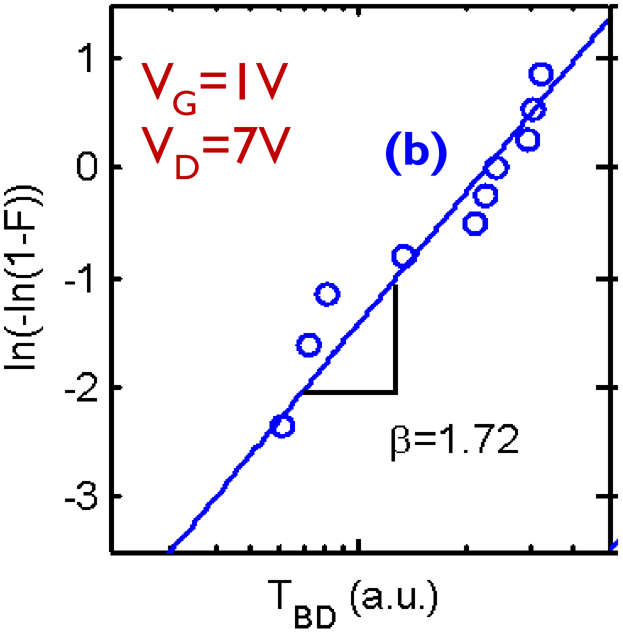
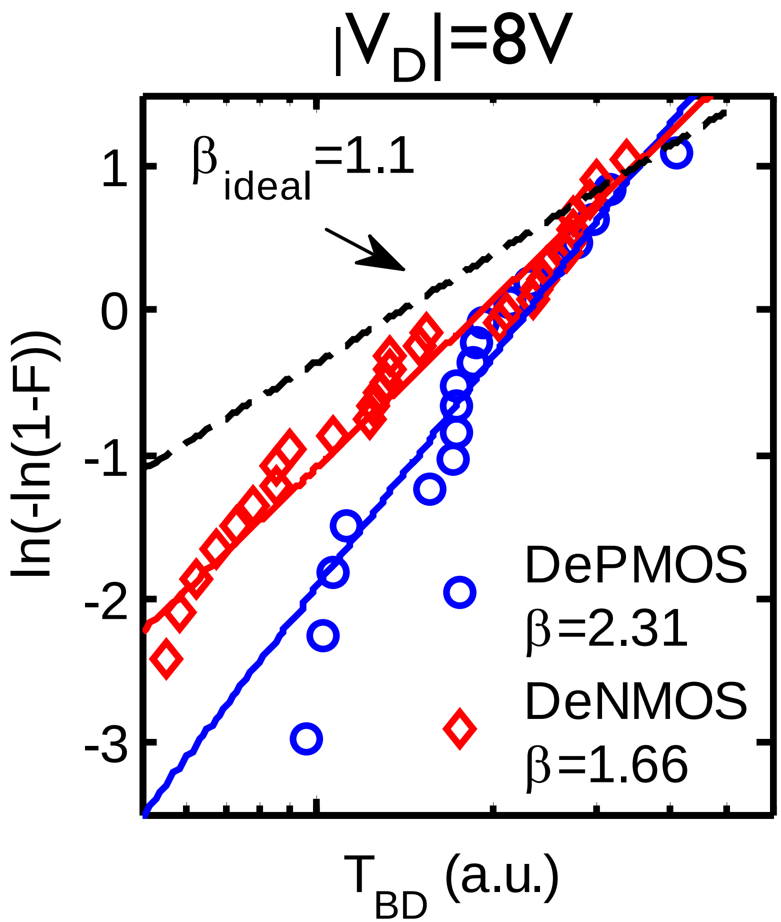
HCI leads to dielectric breakdown!







Weibull slopes for NMOS and PMOS



Classical theory suggests

$$\beta_{\text{ideal}} \equiv M \times \alpha \equiv \frac{x_{\text{o}}}{a_0}\alpha$$

$$\beta_{\text{PMOS}} > \beta_{\text{NMOS}} > \beta_{\text{ideal}}$$

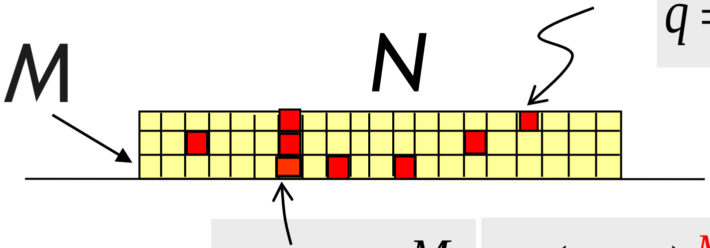
$$x_{o,PMOS} \quad vs. \quad x_{o,NMOS}$$

$$a_{0,PMOS} \quad vs. \quad a_{0,NMOS}$$

$$\alpha_{0,PMOS} \quad vs. \quad \alpha_{0,NMOS}$$

There is a problem here, a test for percolation theory !

Number Weibull vs. time Weibull



$$q = (t/t_0)^{\alpha}$$

$$p = q^{M} = (t/t_0)^{M\alpha} \equiv (t/t_0)^{\beta}$$

The number of boxes filled at failure vs. Time to failure

$$P_0 = (1-p)^N = (1 - Np/N)^N = \exp(-Np)$$

$$\frac{\beta_{\text{time}}}{\beta_{\text{Number}}} \equiv \frac{M\alpha}{M} = \alpha$$

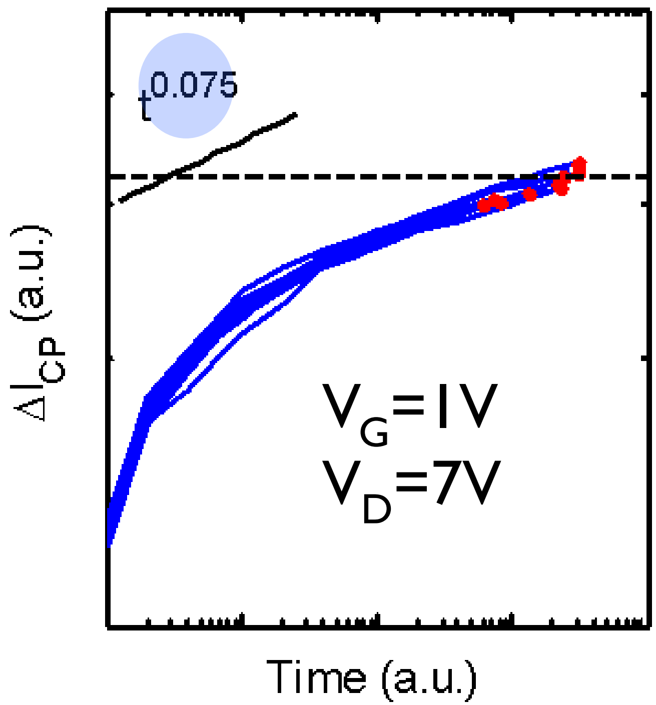
$$1 - F(p) = P_0 = \exp(-Np)$$

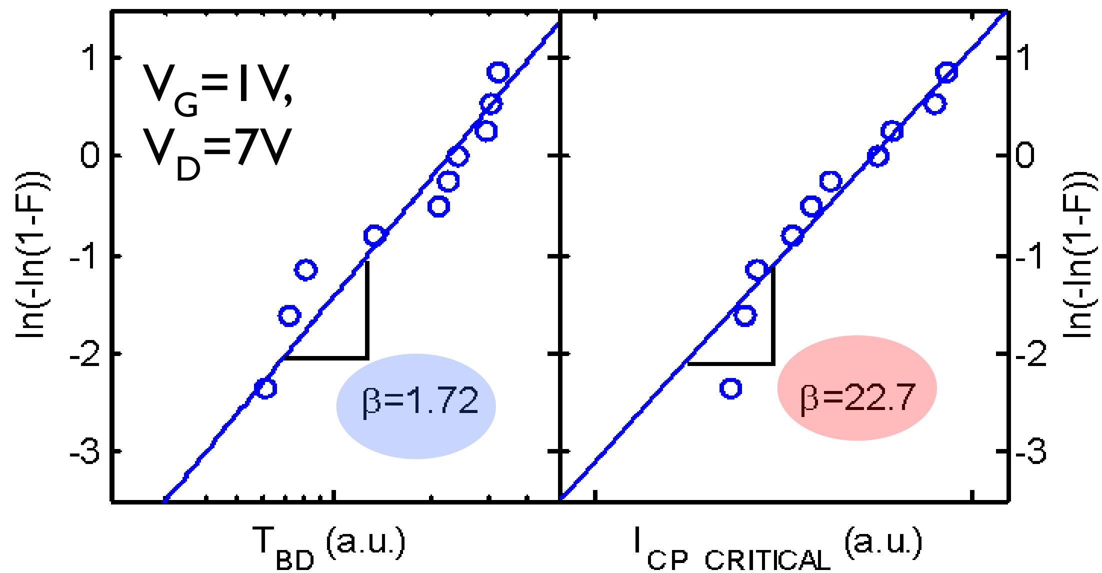
$$W_{\text{number}} \equiv \ln(-\ln(1-F)) = M \times \ln(q) + \ln(N)$$

$$W_{\text{Time}} \equiv \ln(-\ln(1-F)) = M\alpha \ \ln(t) - M\alpha \ \ln(t_0) + \ln(N)$$

Checking time exponent α (DeNMOS)

Use CP or SILC for Number Weibull, TDB for time-Weibull



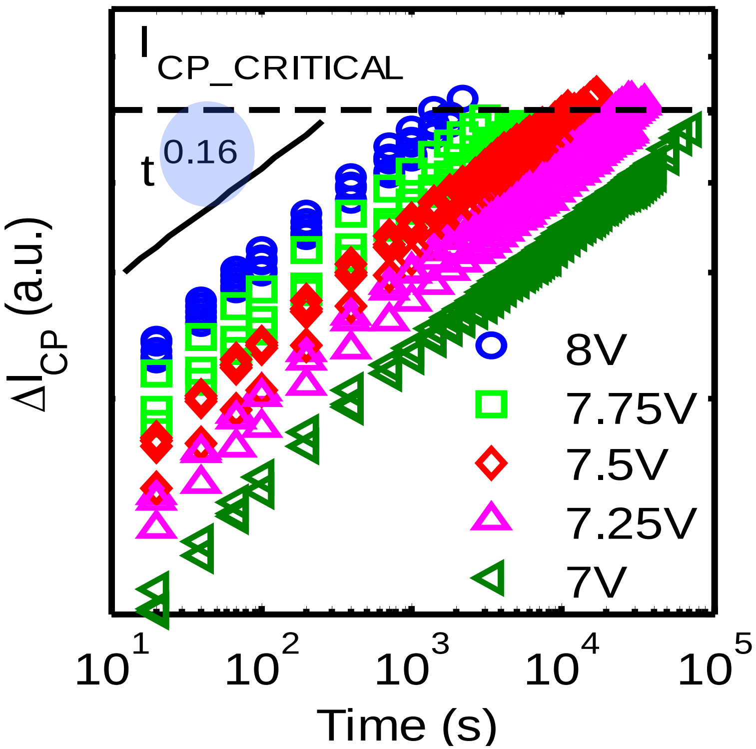


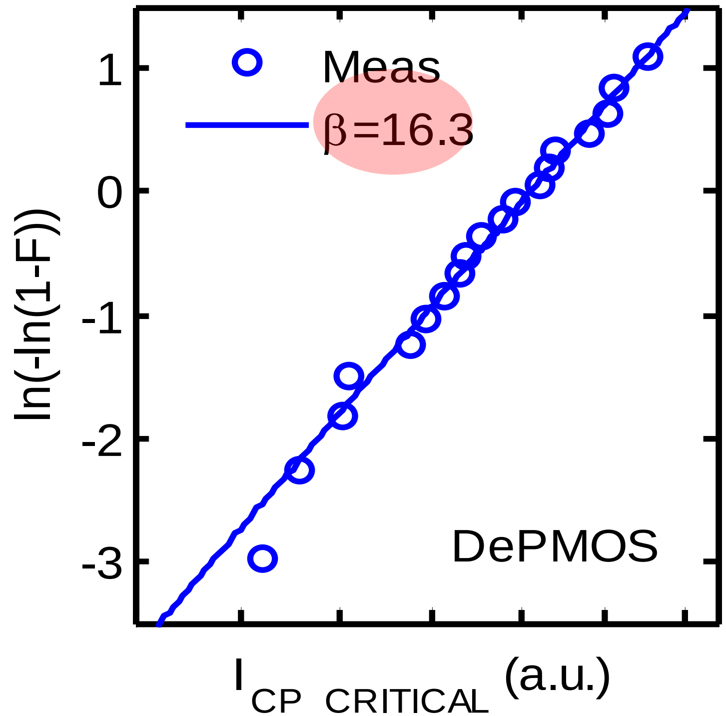
$$\frac{\beta_T}{\beta_N} \equiv \frac{M\alpha}{M} = \alpha$$

Proportional to N_{BD}

Verified, nothing wrong with exponent!

Checking power exponent α (DePMOS)

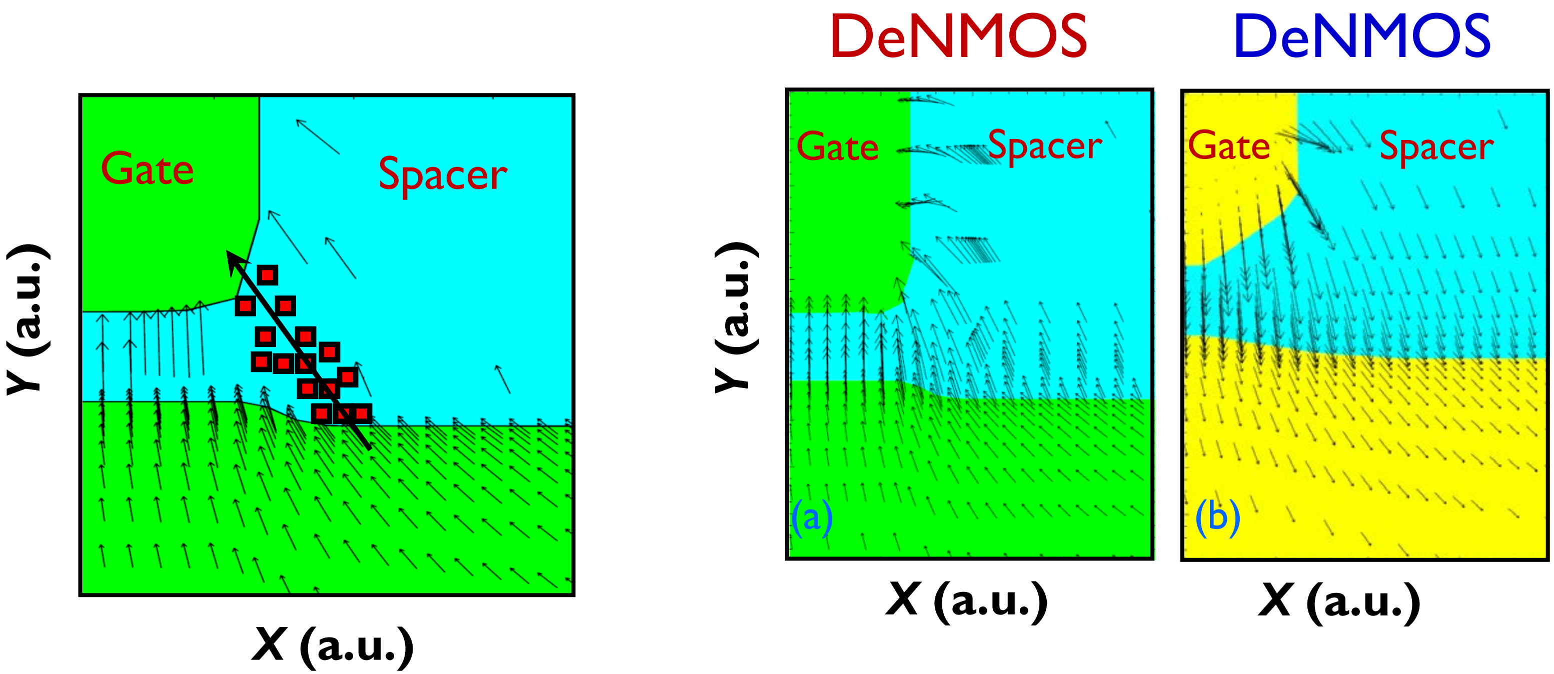




$$\frac{\beta_T}{\beta_N} \equiv \frac{M\alpha}{M} = \alpha$$

Again, nothing wrong with exponent!

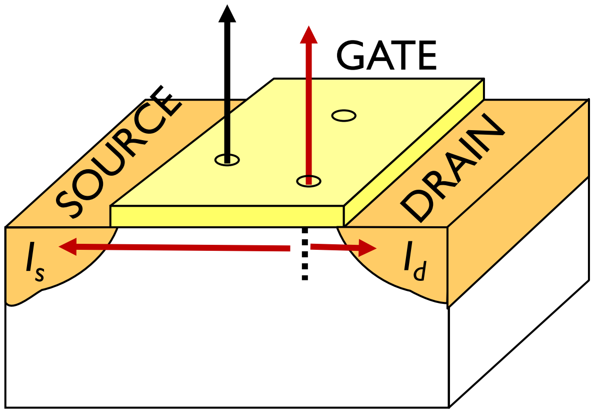
Hypothesis: Perhaps x_o is not the same!

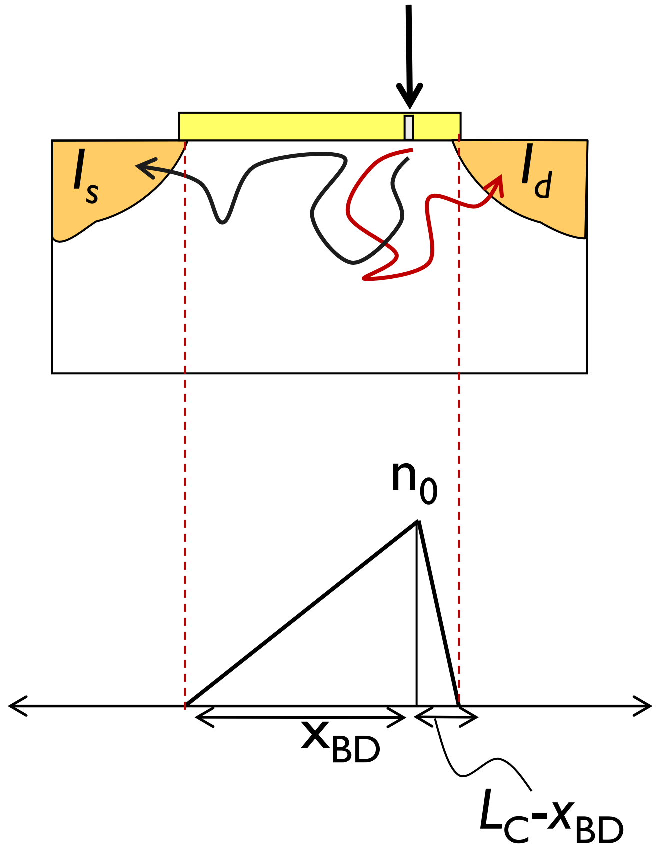


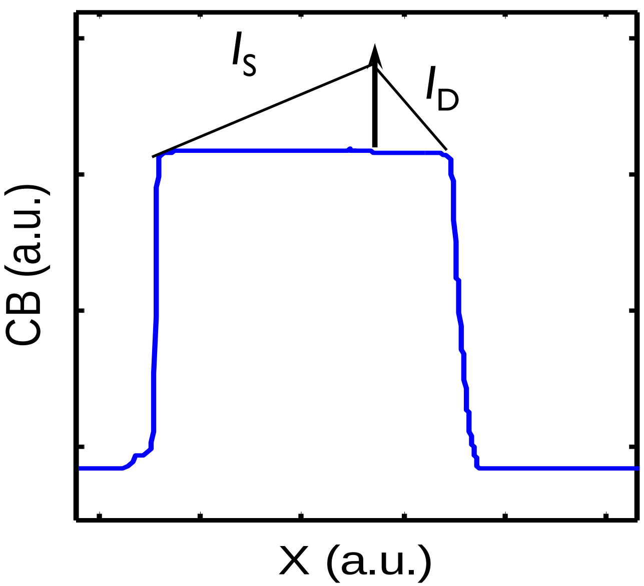
Perhaps the breakdown paths are larger than oxide thickness

Perhaps the path-lengths of NMOS and PMOS are different

Recall: Current ratio technique







So long BD-spot not too close to Source/drain

$$J = D\frac{dn}{dx} + n\mu \quad \text{(X)}$$

$$\nabla \bullet J = 0$$

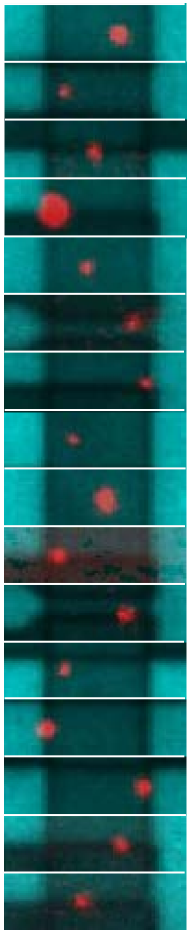
$$D\frac{d^2 n}{dx^2} = 0$$

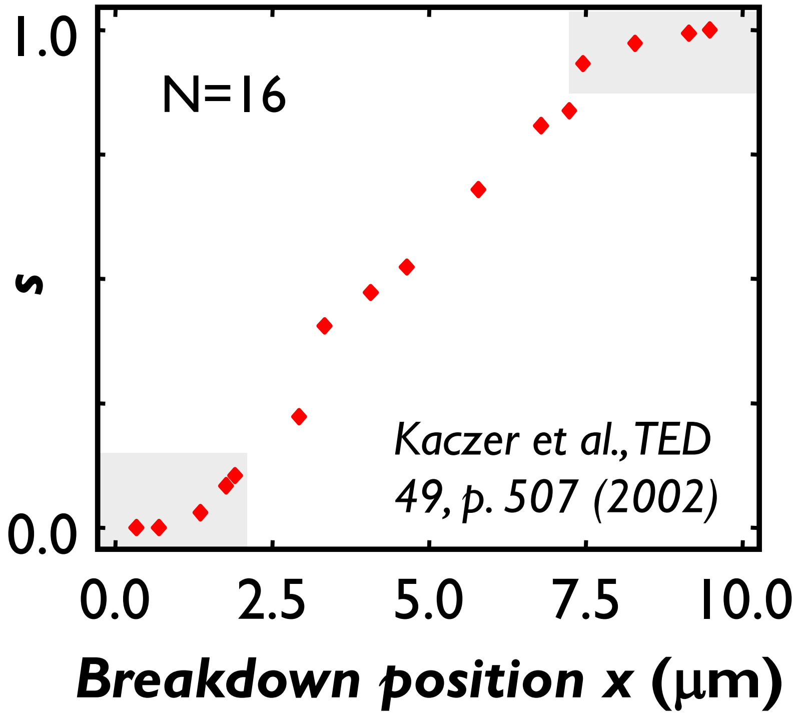
$$n = Ax + B$$

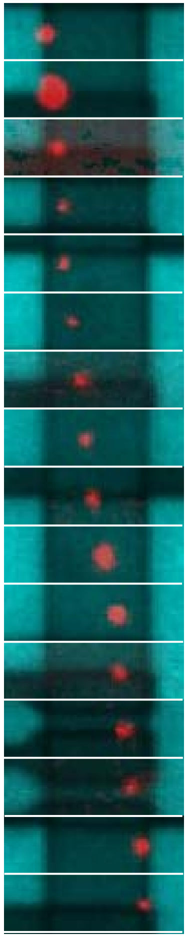
$$J_s = D\frac{n_{perc}}{x_{perc}}$$

$$\frac{J_d}{J_s + J_d} = \frac{x_{perc}}{L_{gate}}$$

Locations close to S/D are challenging

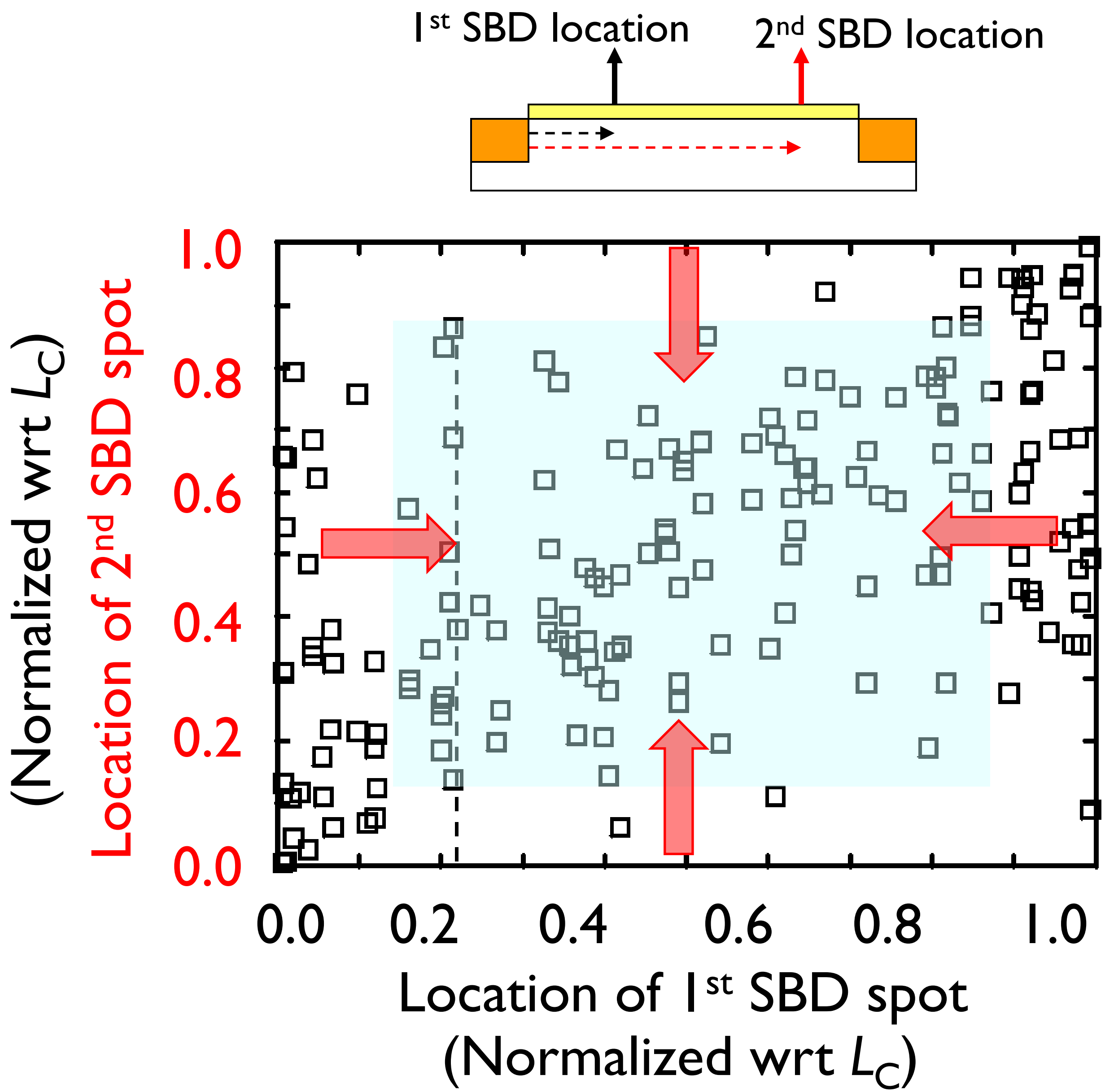




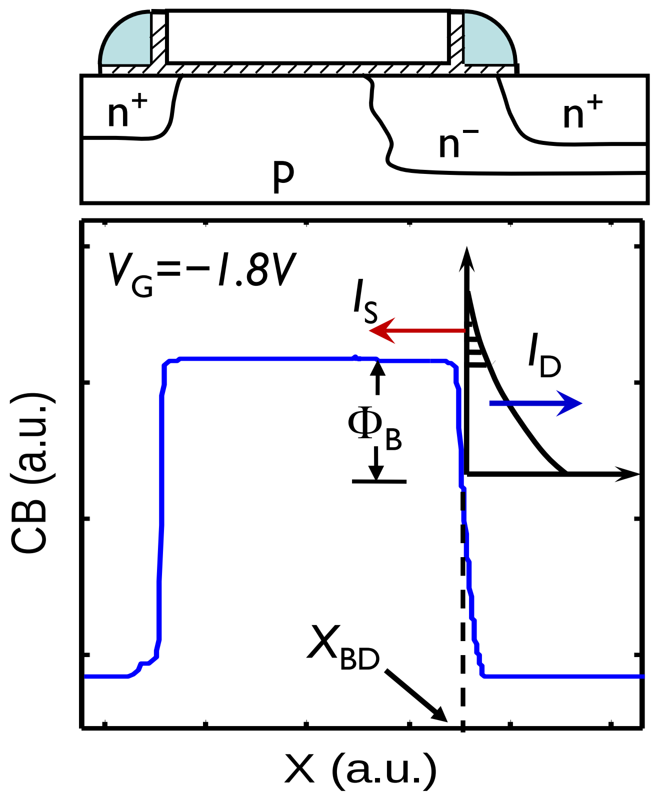


Emission microscopy on *L*=10 μm nFETs confirms the BD position determination method.

Rational for S/D region exclusion



Determination of breakdown spot for a nonuniform potential profile



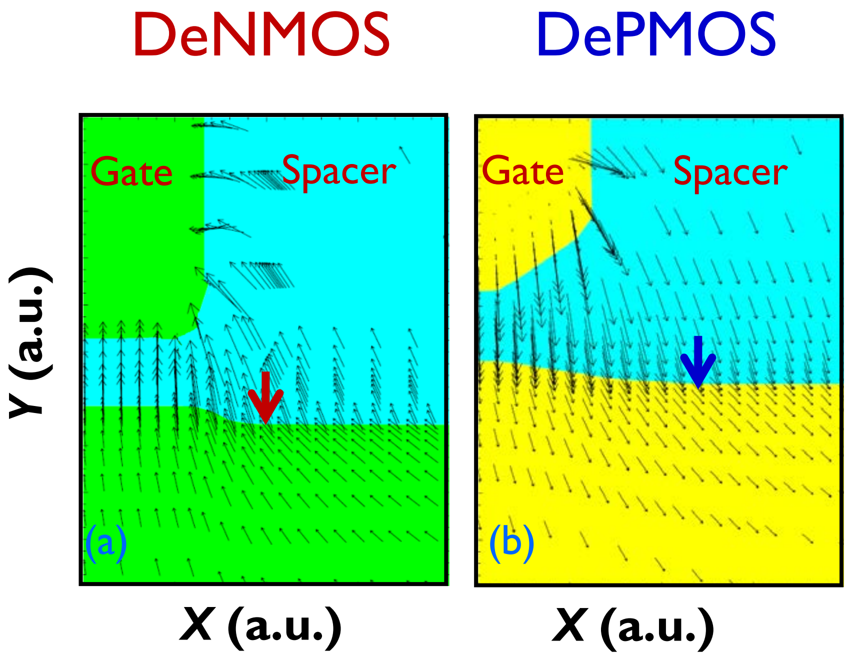
$$I_S = qAD \times \left(n(x) \times e^{-\Phi_B(x)/k_B T} \right) / L_C$$

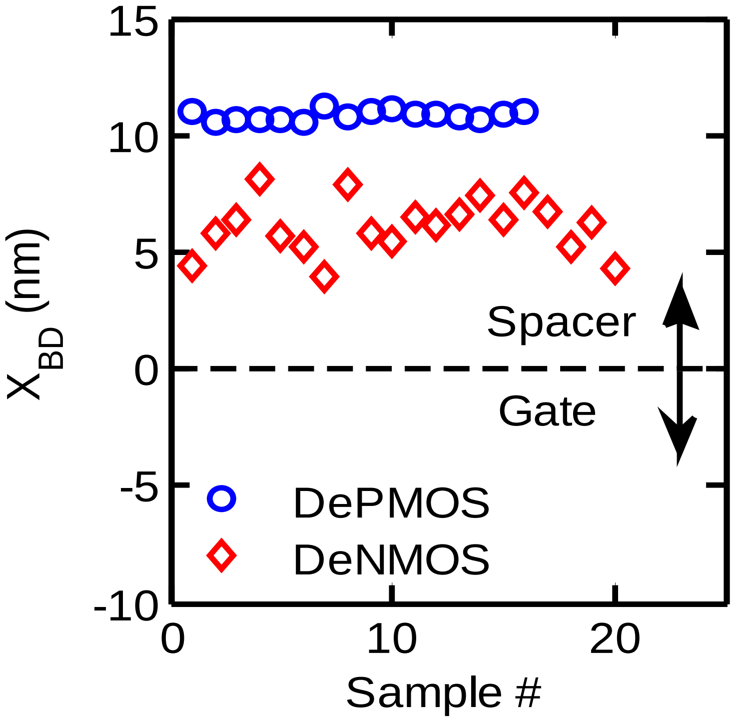
$$I_D = qA \times n(x) \times \upsilon_T$$

$$\frac{I_S}{I_S + I_D} \approx \frac{I_S}{I_D} = \frac{D}{\upsilon_T L_C} e^{-\Phi_B(x)/k_B T}$$

Experiment (LHS) and simulation (RHS) locates BD spot

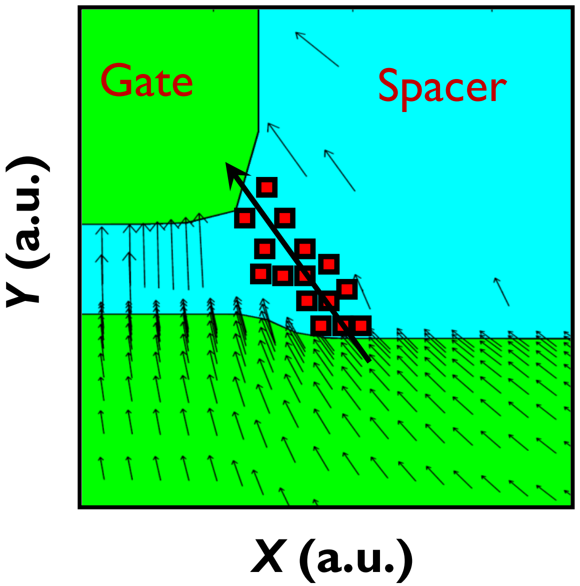
Position determination in non-uniform field



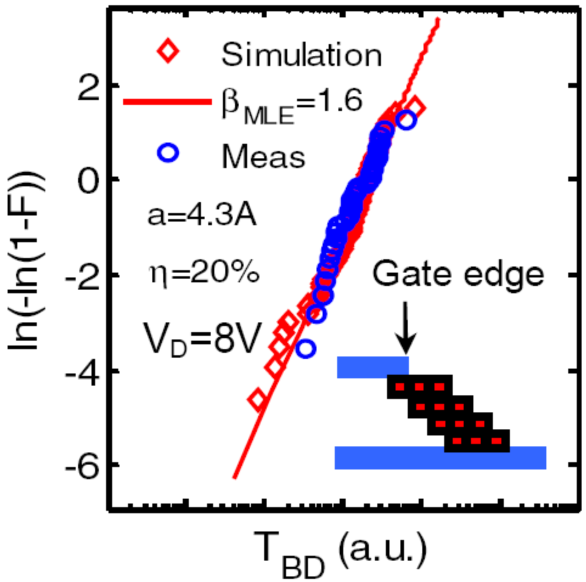


Breakdown occurred in DePMOS slightly further down in the channel compared to DeNMOS

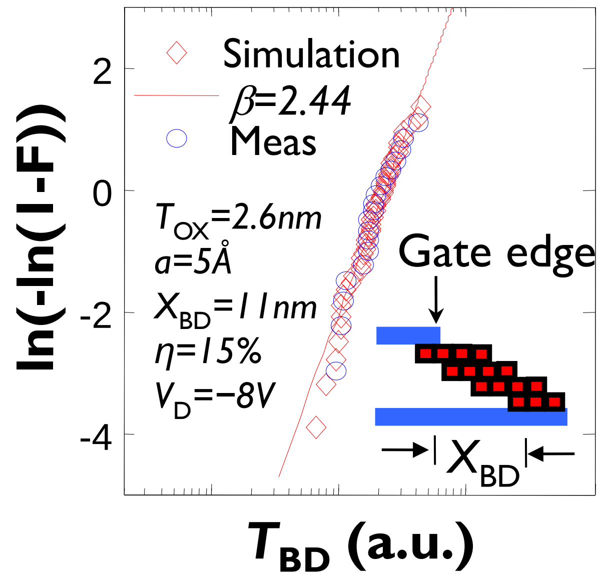
Correlated percolation and TDDB



DeNMOS



DePMOS



$T_{ox,PMOS} > T_{ox,NMOS}$! $a_{0,PMOS} = a_{0,NMOS}$ (same defect-size)

Same parameter set explains both set of data

Conclusions

- Off state HCI degradation appears to be a general phenomena for wide variety of high voltage transistors, including LDMOS, DeNMOS, DePMOS, etc.
- The degradation process follows the same universal relationship as has been discussed for classical ON-state degradation.
- The remarkable fact is the off-state HCI often leads to TDDB which gives rise to many puzzling features.
- Appropriate use of BD position and non-uniform percolation resolves the puzzles about Weibull slopes and power-exponents and in the process establishes percolation theory on solid footing.

Self-Test Questions

1. In PMOS transistors ,which carriers is responsible for off-state HCI?
2. What is the distinction between number-Weibull and time-Weibull?
3. Which measurement is used to determine Number-Weibull? Name another technique that could do the same.
4. What is 'area-scaling'? Will area-scaling hold for off-state BD?
5. What conditions – in general – must be satisfied for area scaling?
6. How did the gate electric field profile influence percolation simulation?
7. For universal curve, is the value of power exponent a fixed number? If not, what exponent should we choose and why?