



# **ECE695: Reliability Physics of Nano-Transistors**

## **Lecture 39: Radiation and Devices – Part 1**

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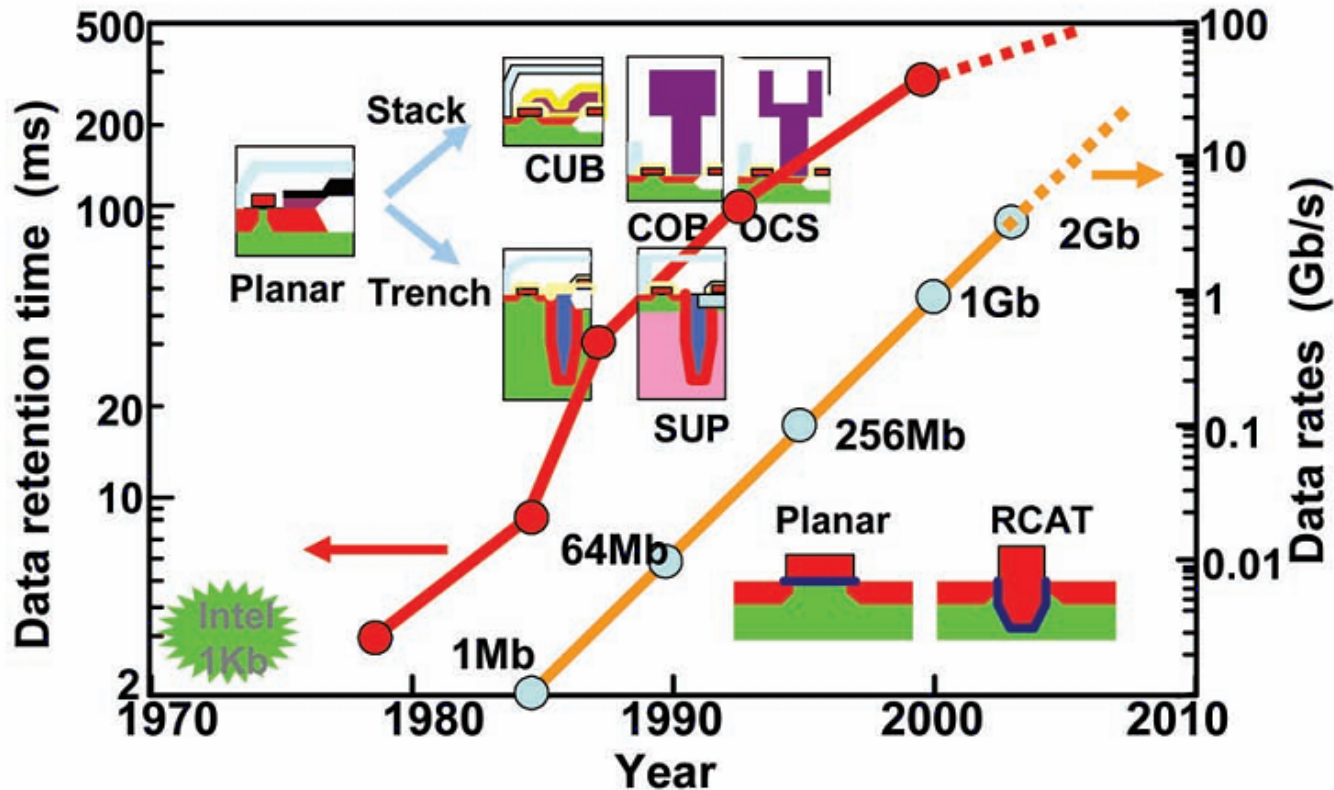
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# Outline

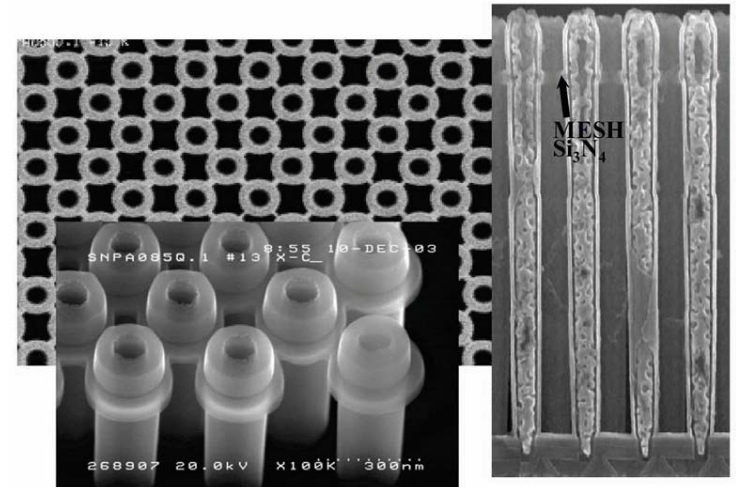
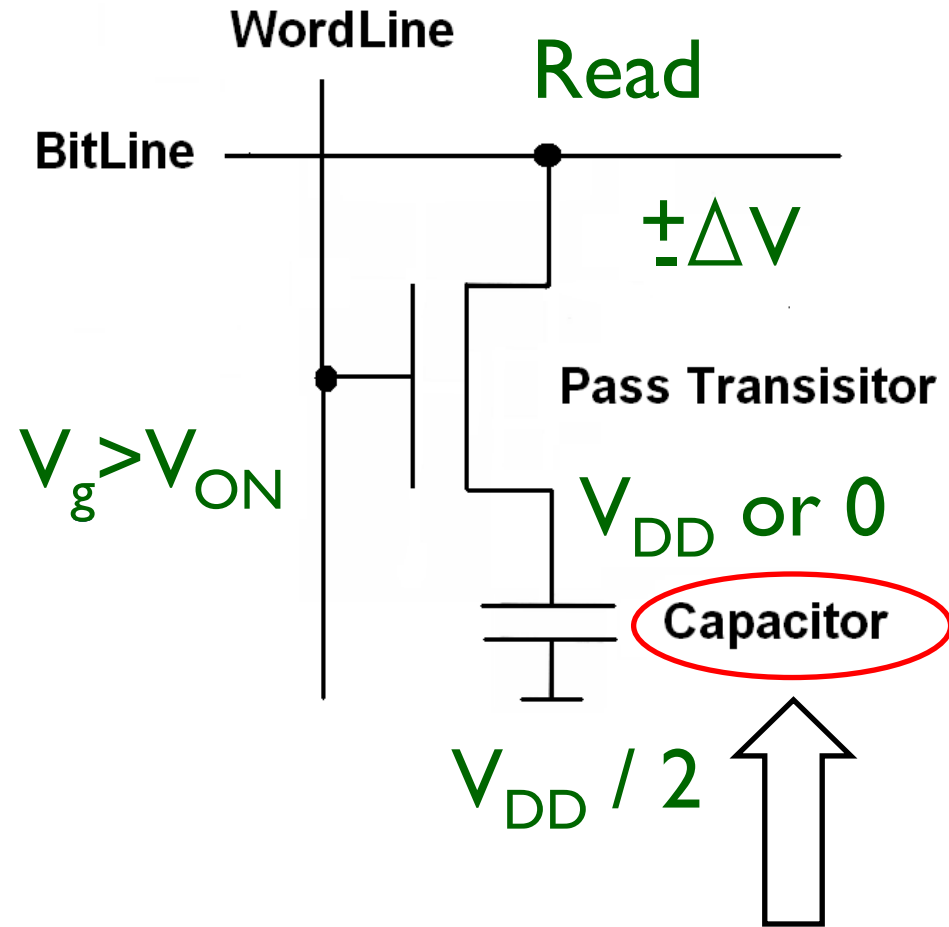
1. Introduction to ZRAM
2. Soft Errors in Zero-capacitor RAM
3. Soft Errors in in Flash memories
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# Evolution Trend for DRAM



Significant challenges lie ahead in the processing of DRAM cells to continue the trends down the road  
[Fabtech, 2006]

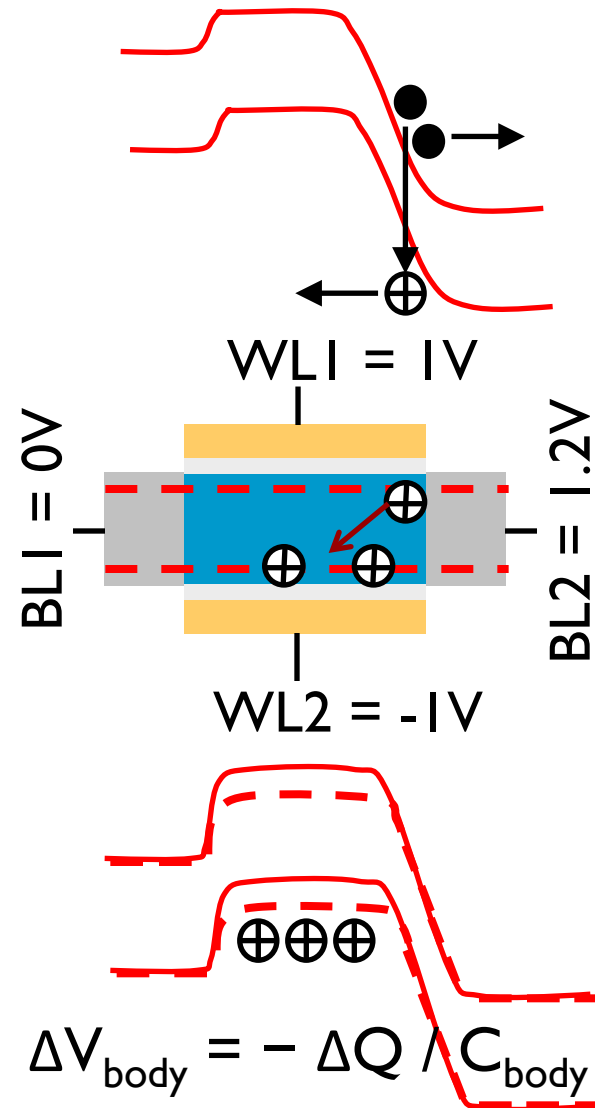
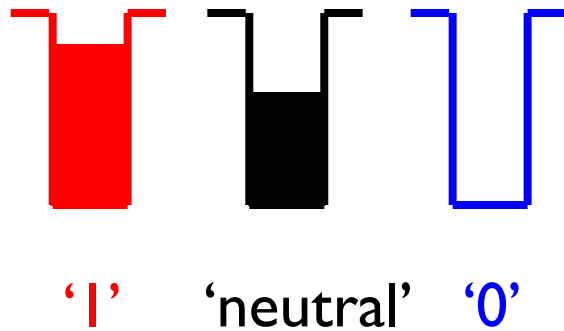
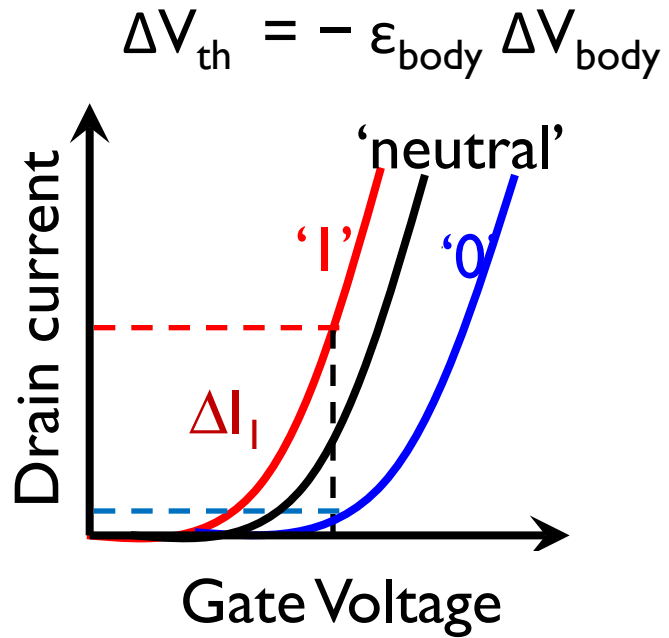
# 1 Transistor-1 Capacitor (1T-1C) Cell



Kim et al, IEDM 2004

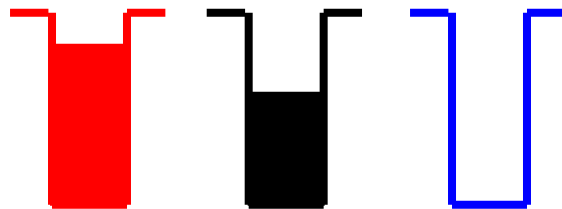
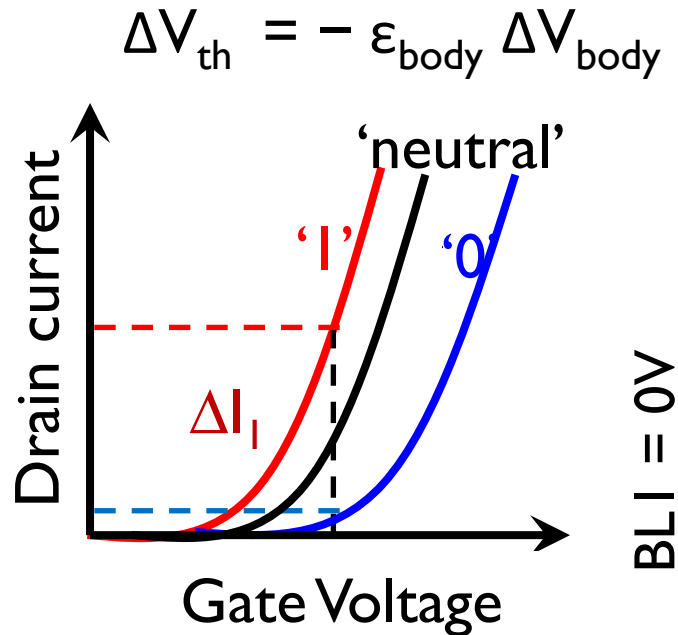
*Scaling Bottleneck !*

# Z-RAM Operations (Writing '1')

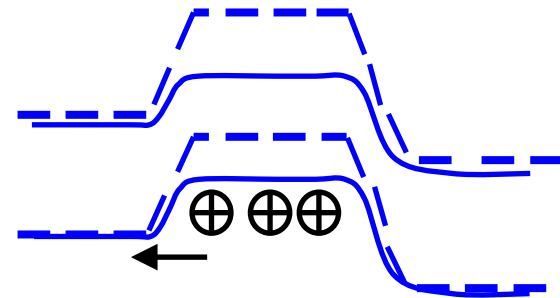
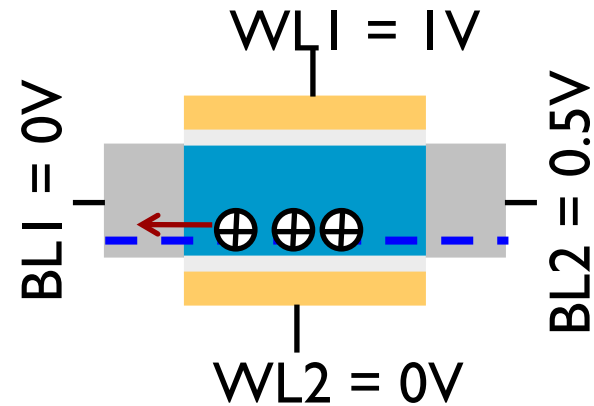


**Excess** holes in body defines '1' Alam ECE-695

# Z-RAM Operations (Writing '0')

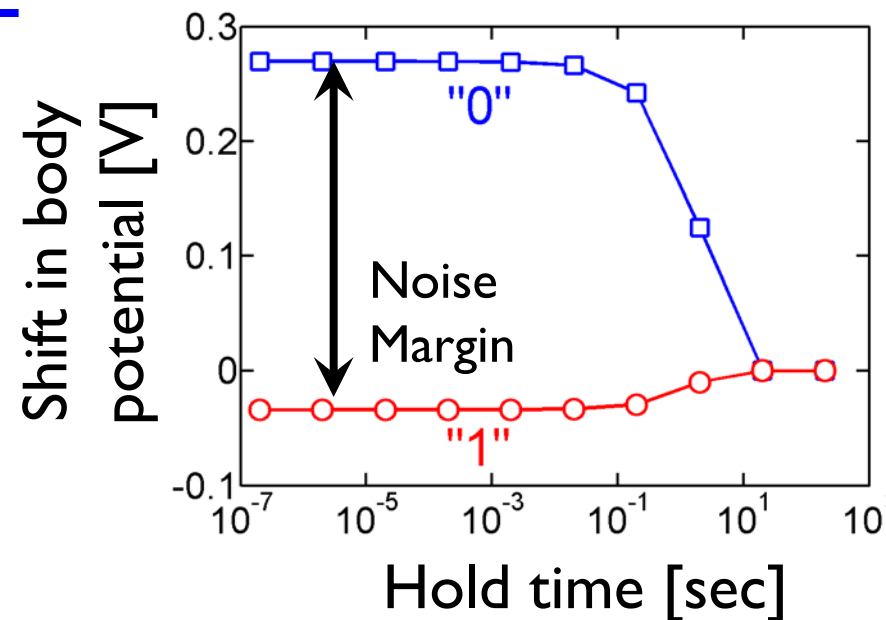
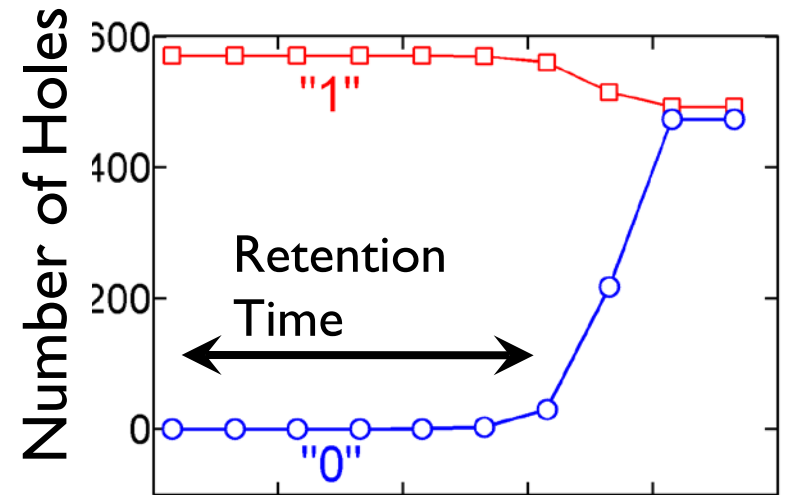
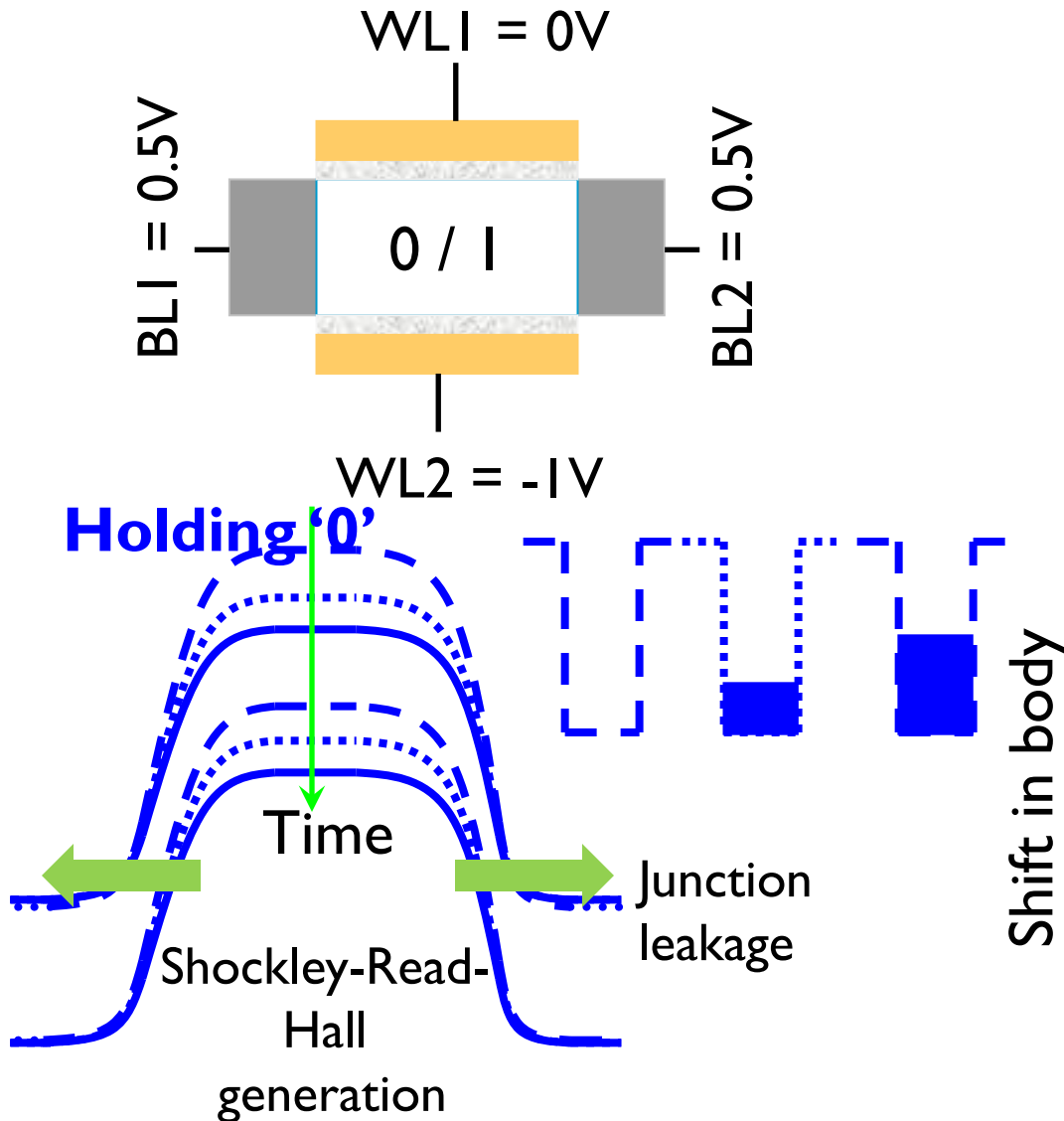


'1' 'neutral' '0'



Shortage of holes in body defines state '0'

# ZRAM performance Metrics



Noise margin is dominated by state '0' in thin body Z-RAM

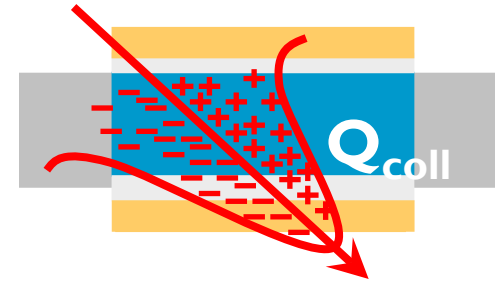
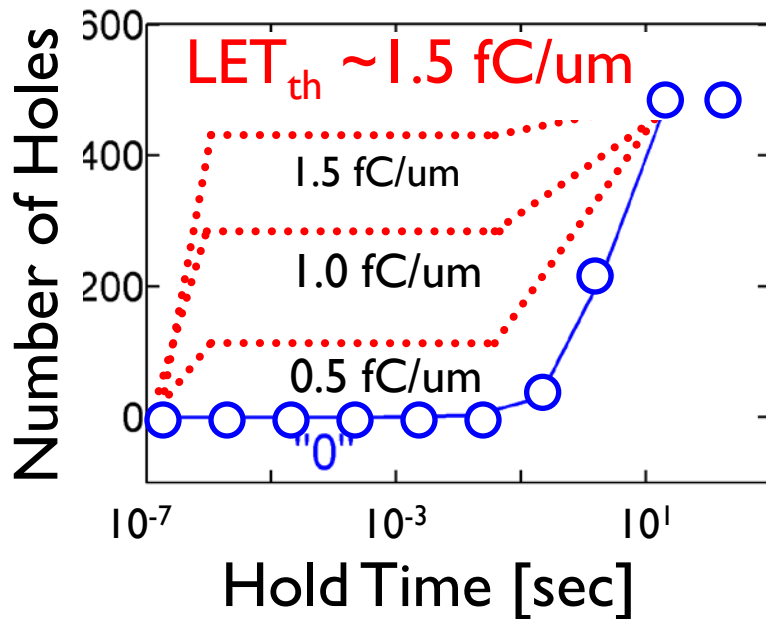


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# Single event upset in Z-RAM

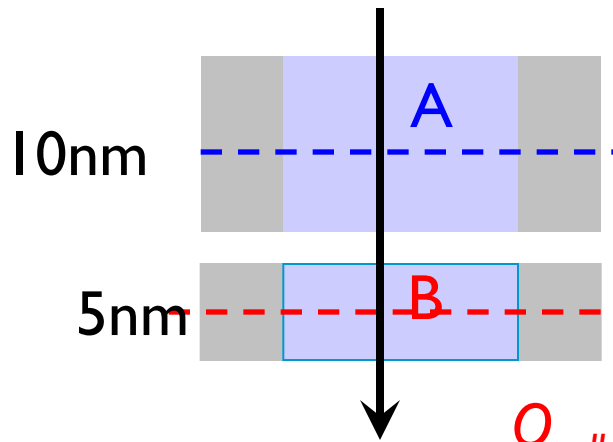
Retention after WRITE 0



$$Q_{stored} = \Delta Q = Q_{steady\ state}$$

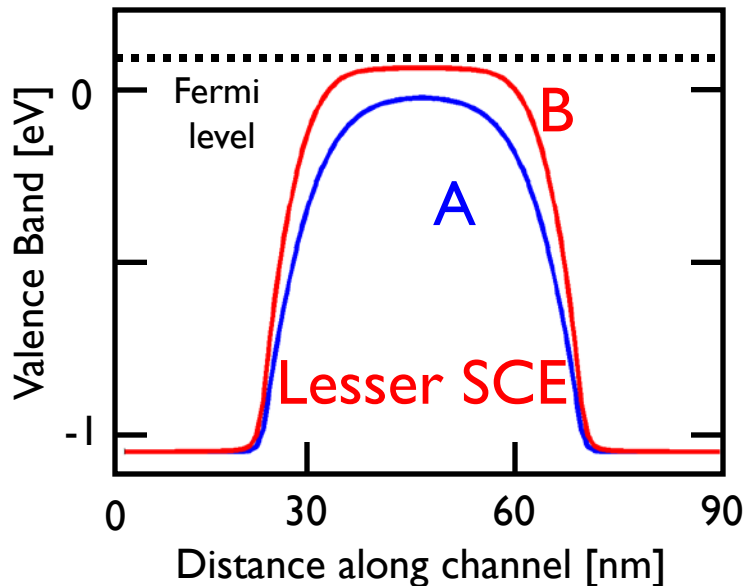
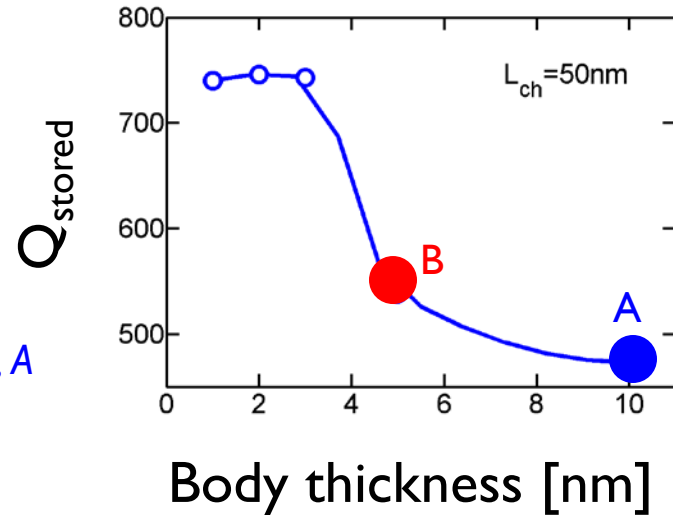
To improve  $LET_{th}$  :  $Q_{stored}$   $\uparrow$  and  $Q_{coll}$   $\downarrow$

# Mitigating soft errors with $t_{\text{body}}$ scaling



$$Q_{\text{coll}, B} = 0.5 \times Q_{\text{coll}, A}$$

$$Q_{\text{stored}, B}, Q_{\text{stored}, A} ?$$



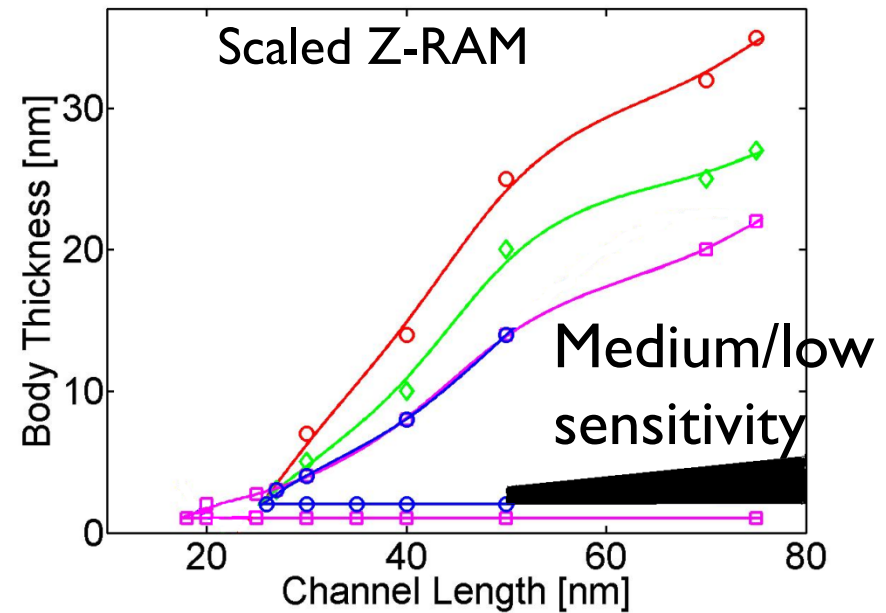
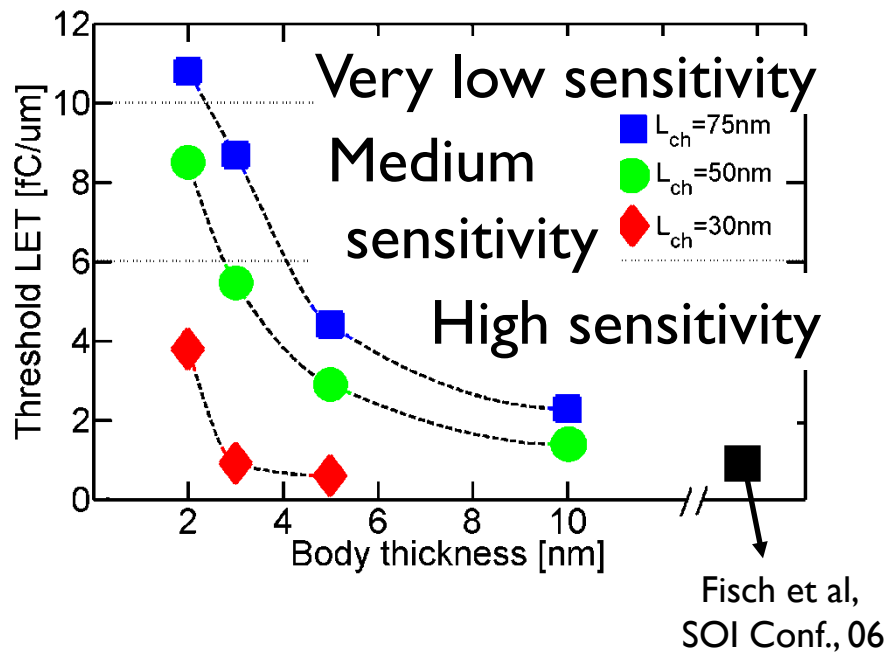
Thinner body:

- Lesser  $Q_{\text{coll}}$
- Greater  $Q_{\text{storage}}$

$$\text{LET}_{\text{th}} B > \text{LET}_{\text{th}} A$$

# Mitigating soft errors with $t_{\text{body}}$ Scaling

Assuming  $\alpha$  particle LET 6 – 10 fC/ $\mu\text{m}$



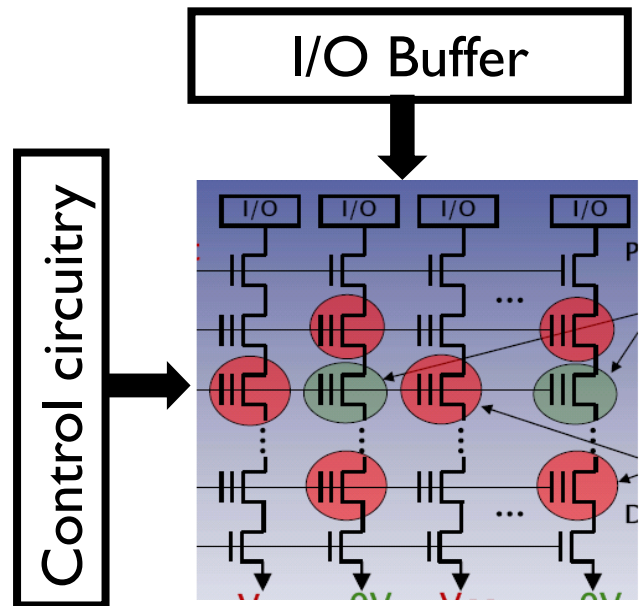
$L_{\text{ch}} > 50\text{nm}$ ,  $t_{\text{body}} < 5\text{nm}$  needed for low/medium sensitivity to  $\alpha$  particles

Butt et al, *IEEE Transaction of Nuclear Science*, 2007

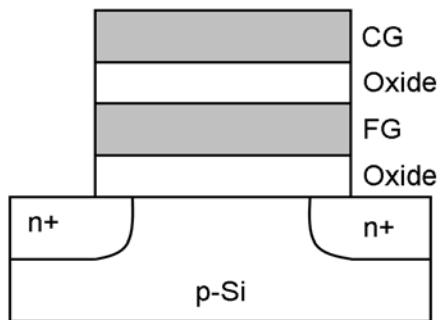
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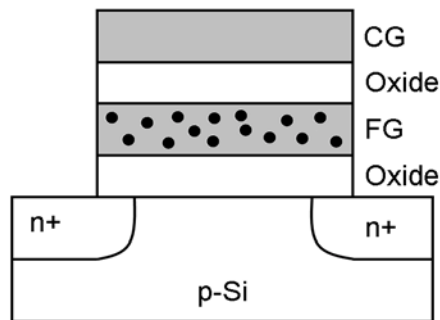
# Flash memories



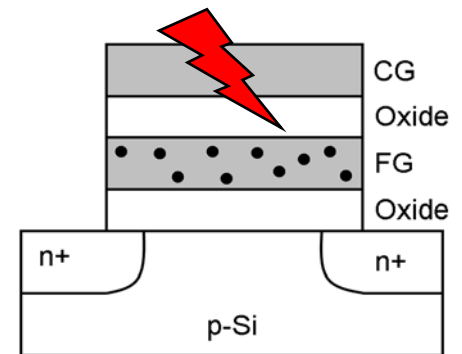
$$\Delta V_{th} = \frac{\Delta Q_{FG}}{C_{FG}}$$



Erased cell



Programmed cell



Disturbed cell

# Experimental Setup

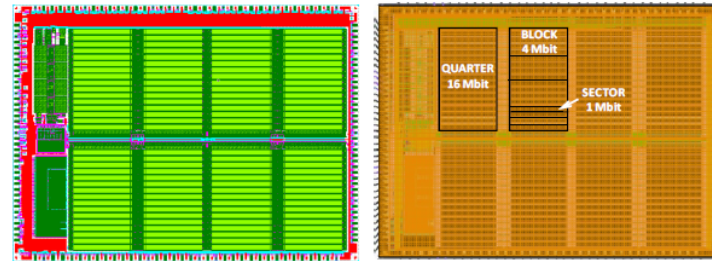
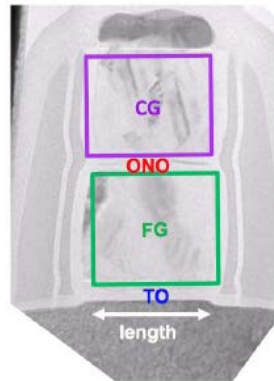


Figure 1. Layout (left) and die (right) of the ANNA test chip (area  $9.230 \times 7.044 \text{ mm}^2$ ) fabricated by STMicroelectronics in CMOS 90 nm technology. The memory array is segmented into 32 blocks of 4 Mbits or 128 sectors of 1 Mbits (total capacity of 128 Mbits per chip).

G. Just,  
IRPS, 2013.

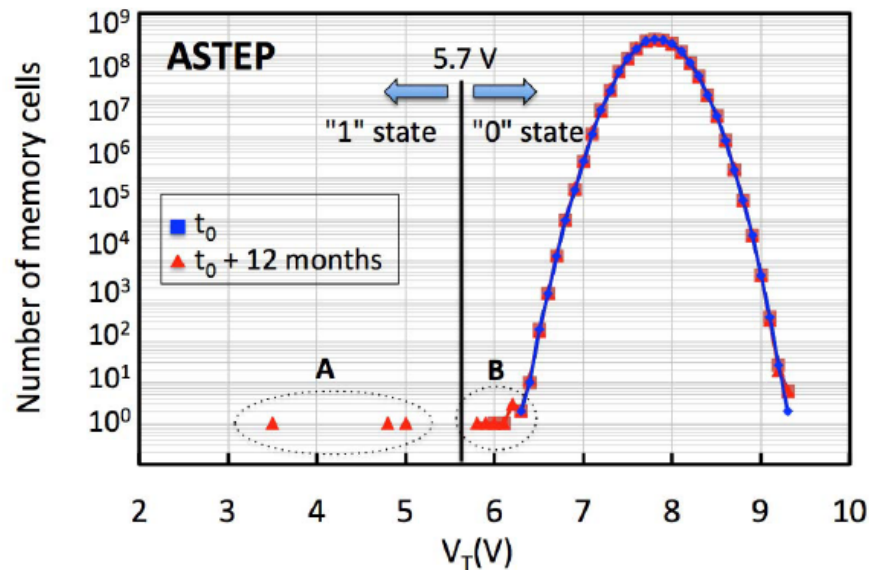


Figure 7. Comparison between the two distributions of  $V_T$  values measured at  $t_0$  and at  $t_0 + 12$  months for population of programmed memory cells exposed to natural radiation on the ASTEP platform.

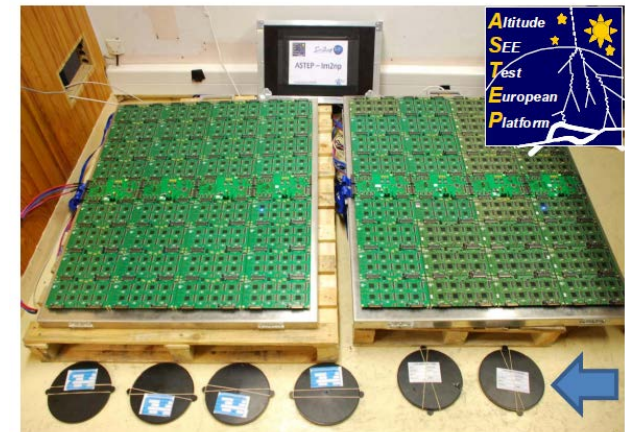
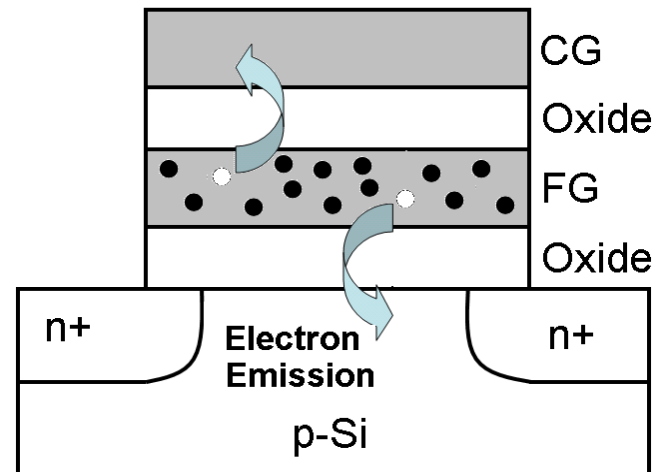
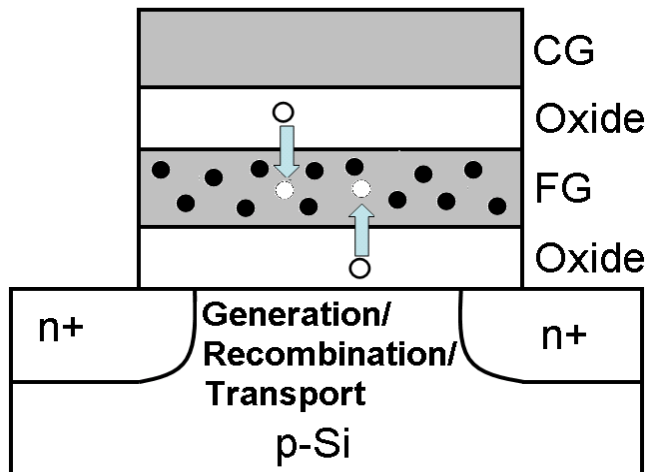
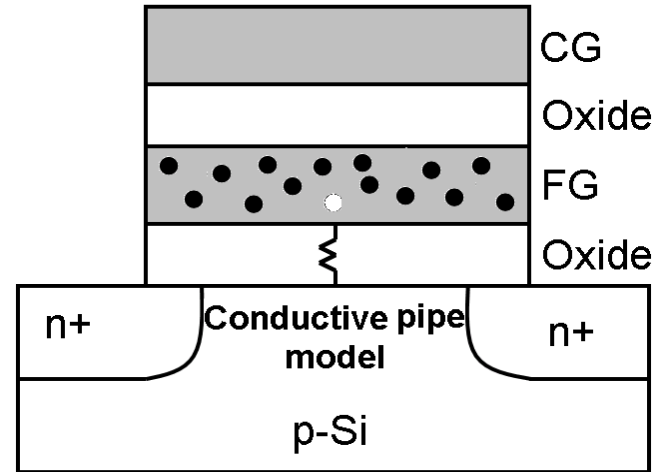
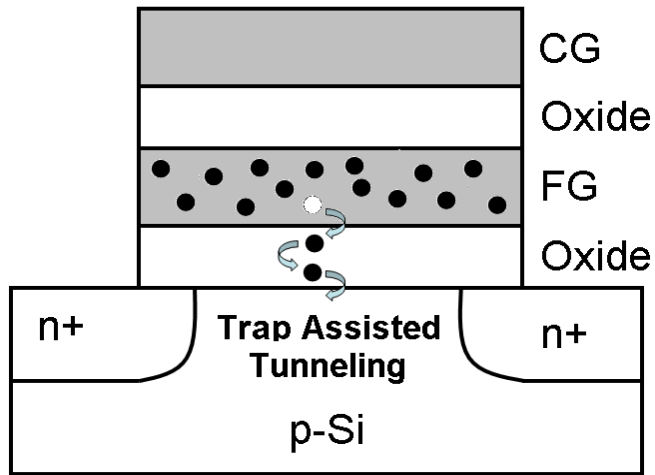


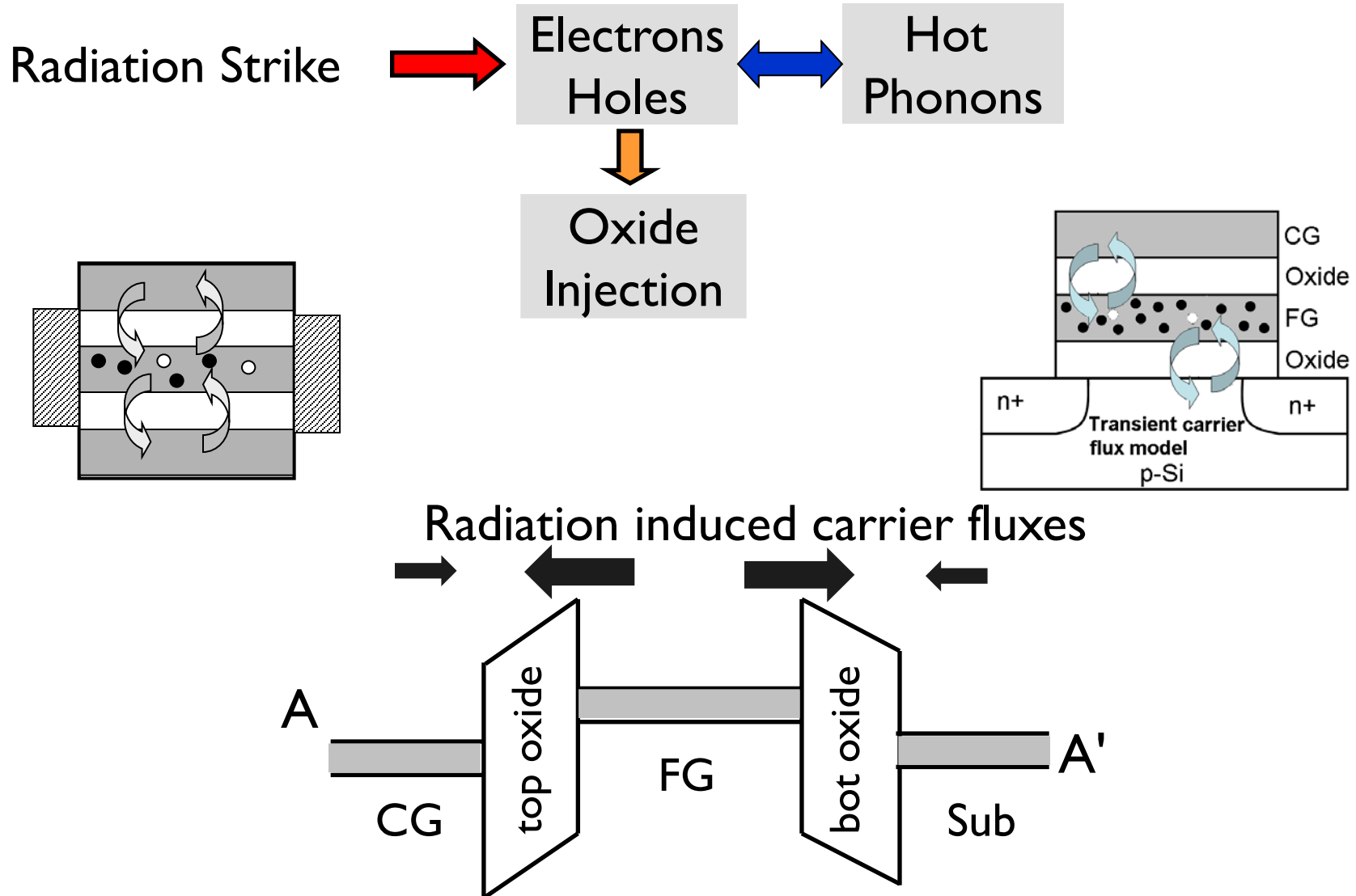
Figure 5. Global view of one of the ASTEP experimental room showing, in the foreground, six wafers of flash memories stored on the ground during their exposition to natural radiation on the ASTEP platform and, in the background, a real-time test setup based on 40nm SRAM circuits [9].

# Possible charge loss mechanisms



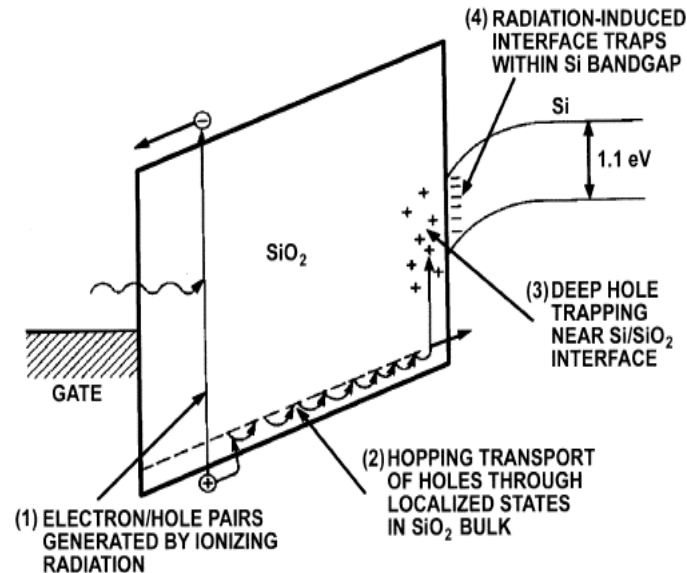


# Charge loss and single event upset

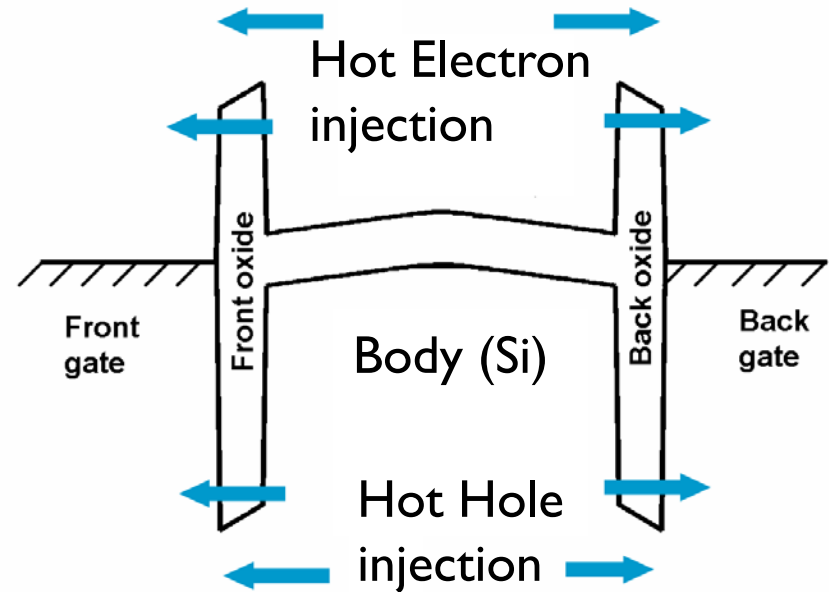


programmed cell  
Alam ECE-695

# Older vs. newer technologies



$t_{\text{ox}} \sim 100\text{nm}$

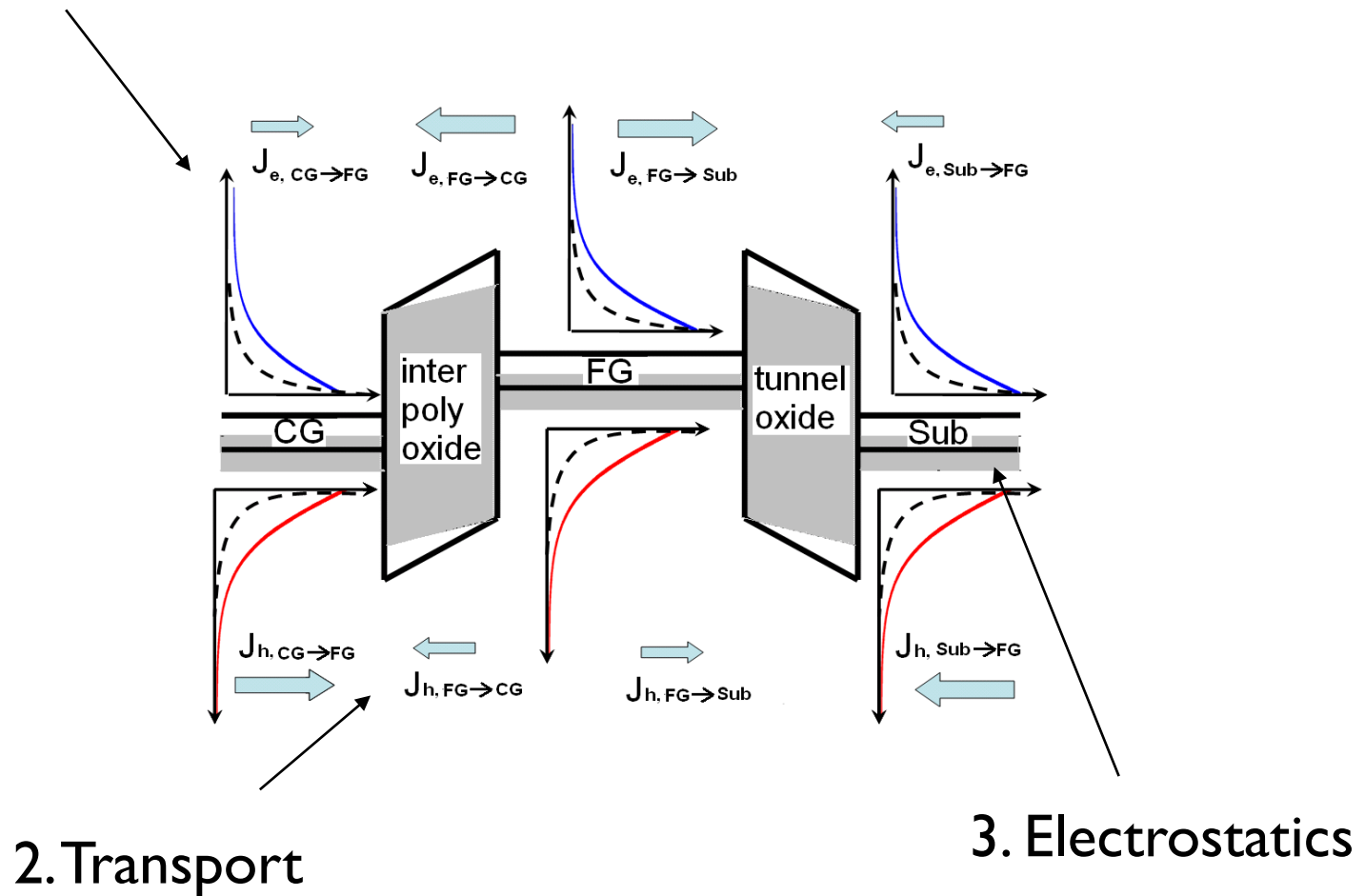


$t_{\text{ox}} = 1 - 10\text{nm}$

Hot carrier injection from silicon into oxide may be responsible for TID in ultrathin oxides

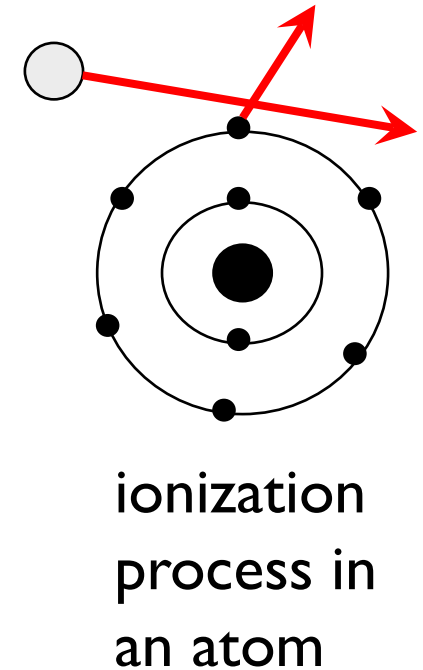
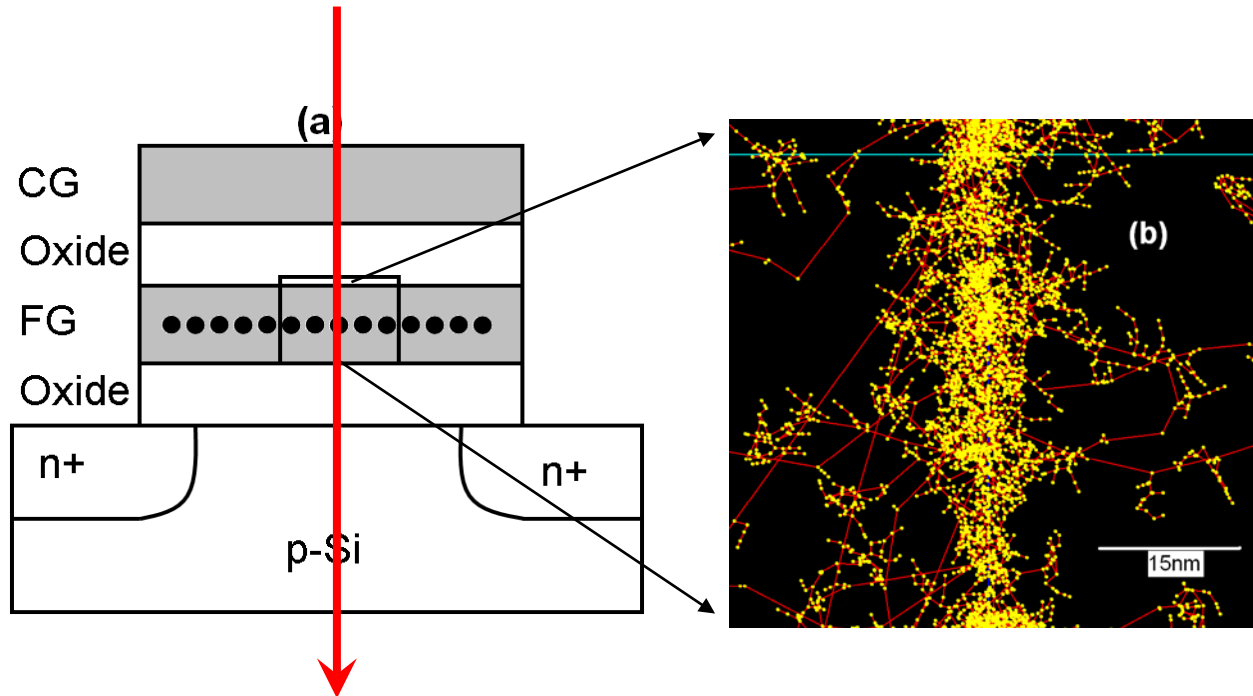
# Transient simulation approach

I. Energy Dynamics (Geant4 > 10eV, Monte-Carlo < 10eV)



# 1. Energy dynamics: Ionization and initial relaxation (10eV – keVs)

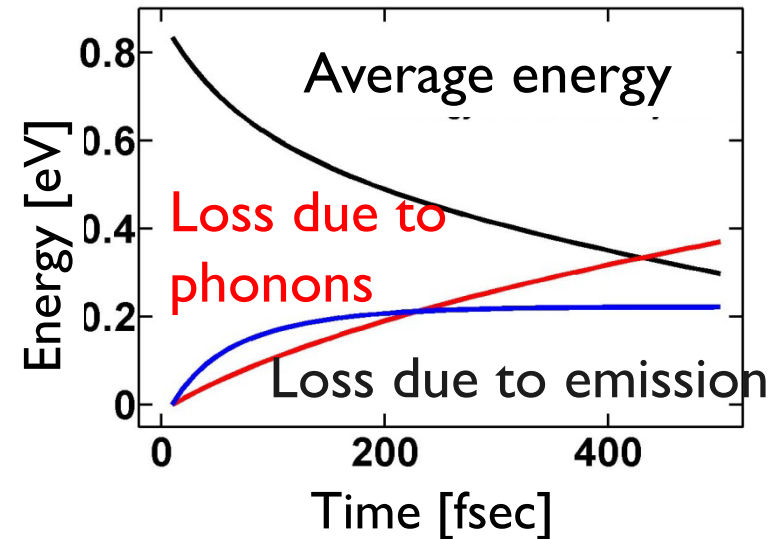
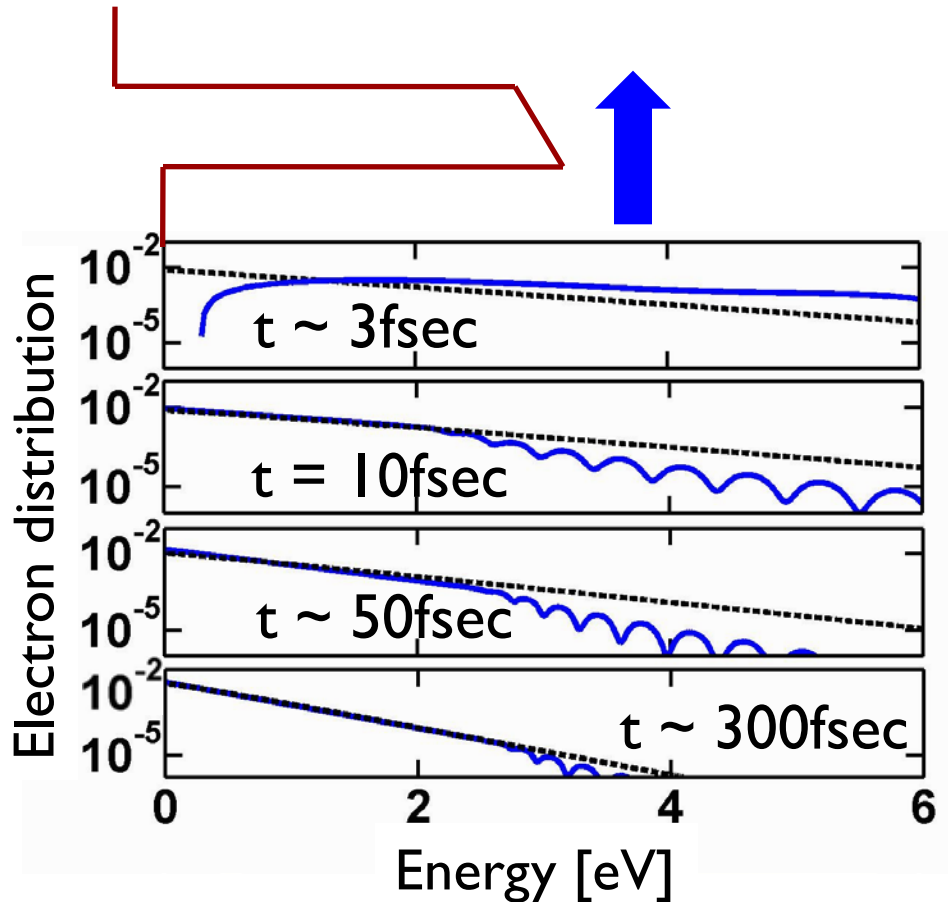
177 MeV Cl ion through FG cell



Geant4 – high energy particle physics based toolkit

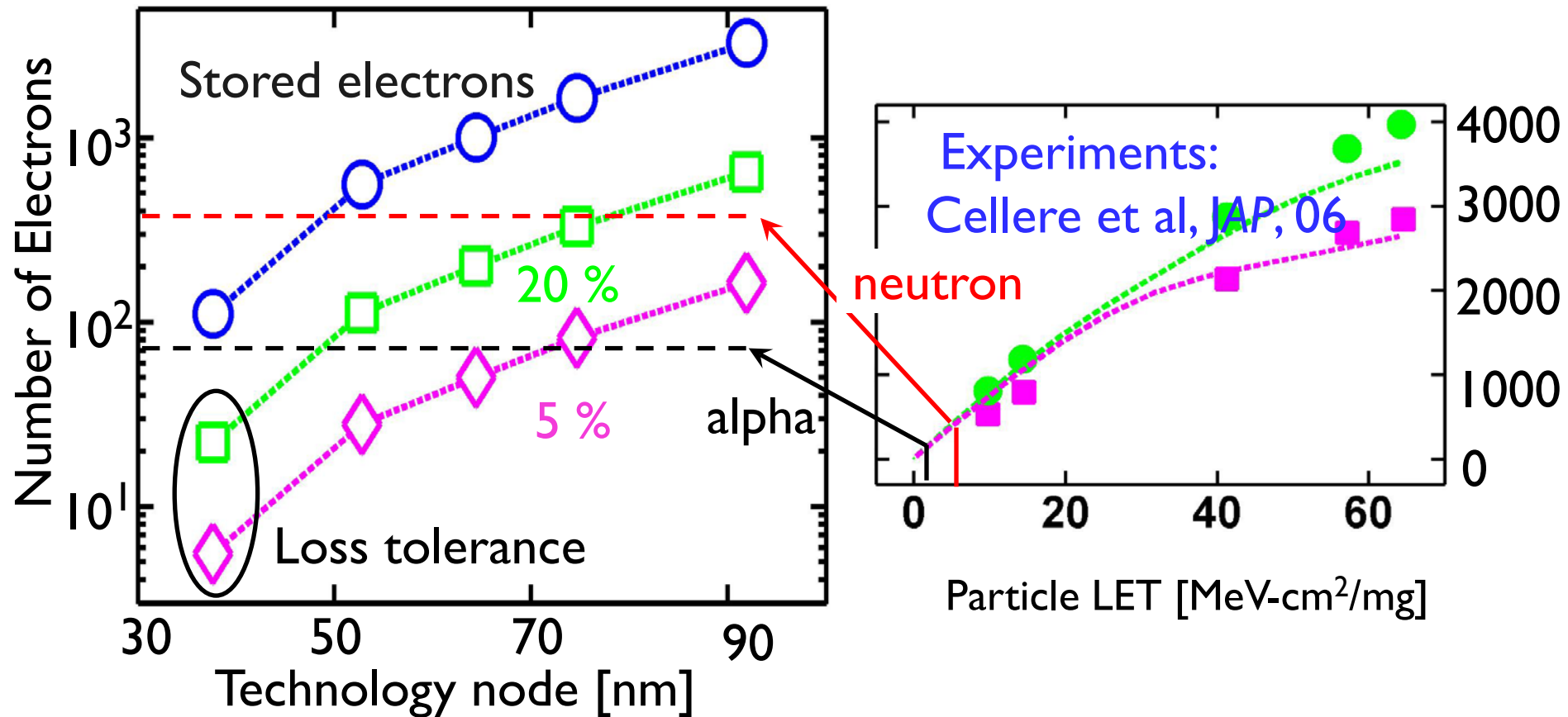
Used for the ionization and energy relaxation ( $\sim 10\text{eV} - \text{keVs}$ )

# Energy dynamics ( $E < 10$ eV, $t > 3$ fsec)



Energy relaxation due to phonon scattering and carriers' emission over oxide

# Sensitivity of FG cell generations



Butt et al, International Reliability Physics Symposium, 2008

# Simulation of cell response

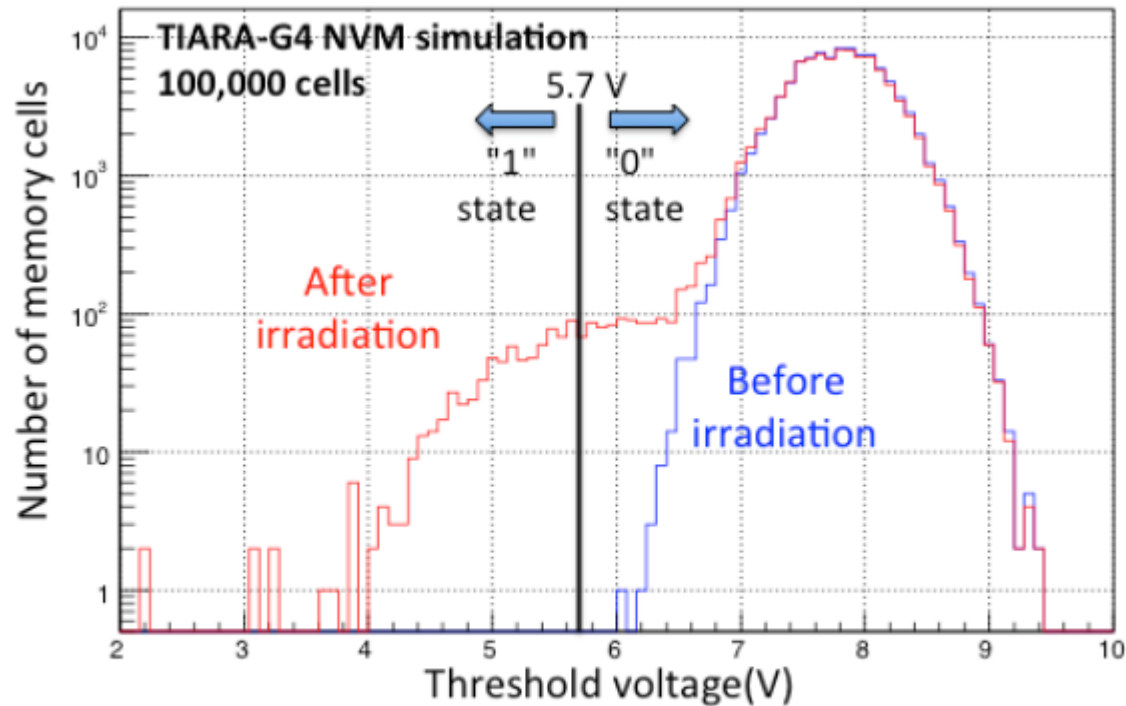


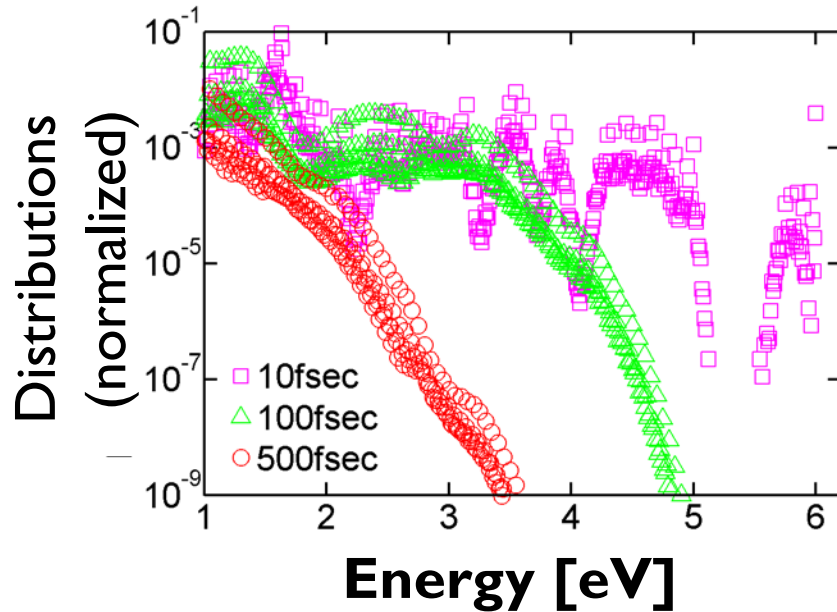
Figure 12. Distributions of  $V_T$  values computed by TIARA-G4 NVM for a population of 100,000 memory cells before and after irradiation with atmospheric neutrons.

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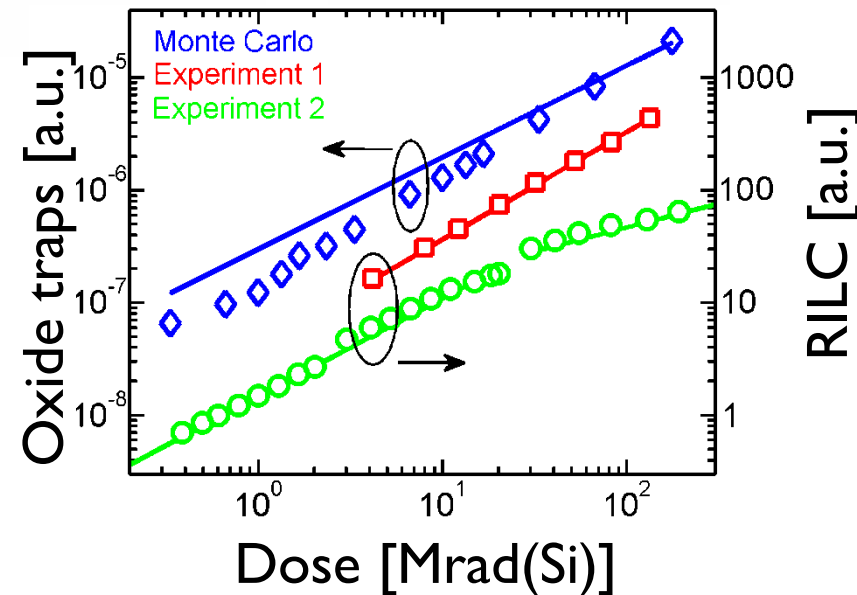
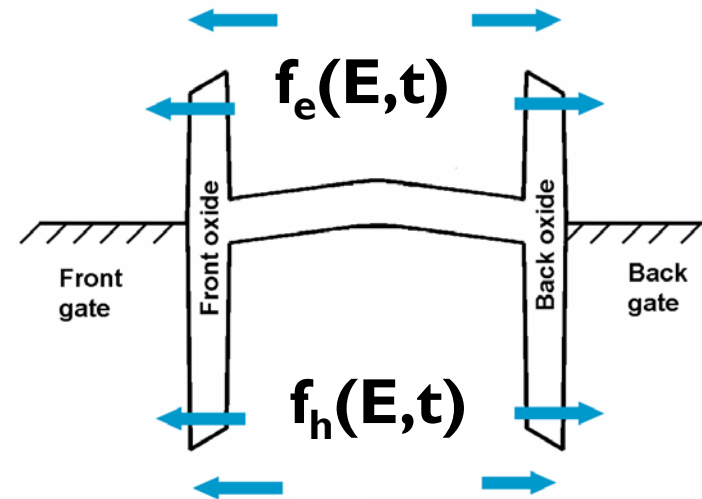


# Generation of permanent defects



Full band ensemble Monte Carlo:

- Solve the Boltzmann equation to get distributions as a function of time
- Includes phonons scattering, ionized impurity scattering/impact ionization



1. Ceschia et al *IEEE Trans. Nucl. Sci.*, 2000
2. Ang et al, *Semicond. Sci. Technol.*, 2000

# Conclusions

1. The footprint of memory is growing rapidly with technology generation. However, memory is susceptible to radiation damage.
2. ZRAM is a simplest memory that have very high density and is a likely successor of DRAM. Soft (reversible) errors in ZRAM is a significant concern.
3. Flash memory does not have classical Soft errors arising from Poisson equation, but it has new kind of soft error arising from hot electron outflow. Error correction is necessary.
4. Hard (irreversible) errors leads to SILC-like anomalous leakage and is a big reliability concern in Flash.

# References

The literature of radiation-damage is rich. Here, I refer to some of the work I have done. They have a comprehensive reference list.

“Scaling Limits of Double-Gate and Surround Gate Z-RAM Cells,” N. Butt and M.A.Alam, , IEEE Transaction on Electron Devices, Special Issue on Modeling and Simulation, 54(9), pp. 2255-2262, 2007.

“Soft Error Trends and New Physical Model for Ionizing Dose Effects in Double Gate Z-RAM Cell,” N. Butt and M.A.Alam, IEEE Trans. on Nuclear Science, 54(6), pp. 2363-2370, 2007.

“Single Event Upsets in Floating Gate Memory Cells,” N. Z. Butt, and M.A.Alam, Proc. of International Reliability Physics Symposium, Apr 2008, pp. 547-555.

Soft Errors Induced by Natural Radiation by Ground Level in Floating Gate Memories, G. Just, et al. IRPS Proc. 2013.

“Soft Error Performance of Z-RAM Floating Body Memories”, D. Fisch, R. Beffa, C. Bassin, 2006 SOI Conference, p. 111.

“Alpha-particle induced upsets in advanced CMOS circuits and technology”, D. F. Heidel et al. IBM J. of Research and Dev 52(3), p. 225, May 2008.

“SEMM-2: A few generation of single-event-effect modeling tools”, H.H.K. Tang, IBM J. Res. And Dev. 52(3), p. 233.

“Circuit design and modeling for soft errors”, A. KleinOowski, IBM J. of Research and Dev. 52(3), p. 255, May 2008.

# Review Questions

1. What is the difference between hard and soft error?
2. What is typical charge loss mechanism for ZRAM ?
3. The soft error in Flash memory is different from that of ZRAM. Explain.
4. How do people accelerate radiation induced damage?
5. If carrier relaxation was faster than thermionic emission rate, would you expect soft errors in ZRAM or SRAM?
6. What is that Geant software can do that traditional Monte Carlo software cannot?