

# SELF-HEATING EFFECTS IN SOI DEVICES AND GAN HEMTS

Dragica Vasileska, ASU



Thanks to ...

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Manan Gada, Seung Kyung Yoo



# Outline

Motivation

Thermal Effects

Previous Work Done in Thermal Modeling

The ASU Model for Addressing Self-Heating

Conclusions



'Painted Mosque' In Tetovo,  
Republic of Macedonia



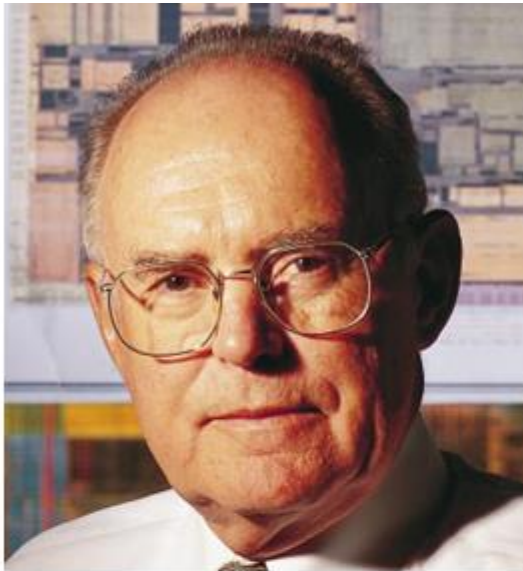
## Motivation

Transistor Scaling

Thermal Effects and Scaling

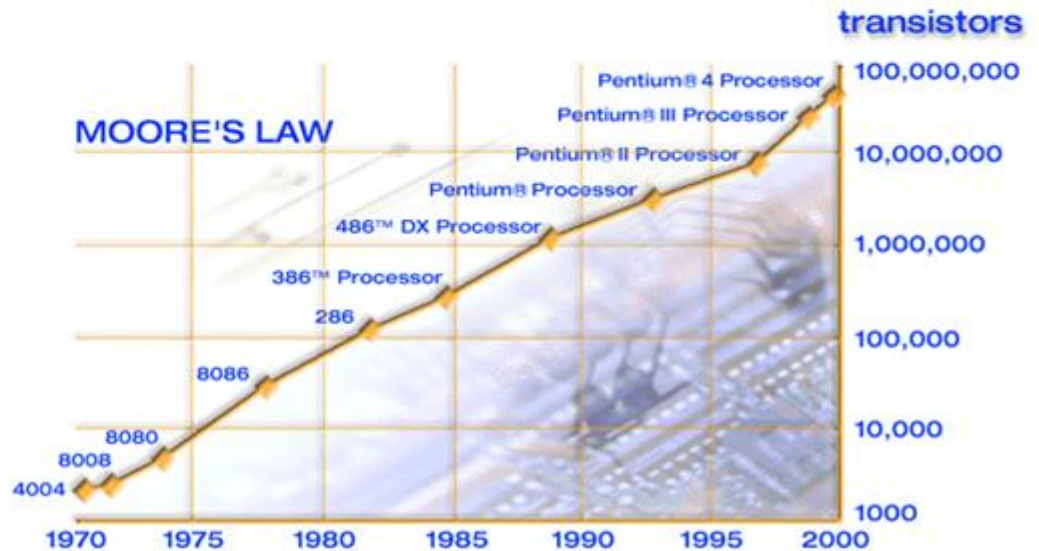


# Transistor Scaling: Moore's Law



Gordon Moore

*“every 1.5 years complexity doubles”*



# Transistor Scaling: Dennard's Law

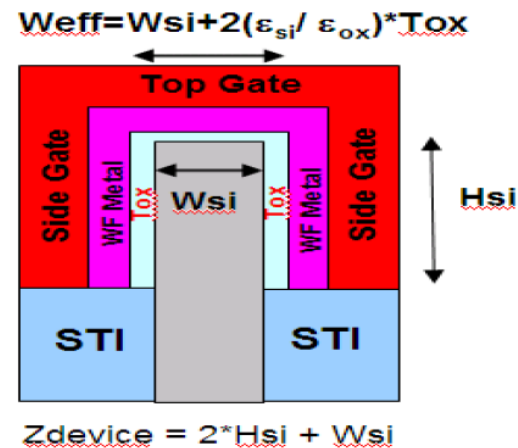
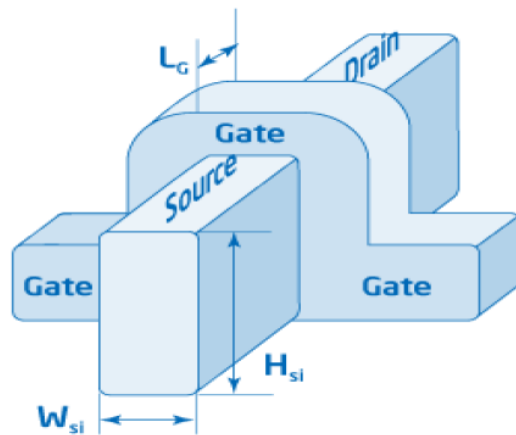
Geometry & Supply voltage	$L_g, W_g$ $T_{ox}, V_{dd}$	K	Scaling K: K=0.7 for example
Drive current in saturation	$I_d$	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ $C_o$ : gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1} (V_g - V_{th}) = KK^{-1}K = K$
$I_d$ per unit $W_g$	$I_d / \mu m$	1	$I_d$ per unit $W_g = I_d / W_g = 1$
Gate capacitance	$C_g$	K	$C_g = \epsilon_o \epsilon_{ox} L_g W_g / t_{ox} \rightarrow KK/K = K$
Switching speed	$\tau$	K	$\tau = C_g V_{dd} / I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	$A_{chip}$	$\alpha$	$\alpha$ : Scaling factor $\rightarrow$ In the past, $\alpha > 1$ for most cases
Integration (# of Tr)	N	$\alpha/K^2$	$N \rightarrow \alpha/K^2 = 1/K^2$ , when $\alpha=1$
Power per chip	P	$\alpha$	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha = 1$ , when $\alpha=1$

# More Moore ...

## Multi-Gate Transistors Implementation

### Multi-Gate Fin Transistor:

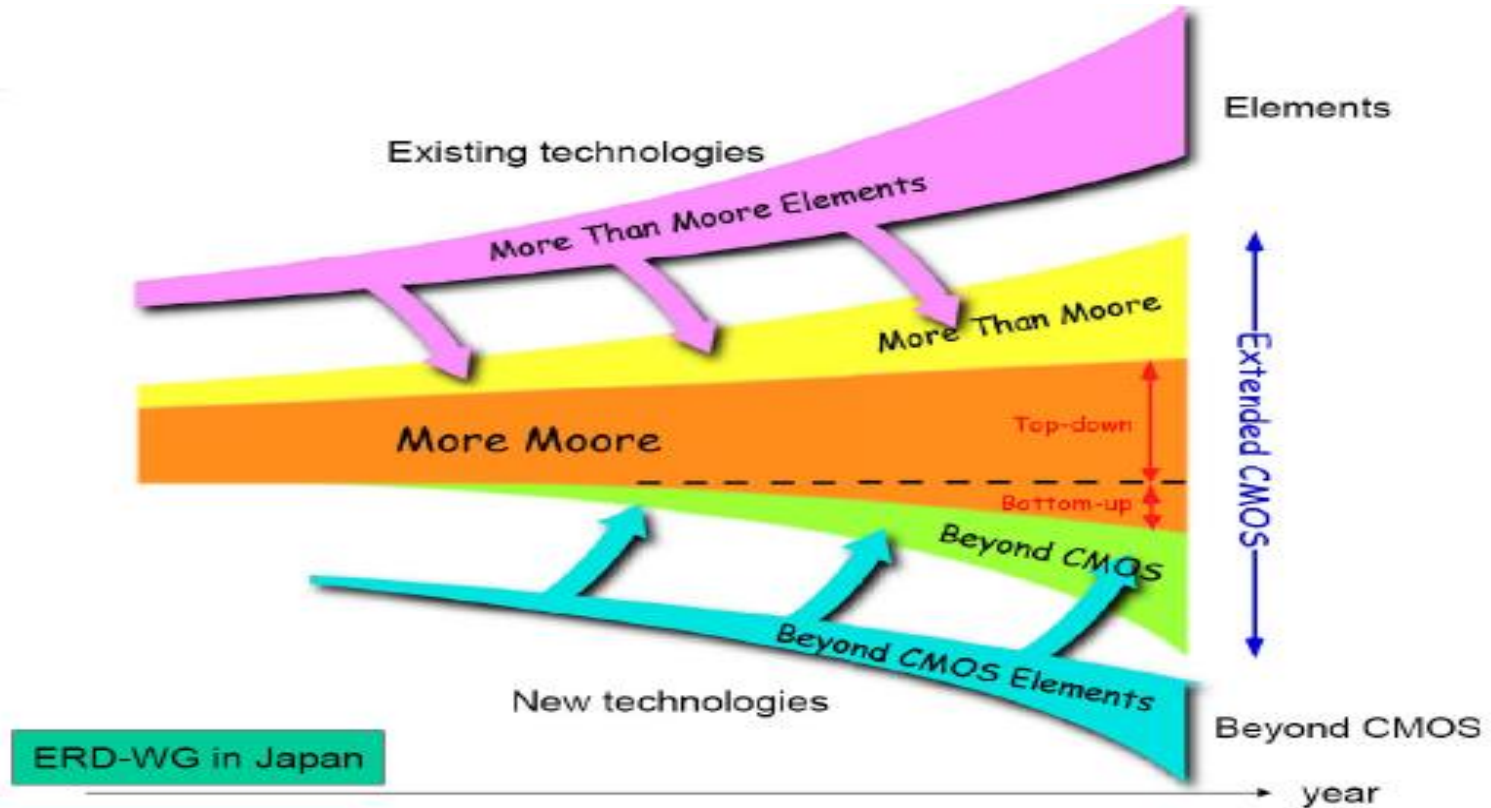
- ++ Self Aligned structure for S/D
- Non-Planar structure



### Multi-Gate Fin Transistor



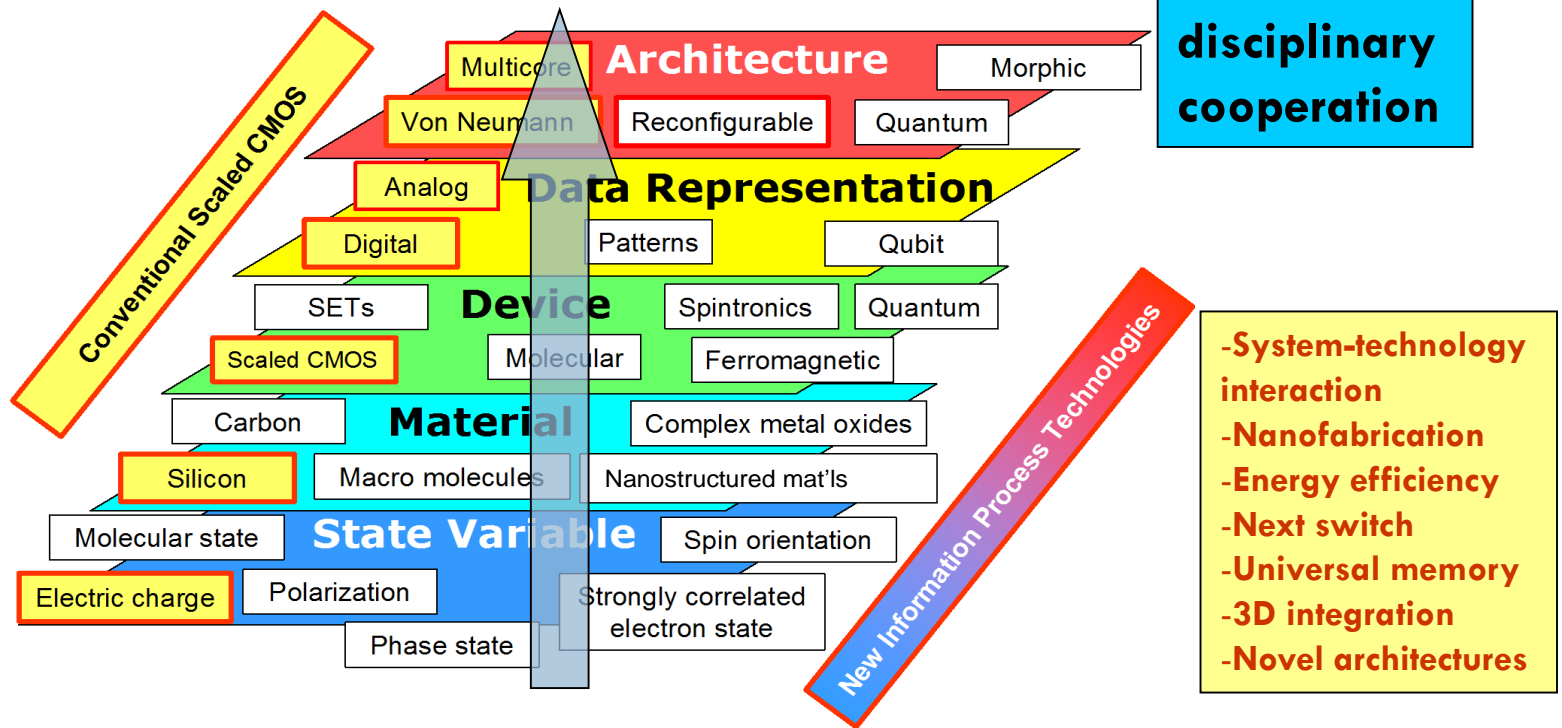
# More Than Moore and Beyond CMOS



ITRS-ERD vision of the role of Beyond CMOS and More than Moore elements to form future extended CMOS platforms (2010).

# 2020 and Beyond ...

## Transversal Research Projects

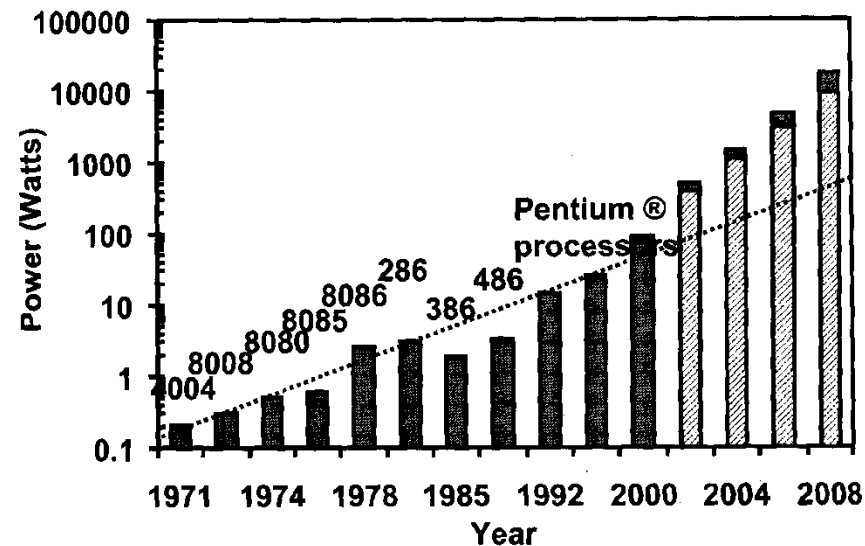


- Advanced component technology + advanced system design
- Beyond CMOS + advanced More than Moore integration with More Moore

**For systems 2020 and beyond**

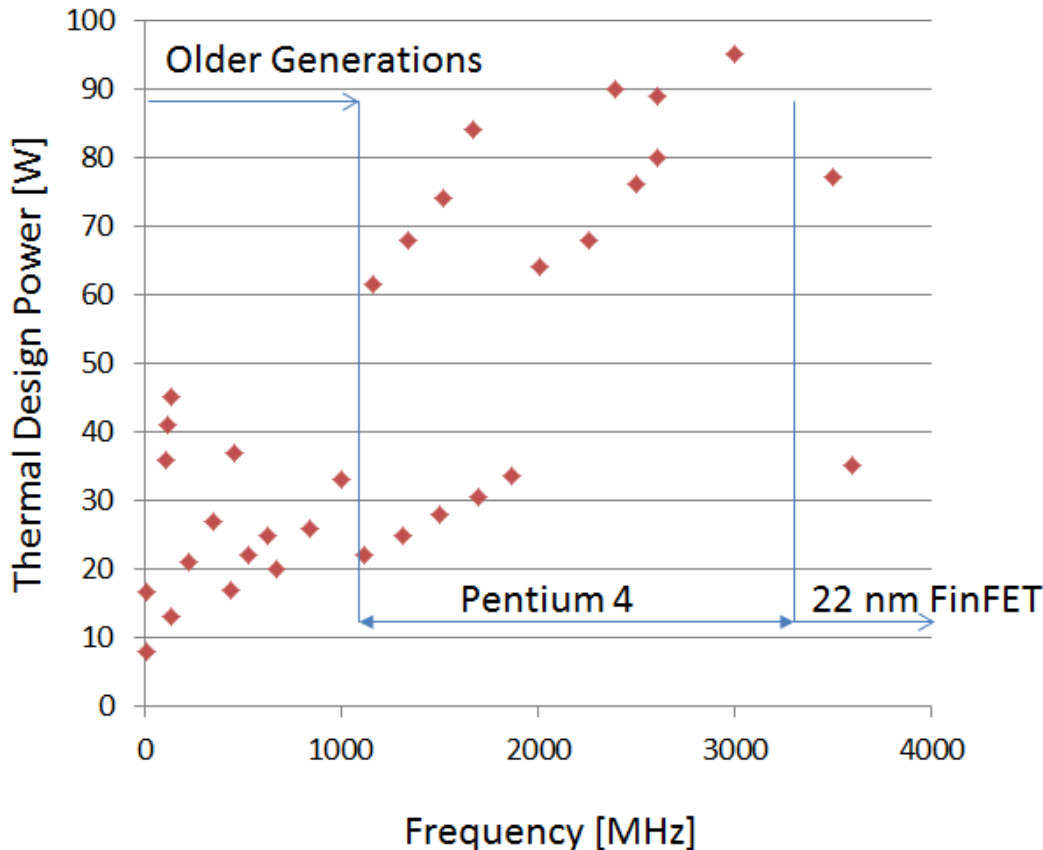
# Thermal Effects and Scaling

- Intel VP Patrick Gelsinger (ISSCC 2001)
  - ▣ If scaling continues at present pace, by 2005, high speed processors would have power density of nuclear reactor, by 2010, a rocket nozzle, and by 2015, surface of sun.
  - ▣ “Business as usual will not work in the future.”
- Intel stock dropped 8% on the next day
- But attention to power is increasing





# Thermal Design Power



- The **thermal design power (TDP)**, sometimes called **thermal design point**, refers to the maximum amount of power the cooling system in a computer is required to dissipate.
- For example, a laptop's CPU cooling system may be designed for a 20 watt TDP, which means that it can dissipate up to 20 watts of heat without exceeding the maximum junction temperature for the computer chip.



'Church of St. Pantelejmon', Skopje, Republic of Macedonia (12th century Byzantine church)

## Thermal Effects

Electro-Thermal Effects

Thermo-Electric Effects

Analogy Between Electrical and Thermal Variables

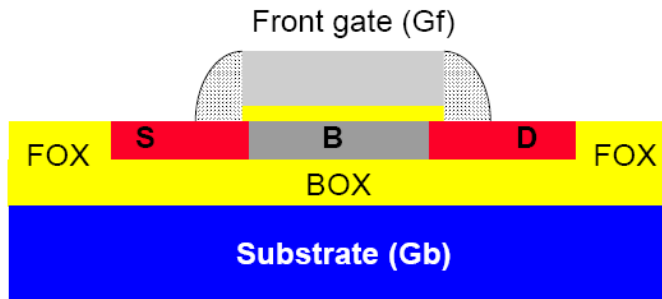
# Electro-Thermal Effects

- Joule Heating:
  - ▣ When an electric current flows through a solid or liquid with finite conductivity, electric energy is converted to heat through resistive losses in the material.
  - ▣ The heat is generated on the microscale when the conduction electrons transfer energy to the conductors atoms through collisions.
  - ▣ Joule heating is in some cases unwanted, and efforts are made to reduce it.
    - However, many applications rely on Joule heating;
      - some of these use the effect directly, such as cooking plates,
      - while other applications, such as microvalves for fluid control, use the effect indirectly through thermal expansion.



# Why Electro-Thermal Effects in Devices?

## Reason for Observation of Self-Heating

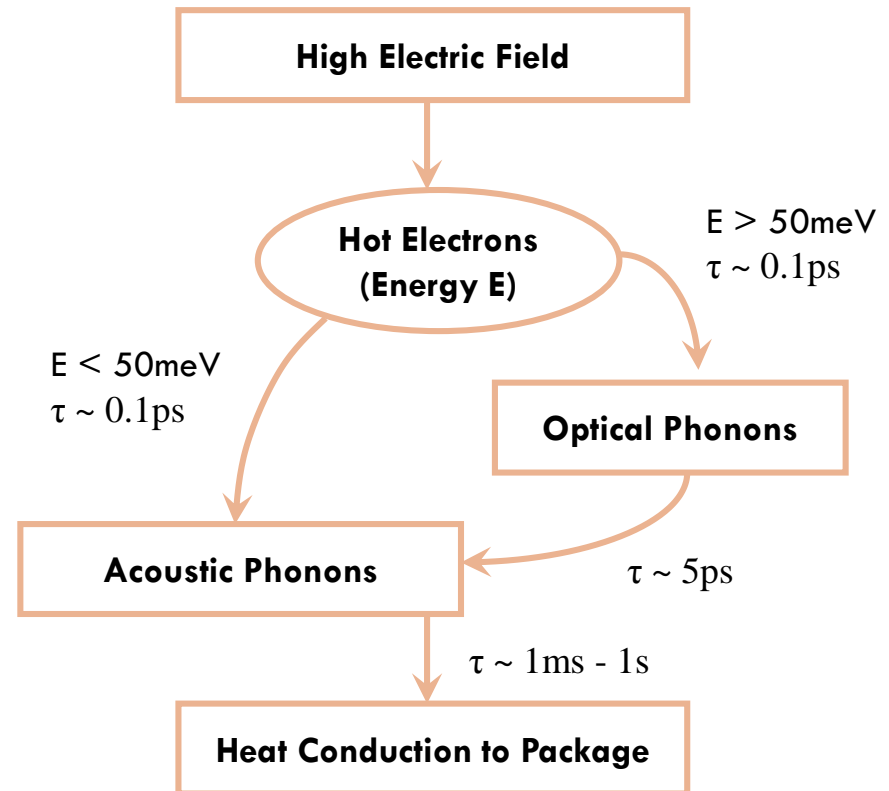


Fully depleted (FD) body

Material	$k_{th}$ (W/mK)
Si	148
Ge	60
Silicides	40
Si (10 nm)	13
SiO <sub>2</sub>	1.4



## MUSTs in the Theoretical Model



# Implementation of Electro-Thermal Effects in Commercial Simulators

- Silvaco ATLAS implements **Wachutka** model for lattice heating which accounts for:
  - ▣ Joule heating
  - ▣ Cooling due to carrier generation and recombination
  - ▣ Peltier and Thomson effects

$$C \frac{\partial T_L}{\partial t} = \nabla \cdot (k \nabla T_L) + H$$

Heat capacitance per unit volume

Thermal conductivity

Heat generation

# Heat Generation Model

- In the past, the heat generation model was simply:

$$H = (J_n + J_p) \cdot E$$

- Presently:

$$\begin{aligned}
 H = & \frac{|J_n|^2}{q\mu_n n} + \frac{|J_p|^2}{q\mu_p p} - & \longrightarrow & \text{Joule heating term} \\
 & -T_L (J_n \nabla P_n) - T_L (J_p \nabla P_p) + & \longrightarrow & \text{Peltier and Joule-Thomson effects} \\
 & + q(R - G) \left[ T_L \left( \frac{\partial \phi_n}{\partial T_{n,p}} \right) - \phi_n - T_L \left( \frac{\partial \phi_p}{\partial T_{n,p}} \right) + \phi_p \right] - & \longrightarrow & \text{Recombination and} \\
 & -T_L \left[ \left( \frac{\partial \phi_n}{\partial T_{n,p}} \right) + P_n \right] \nabla \cdot J_n - T_L \left[ \left( \frac{\partial \phi_p}{\partial T_{n,p}} \right) + P_p \right] \nabla \cdot J_p & & \text{Generation heating} \\
 & & & \text{and cooling terms}
 \end{aligned}$$

# Non-Isothermal Current Densities

- When SILVACO GIGA module is being invoked, the electron and hole current densities are modified to account for spatially varying lattice temperatures:

$$J_n = -q\mu_n n (\nabla \phi_n + P_n \nabla T_L)$$

$$J_p = -q\mu_p p (\nabla \phi_p + P_p \nabla T_L)$$

- Where  $P_n$  and  $P_p$  are absolute thermoelectric powers for electrons and holes and are calculated using:

$$P_n = -\frac{k_B}{Q} \left( \frac{5}{2} + \ln \left( \frac{N_c}{n} \right) + KSN + \zeta_n \right)$$

$$P_p = \frac{k_B}{Q} \left( \frac{5}{2} + \ln \left( \frac{N_v}{p} \right) + KSP + \zeta_p \right)$$

# Thermo-Electric Effects



Seebeck effect

Seebeck effect is coupling of two potentials, the electrochemical potential and the temperature.



Thermoelectric effect

When an electric current is passed through a conductor having a temperature gradient over its length, heat will be either absorbed by or expelled from the conductor.

Peltier illustrated that heat flux and electrical current can be coupled.

Thomson effect

Peltier effect

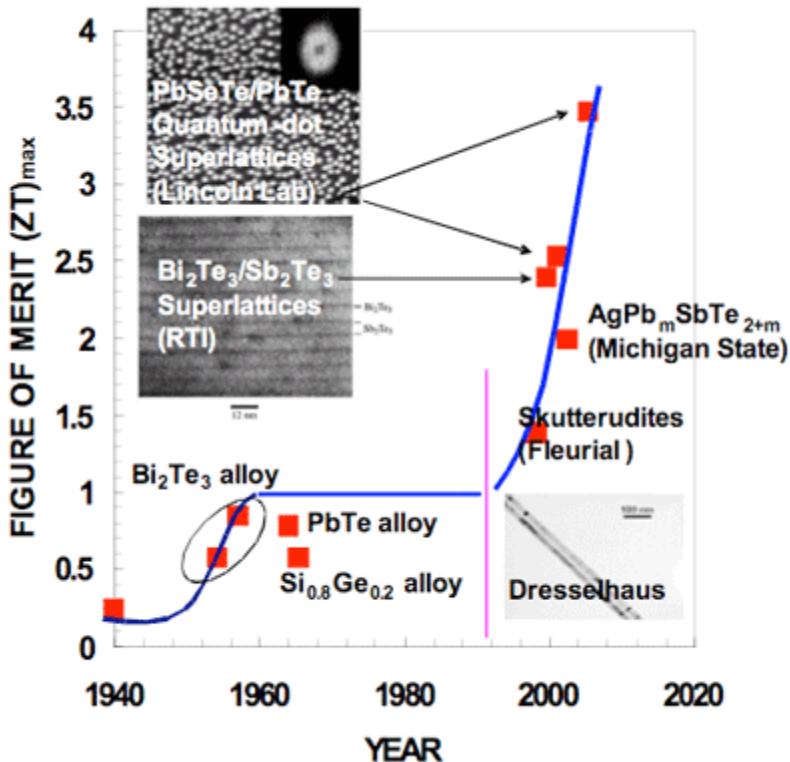




# Thermo-Electric Effects Explained

- When any two metals are connected together, a voltage is developed which is a function of the temperatures of the junctions and (mainly) the difference in temperatures.
- It was later found that the Seebeck voltage is the sum of two effects: the ***Peltier effect***, and the ***Thompson effect***.
  - ▣ The ***Peltier effect*** explains a voltage generated in a junction of two metal wires.
  - ▣ The ***Thompson effect*** explains a voltage generated by the temperature gradient in the wires.

# Peltier Effect: ZT Factor Over the Years



$$ZT = S^2T \sigma / \kappa$$

- The ZT of a thermoelectric material is a dimensionless unit that is used to compare the efficiencies of various materials.
- ZT is determined by three physical parameters:
  - the thermopower  $S$  (also known as Seebeck factor),
  - the electrical conductivity  $\sigma$ , the thermal conductivity  $k = k_e + k_{ph}$ , where the  $k_e$  and  $k_{ph}$  are the thermal conductivities of electrons and phonons, respectively,
  - and the absolute temperature  $T$

# Analogy Between Electrical and Thermal Variables

$$J = \sigma E = -\sigma \frac{dV}{dx} \therefore \text{current density}$$

$$F = -\kappa \frac{dT}{dx} \therefore \text{heat flux}$$

$$\left\{ \begin{array}{l} J \Leftrightarrow F \\ V \Leftrightarrow T \\ \sigma \Leftrightarrow \kappa \end{array} \right.$$

Skopje, Capitol of Republic of Macedonia



Previous Work Done in Thermal Modeling

# Previous Work in Thermal Modeling

- Mostly, the previous work performed and related to thermal modeling can be split into:
  - ▣ Solutions of the Phonon Boltzmann Transport Equation
  - ▣ Analysis of self-heating effects in devices



# Phonon BTE Solvers

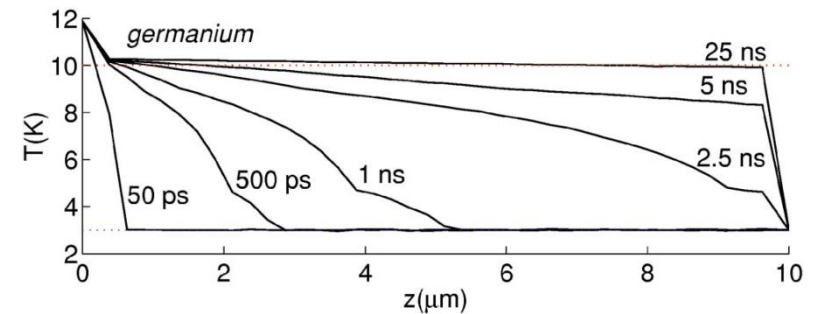
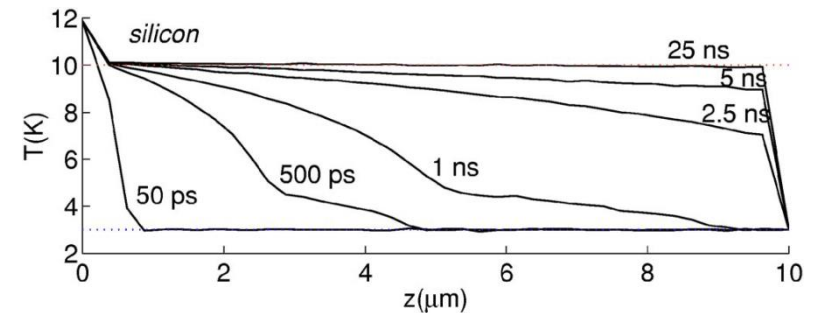
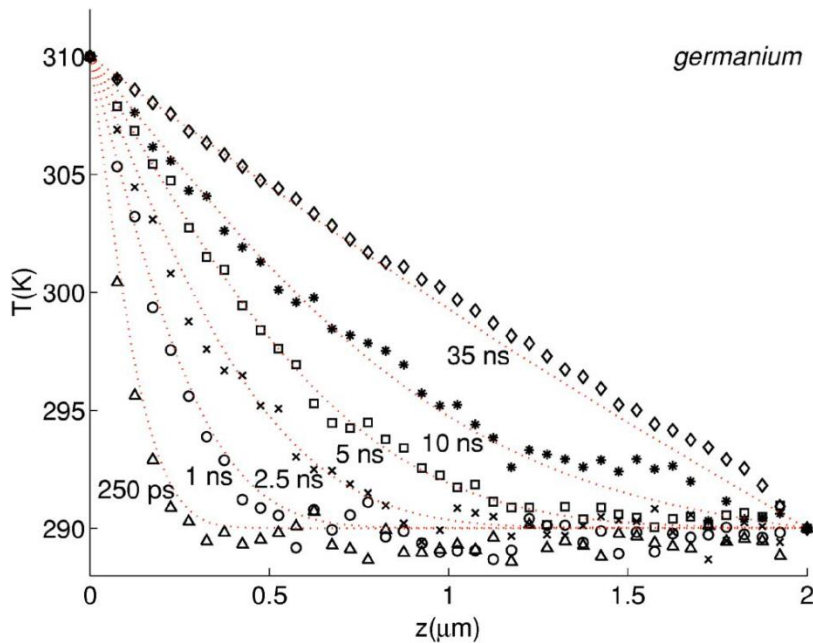
- **Peterson** performed a Monte Carlo Simulation for phonons in the Debye approximation and using single relaxation time
- **Mazumder and Majumdar** followed Peterson approach but included the dispersion relation and the different acoustic polarization branches
  - Limit: The N and the U processes are not treated separately although they do not contribute the same way to the thermal conductivity

\* Peterson, R. B. (1994). "Direct Simulation of Phonon-Mediated Heat Transfer in a Debye Crystal." *Journal of Heat Transfer*, Vol. 116(4), pp. 815-822.

\* Mazumder, S. and Majumdar, A. (2001). "Monte Carlo Study of Phonon Transport in Solid Thin Films Including Dispersion and Polarization." *Journal of Heat Transfer*, Vol.123(4), pp. 749-759.

# Phonon BTE Solvers, Cont'd

- **Lacroix** further generalized the model:
  - By incorporation of N and U processes
  - Transient conditions are also being considered



Lacroix, D., Joulain, K. and Lemonnier, D. (2005). "Monte Carlo Transient Phonon Transport in Silicon and Germanium at Nanoscales." *Physical Review B*, Vol. 72(6), pp. 064305/1-11.

# Modeling Self-Heating in Devices

- Work of ***Eric Pop, Goodson, Robert Dutton***
  - ▣ Non-parabolic model with analytical phonon dispersion
  - ▣ study heat transfer and energy conversion processes at nanoscales. Applications include semiconductor devices and packaging, thermoelectric and photonic energy conversion, and microfluidic heat exchangers.
- Work of ***Kelsall and Sadi***
  - ▣ Nanoscale transistors, GaN HEMTs

## Popova Sapka Ski Resort, Tetovo, Republic of Macedonia



## The ASU Model to Addressing Self-Heating

### Theoretical Model

### Application of the Model to Modeling of:

FD SOI Devices, Dual Gate Structures, SOD and SOAIN Devices

Nanowire Transistors

GaN HEMTs

# Theoretical Model

$$\left( \frac{\partial}{\partial t} + v_e(\mathbf{k}) \cdot \nabla_r + \frac{e}{\hbar} E(\mathbf{r}) \cdot \nabla_k \right) f = \sum_q \left\{ W_{e,q}^{\mathbf{k}+\mathbf{q} \rightarrow \mathbf{k}} + W_{a,-q}^{\mathbf{k}+\mathbf{q} \rightarrow \mathbf{k}} - W_{e,-q}^{\mathbf{k} \rightarrow \mathbf{k}+\mathbf{q}} - W_{a,q}^{\mathbf{k} \rightarrow \mathbf{k}+\mathbf{q}} \right\}$$

$$\left( \frac{\partial}{\partial t} + v_p(q) \cdot \nabla_r \right) g = \sum_k \left\{ W_{e,q}^{\mathbf{k}+\mathbf{q} \rightarrow \mathbf{k}} - W_{a,q}^{\mathbf{k} \rightarrow \mathbf{k}+\mathbf{q}} \right\} + \left( \frac{\partial g}{\partial t} \right)_{p-p}$$



J. Lai and A. Majumdar, "Concurrent thermal and electrical modeling of submicrometer silicon devices", J. Appl. Phys. , Vol. 79, 7353 (1996).

$$C_{LO} \frac{\partial T_{LO}}{\partial t} = \frac{3nk_B}{2} \left( \frac{T_e - T_L}{\tau_{e-LO}} \right) + \frac{nm^* v_d^2}{2\tau_{e-LO}} - C_{LO} \left( \frac{T_{LO} - T_A}{\tau_{LO-A}} \right),$$

$$C_A \frac{\partial T_A}{\partial t} = \nabla \cdot (k_A \nabla T_A) + C_{LO} \left( \frac{T_{LO} - T_A}{\tau_{LO-A}} \right) + \frac{3nk_B}{2} \left( \frac{T_e - T_L}{\tau_{e-L}} \right).$$



# Theoretical Model ...

Energy gain from the electrons

Energy loss to acoustic phonons

$$C_{LO} \frac{\partial T_{LO}}{\partial t} = \frac{3nk_B}{2} \left( \frac{T_e - T_L}{\tau_{e-LO}} \right) + \frac{nm^* v_d^2}{2\tau_{e-LO}} - C_{LO} \left( \frac{T_{LO} - T_A}{\tau_{LO-A}} \right),$$

$$C_A \frac{\partial T_A}{\partial t} = \nabla \cdot (k_A \nabla T_A) + C_{LO} \left( \frac{T_{LO} - T_A}{\tau_{LO-A}} \right) + \frac{3nk_B}{2} \left( \frac{T_e - T_L}{\tau_{e-L}} \right).$$

Heat Diffusion

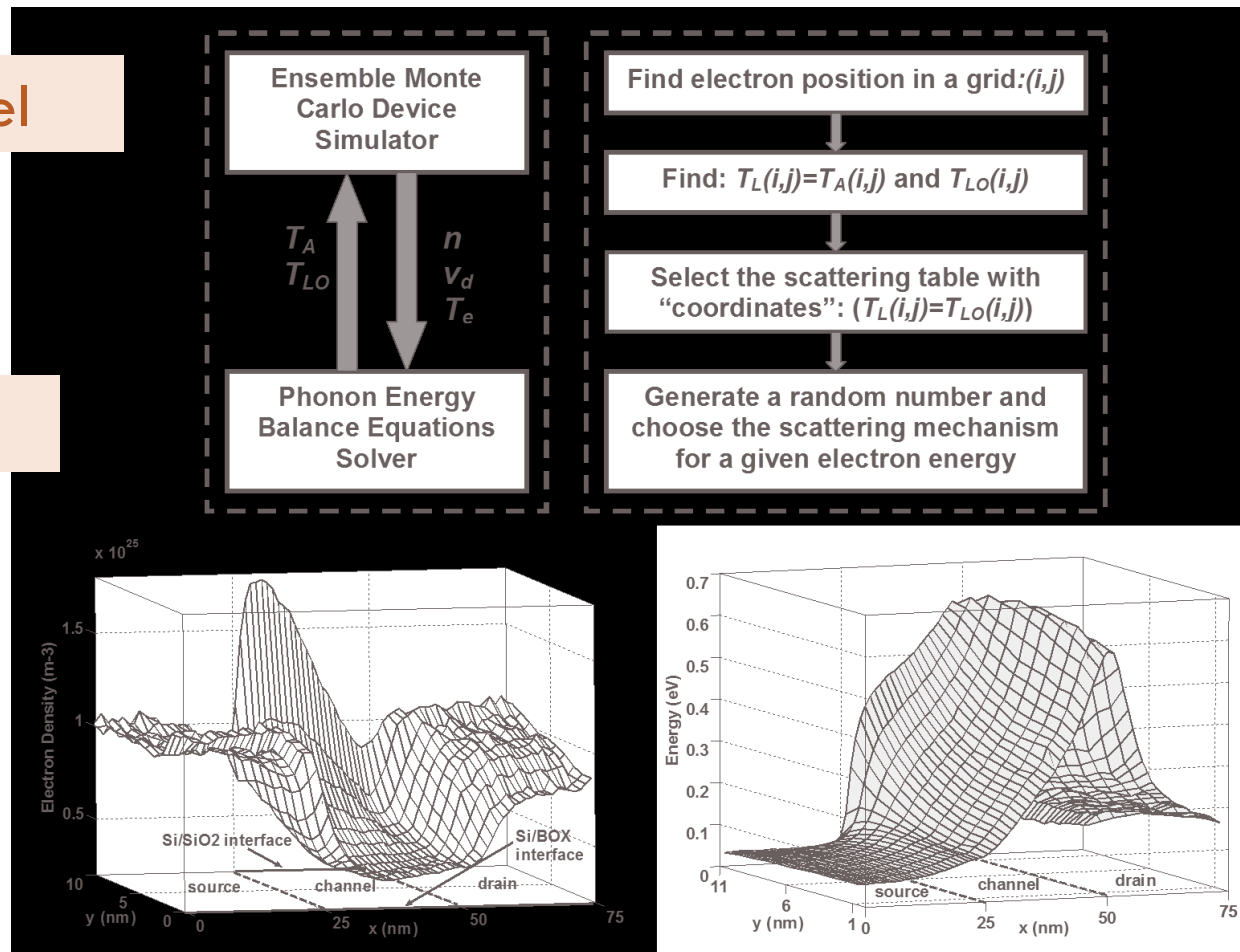
Gain term due to optical phonons

Gain term due to electrons (omitted if acoustic phonon scattering is treated as elastic scattering process)

# Theoretical Model ...

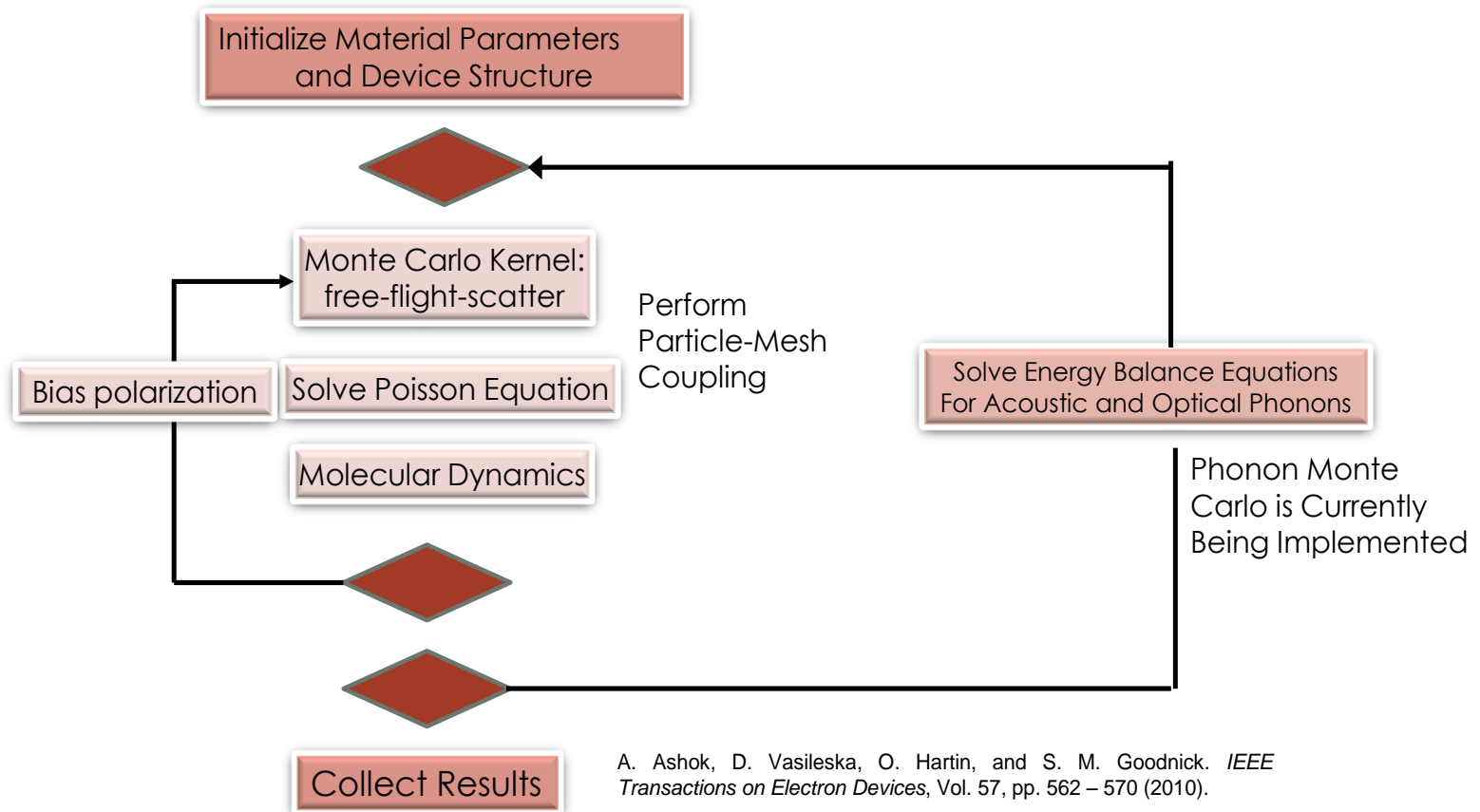
Particle Model

Fluid Model



# Theoretical Model ...

## □ Gummel cycles



# Theoretical Model: Thermal Conductivity

- Solid transmit thermal energy by two modes , either one of which, or both, may operate.
  1. In all solids , energy may be transferred by means of elastic vibrations of the lattice moving through the crystal in the form of waves .
  2. In some solids , notably metals , free electrons moving through the lattice also carry energy in a manner similar to thermal conduction by a True gas phase .

**Thermal Conductivity:  $k = k_e + k_p$**

# Thermal Conductivity

$$k_p = \frac{1}{3} \mathbf{C} \mathbf{v} l$$

Specific heat      Sound velocity      Phonon *mfp*

Specific heat :

If  $T > \Theta$ ,     $\mathbf{C} \sim \text{constant}$   
If  $T \ll \Theta$ ,     $\mathbf{C} \sim T^d$  (d: dimension)

Mean free path:

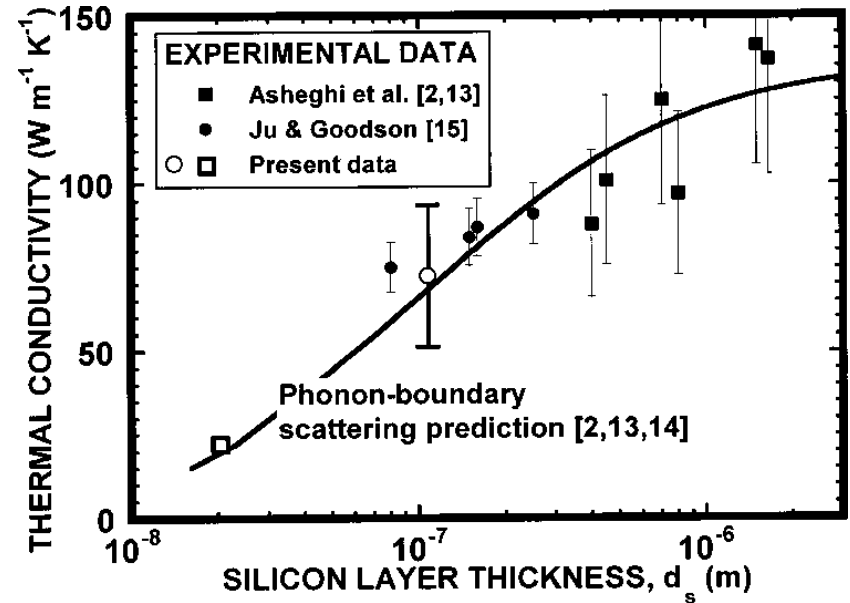
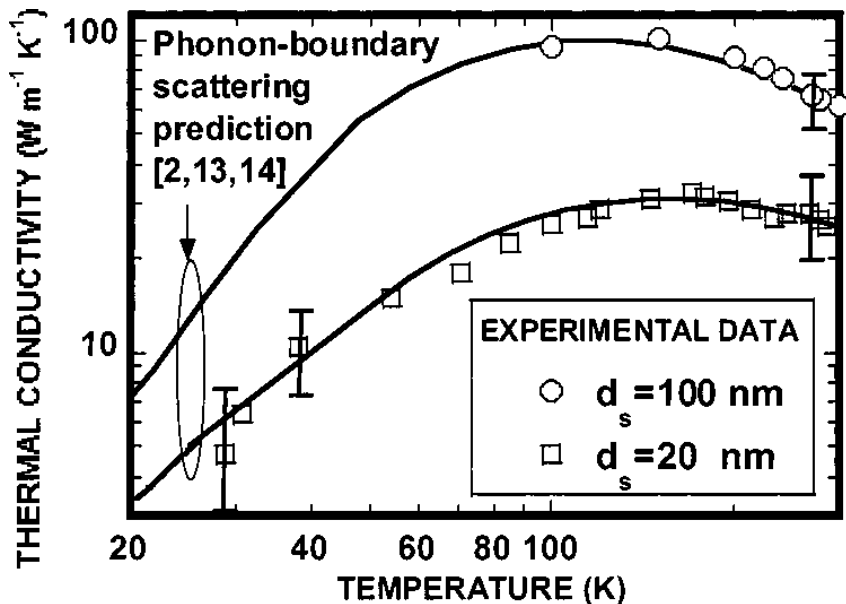
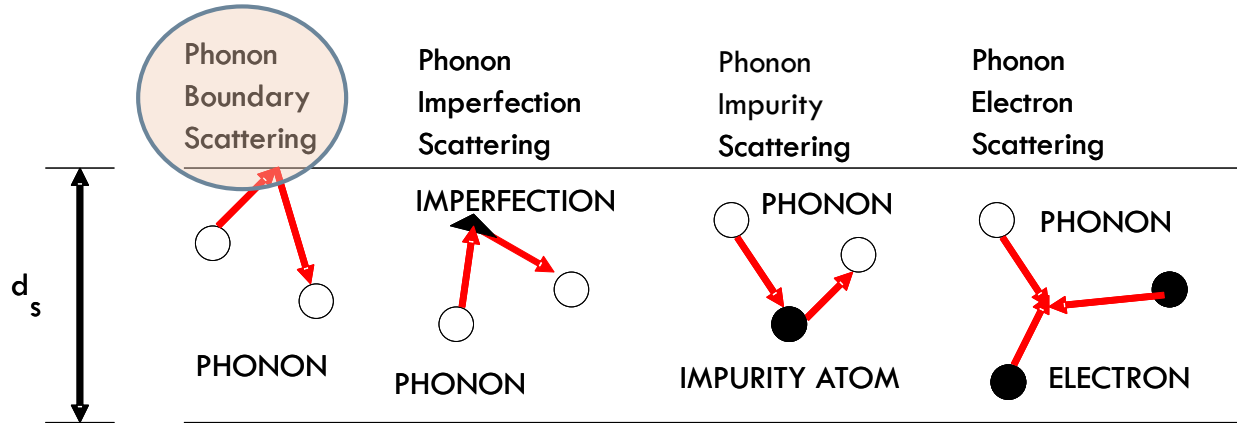
$$\frac{1}{l} = \frac{1}{l_{st}} + \frac{1}{l_{um}}$$

Static scattering (phonon -- defect, boundary):  $l_{st} \sim \text{constant}$

Umklapp phonon scattering:  $l_{um} \sim e^{\Theta/T}$



# Thermal Conductivity of Thin Films



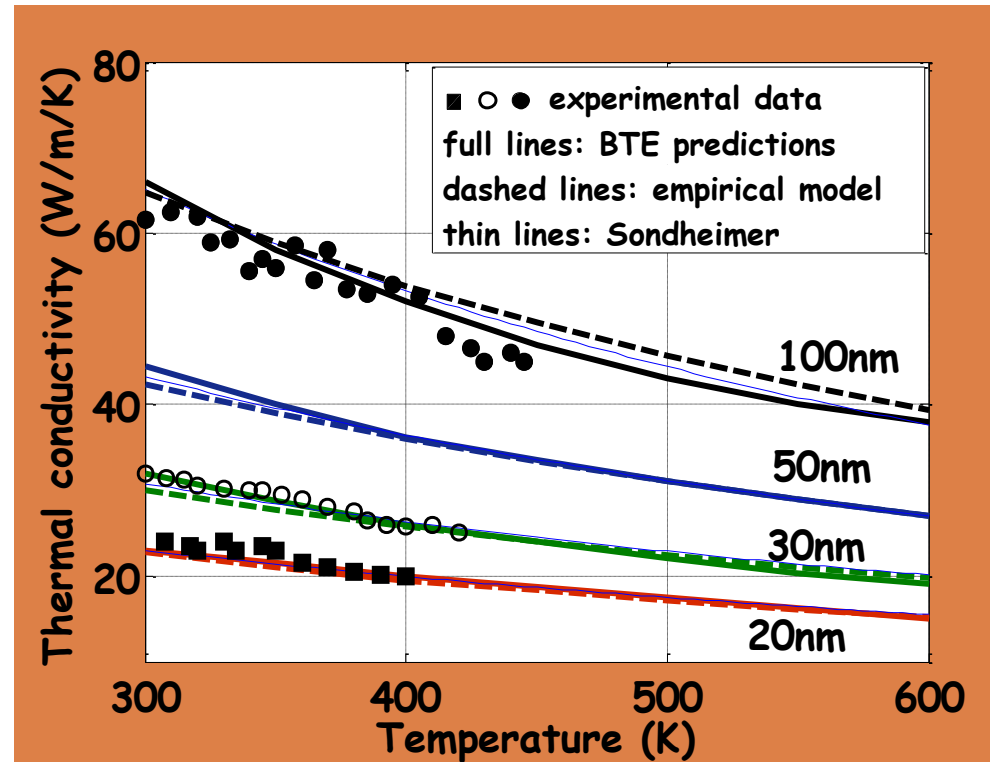
# Analytical Model for Thin Films

$$\kappa(z) = \kappa_0(T) \int_0^{\pi/2} \sin^3 \theta \left\{ 1 - \exp\left(-\frac{a}{2\lambda(T)\cos\theta}\right) \cosh\left(\frac{a-2z}{2\lambda(T)\cos\theta}\right) \right\} d\theta$$

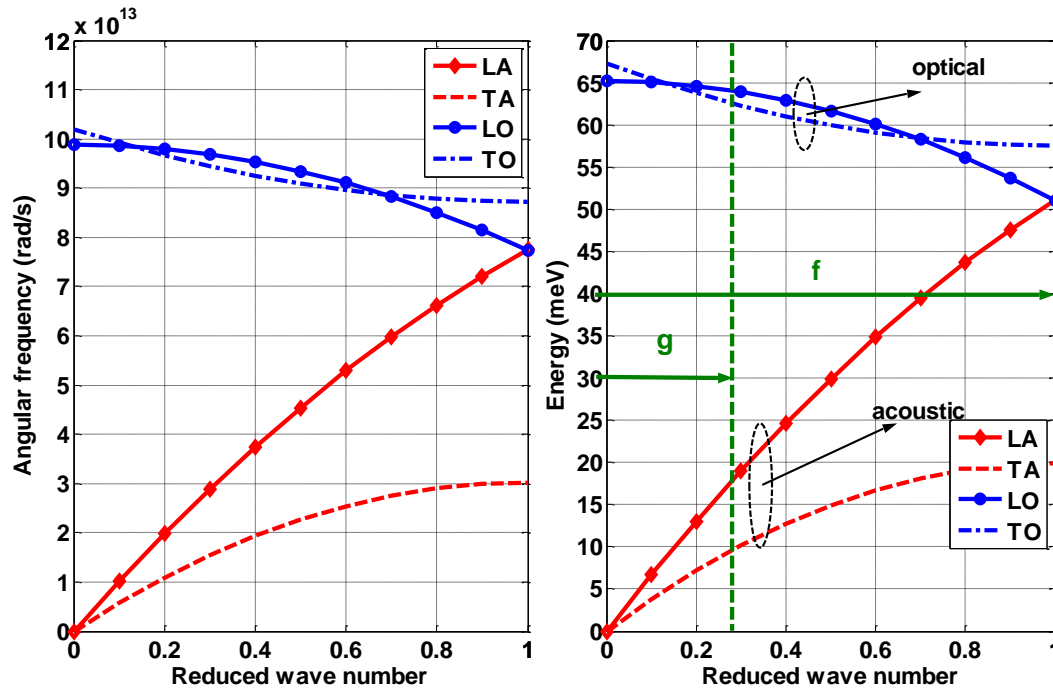
$$\lambda(T) = \lambda_0(300/T)$$

$$\kappa_0(T) = \frac{135}{a+bT+cT^2} \text{ W/m/K}$$

- E. H. Sondheimer, "The Mean Free Path of Electrons in Metals", *Advances in Physics*, Vol. 1, no. 1, Jan. 1952, reprinted in *Advances in Physics*, Vol. 50, pp. 499-537, 2001.
- M. Asheghi, M. N. Touzelbaev, K. E. Goodson, Y. K. Leung, and S. S. Wong, "Temperature Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates," *ASME Journal of Heat Transfer*, Vol.120, pp. 30-33, 1998.



# Theoretical Model – Phonon Dispersions

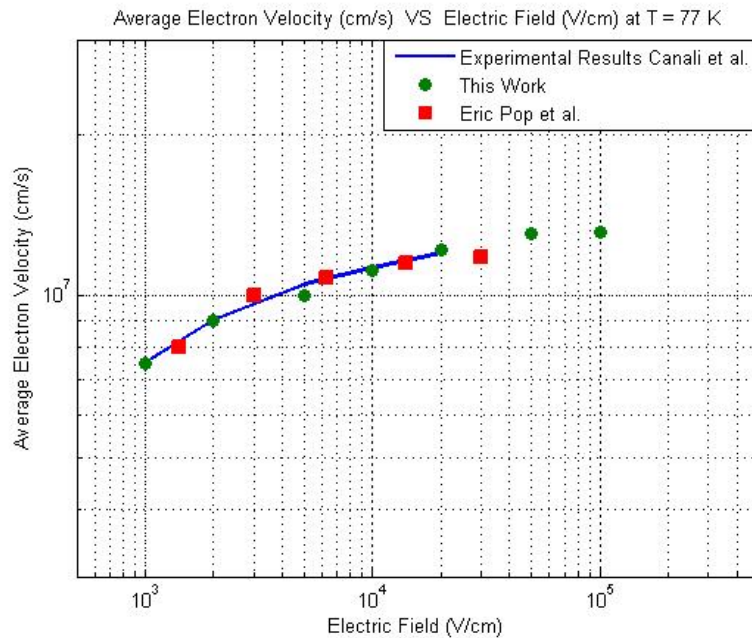


QUADRATIC FIT TO  
PHONON DISPERS-  
SIONS

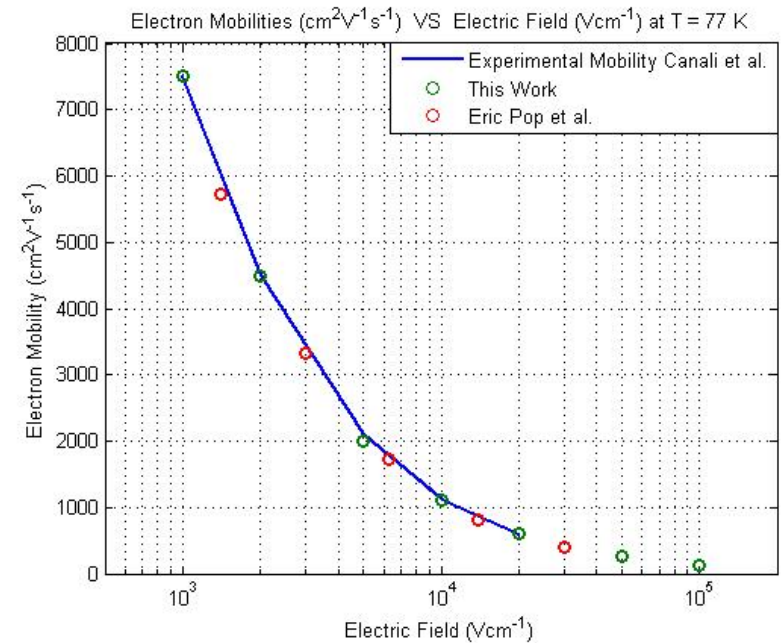
	$\omega_o$ ( $10^{13}$ rad/s)	$v_s$ ( $10^5$ cm/s)	$c$ $10^{-3}$ $\text{cm}^2/\text{s}$
LA	0.00	9.01	-2.00
TA	0.00	5.23	-2.26
LO	9.88	0.00	-1.60
TO	10.20	-2.57	1.11

# Phonon Dispersions: Proof of Concept

## Drift Velocity in Silicon at T=77K

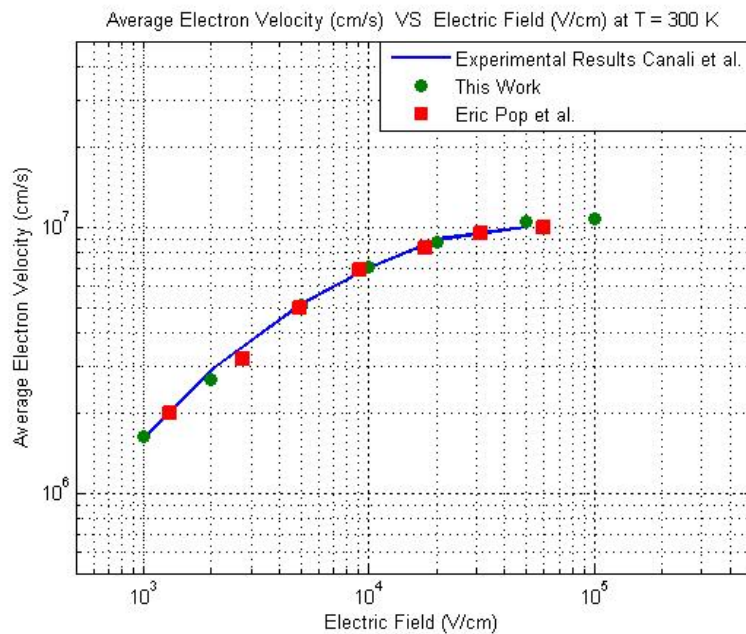


## Mobility at T=77K

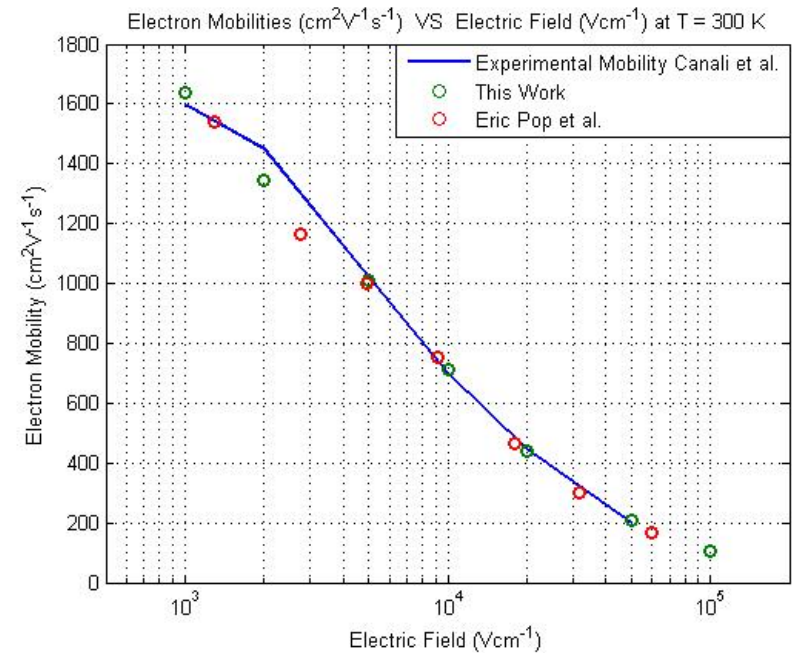


# Phonon Dispersions: Proof of Concept

## Drift Velocity in Silicon at T=300K



## Mobility at T=300K



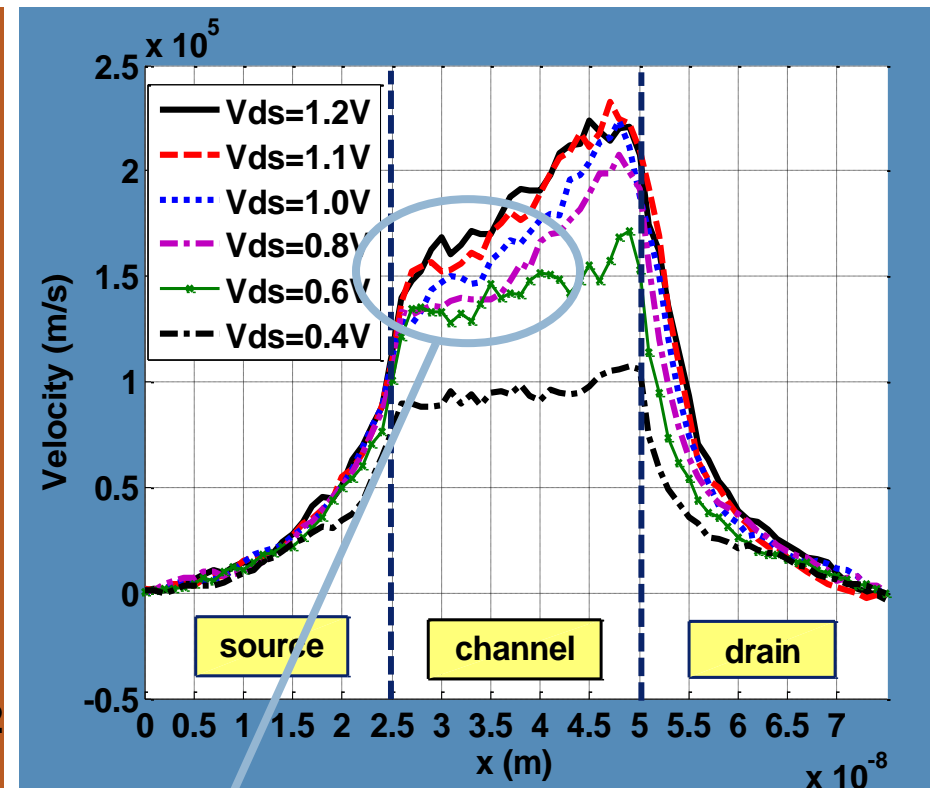
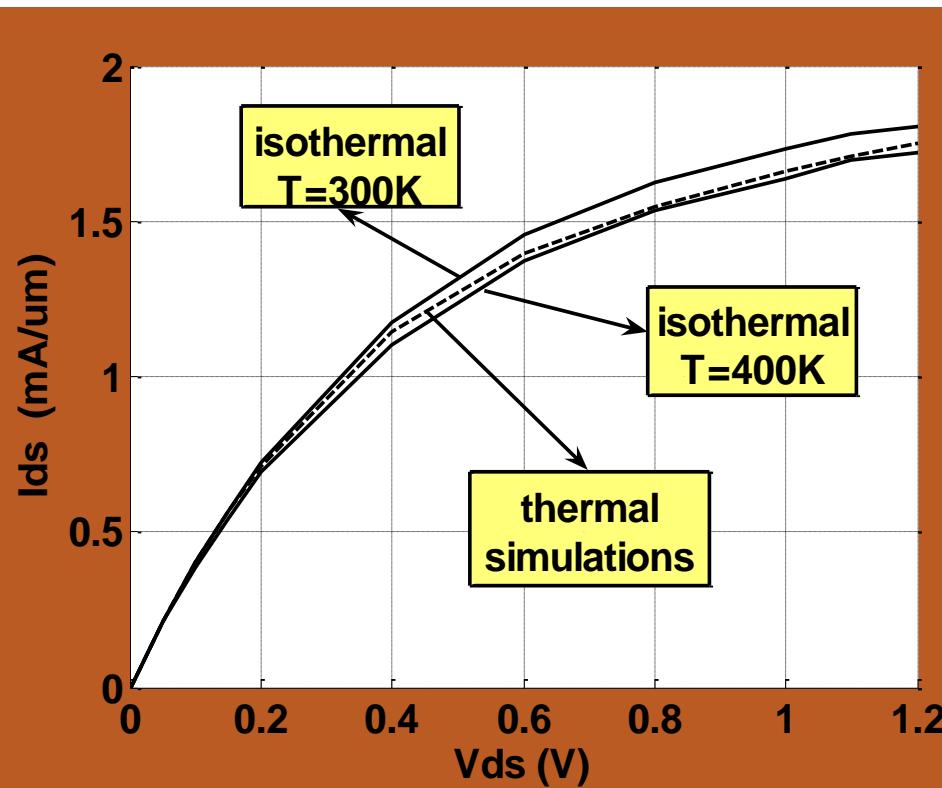


## FULLY DEPLETED SOI DEVICES

Lake Powell, Arizona

# Simulation Results: FD SOI Devices

## □ 25 nm Channel Length Device

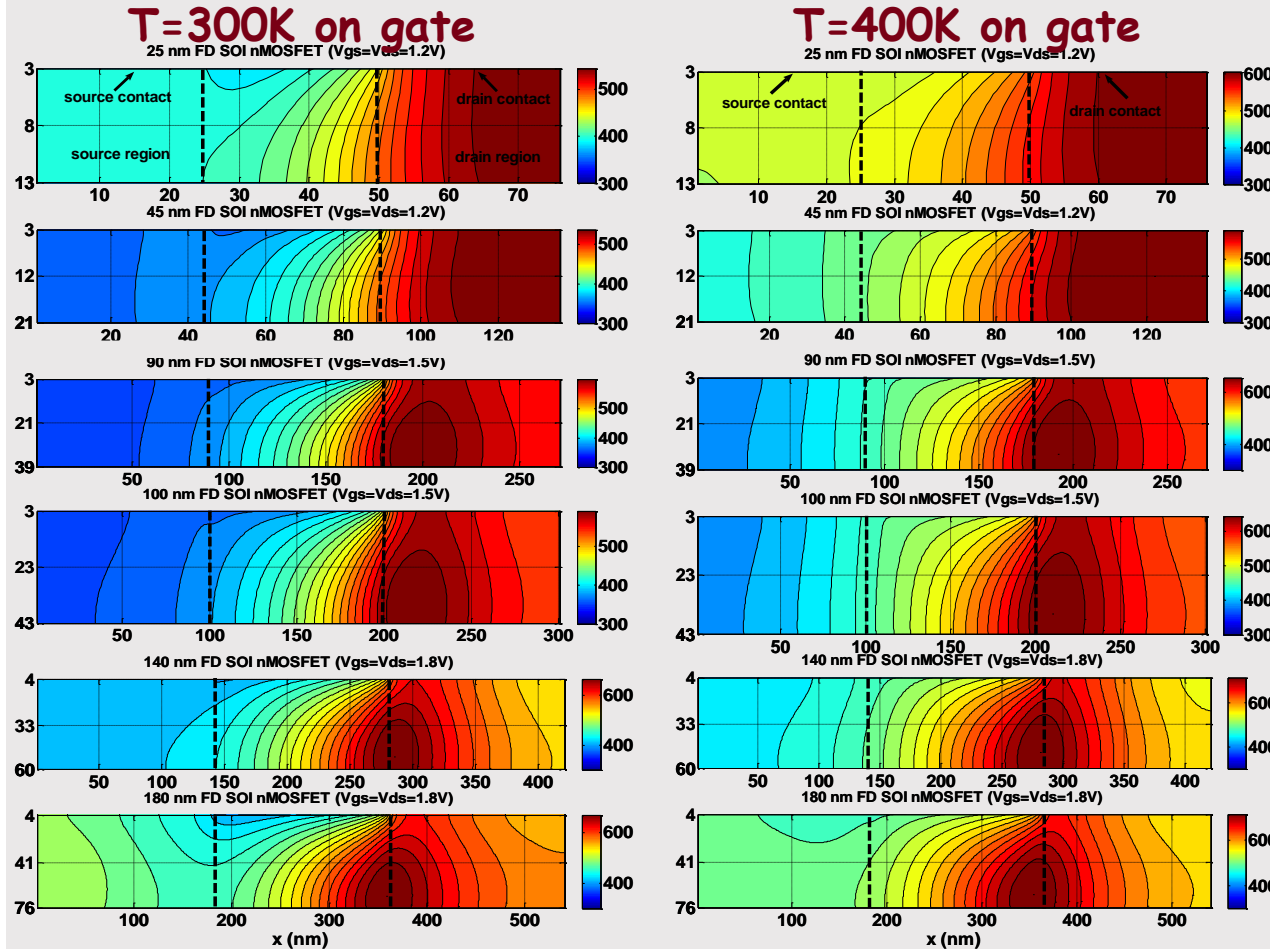


K. Raleva, D. Vasilevska, S. M. Goodnick and T. Dzekov, "Modeling thermal effects in nano-devices", *Journal of Computational Electronics*, DOI 10.1007/s10825-008-0189-3 © Springer Science+Business Media LLC 2008, *J. Computational Electronics*, Vol. 7, pp. 226-230 (2008).

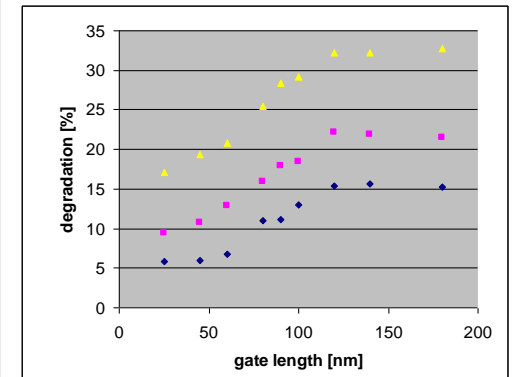
Carriers are in the velocity overshoot



# Heat Dissipation Across Technology Nodes



Parameter is the temperature on the Gate Electrode.



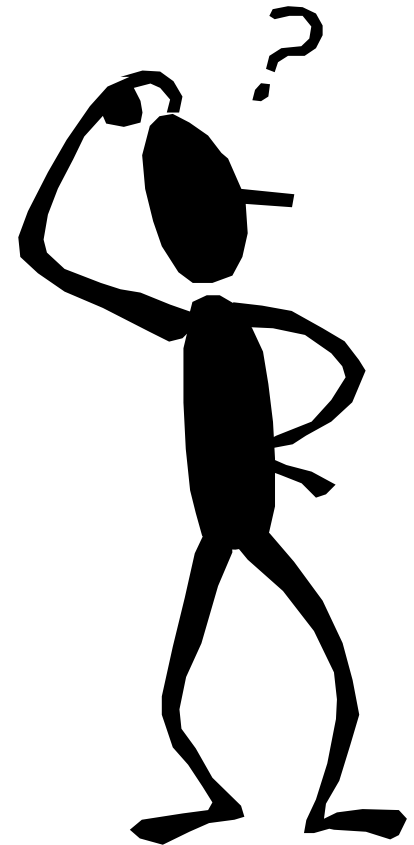
Neumann Boundary Conditions are imposed at the Artificial Boundaries and the Source and Drain contacts

# Can We Lower Self-Heating Effects?

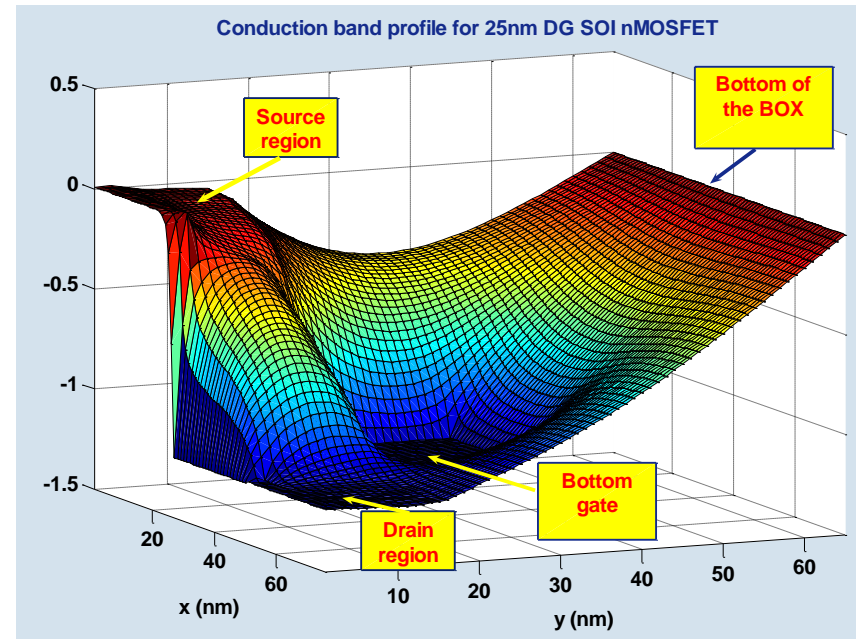
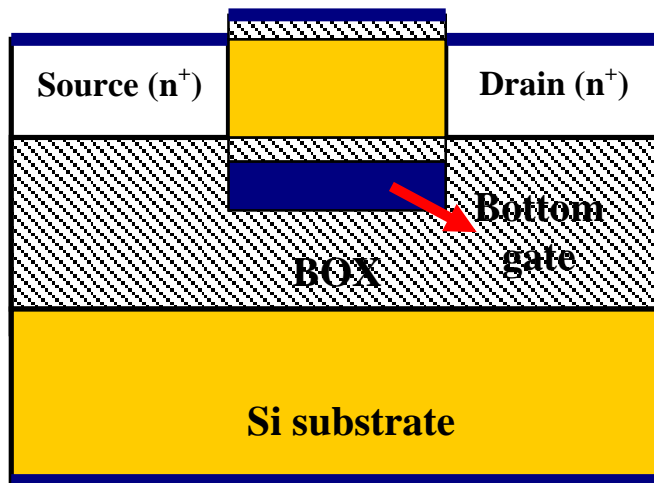
- Dual-Gate Devices
- SOI vs. SOD vs. SOAIN

S.M. Goodnick, D. Vasileska, K. Raleva, "Is Dual Gate Device Better From a Thermal Perspective?", *Proceedings of 2008 SISPAD Conference*, pp. 125 - 128.

K. Raleva, D. Vasileska, S. M. Goodnick, Is SOD Technology the Solution to Heating Problems in SOI Devices?, *Electron Device Letters, IEEE*, Volume 29, Issue 6, June 2008 Page(s):621 - 624.



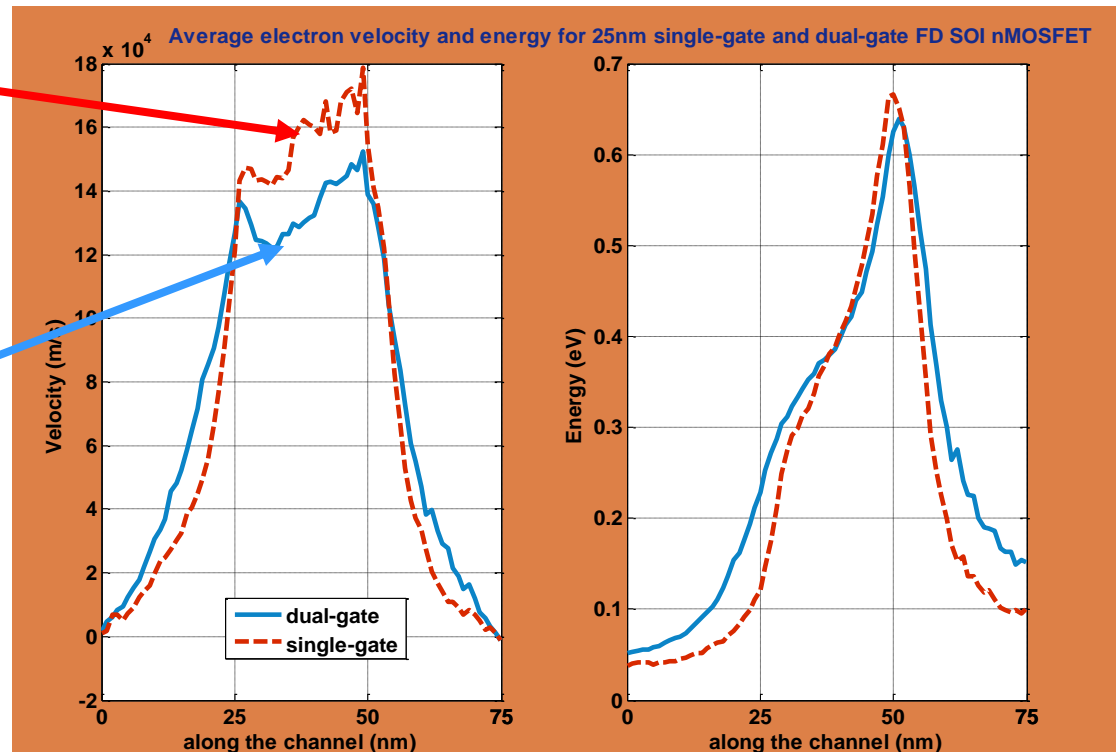
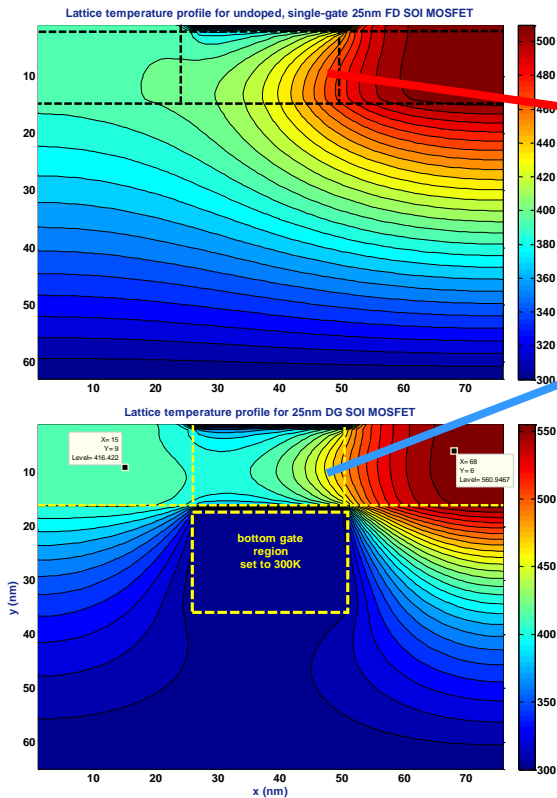
# Dual-Gate SOI Devices



S.M. Goodnick, D. Vasileska, K. Raleva, "Is Dual Gate Device Better From a Thermal Perspective?", *Proceedings of the 2008 SISPAD Conference*, pp. 125 - 128.

# A Closer Look ...

## Single gate lattice temperature profile



## Dual gate lattice temperature profile

# Where Does the Benefit of the DG Structure Come From?



For almost the same Current degradation DG devices offer **1.5-1.7** times more current

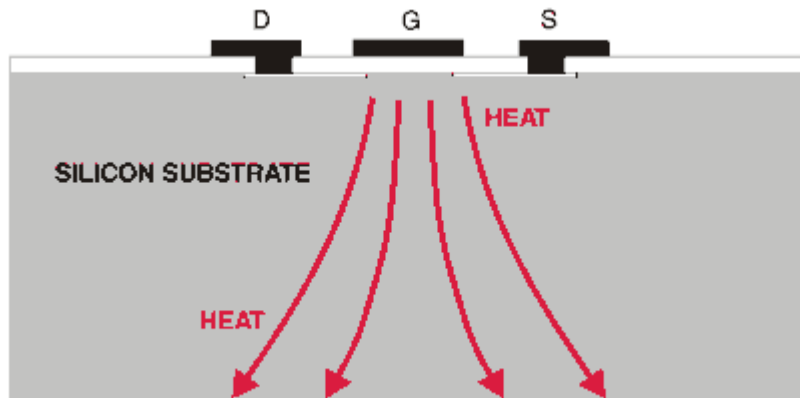
25nm FD SOI nMOSFET

Type of simulation	Gate temperature	Bottom of the BOX temperature	Current (mA/um)	Current decrease (%)
isothermal	300K	300K	1.9428	\
thermal	300K	300K	1.7644	<b>9.18</b>
thermal	400K	300K	1.6641	<b>14.35</b>
thermal	600K	300K	1.4995	<b>22.82</b>

25nm DG SOI nMOSFET

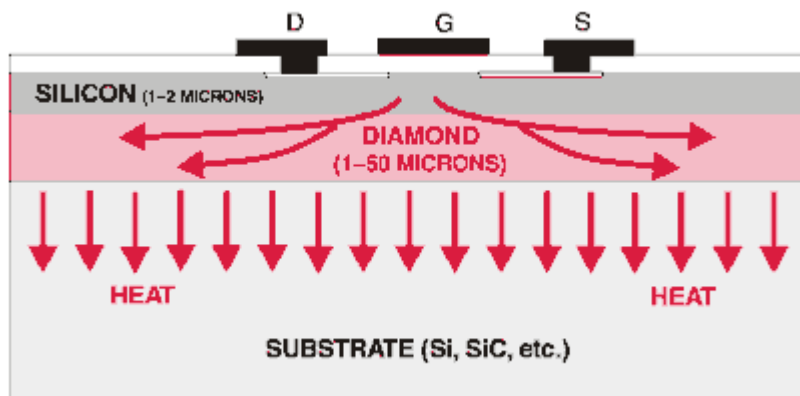
25nm DG SOI nMOSFET (Vgate-top=Vgate-bottom=1.2V; Vdrain=1.2V; Vsource=0V; Vsubstrate=0V)					
Type of simulation	Top gate temperature	Bottom gate temperature	Bottom of the BOX temperature	Current (mA/um)	Current decrease (%)
isothermal	300K	300K	300K	3.0682	\
thermal	300K	300K	300K	2.7882	<b>9.13</b>
thermal	400K	400K	300K	2.6274	<b>14.37</b>
thermal	600K	600K	300K	2.3153	<b>24.54</b>

# SOI vs. SOD vs. SOAIN



Silicon-On-Diamond and Silicon-On-Aluminum Nitride (SOAIN) Technologies as viable alternatives to Silicon-On-Insulator Devices

Standard Si technology



SOD technology

BOX Material	Dielectric constant	$K_{th}$ (W/mK)
SiO <sub>2</sub>	3.9	1.38
Diamond	5.68	2000
AlN	9.14	272

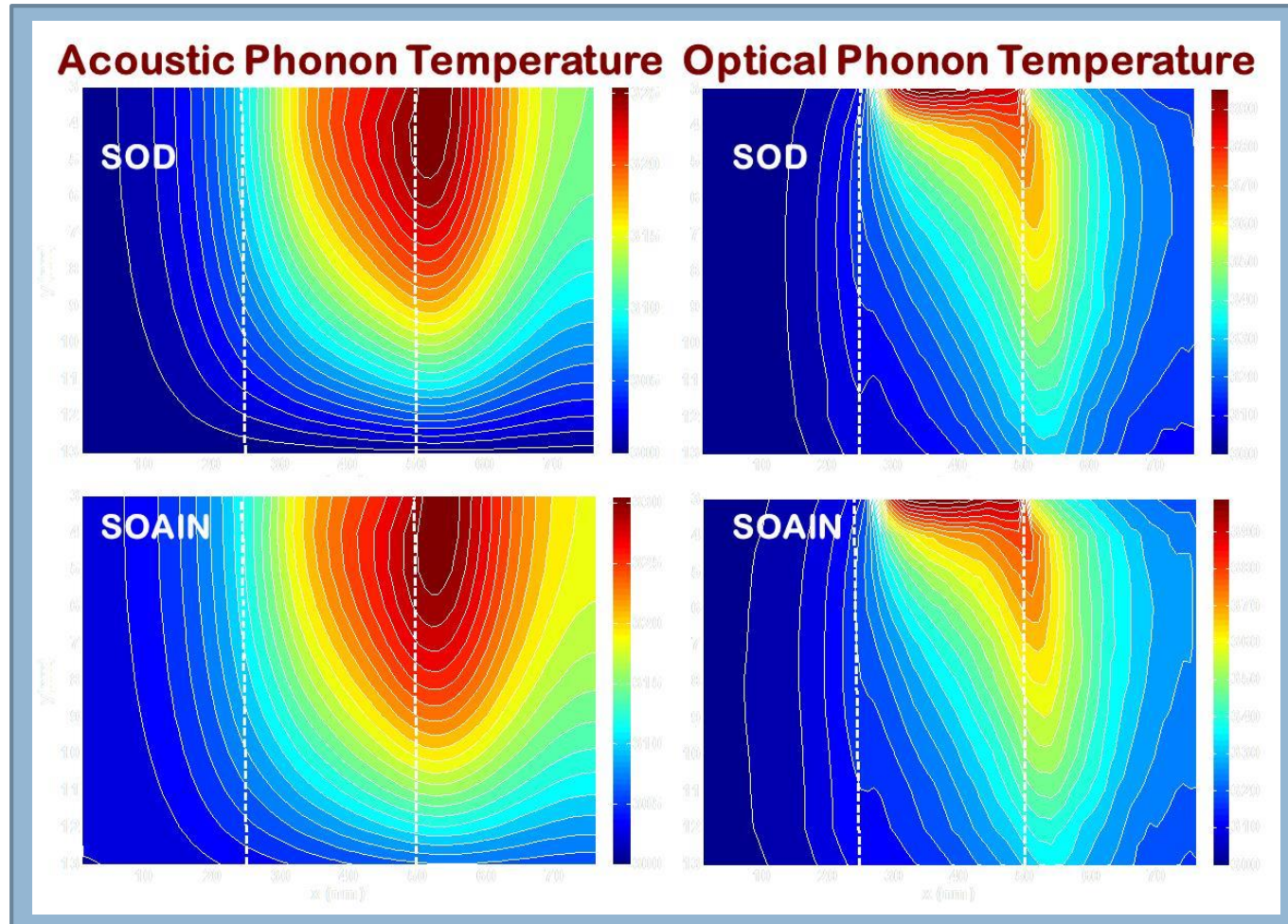
# Current Degradation

Device	Device width=3um (without substrate)			Device width=3um (with substrate)		
	Current (mA/um) isothermal	Average Current (mA/um) thermal	Current Decrease (%)	Current (mA/um) isothermal	Average Current (mA/um) thermal	Current Decrease (%)
SOI	1.82	1.70	7.05	1.82	1.70	7.05
SOAIN	1.85	1.82	1.55	1.88	1.84	2.18
SOD	1.84	1.81	1.41	1.84	1.82	1.08

K. Raleva, D. Vasileska, S. M. Goodnick, Is SOD Technology the Solution to Heating Problems in SOI Devices?, Electron Device Letters, IEEE, Volume 29, Issue 6, June 2008 Page(s):621 - 624.



# Heat Spreading



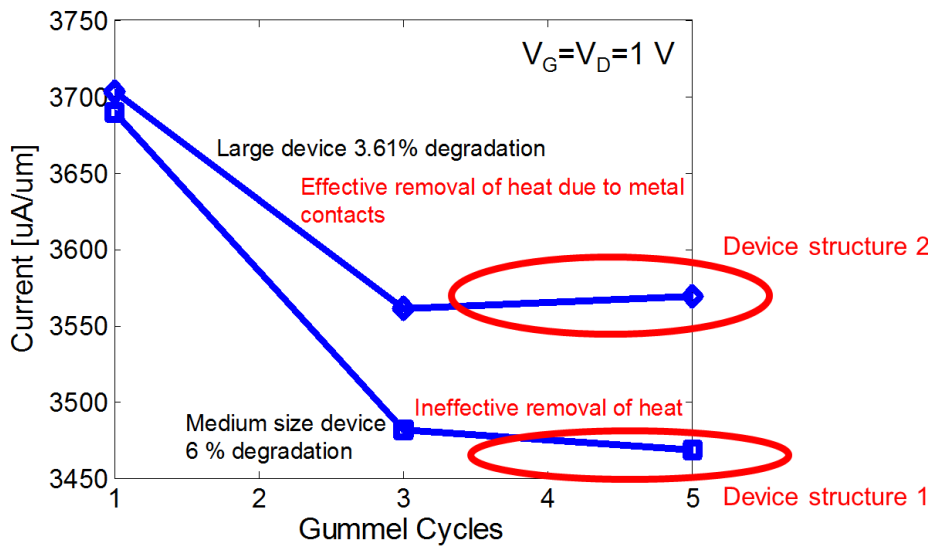


# NANOWIRE TRANSISTORS

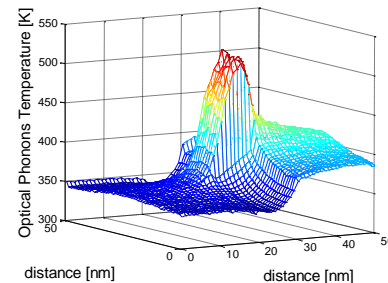
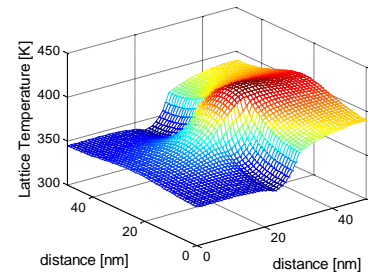
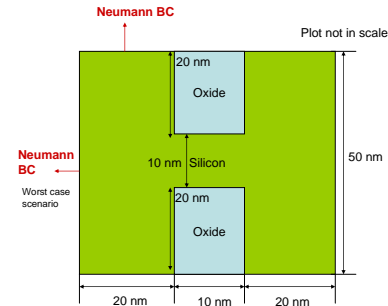
Lake Powell, Arizona

# Nanowires – The Role of the Contacts

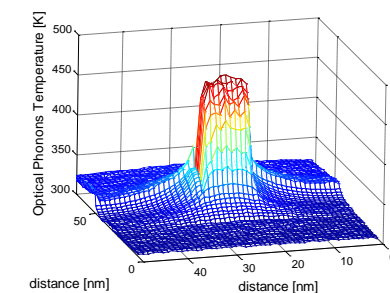
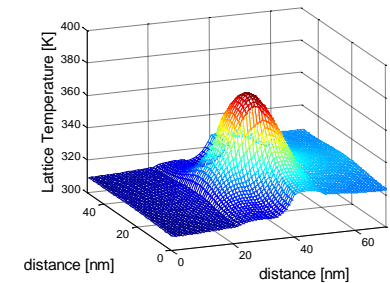
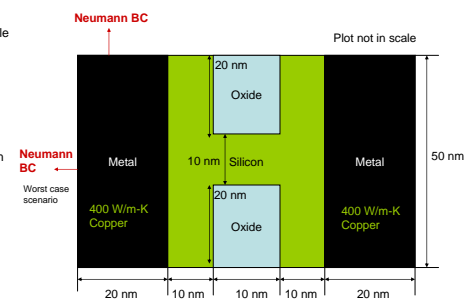
Convergence plot



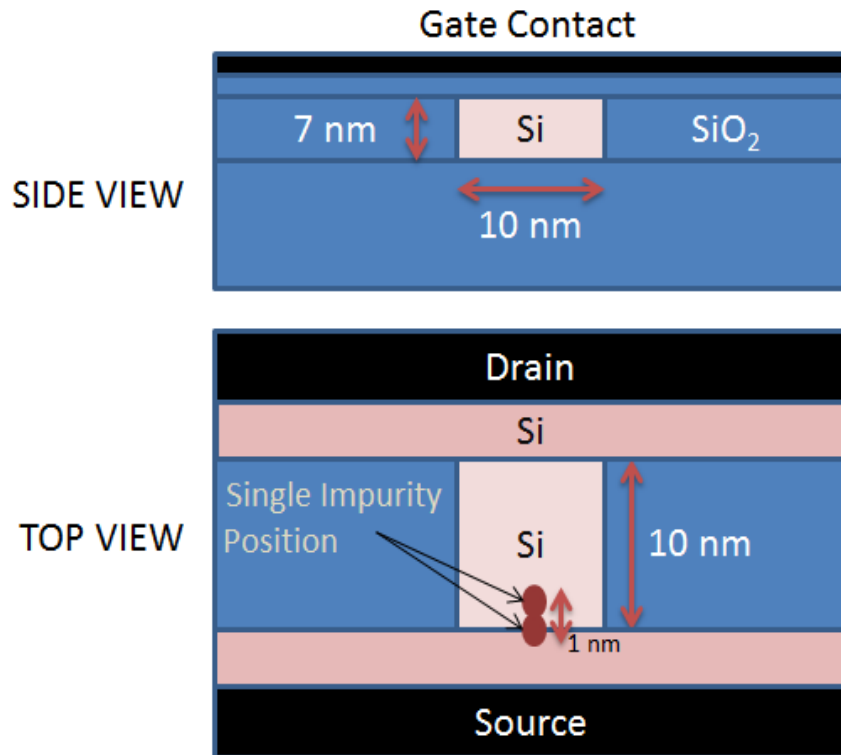
20 nm long contact + without metal nodes



30 nm long contact + with metal nodes



# Nanowires – Unintentional Dopant



## SINGLE IMPURITY IMPACT

GUMMEL CYCLE	No impurity case [ $\mu\text{A}/\mu\text{A}$ ]	Source Edge [ $\mu\text{A}/\mu\text{A}$ ]	1 nm Towards Drain [ $\mu\text{A}/\mu\text{A}$ ]
1	4154	4122	4075
3	4068	4030	3974
5	4052	4035	3968
<b>Degradation</b>	N/A	0.47%	2.12%

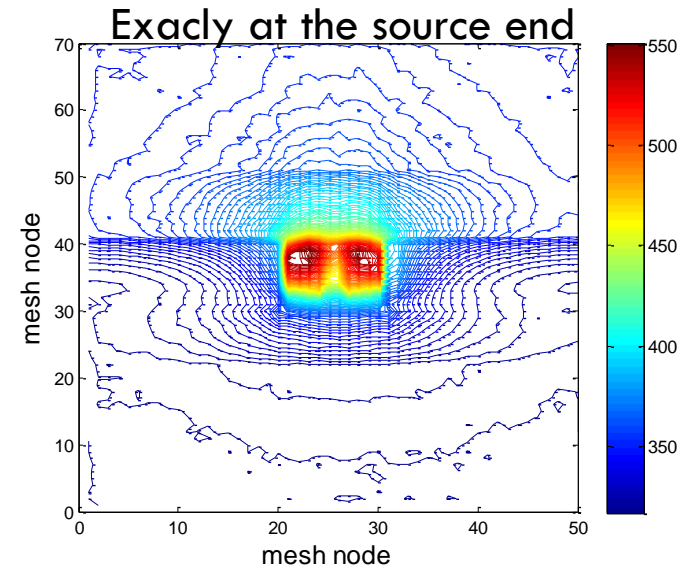
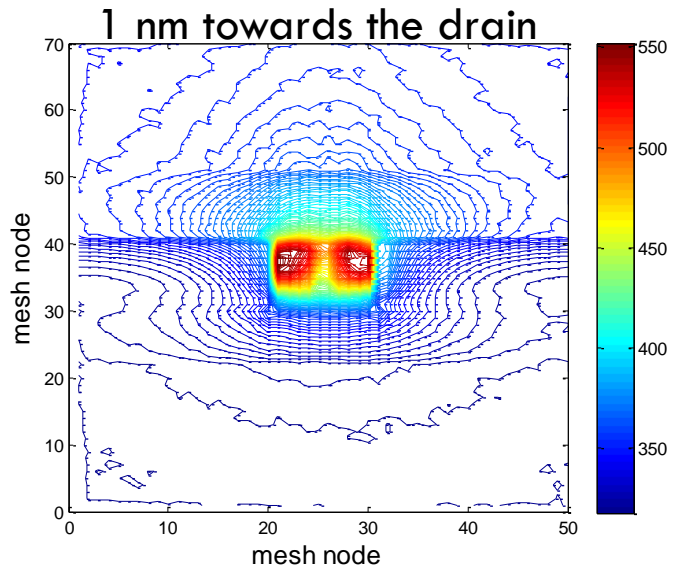
Screening of the source charges  
Reduces the impact of the negative trap.

Maximal impact

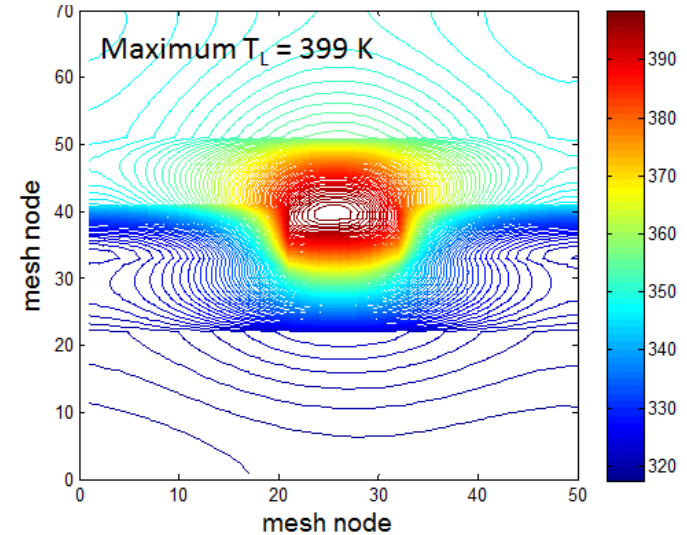
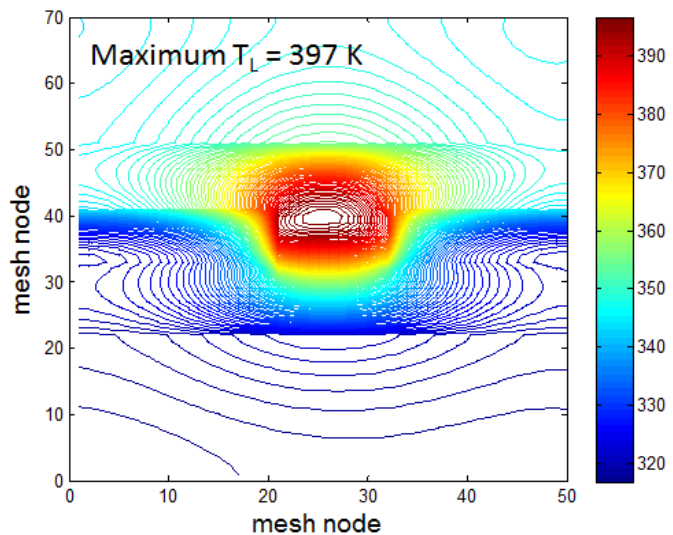


# Unintentional Dopant

optical



acoustic

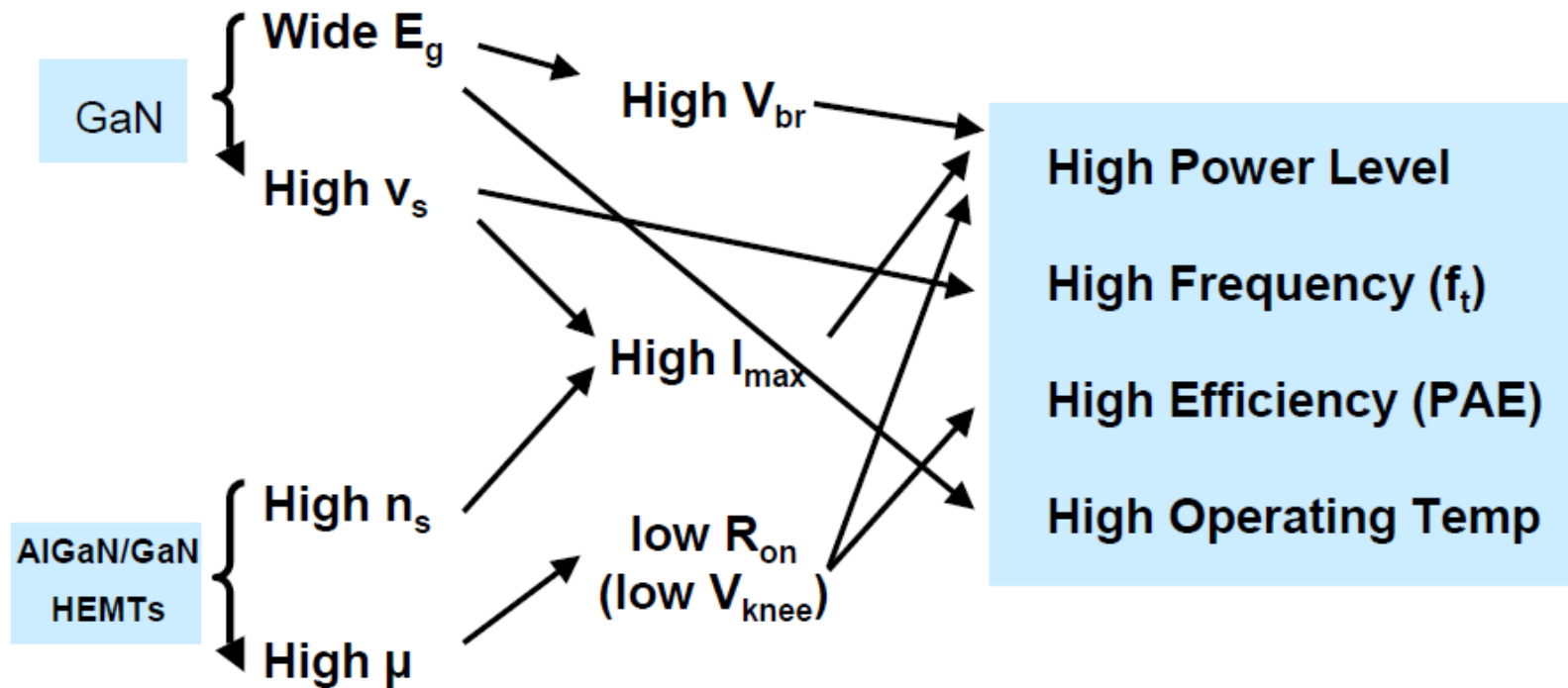




# GaN HEMTS

Rainbow Bridge, Arizona

# Why GaN HEMTs?

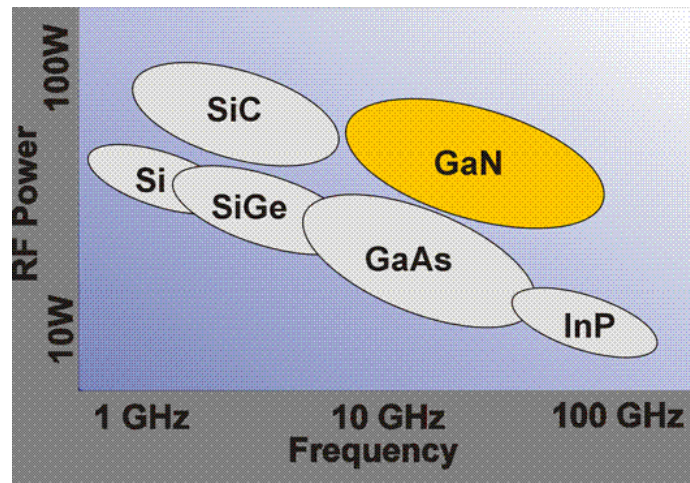


**Promising Microwave Power Device**



# Simulation Results: GaN HEMTs

## □ Why GaN HEMTs?

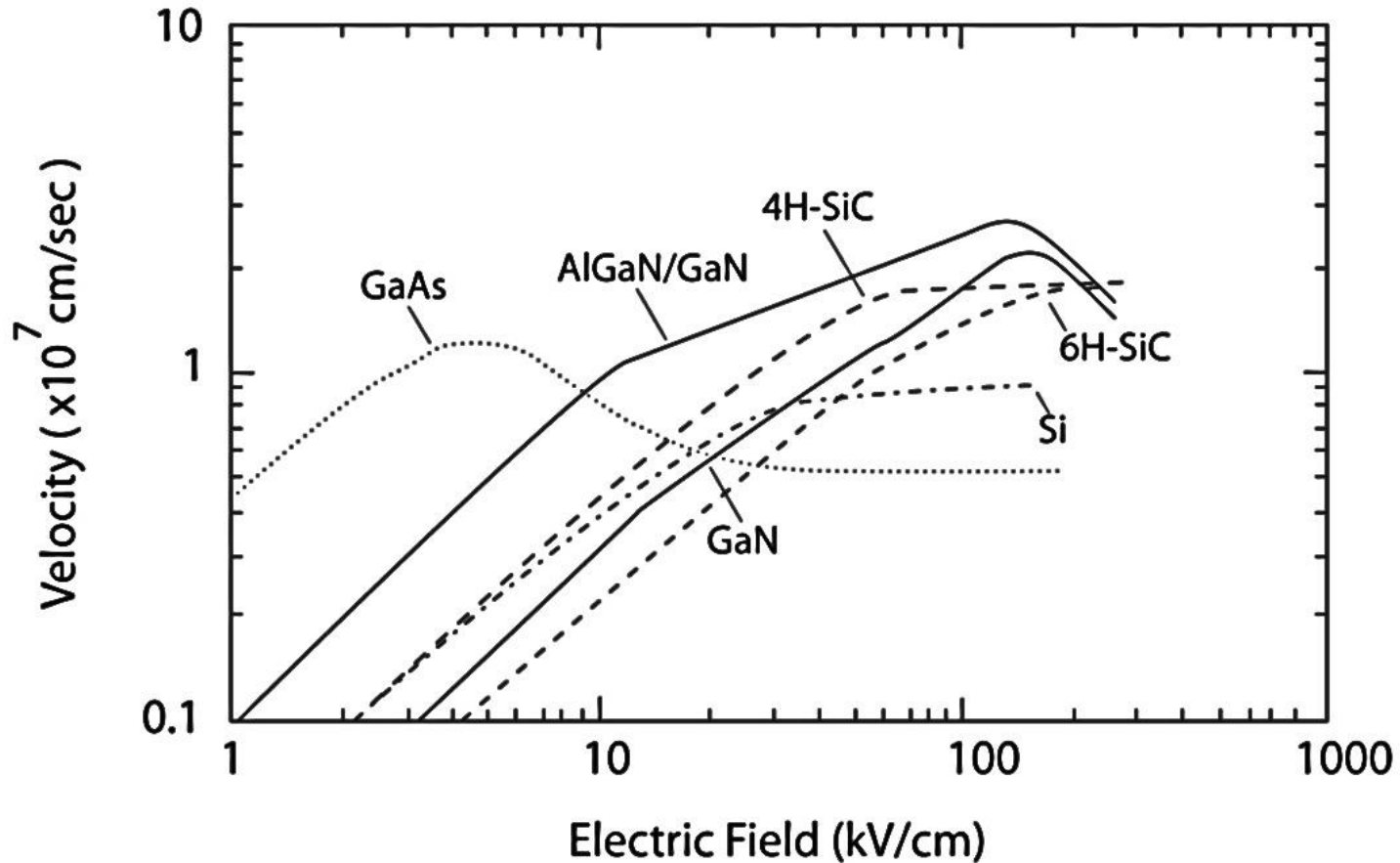


## ● Where Gallium Nitride Outstrips Other Semiconductor Materials

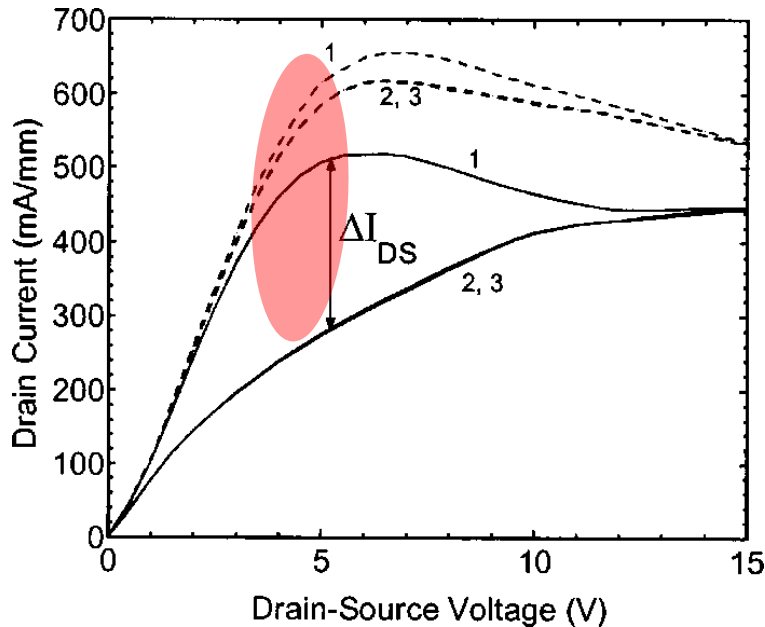
Semiconductor (commonly used compounds)		Silicon	Gallium arsenide (AlGaAs/InGaAs)	Indium phosphide (InAlAs/InGaAs) <sup>a</sup>	Silicon carbide	Gallium nitride (AlGaN/GaN)
Characteristic	Unit					
Bandgap	eV	1.1	1.42	1.35	3.26	3.49
Electron mobility at 300 K	cm <sup>2</sup> /Vs	1500	8500	5400	700	1000-2000
Saturated (peak) electron velocity	X10 <sup>7</sup> cm/s	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	2.0 (2.0)	1.3 (2.1)
Critical breakdown field	MV/cm	0.3	0.4	0.5	3.0	3.0
Thermal conductivity	W/cm•K	1.5	0.5	0.7	4.5	>1.5
Relative dielectric constant	ε <sub>r</sub>	11.8	12.8	12.5	10.0	9.0

<sup>a</sup> The compounds are loosely known as indium-based.

# GaN HEMTs ...

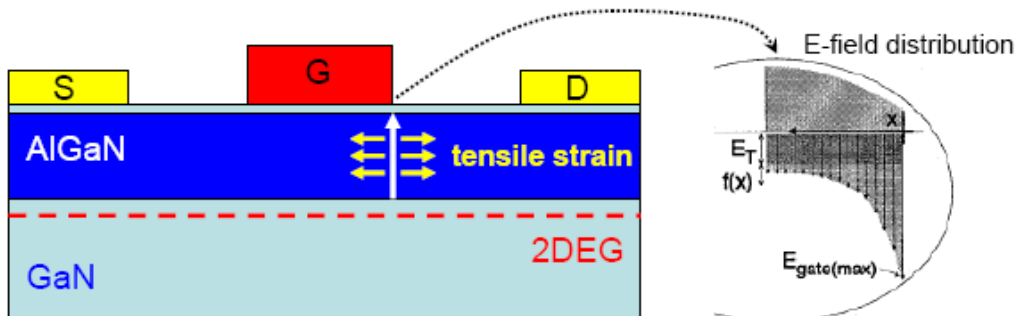


# Problems With GaN HEMTs



**Current Collapse induced in GaN HEMT device characteristics as a result of short-term ( $\sim 10$  hours) DC bias stress.**

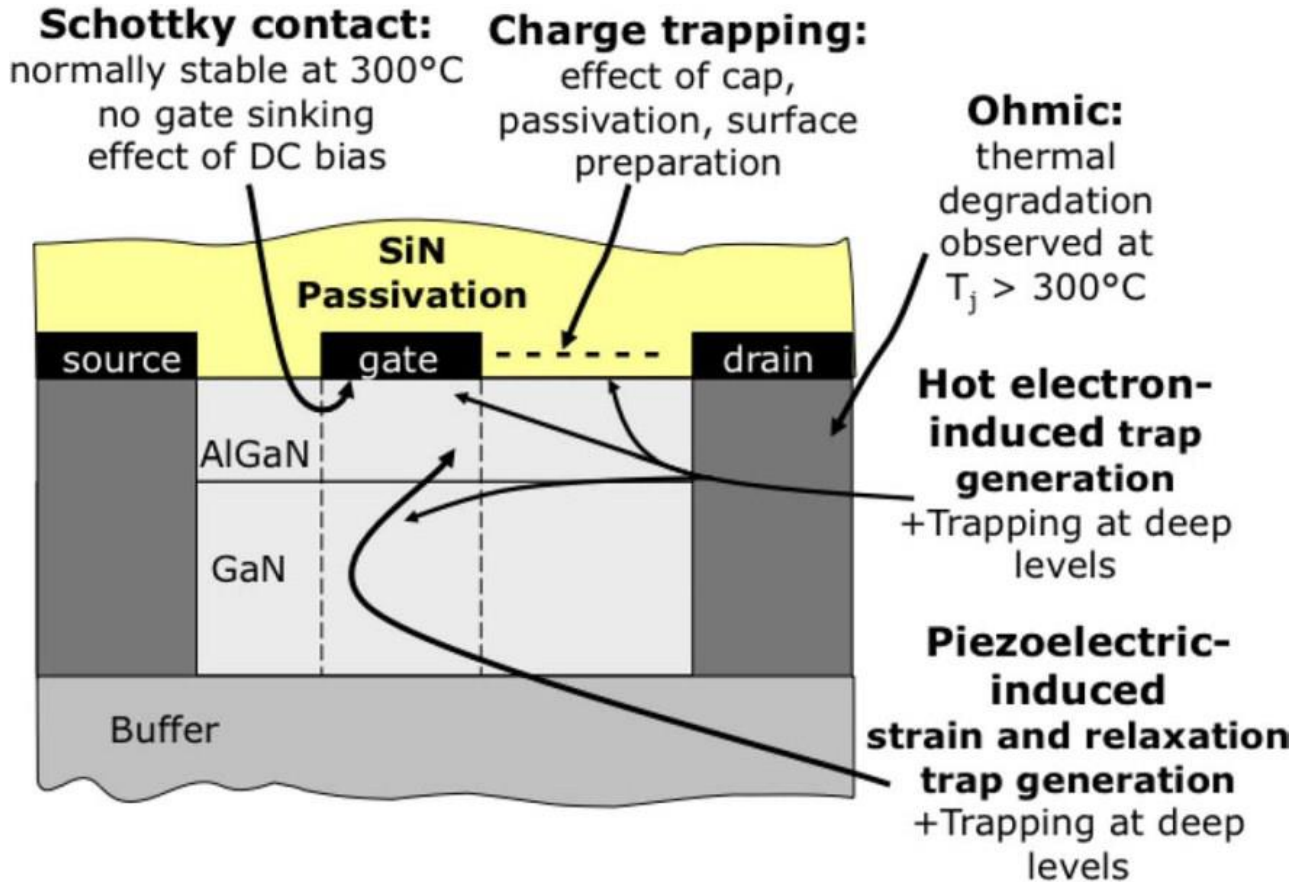
Trapping of hot electrons by trap/defect sites in the AlGaN buffer layer as well as GaN substrate reduces the net polarization charge.



J. A. del Alamo and J. Joh, GaN HEMT reliability, Microelectronics Reliability, Volume 49, Issues 9-11, September-November 2009, Pages 1200-1206.

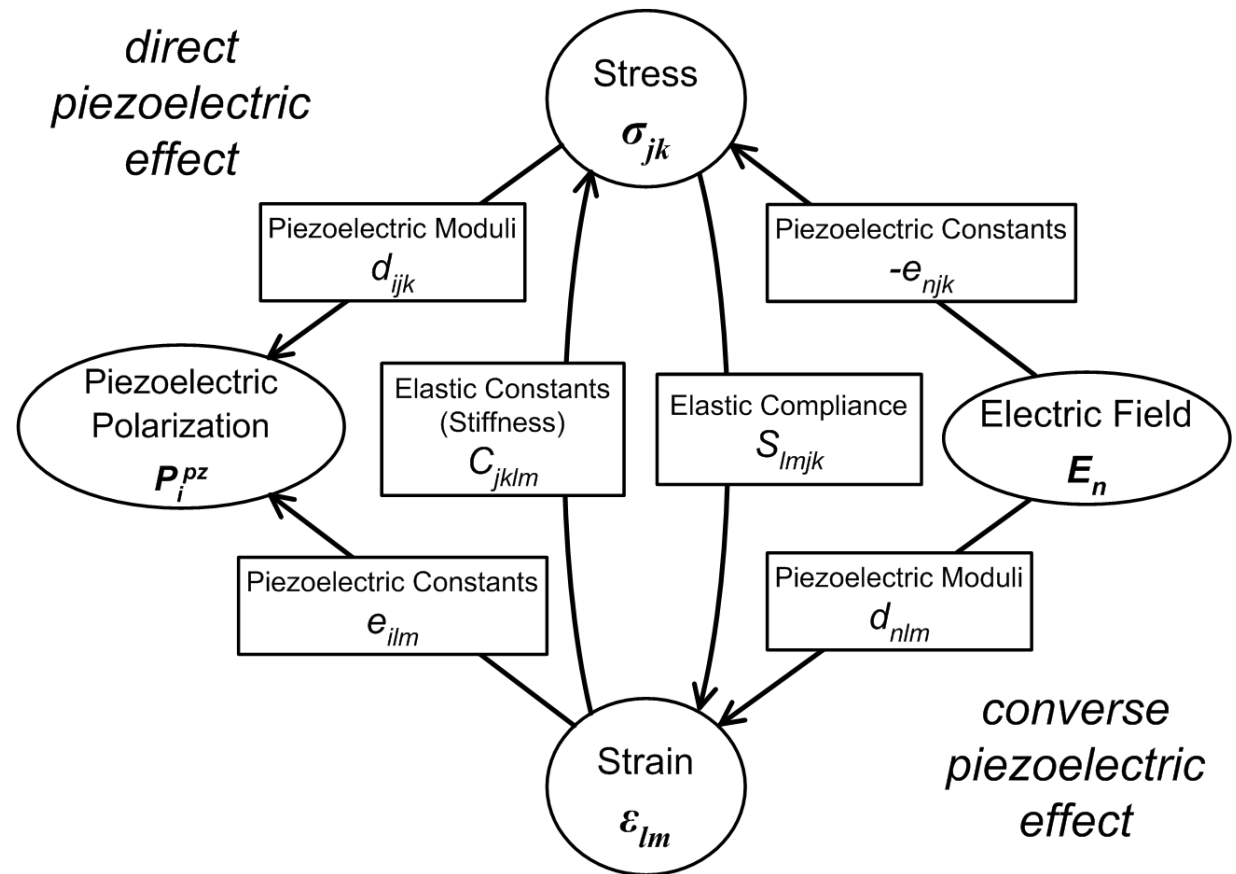


# Problems With GaN HEMTs ...



# MODELING REQUIREMENTS

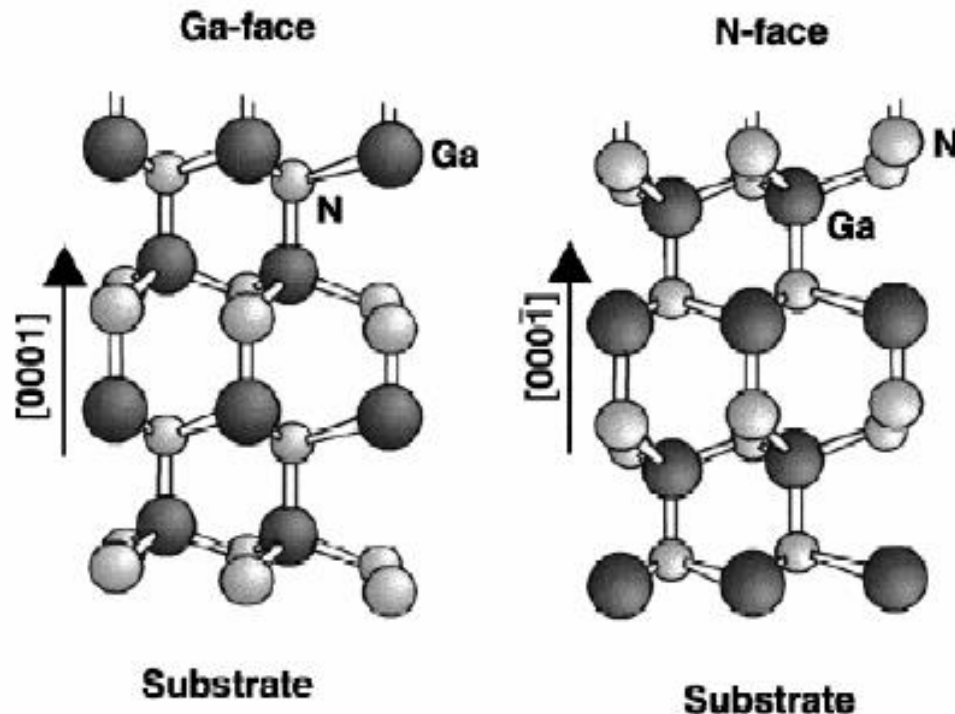
## INCORPORATION OF ELECTROMECHANICAL COUPLING



## SELF-HEATING EFFECT

# GaN HEMTs Basics

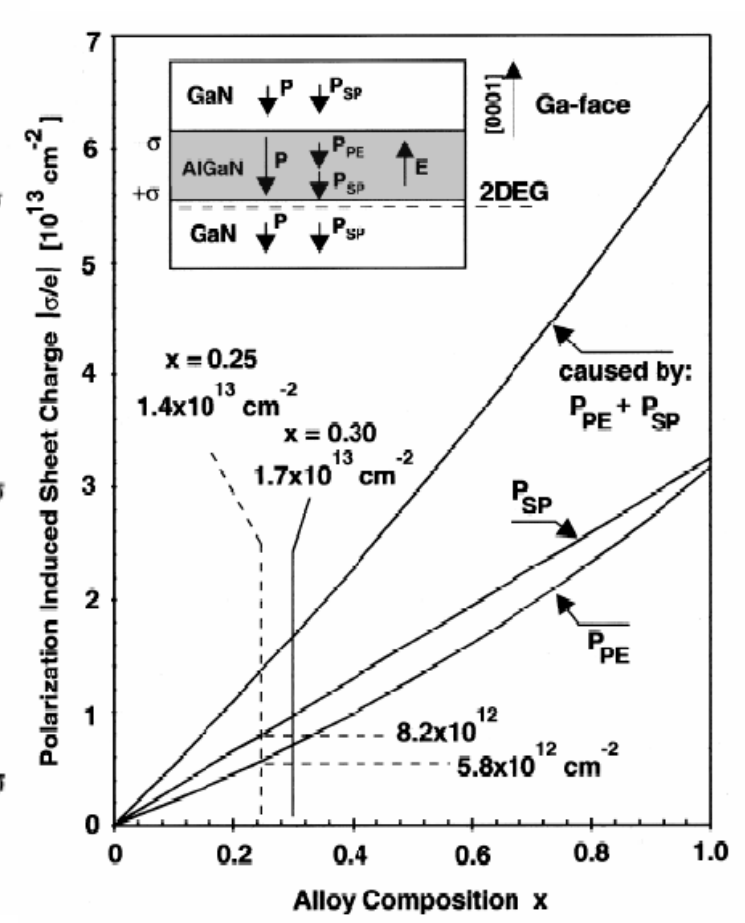
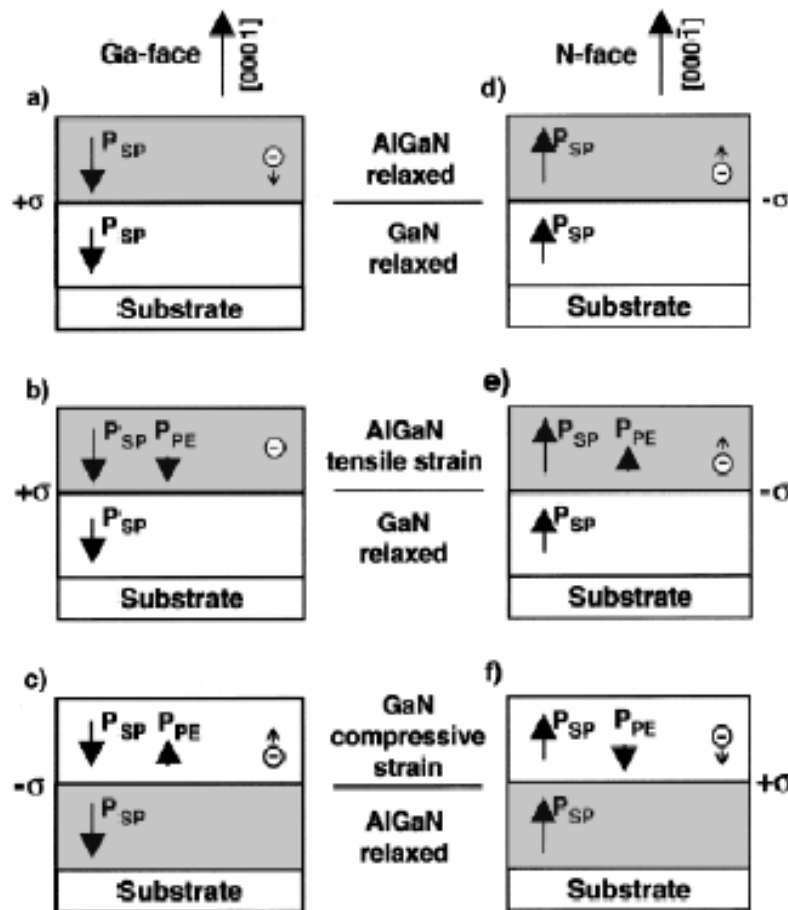
## □ Wurtzite AlGaN/GaN



AlGaN/GaN grown on sapphire by MOCVD is always Ga-faced, but material grown by MBE can have either Ga- or N-faced surface depending on the existence of AlN nucleation layer.

# GaN HEMTs Basics ...

## □ Spontaneous and Piezoelectric Polarization Charge

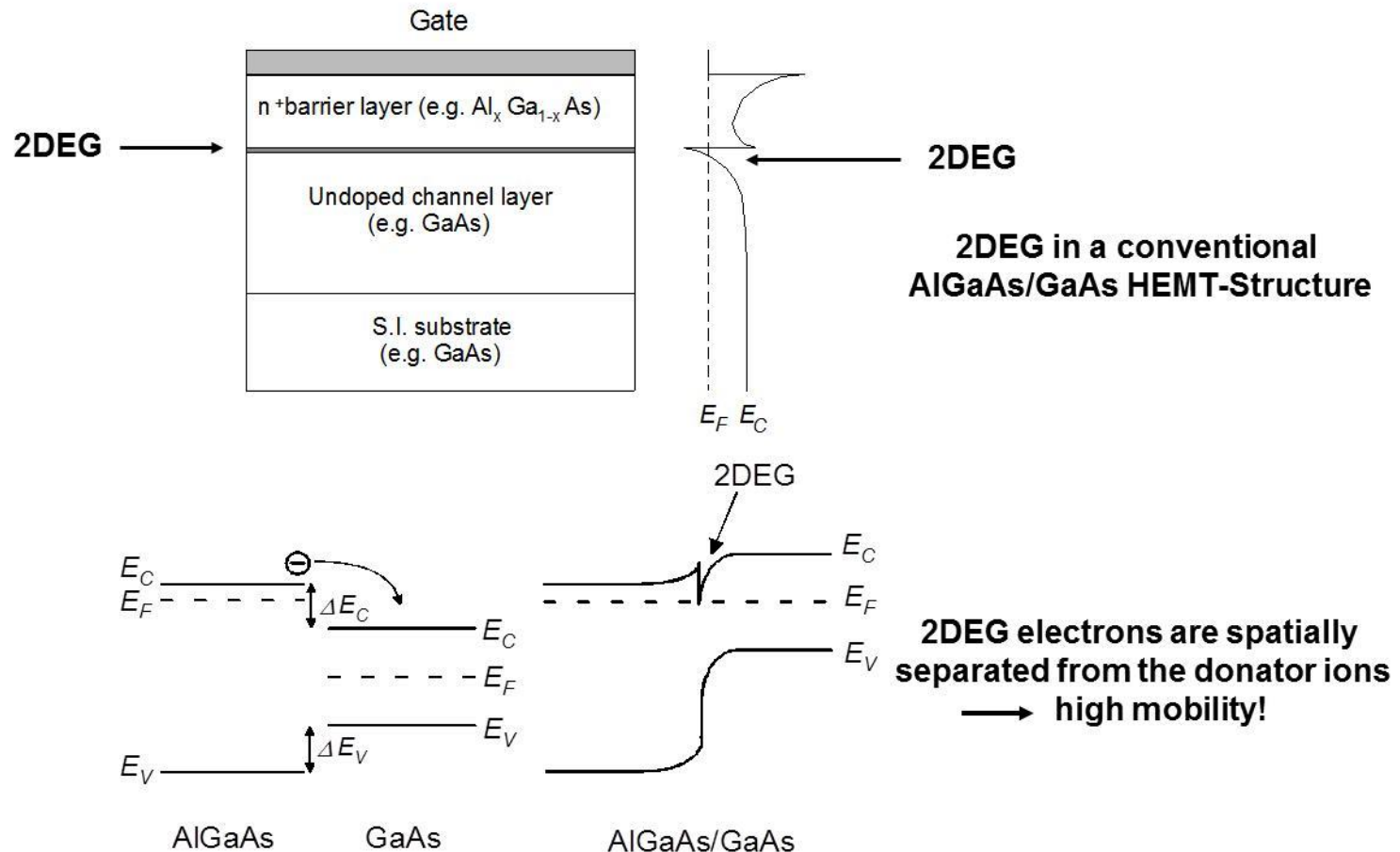




# GaN HEMTs ...

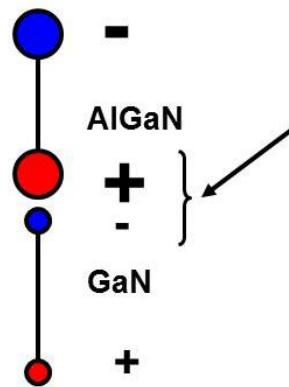
## Comparison to GaAs devices

### Two-Dimensional Electron Gas - 2DEG



# GaN HEMTs ...

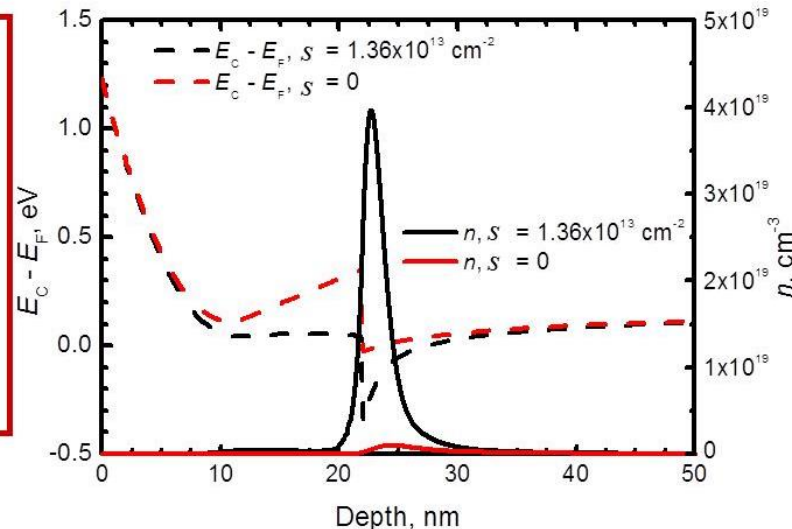
## □ What is different in GaN HEMTs ...



At the AlGaN/GaN interface occurs a positive net charge  $+\sigma$  leading to the formation of a 2DEG in the GaN.

**Two important messages:**

- Only a small portion of the 2DEG electrons is caused by the barrier doping !
- Even without any doping very high 2DEG sheet concentrations are possible!



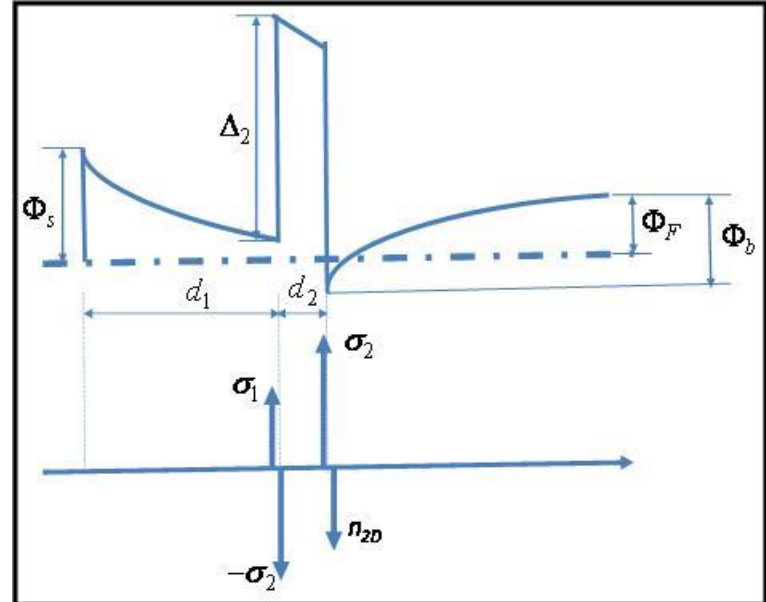


# Electro-mechanical coupling model developed at ASU

Model implemented in Synopsys Sentaurus simulation software.

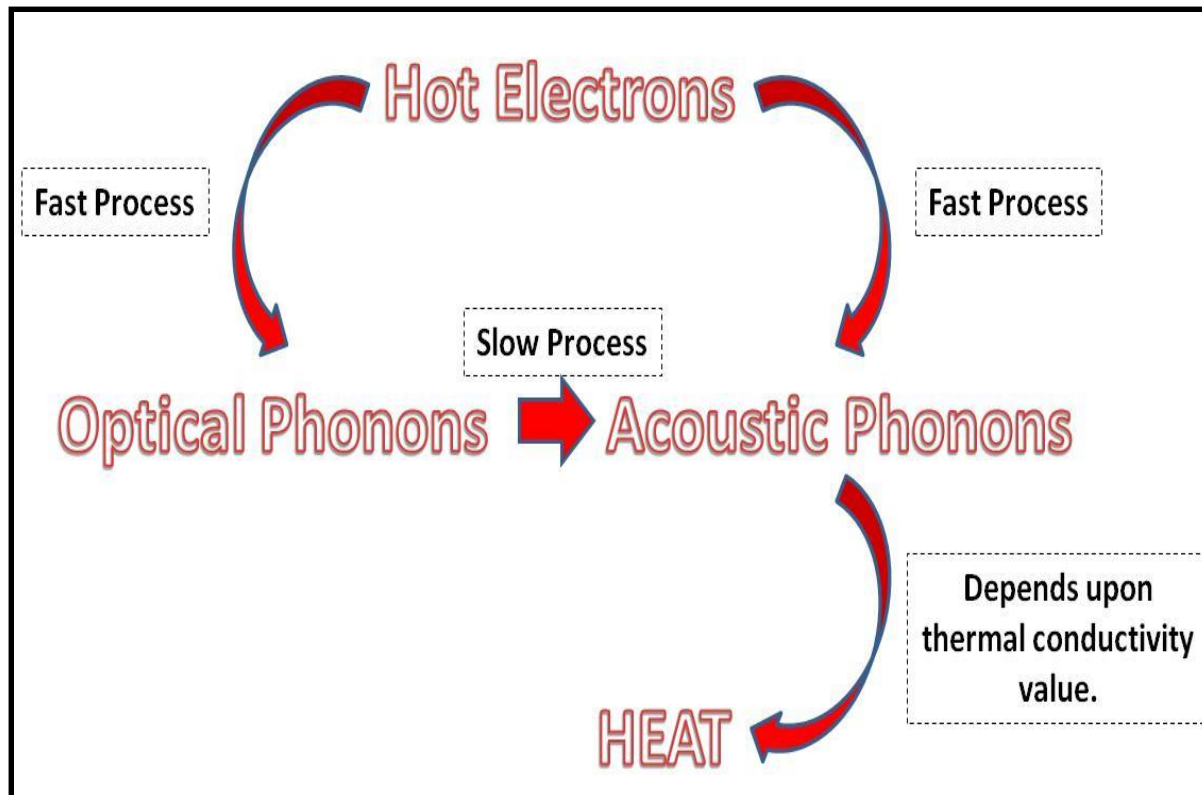
Basic idea of the method:

$$P_{PE}^{\alpha} = 2\Xi_x^{\alpha} \left( e_{31}^{\alpha} - \frac{c_{13}^{\alpha}}{c_{33}^{\alpha}} e_{33}^{\alpha} \right) + E_z^{\alpha} \frac{e_{33}^{\alpha 2}}{c_{33}^{\alpha}}$$



# Energy relaxation processes

## Acoustic and optical phonon bath

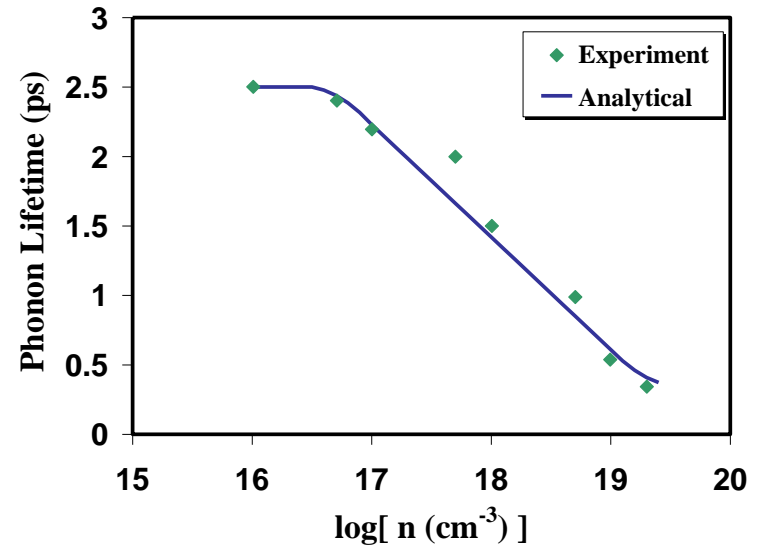


# Energy balance Equation Solver for Phonons

**Depends on  $n(i,j)$**

$$C_{LO} \frac{\partial T_{LO}}{\partial t} = \frac{3nk_B}{2} \left( \frac{T_e - T_L}{\tau_{e-LO}} \right) + \frac{nm^* v_d^2}{2\tau_{e-LO}} - C_{LO} \left( \frac{T_{LO} - T_A}{\tau_{LO-A}} \right),$$

$$C_A \frac{\partial T_A}{\partial t} = \nabla \cdot (k_A \nabla T_A) + C_{LO} \left( \frac{T_{LO} - T_A}{\tau_{LO-A}} \right) + \frac{3nk_B}{2} \left( \frac{T_e - T_L}{\tau_{e-L}} \right).$$



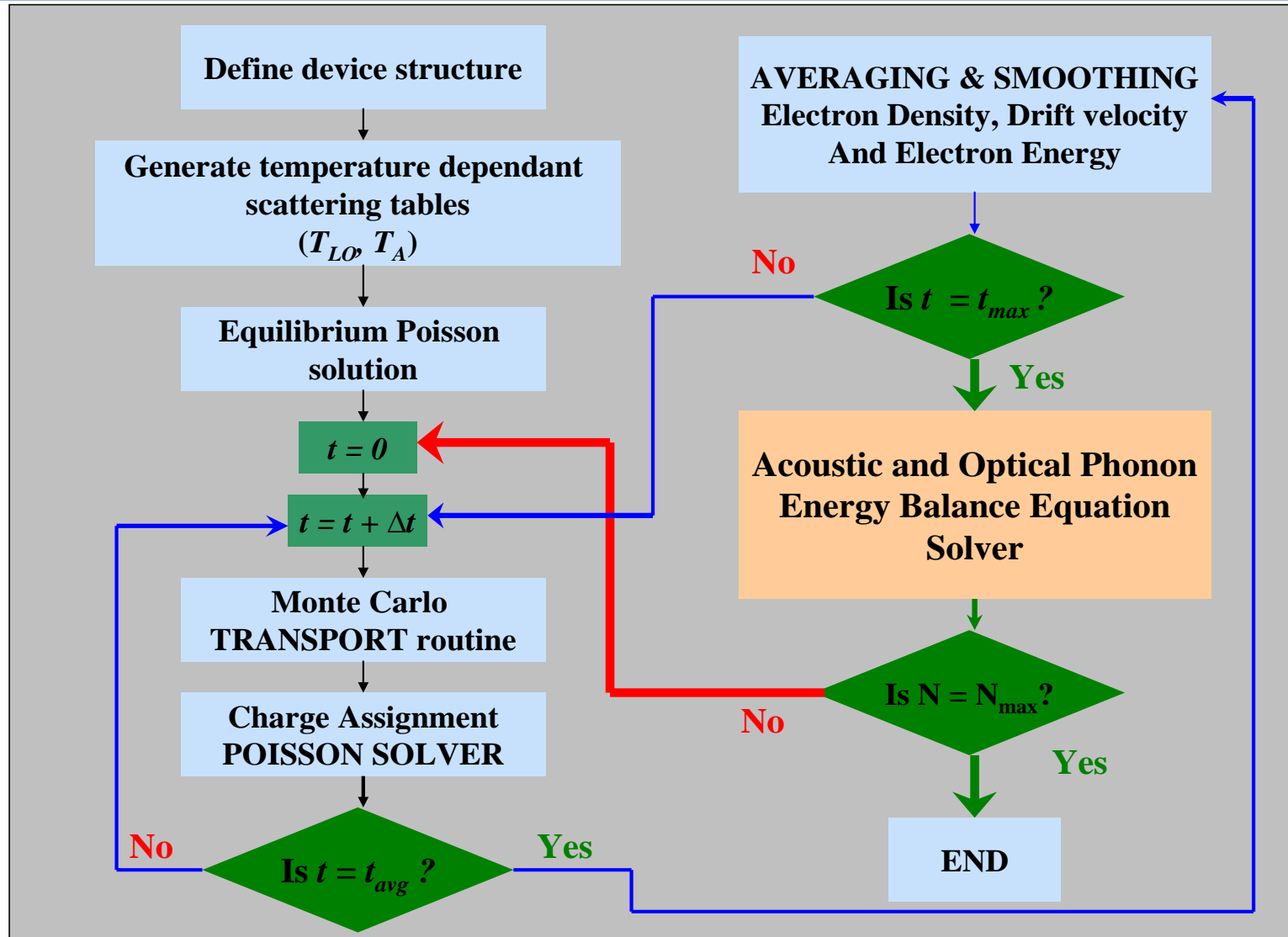
Carrier density dependent phonon lifetime,  $\tau_{LO}$

**Optical Phonon Lifetime  $\rightarrow$  function of carrier density  $n(i,j)$**

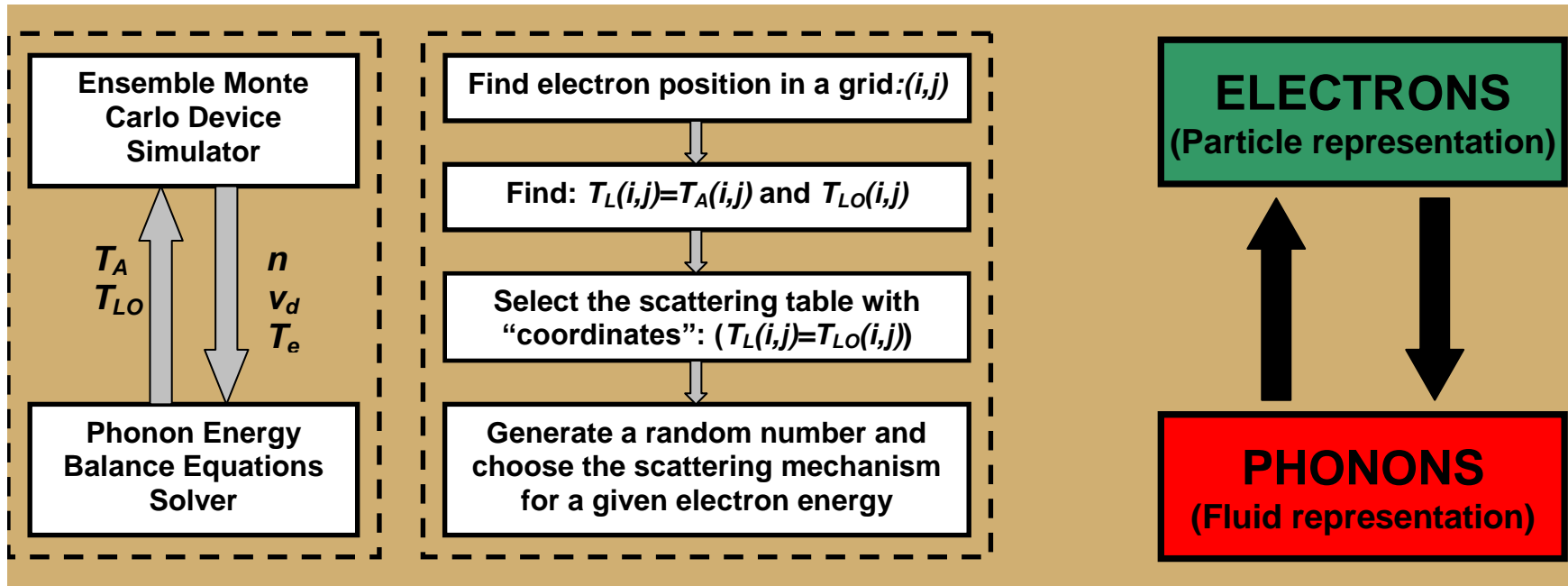
**Carrier density dependant phonon lifetimes results in an indirect dependence of the choice of SCATTERING MECHANISM on the CARRIER DENSITIES**



# Flow-chart of Electro-thermal simulator



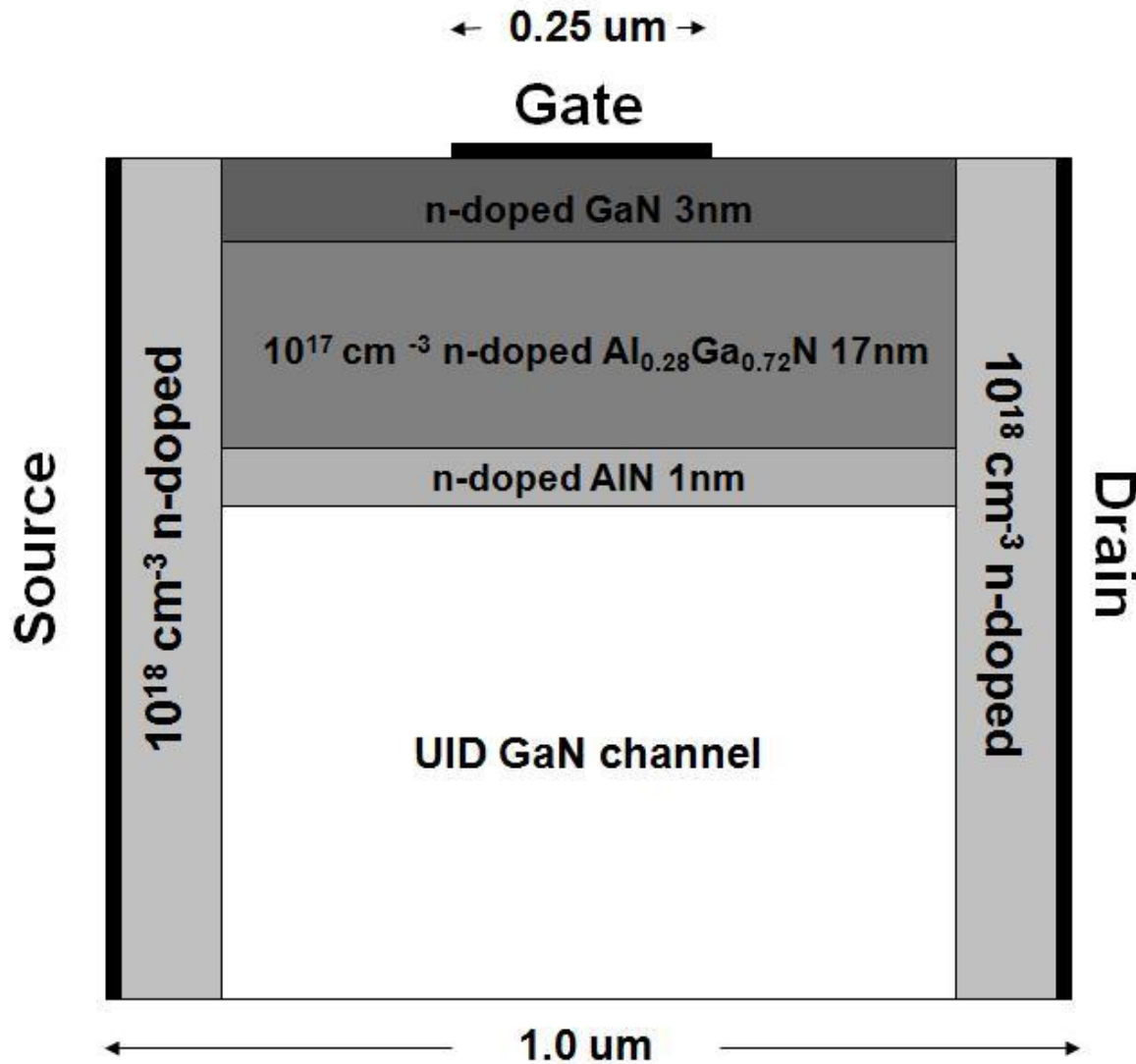
# Exchange of variables between solvers



## Modifications to our existing Monte Carlo Simulator

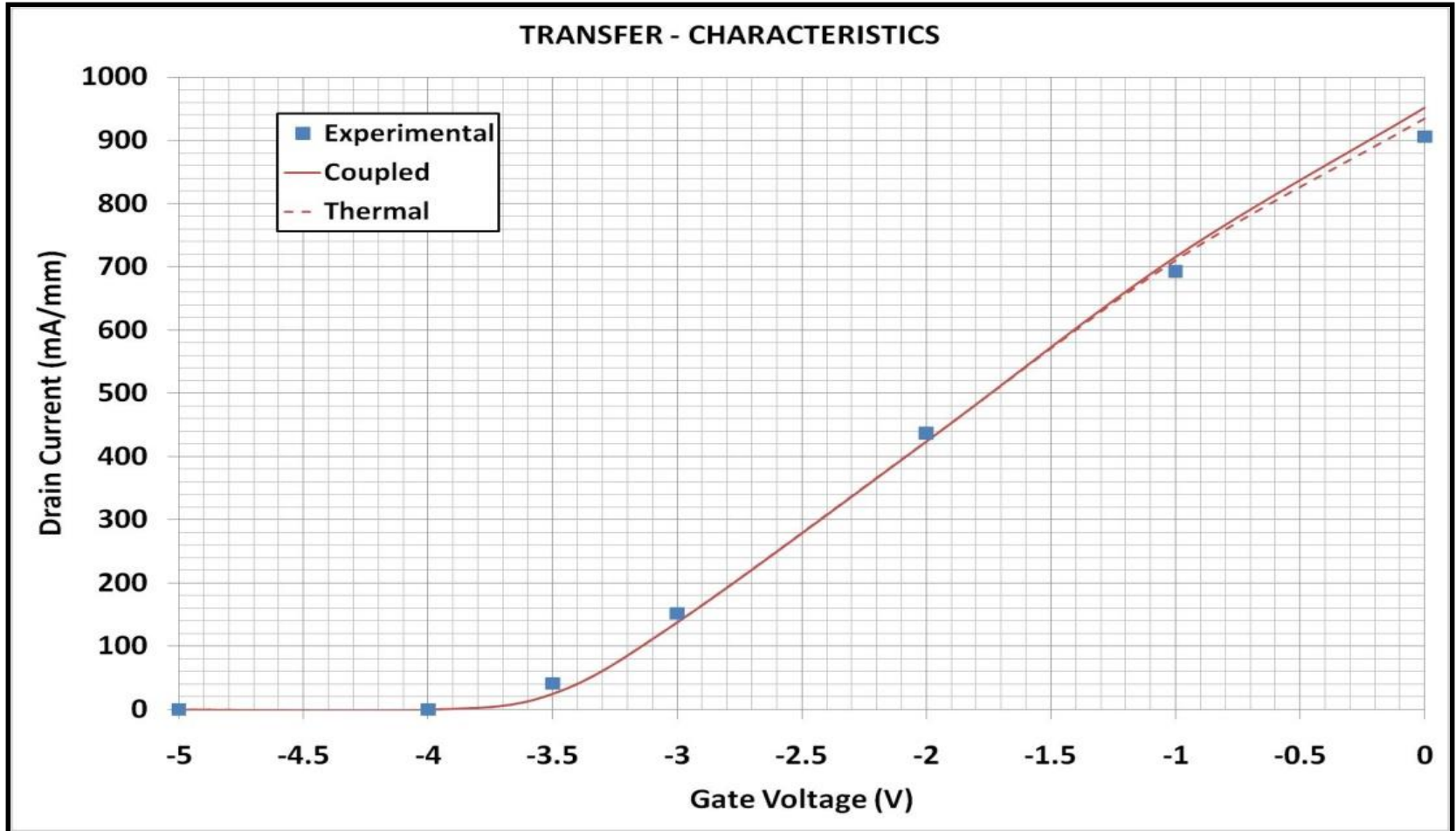
- Temperature dependent Scattering Tables.
- Averaging and smoothing of electron density, drift velocity and electron energy for solving phonon balance equations.
- Density dependent phonon lifetimes – analytical model fitted to experimental values.

# Simulated structure

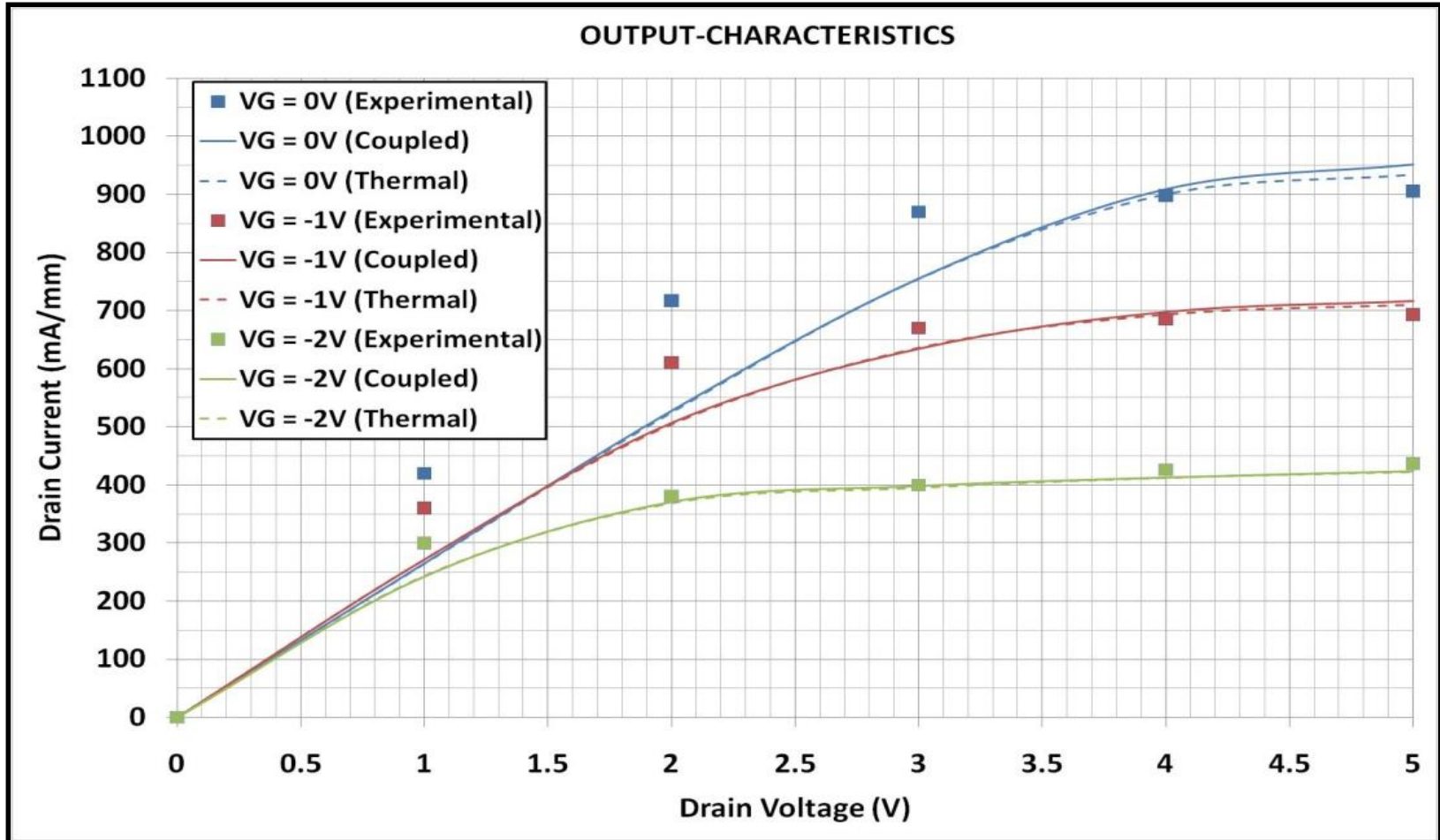


J. A. del Alamo  
structure

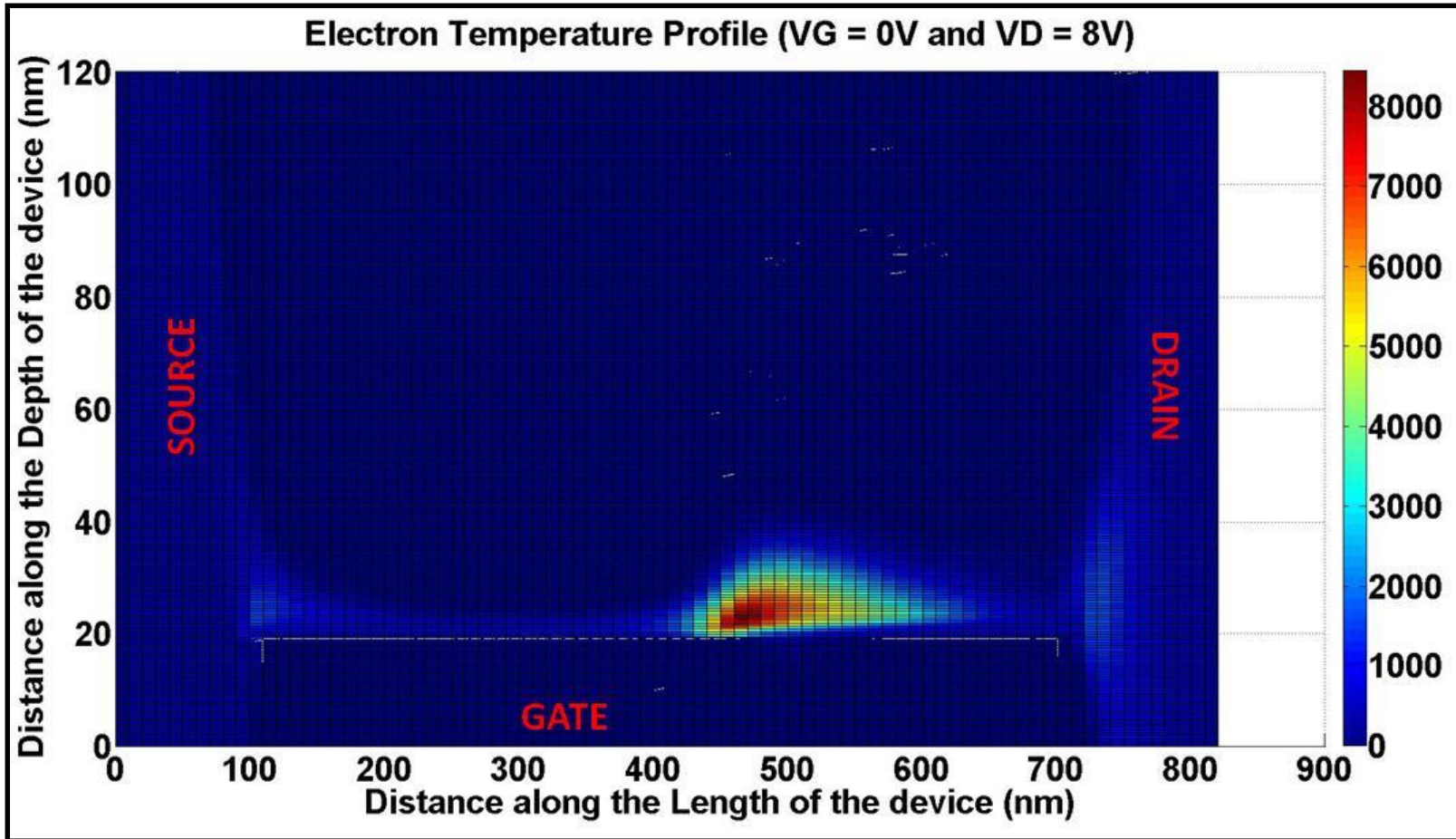
# $I_d$ - $V_G$ Characteristic



# $I_d$ - $V_d$ characteristic

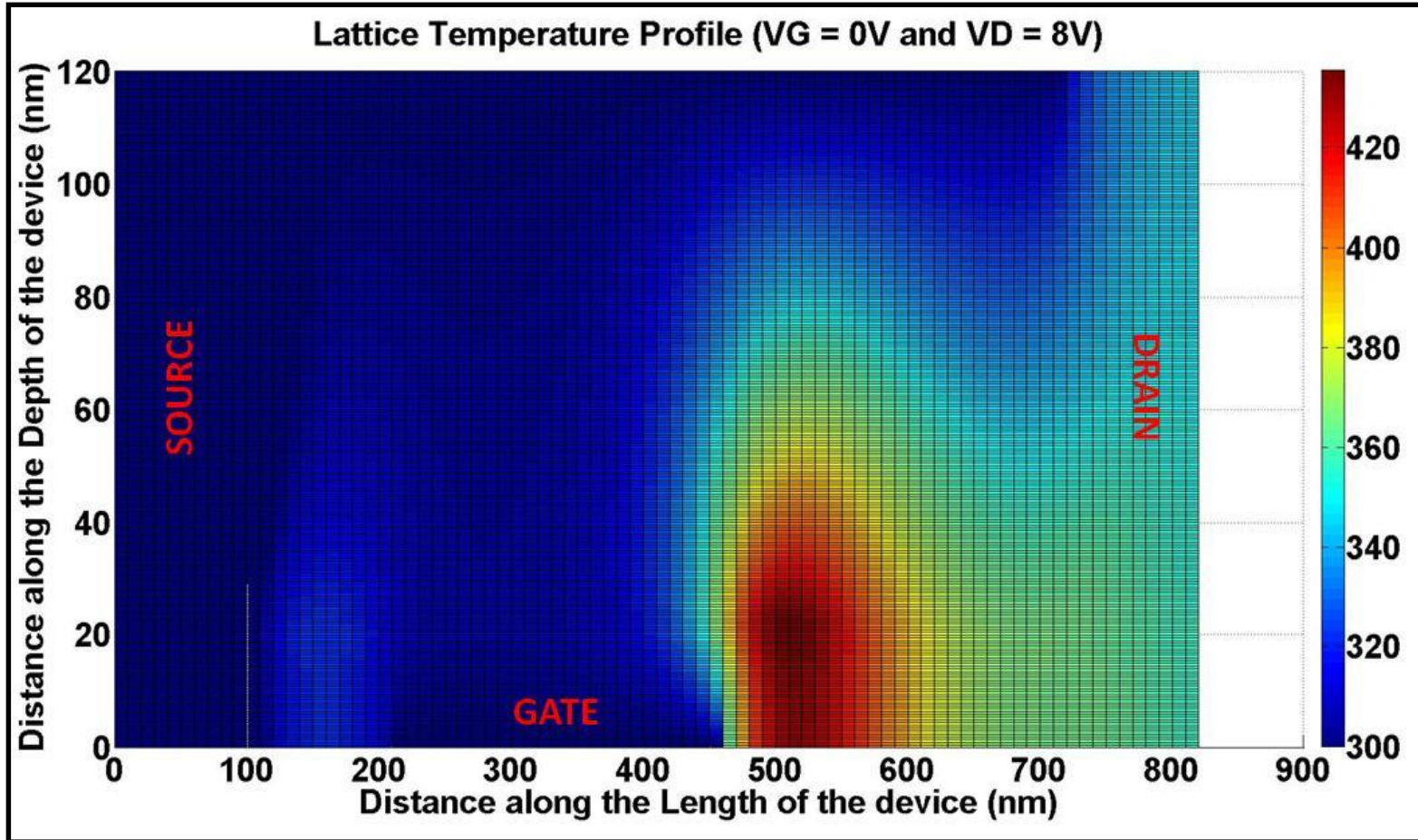


# Electron temperature map

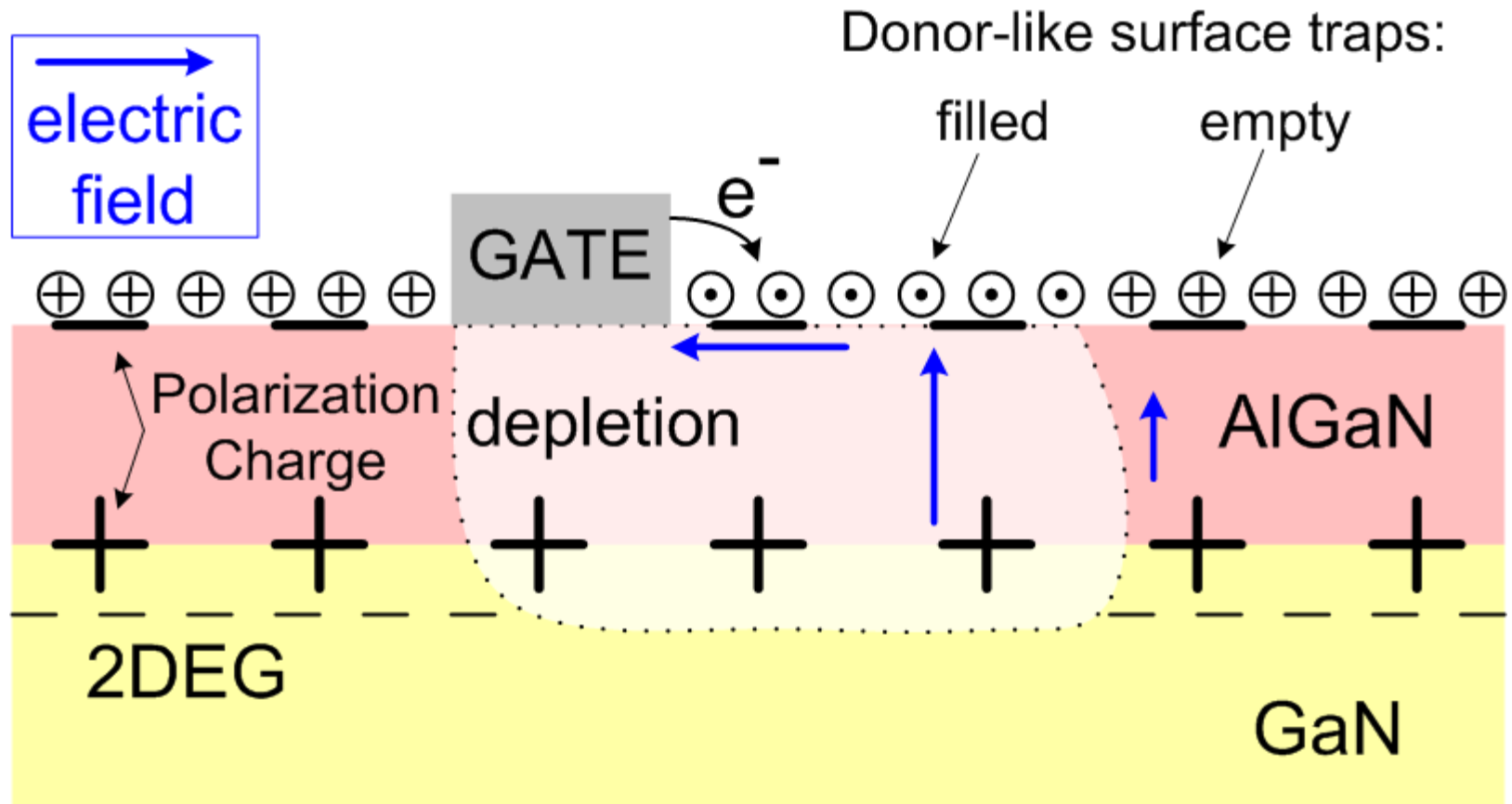




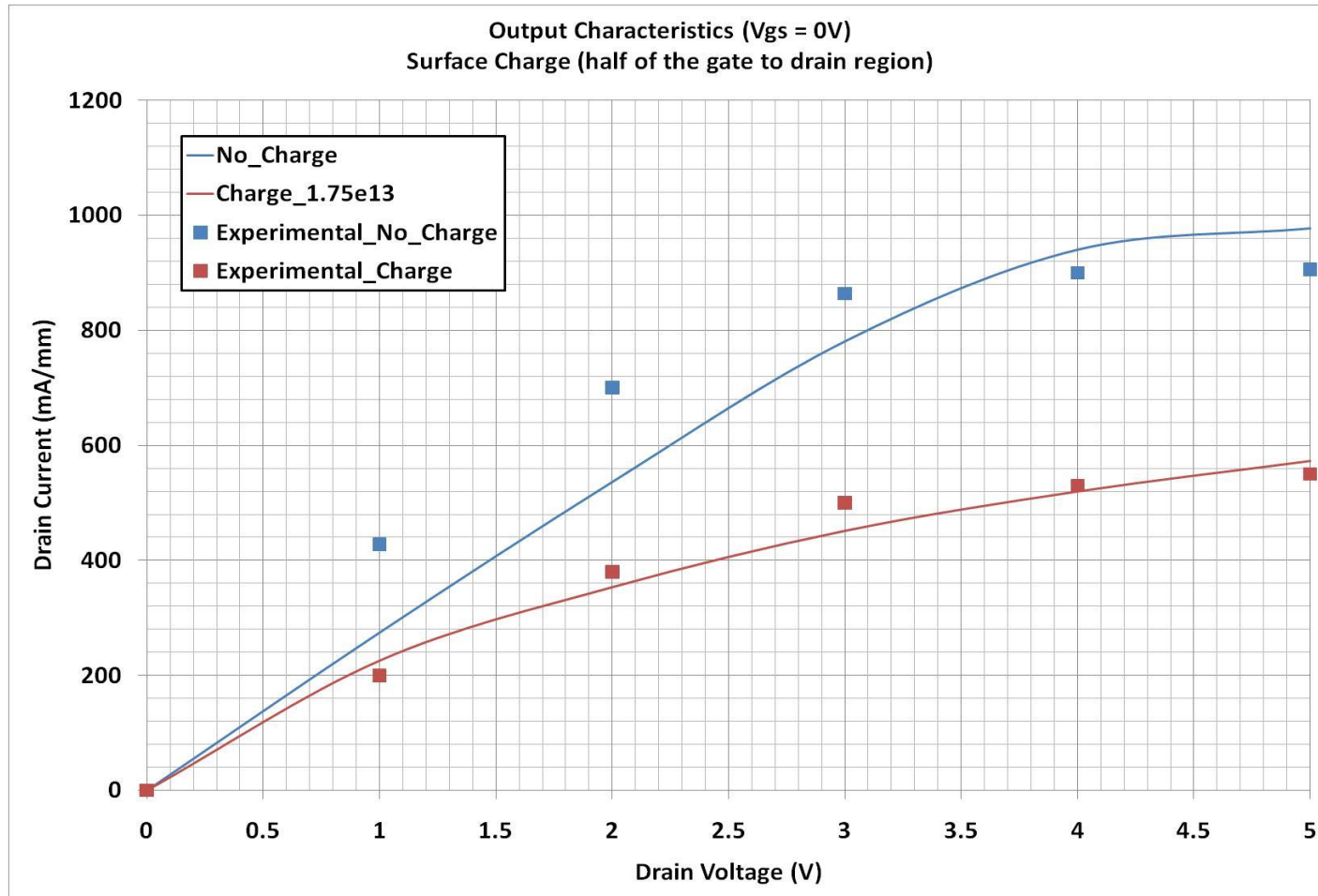
# Acoustic phonon temperature map



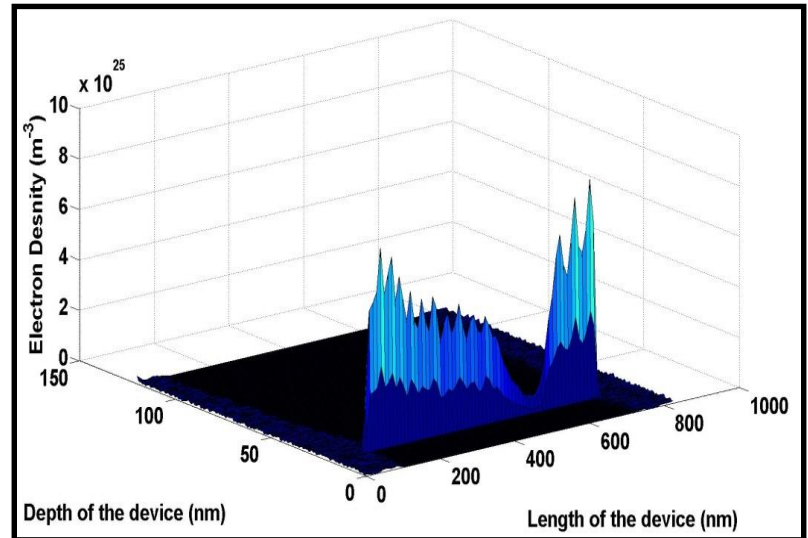
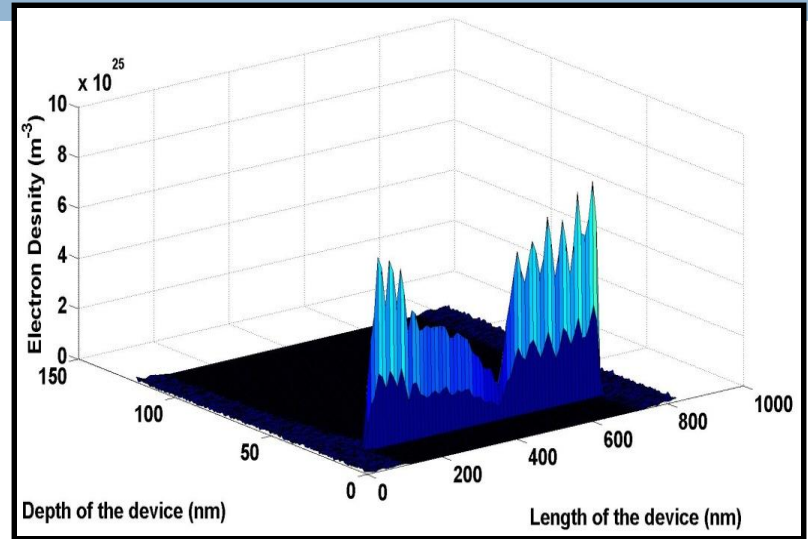
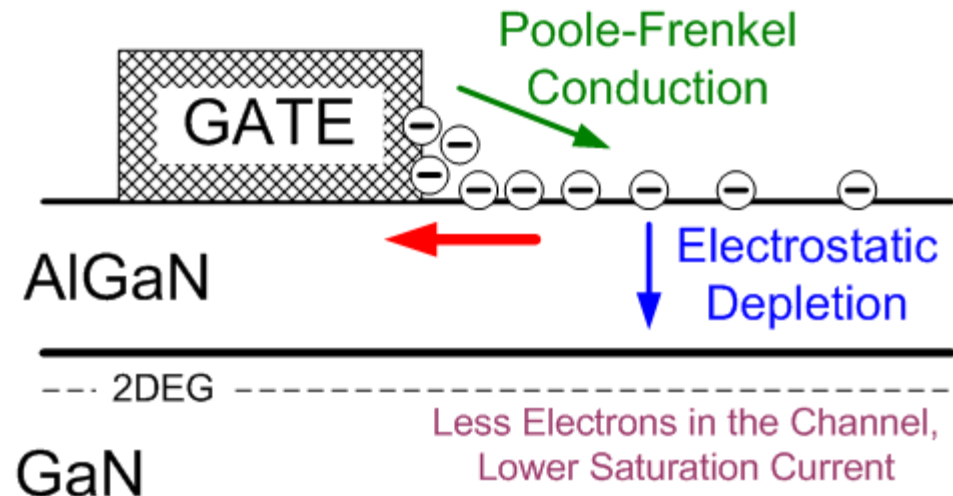
# Current collapse



# Supporting Evidence: $I_d$ - $V_d$ curve

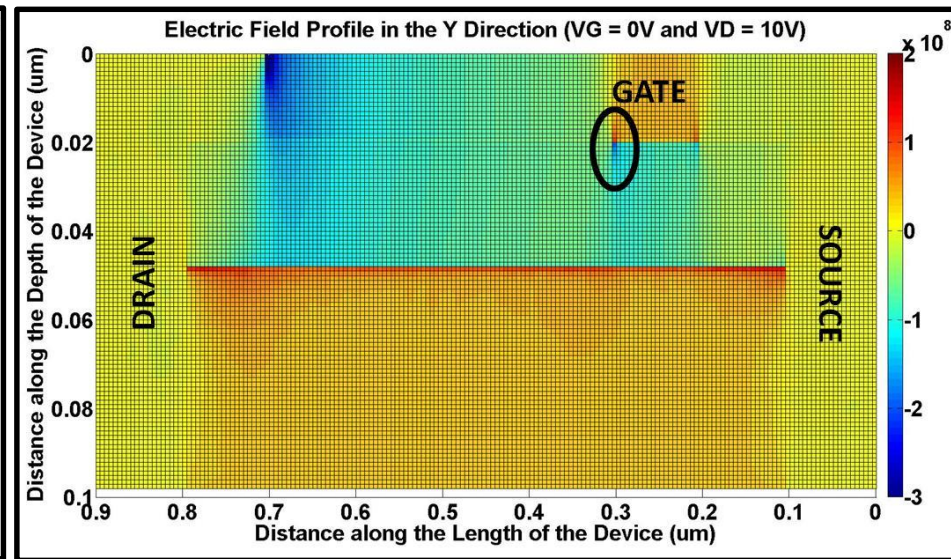
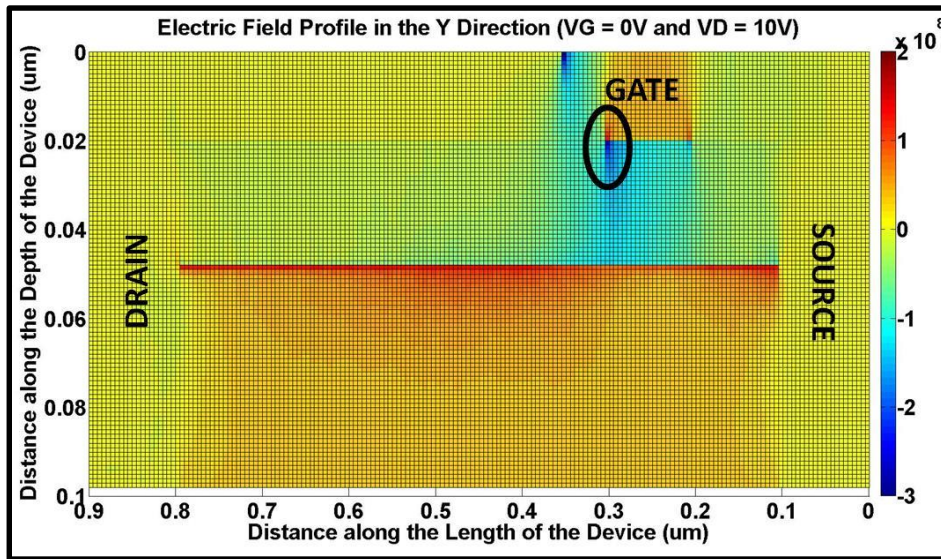


# Mechanism responsible for current collapse

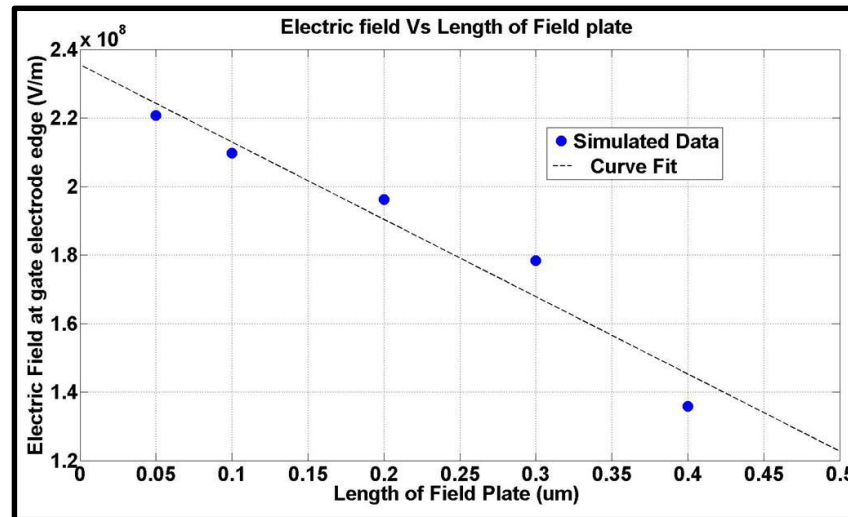




# Simulation Results

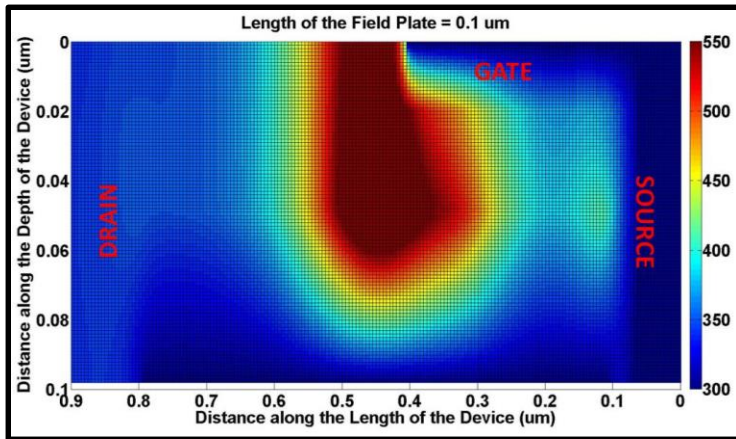


Electric Field Profile in the device with (a)  $0.05 \mu m$  and (b)  $0.4 \mu m$  shield lengths respectively

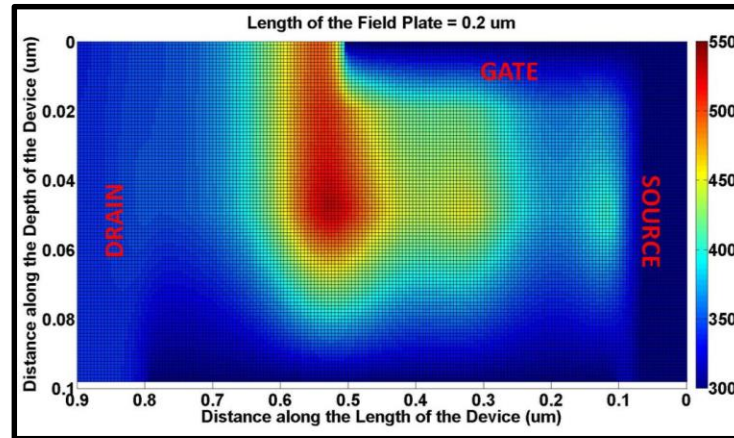


Vertical component of the Electric field at the gate drain edge Vs. field plate length

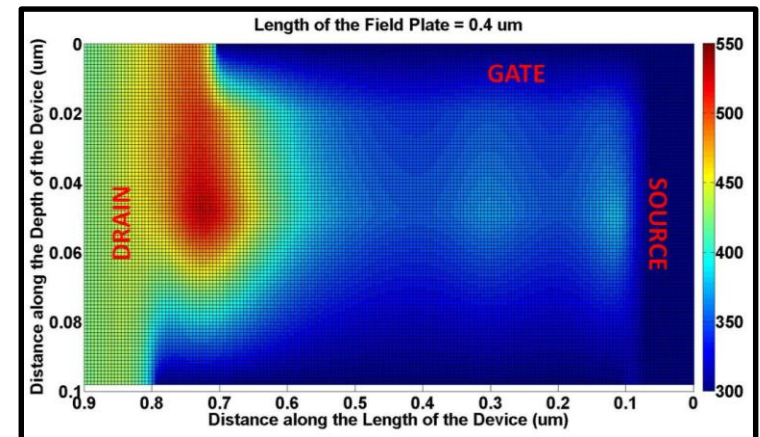
# Simulation Results



Lattice Temperature Profiles in the AlGaIn/GaN HEMT for varying shield lengths  
(a) 0.1  $\mu\text{m}$  (b) 0.2  $\mu\text{m}$  and (c) 0.4  $\mu\text{m}$

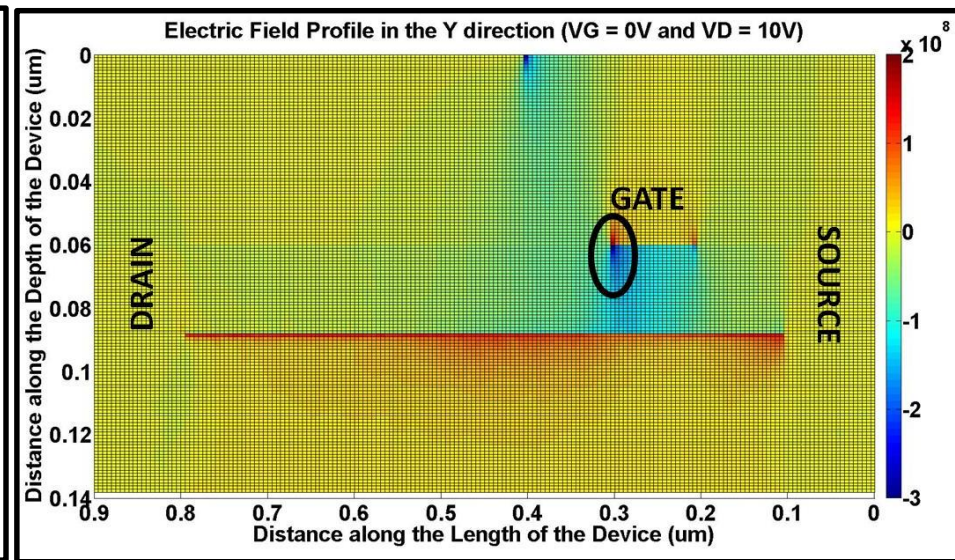
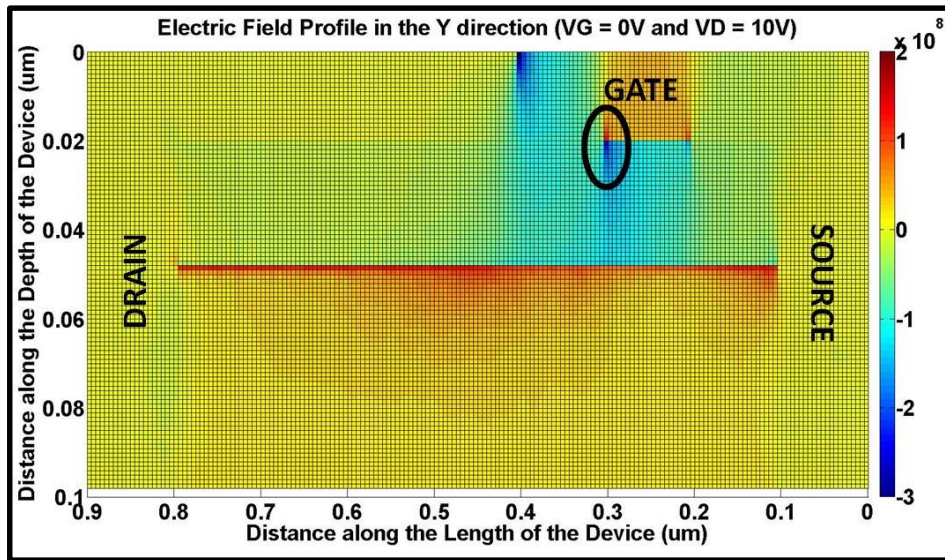


As the peak electric field moves far away from the gate-drain edge, the peak electron velocity also moves with it. The peak lattice temperature follows the peak electron velocity, as the energy of the electrons is highest in this region.

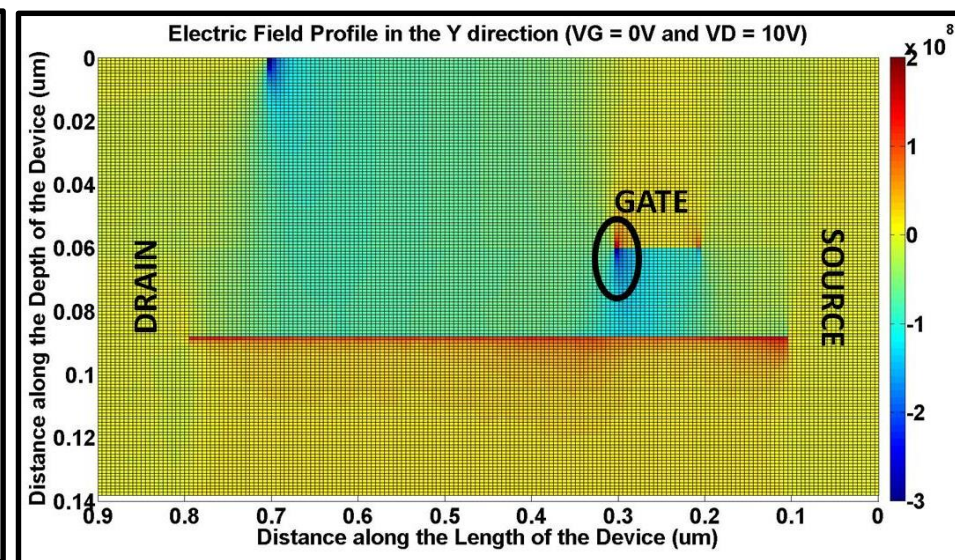
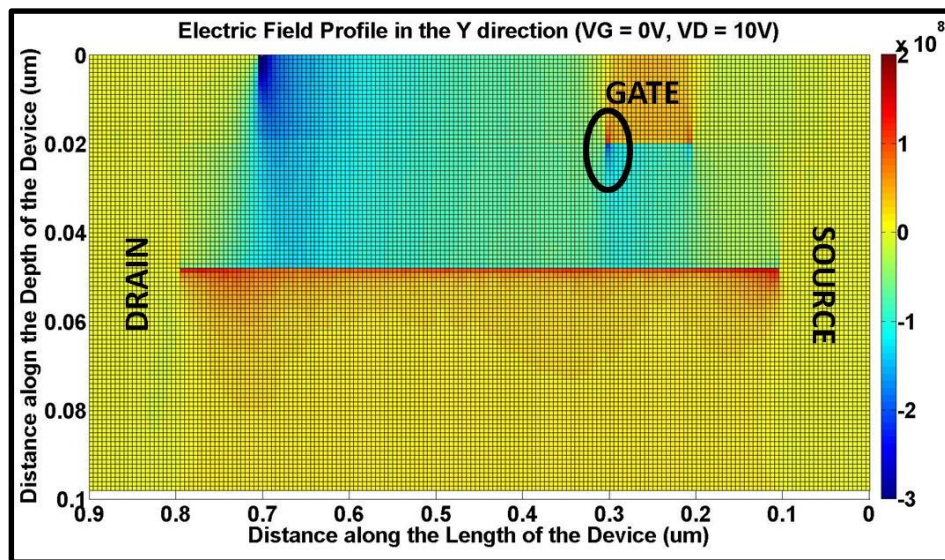




# Simulation Results



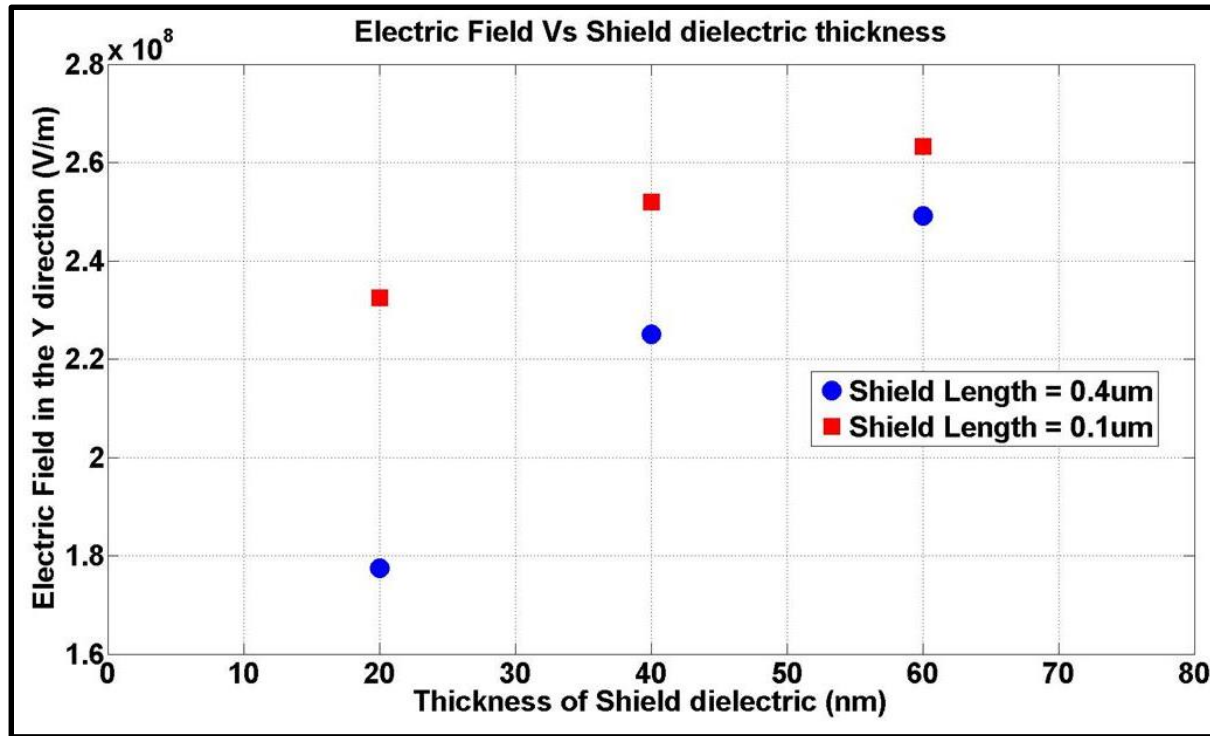
Electric Field Profile in the device for a shield length of  $0.1 \mu m$  (a) 20 nm and (b) 60 nm shield dielectric lengths respectively



Electric Field Profile in the device for a shield length of  $0.4 \mu m$  (a) 20 nm and (b) 60 nm shield dielectric lengths respectively



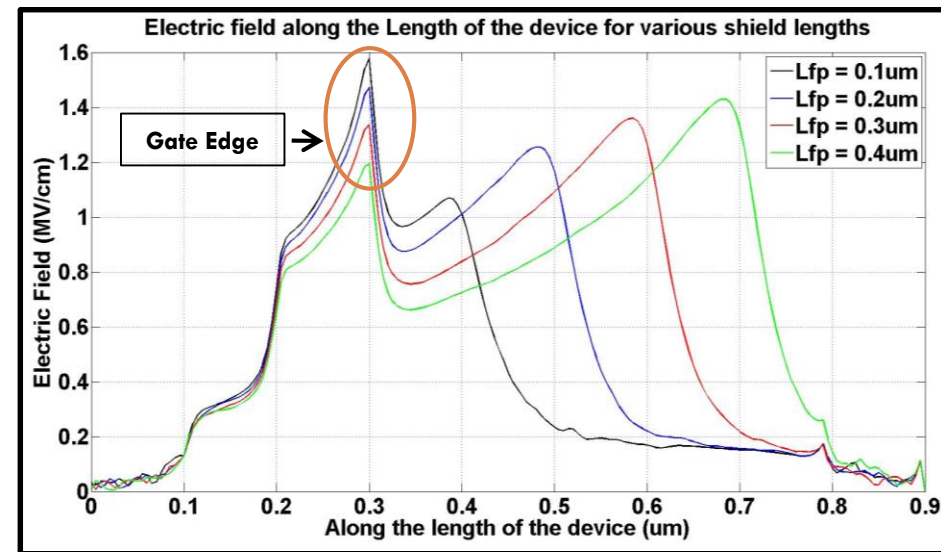
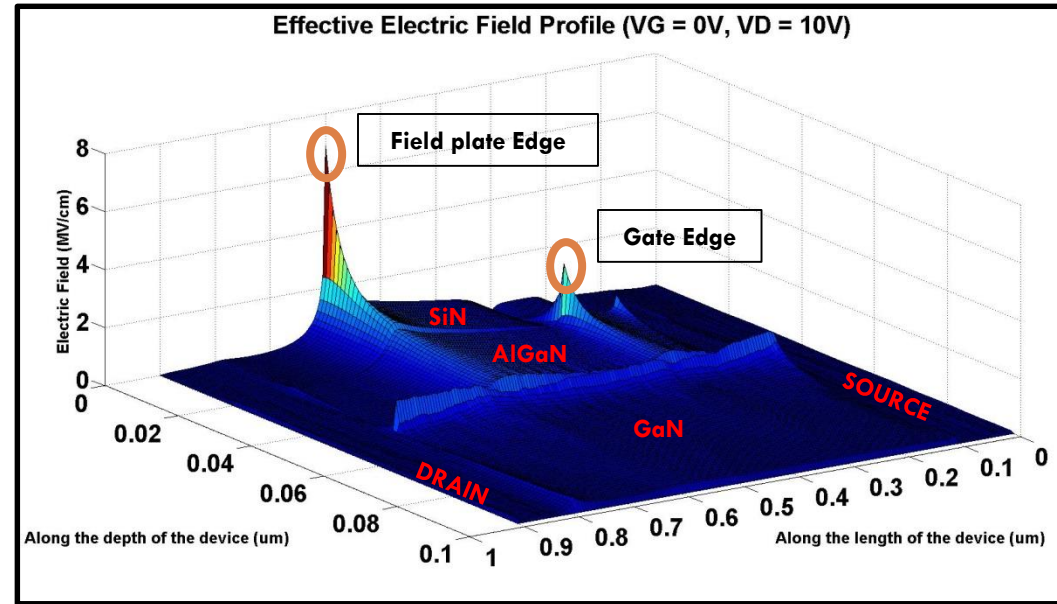
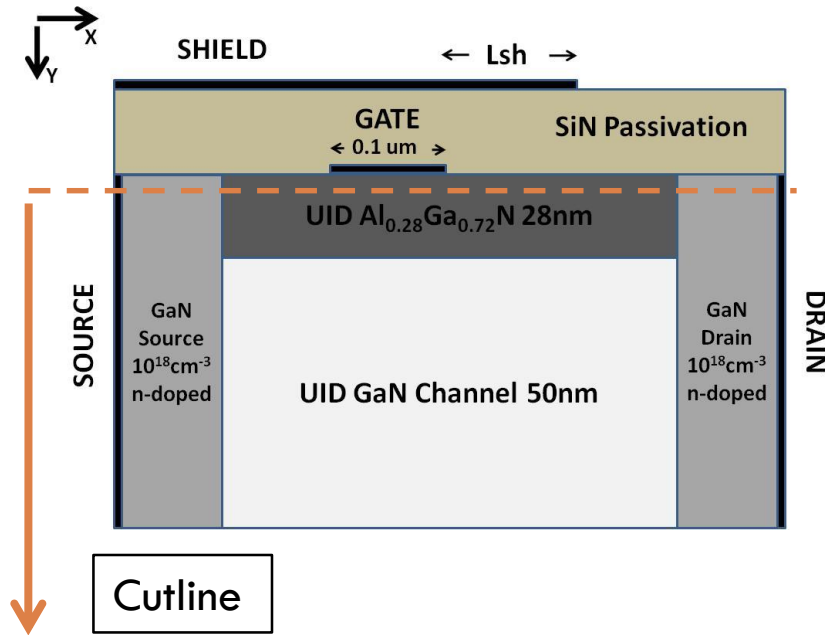
# Simulation Results



Vertical component of the Electric field at the gate drain edge  
Vs. shield dielectric thickness for varying field plate length

- As the shield length increases, the electric field near the critical gate-drain edge reduces. This is because, as the shield electrode length increases, it spreads the electric field over a wider region.
- As the shield dielectric thickness increases, its ability to capacitively couple the electric field with the structure reduces. This results in increase in the electric field near the gate drain edge for a given shield plate length.
- As the field near the gate-drain edge reduces, the potential for electron trapping in the defect sites also reduces and improves the reliability performance of the device structure.

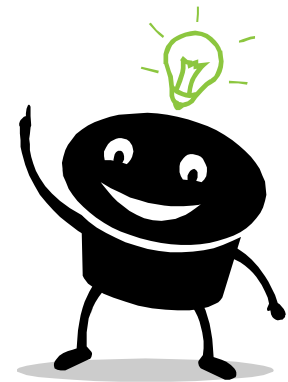
# Simulation Results



- We clearly observe from the electric cutline that as the field plate length is increased the electric field at the gate edge is reduced.
- We also observe that the electric field at the shield edge keeps increasing as its length increases. This is due to the fact that the edge of the shield plate is getting closer to the drain electrode.

Effective Electric field in the AlGaIn Layer for various field plate lengths

# PROPOSED RESEARCH AT ASU



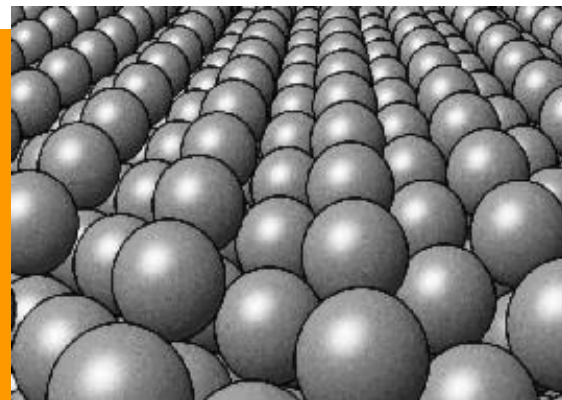
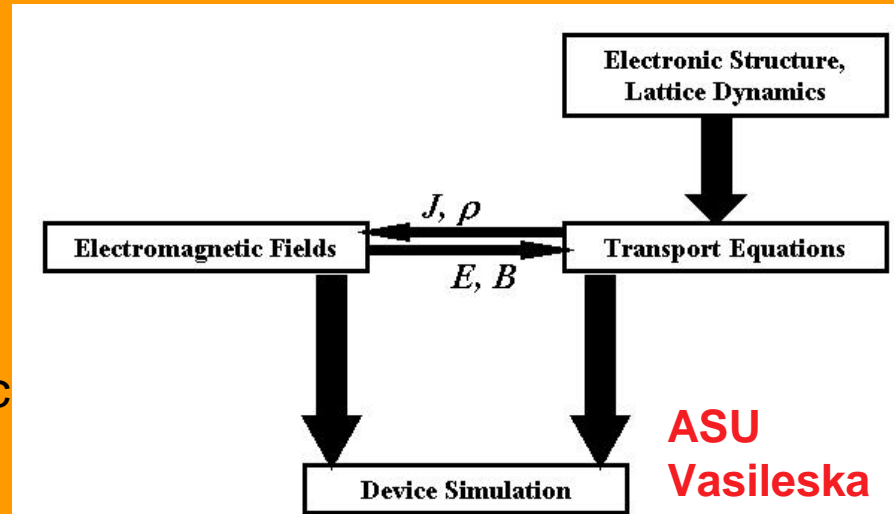
# Proposed Tasks

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- Creation of regional scattering tables near the PITS and CRACKS
- Formulation of DEFORMATION POTENTIAL THEORY from results obtained with first principle calculations

# Proposed Research ...

- Develop theoretical understanding for the formation of cracks in GaN HEMTs
- Approach:
  - Semiconductor device simulation to get the electric field profiles in the critical device region
  - Use these external fields into the **molecular dynamics calculations** to see if they are sufficient to nucleate a crack or a permanent defect



Purdue  
Klimeck



- ❑ Self-heating effects are important factor that must be accounted for as they limit device lifetime
- ❑ In ultra-nanoscale devices, due to the ballistic transport of the carriers, the heat dissipation occurs at the contacts (**thermal Landauer picture**)
- ❑ In GaN HEMTs heat plays considerable role with respect of the observation of the current collapse phenomena by modifying the vertical electric fields

Lake Ohrid, Republic of Macedonia

## Conclusions

# Thanks to ...

Army Research Laboratory



National Science Foundation

