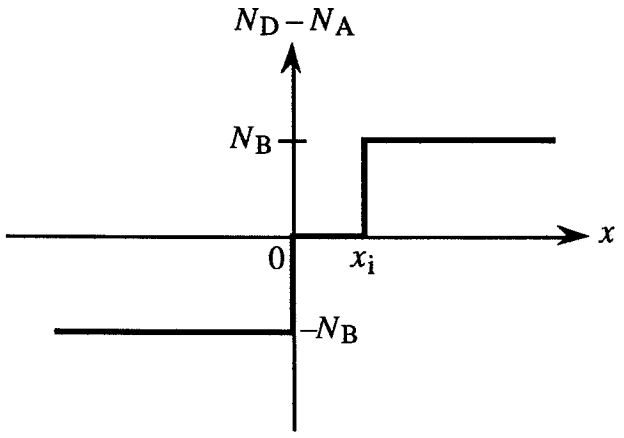
Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**B**
Test:	**B7**
Type:	***Open* Book, *Open* Notes**

Problem Weighting--- **T2-1...25 (5 each part)**
T2-2...49 (7 each part)
T2-3...26 (a-16, b-10)

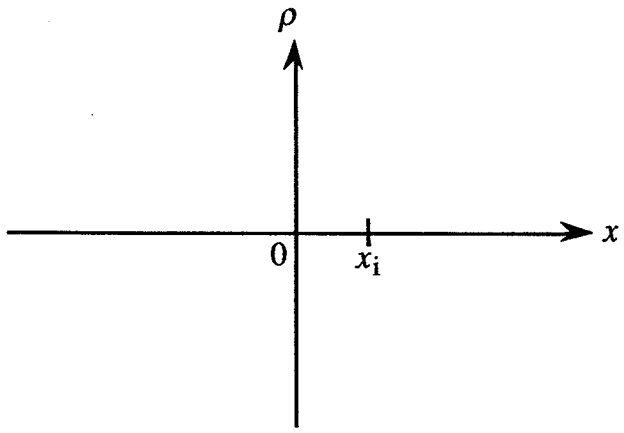
T2 – 1

A *pn* junction has the doping profile sketched below. Throughout this problem assume the carrier concentrations may be neglected ($n = 0, p = 0$) in the $0 \le x \le x_i$ region of the diode.



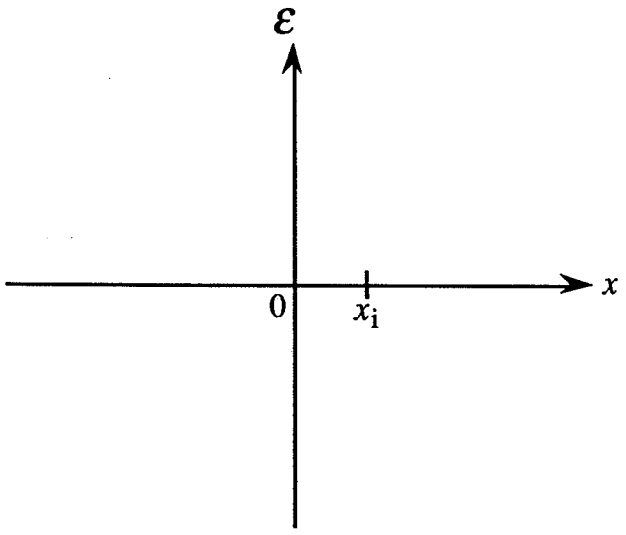
(a) What is the built-in voltage across the junction? Justify your answer.

(b) Invoking the depletion approximation, make a sketch of the charge density inside the diode. Label significant ρ and x values.



(Continued)

(c) Obtain an analytical solution for the electric field, $\mathcal{E}(x)$, at all points inside the depletion region ($-x_p \leq x \leq x_n$). Show all work and make a sketch of the deduced $\mathcal{E}(x)$ versus x.



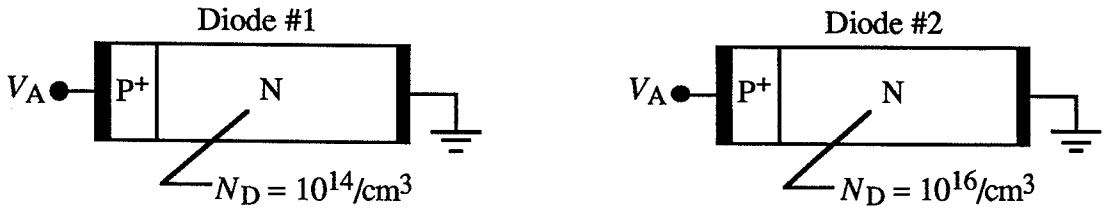
(Continued)

(d) In a standard *pn* step junction $N_A x_p = N_D x_n$. How are x_n and x_p related here?

(e) Draw the energy band diagram for the diode under equilibrium conditions. Clearly identify the points $x = 0$ and $x = x_i$ on your diagram. Also indicate how your diagram differs from that of a simple *pn* step junction where $N_A = N_D = N_B$.

T2 – 2

Two Silicon p^+-n step junction diodes maintained at 300K are physically identical except for the n-side doping. In diode #1, $N_D = 10^{14}/cm^3$; in diode #2, $N_D = 10^{16}/cm^3$. Compare the operation of the two diodes by answering the questions that follow.



NOTE:
- NO CREDIT will be given for correct answers without explanations.
- The explanation MUST be inside the box provided.
- Your explanation may include equations.
- Be sure to circle the correct answer after each question. A "same" answer or #1=#2 is possible.

Which diode will exhibit...

(a) The larger built-in voltage (V_{bi})? Ans⇒ #1 #2 #1=#2

Explanation...

(Continued)

(b) The larger breakdown voltage (V_{BR})? Ans⇒ #1 #2 #1=#2

Explanation...

(c) The larger junction capacitance (C_J) at a given reverse bias voltage when $|V_A| >> V_{bi}$.

Ans⇒ #1 #2 #1=#2

Explanation...

(d) The larger reverse bias current at a $|V_A|$ > few volts if the diodes are assumed to be ideal?

Ans⇒ #1 #2 #1=#2

Explanation...

(Continued)

(e) The larger reverse bias current at a $|V_A| >$ few volts if the diodes are NOT assumed to be ideal? Ans⇒ #1 #2 #1=#2

Explanation...

(f) The larger diffusion capacitance (C_D) at a given applied forward bias and frequency? (Assume operation in the forward bias "ideal" region.) Ans⇒ #1 #2 #1=#2

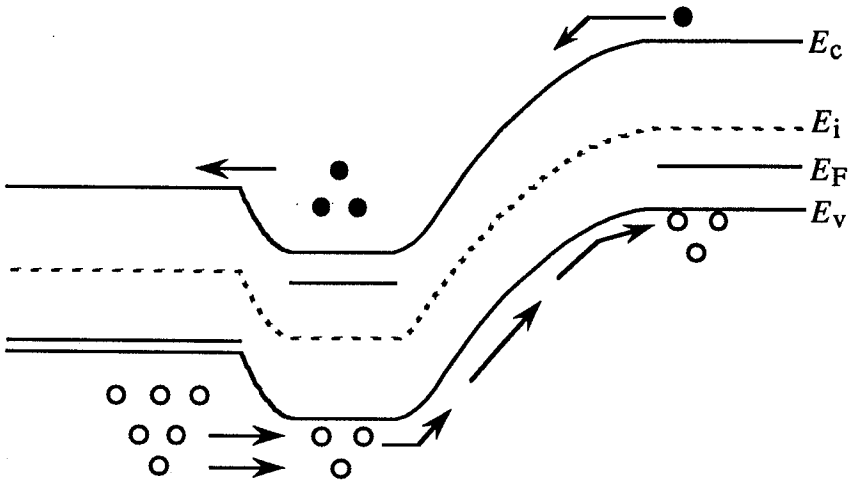
Explanation...

(g) The larger storage time (t_s) under transient conditions if I_F and I_R are the same? Ans⇒ #1 #2 #1=#2

Explanation...

T2 – 3

(a) The diagram below pictures the major carrier activity in a *pnp* BJT under active (normal active) mode biasing. Construct a similar diagram picturing the major carrier activity in the SAME *pnp* BJT under INVERTED (inverted active) mode biasing. (Include a few words of explanation as necessary to forestall a misinterpretation of your diagram.)



INVERTED MODE

(Continued)

(b) The previously pictured BJT is accidentally connected up backward so that the collector functions as the emitter and the emitter functions as the collector. In the backward connection with $V_{CB} > 0$ and $V_{EB} < 0$ the device exhibits a lower gain and is more sensitive to base width modulation.

(i) Explain why the backward connection leads to a lower gain.

(ii) Explain why the backward connection leads to a greater sensitivity to base width modulation.