Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**B**
Test:	**B15**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

Problem Weighting--- **2-1...18 (6 each part)**
2-2...42 (6 each part)
2-3...40 (a-6, b-12, c-8, d-6, e-8)

2 - 1

General Information

As concisely as possible, define 3 of the following 4 terms:

(a) Doping profile

(b) Depletion approximation

(c) Zener process

(d) Base-width modulation

2 - 2

PN Junction Diode

The energy band diagram shown in Fig. 2-2 characterizes a step junction diode maintained at room temperature. Answer the questions which follow using the information conveyed in the diagram and the data adjacent to the diagram.

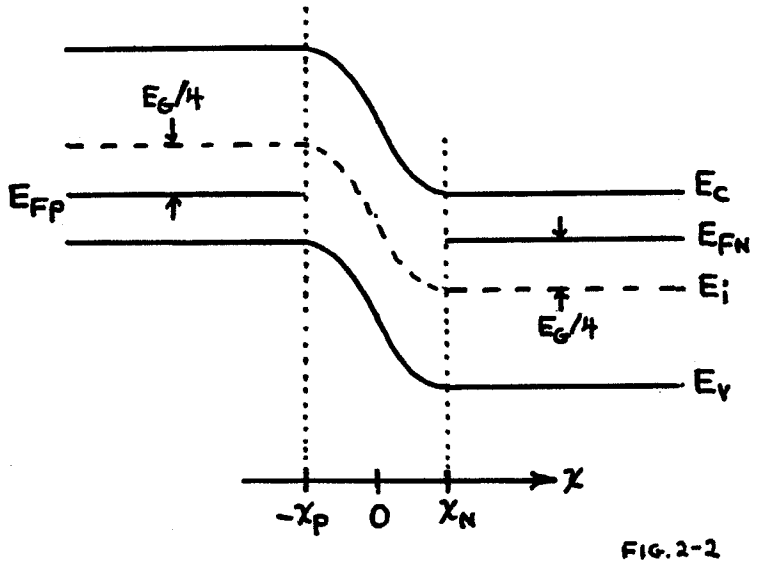

FIG. 2-2

Data

$E_{FP} - E_{Fn} = E_G/4$

$E_G = 1.00eV$

$kT = 0.0258eV$

$K_S = 10.0$

$\varepsilon_o = 8.85 \times 10^{-14} f/cm$

$A(area) = 10^{-2}\ cm^2$

$x_p + x_n = 10^{-3} cm$

(a) What is the magnitude of the reverse-bias voltage (V_A) being applied to the device? Explain how you arrived at your answer.

(b) Determine V_{bi}, the built-in voltage.

(c) What will be the junction (or depletion-layer) capacitance exhibited by the diode at the pictured bias point?

(d) Make a rough sketch of the carrier concentrations, n and p, for the $x \leq -x_p$ and $x \geq x_n$ portions of the diode. (Low level injection conditions prevail.)

(e) Would you expect the device to exhibit a significant diffusion capacitance at the applied bias point? Explain.

(f) If the diode were pulsed from the pictured bias point to a larger reverse bias at t = 0, would you expect to observe a current transient characterized by a storage delay time t_s? Explain.

(g) What additional information would you require in order to compute the recombination-generation current flowing through the diode at the pictured bias point? Explain.

2 - 3

Bipolar Junction Transistor

Consider the silicon BJT pictured in Fig. 2-3. The transistor is maintained at room temperature and has uniformly doped emitter, base, and collector regions. $N_{AE} = 10^{17}/cm^3$, $N_{DB} = 10^{16}/cm^3$, and $N_{AC} = 10^{15}/cm^3$.

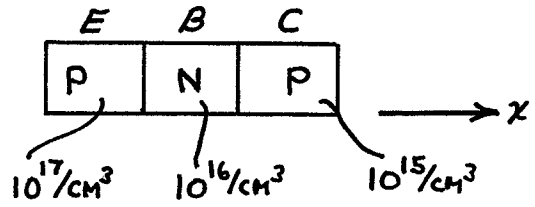

FIG. 2-3

(a) Sketch the <u>equilibrium</u> energy band diagram for the device. Show E_C, E_i, E_V, and E_F on your diagram; label the E, B, and C regions. (You need display only the correct <u>relative</u> positioning of the Fermi level in the three transistor regions.)

(b) Invoking the depletion approximation and assuming equilibrium conditions prevail, sketch the electrostatic variables ρ, $\mathcal{E}$, and V as a function of position (x) inside the transistor. Set x = 0 at the Emitter-Base metallurgical junction. Be sure to label the axes of your three sketches.

(c) Sketch the <u>minority and majority</u> carrier distributions in the quasi-neutral regions of the given PNP transistor under <u>active mode</u> biasing. Assume low level injection conditions prevail and $W_B << L_B$.

(d) (i) Define in <u>words</u> what is meant by "emitter efficiency".

(ii) In a PNP transistor, is the emitter efficiency maximized by making $N_{AE} >> N_{DB}$ or $N_{DB} >> N_{AE}$? Explain.

(e) (i) Name the two phenomena that limit the maximum reverse bias voltage which can be applied to the CB junction.

(ii) How does one design a BJT so as to make the reverse bias voltage sustained by the CB junction as large as possible?