Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**B**
Test:	**B16**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

Problem Weighting is noted adjacent to each problem.

NAME_____ 2-1 _____SCORE

As concisely as possible -- using words, figures, or a combination of words and figures (but no equations) -- define:

(6) (a) Avalanche Breakdown

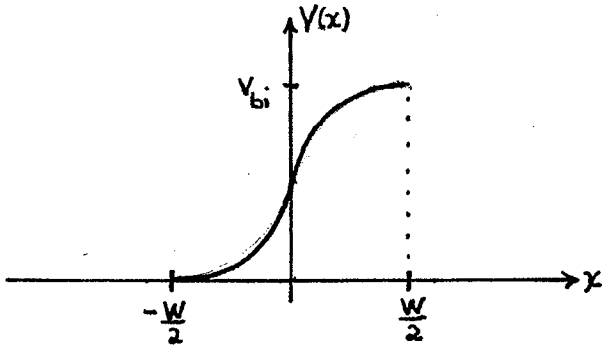
(6) (b) Recombination-Generation Current

(6) (c) Punch-Through

NAME_____ 2-2 _____SCORE

The electrostatic potential (V) versus x in the depletion region of a p-n junction under equilibrium conditions is

$$V(x) = \frac{V_{bi}}{2}\left(1 + \sin\frac{\pi x}{W}\right) \qquad \ldots -W/2 \leq x \leq W/2$$



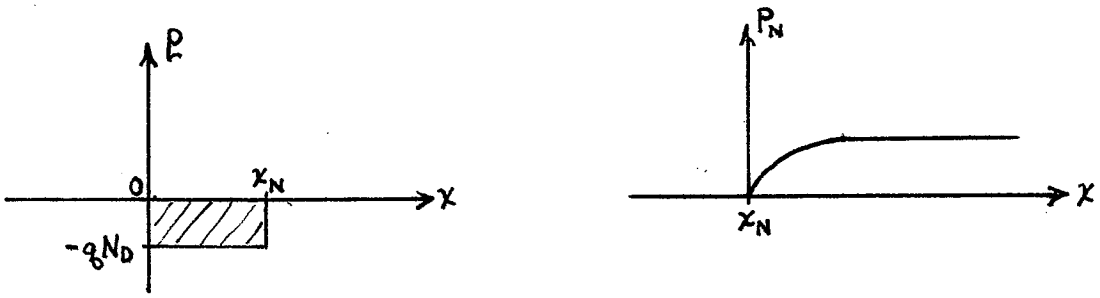
(6) (a) Establish an expression for the electric field ($\mathcal{E}$) versus x in the depletion region ($-W/2 \leq x \leq W/2$) and sketch $\mathcal{E}(x)$ vs. x.

(6) (b) Establish an expression for the charge density (ρ) versus x in the depletion region and sketch $\rho(x)$ vs. x.

(6) (c) Invoking the depletion approximation, establish an expression for $N_D - N_A$ versus x in the depletion region and sketch $N_D - N_A$ vs. x.

NAME_____ 2-3A _____SCORE

Charge density and minority carrier concentration versus position plots are often used to describe the situation inside semiconductor devices. The ρ vs. x $(0 \leq x \leq x_n)$ and p_n vs. x $(x \geq x_n)$ inside a p^+-n step junction diode are shown below.



(6) (a) Is the diode forward or reverse biased? To receive credit, explain how you arrived at your answer.

(6) (b) Using dashed lines, modify the plots in the statement of the problem to indicate (roughly) the effect of doubling the magnitude of the applied bias. (Write NO EFFECT if a plot remains unchanged.)

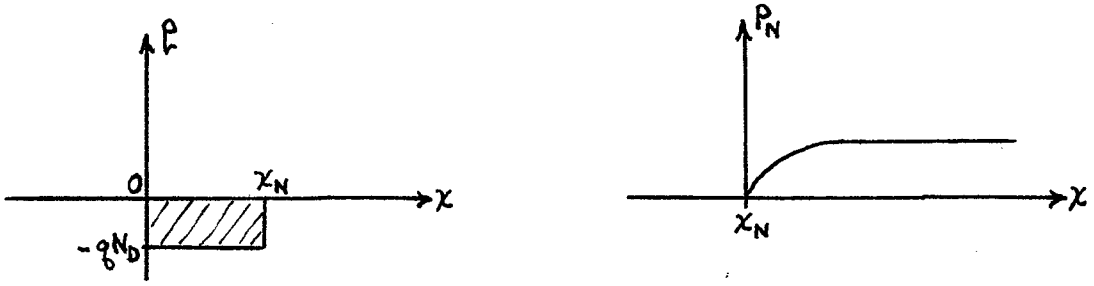
(5) (c) Suppose the diode is pulsed from V_R (a reverse bias) to $2V_R$. What will be the storage delay time? EXPLAIN.

(5) (d) How is the junction capacitance affected by changing the applied bias from V_R (a reverse bias) to $2V_R$. EXPLAIN.

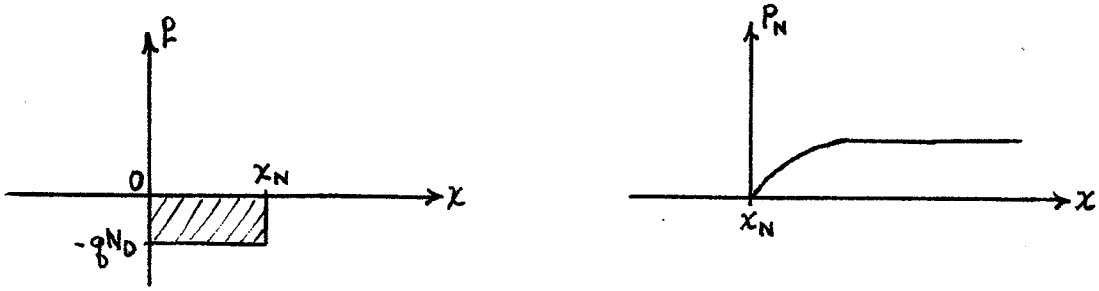
(continued)

NAME_____ 2-3B _____SCORE

(6) (e) On the diagrams reproduced below, indicate the effect of increasing τ_p by a factor of 4. τ_p is the minority carrier lifetime on the n-side.



(6) (f) On the diagrams reproduced below, indicate the effect of doubling N_D.



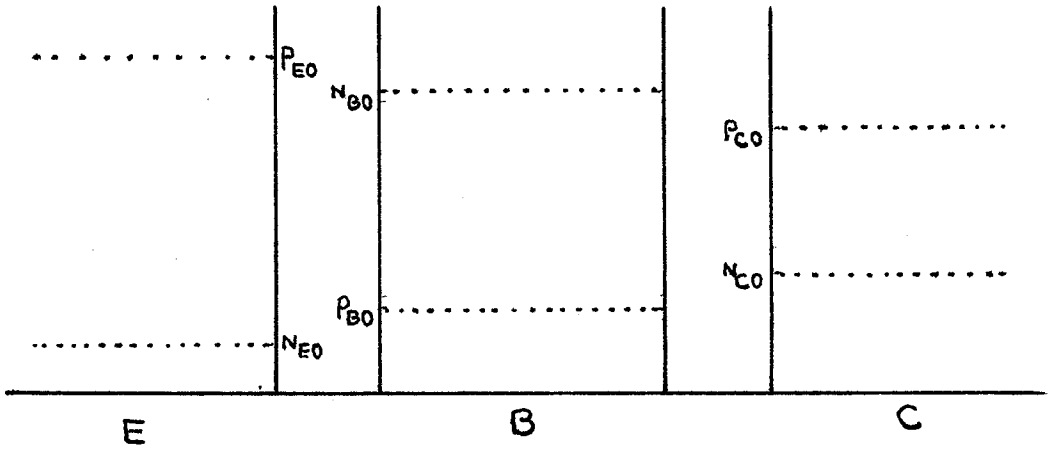
(5) (g) What determines the <u>minimum</u> capacitance that will be exhibited by a given p^+-n junction diode? EXPLAIN.

NAME_____ 2-4 _____SCORE

(4) (a) In the following table indicate whether the emitter-base and collector-base junctions of a BJT are reverse biased or forward biased.

region of operation	emitter-base	collector-base
Active		
Cut-Off		
Saturation		
Inverse Active		

(9) (b) Sketch the minority and majority carrier distributions in the quasi-neutral regions of a PNP transistor under active mode biasing. Assume low level injection and $W_B << L_B$.



(6) (c) What effect does reducing the base width (W_B) have on the base transport factor (α_T) of a PNP transistor? Explain your answer without using equations.

(6) (d) What effect does increasing the base doping (N_{DB}) have on the emitter injection efficiency of a PNP transistor? Explain your answer without using equations.