Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**B**
Test:	**B17**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

Problem Weighting--- **T2-1...25 (5 each part)**
T2-2...29 (a-7, b-5, c-5, d-12)
T2-3...22 (a-5, b-5, c-6, d-6)
T2-4...24 (4 each part)

T2 - 1

As concisely as possible -- using words, figures, or a combination of words and figures (but no equations) -- define:

(a) Avalanche Breakdown

(b) Recombination - Generation Current

(c) Base Transport Factor

(d) Punch-Through

Also...

(e) Sketch the minority carrier distribution, $\Delta p_B(x)$, in the base of a PNP bipolar junction transistor ($W << L_B$) under active mode biasing.

T2 - 2

The doping profile inside a special PN junction diode is pictured in Fig. T2-2 and defined mathematically to the right of Fig. T2-2.

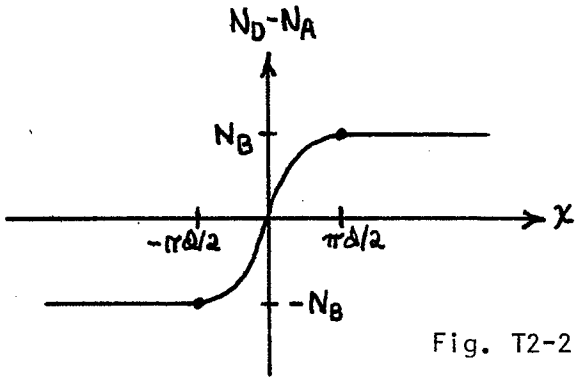


Fig. T2-2

$$N_D - N_A = \begin{cases} -N_B & \ldots x \leq -\frac{\pi d}{2} \\ N_B \sin\frac{x}{d} & \ldots \frac{\pi d}{2} \leq x \leq \frac{\pi d}{2} \\ N_B & \ldots x \geq \frac{\pi d}{2} \end{cases}$$

For the cited junction:

(a) Establish an expression for the built-in voltage (V_{bi}).

(b) If the depletion approximation is invoked, one must have $x_p = x_n = W/2$, where W is the total depletion width. Explain why (no equations please).

(c) Invoking the depletion approximation, and assuming $W/2 > \pi d/2$ for all biases of interest, make a sketch of the charge density (ρ) inside the junction as a function of x.

(d) Establish expressions for the electric field ($\mathcal{E}$) at all points inside the device. (A separate expression is required for $x \leq -W/2$, $-W/2 \leq x \leq -\pi d/2$, $-\pi d/2 \leq x \leq \pi d/2$, $\pi d/2 \leq x \leq W/2$, and $x \geq W/2$.)

T2 - 3

The steady-state carrier concentrations inside a PN junction diode are as shown in Fig. T2-3.

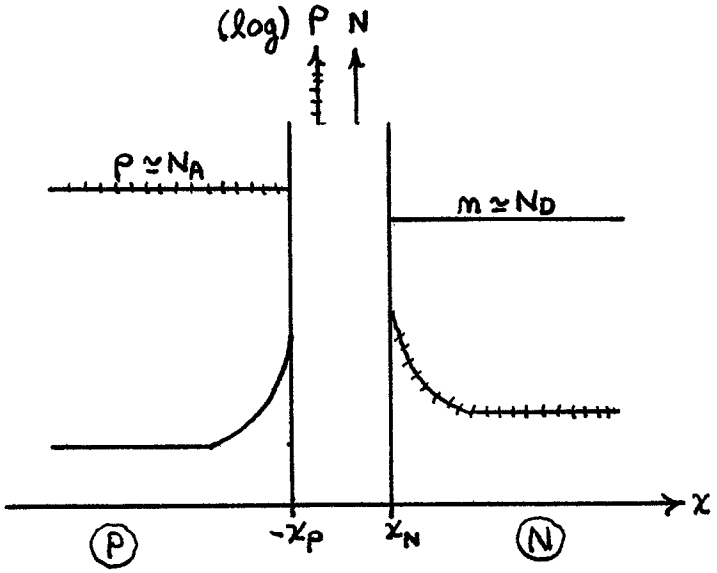


Fig. T2-3

(a) Is the diode forward or reverse biased? Explain how you arrived at your answer.

(b) Do low level injection conditions prevail inside the diode? Explain how you arrived at your answer.

(c) Qualitatively, what is the physical relationship between the pile-up or store of minority carriers near the depletion region edges and the diffusion admittance (Y_D)?

(d) Qualitatively, what is the physical relationship between the pile-up or store of minority carriers near the depletion region edges and the storage delay time (t_s) observed in the forward-to-reverse transient response?

T2 - 4

The reverse-bias current voltage (I-V_A), junction capacitance (C_J-V_A), and forward-to-reverse bias transient response (i-t) of a P^+-N step junction Si diode maintained at room temperature have been recorded in the answer booklet. Answer the following questions by adding a dashed line to the appropriate figure in the answer booklet.

NOTE: (1) An answer of NO EFFECT (dashed line same as answer booklet line) is possible. In such cases write NO EFFECT.

(2) Explanations are NOT required and will receive no credit.

Roughly indicate how the

(a) I - V_A characteristic,

(b) C_J - V_A characteristic, and

(c) i - t characteristic

would be modified if the n-side doping (N_D) were increased by a factor of 2. All other parameters remain the same.

Roughly indicate how the

(d) I - V_A characteristic,

(e) C_J - V_A characteristic, and

(f) i - t characteristic

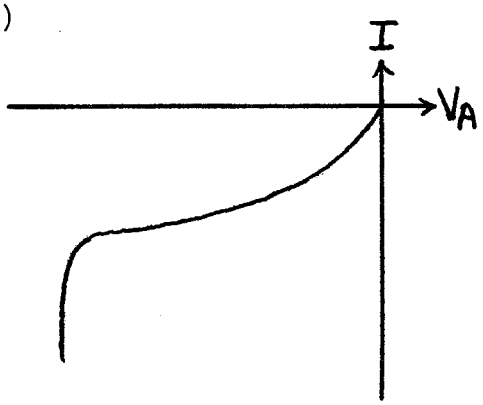
would be modified if the minority carrier lifetime on the n-side (τ_p) and the effective depletion-region generation lifetime (τ_o) were increased by a factor of 2. All other parameters remain the same.

T2 - 4

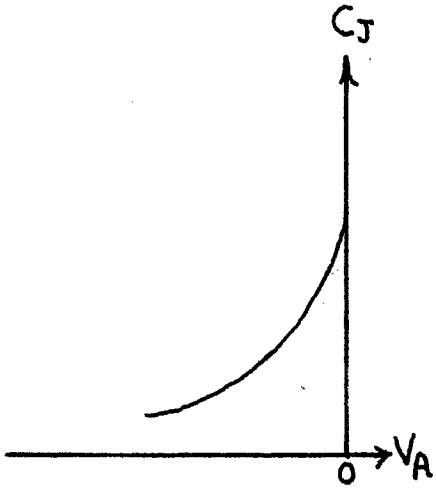
NAME_____ B17-6

SCORE_____

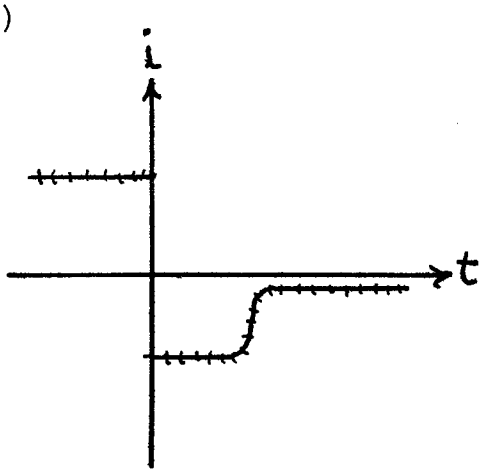
(a)



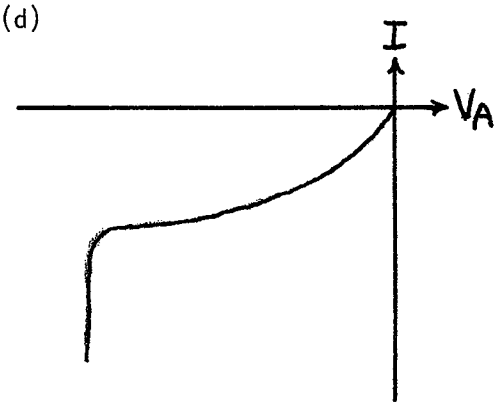
(b)



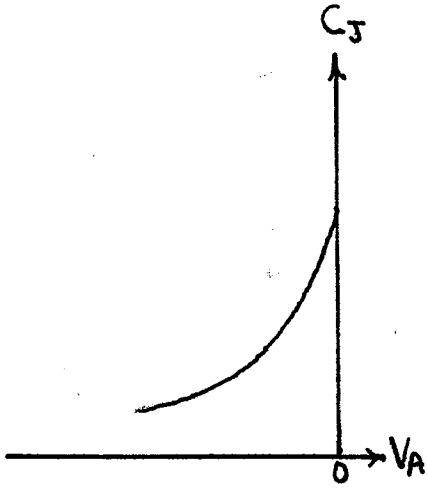
(c)



(d)



(e)



(f)