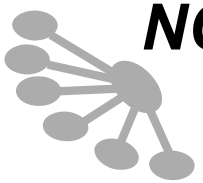
EE-612:
Lecture 19:
Series Resistance

Mark Lundstrom
Electrical and Computer Engineering
Purdue University
West Lafayette, IN USA
Fall 2006



NCN

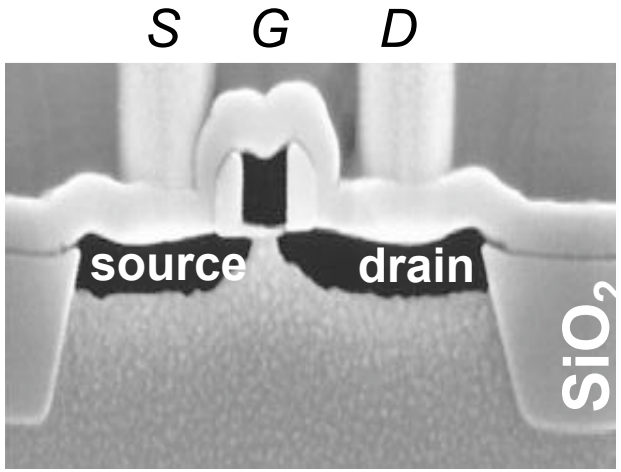
www.nanohub.org

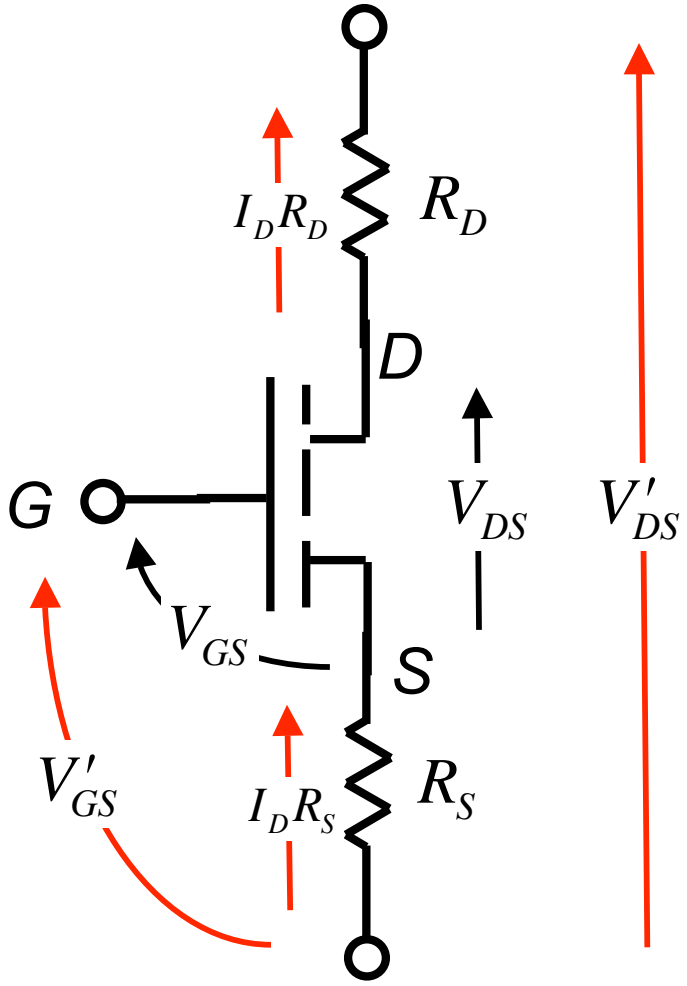
PURDUE UNIVERSITY

outline

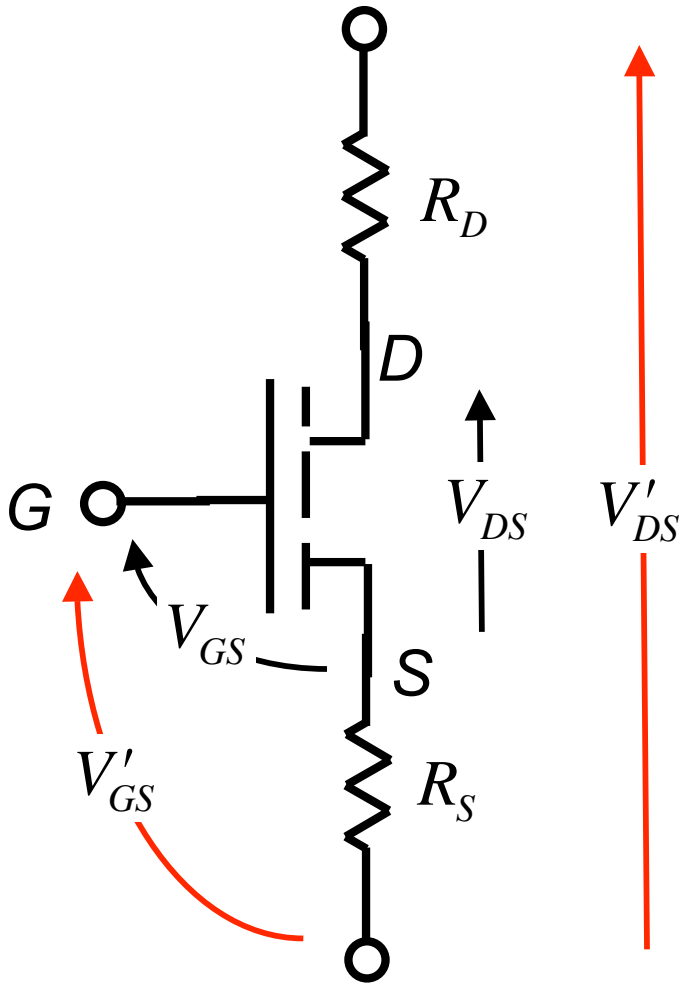
1) Effect on I-V
2) Series resistance components
3) Metal-semiconductor resistance
4) Other series resistance components
5) A look at the ITRS
6) Effective Channel Length

series resistance (DC)



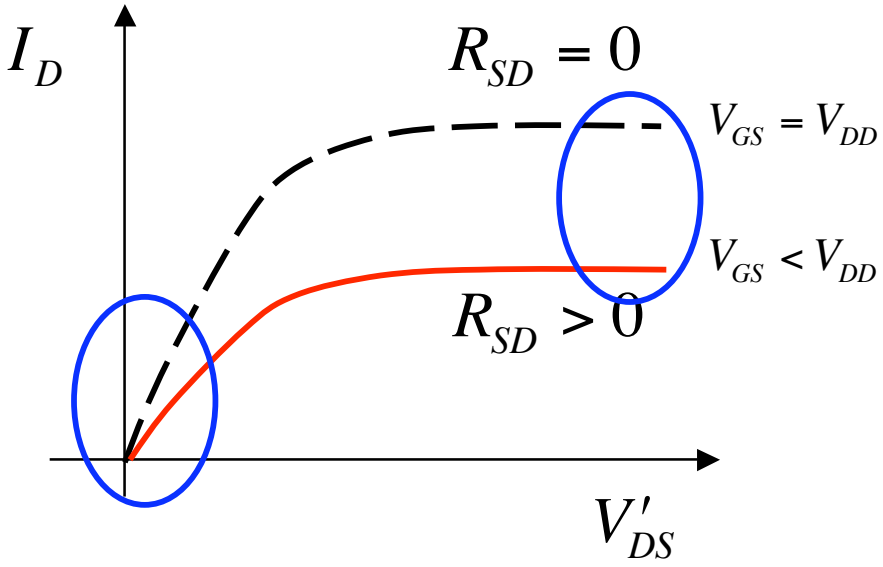


series resistance (DC)



$$V_{GS} = V'_{GS} - I_D R_S$$

$$V_{DS} = V'_{DS} - I_D\left(R_S + R_D\right)$$

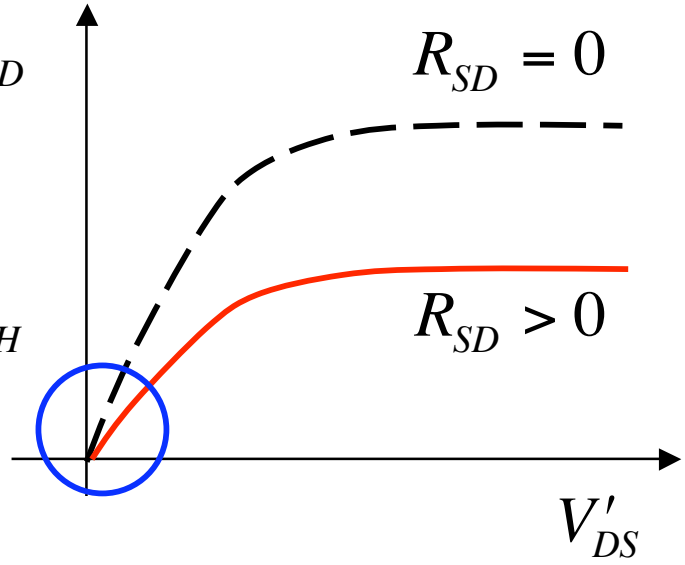


series resistance (small V_{DS})

$$\left.\begin{aligned} V_{GS} &= V'_{GS} - I_D R_S \\ V_{DS} &= V'_{DS} - I_D\left(R_S + R_D\right) \end{aligned}\right\}$$

$$I_D^i = \frac{W}{L}\mu_{eff} C_G \left(V_{GS} - V_T\right) V_{DS} = V_{DS} / R_{CH}$$

$$I_D = V_{DS} / \left(R_{CH} + R_S + R_D\right)$$

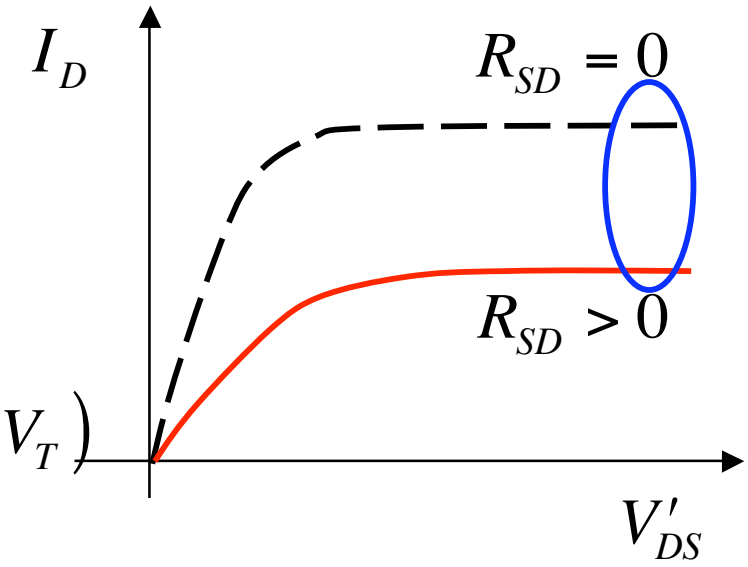


$$\Delta I_D = I_D^i - I_D = V_{DS}\left(\frac{1}{R_{CH}} - \frac{1}{R_{CH} + R_{SD}}\right) = \frac{V_{DS}}{R_{CH}}\left(\frac{R_{SD}}{R_{CH} + R_{SD}}\right)$$

$$\frac{\Delta I_D}{I_D^i} = \left(\frac{R_{SD}}{R_{TOT}}\right)$$

series resistance (large V_{DS})

$$V_{GS} = V'_{GS} - I_D R_S$$
$$V_{DS} = V'_{DS} - I_D\left(R_S + R_D\right)$$



$$I_D^i = WC_G\upsilon_{SAT}\left(V_{GS} - V_T\right) = G_0\left(V_{GS} - V_T\right)$$

$$I_D = G_0\left(V'_{GS} - I_D R_S - V_T\right)$$

$$I_D\left(1 + G_0 R_S\right) = G_0\left(V'_{GS} - V_T\right) = I_D^i$$

$$I_D = \frac{I_D^i}{\left(1 + G_0 R_S\right)}$$

series resistance (large V_{DS})

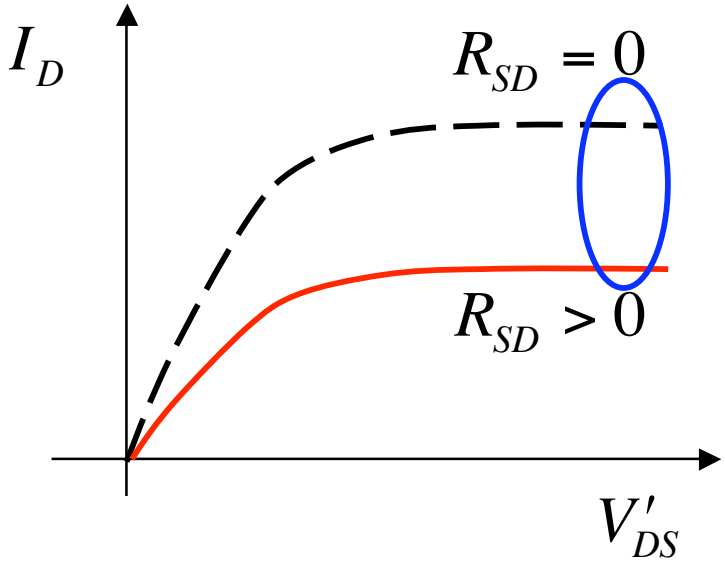
$$I_D = \frac{I_D^i}{\left(1 + G_0 R_S\right)}$$

$$\Delta I_D = I_D^i - \frac{I_D^i}{\left(1 + G_0 R_S\right)}$$

$$\frac{\Delta I_D}{I_D^i} = \frac{G_0 R_S}{\left(1 + G_0 R_S\right)} = \frac{R_S}{\left(1/G_0 + R_S\right)}$$

$$I_D^i = G_0\left(V_{GS} - V_T\right)$$

$$G_0 \approx I_{ON}/V_{DD} = 1/R_{ON}$$

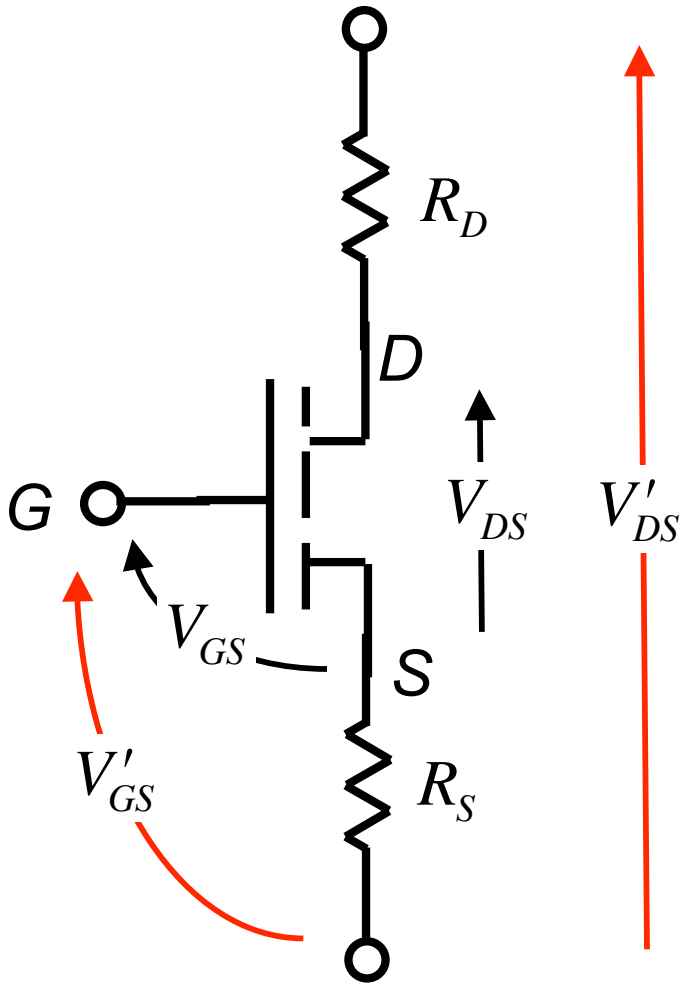


$$\frac{\Delta I_D}{I_D^i} \approx \frac{R_S}{\left(R_{ON} + R_S\right)} = \frac{R_S}{R_{TOT}}$$

outline

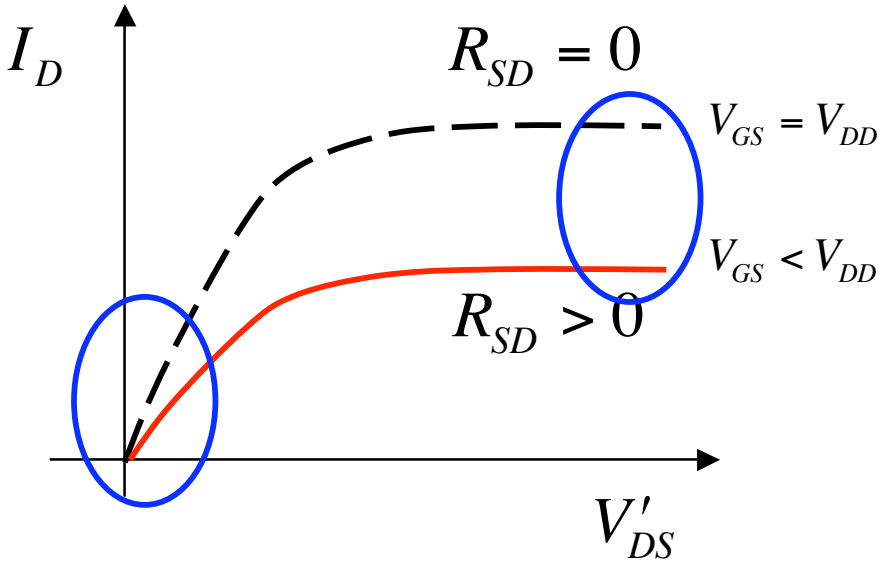
1) Effect on I-V
2) **Series resistance components**
3) Metal-semiconductor resistance
4) Other series resistance components
5) A look at the ITRS
6) Effective channel length

series resistance (DC)

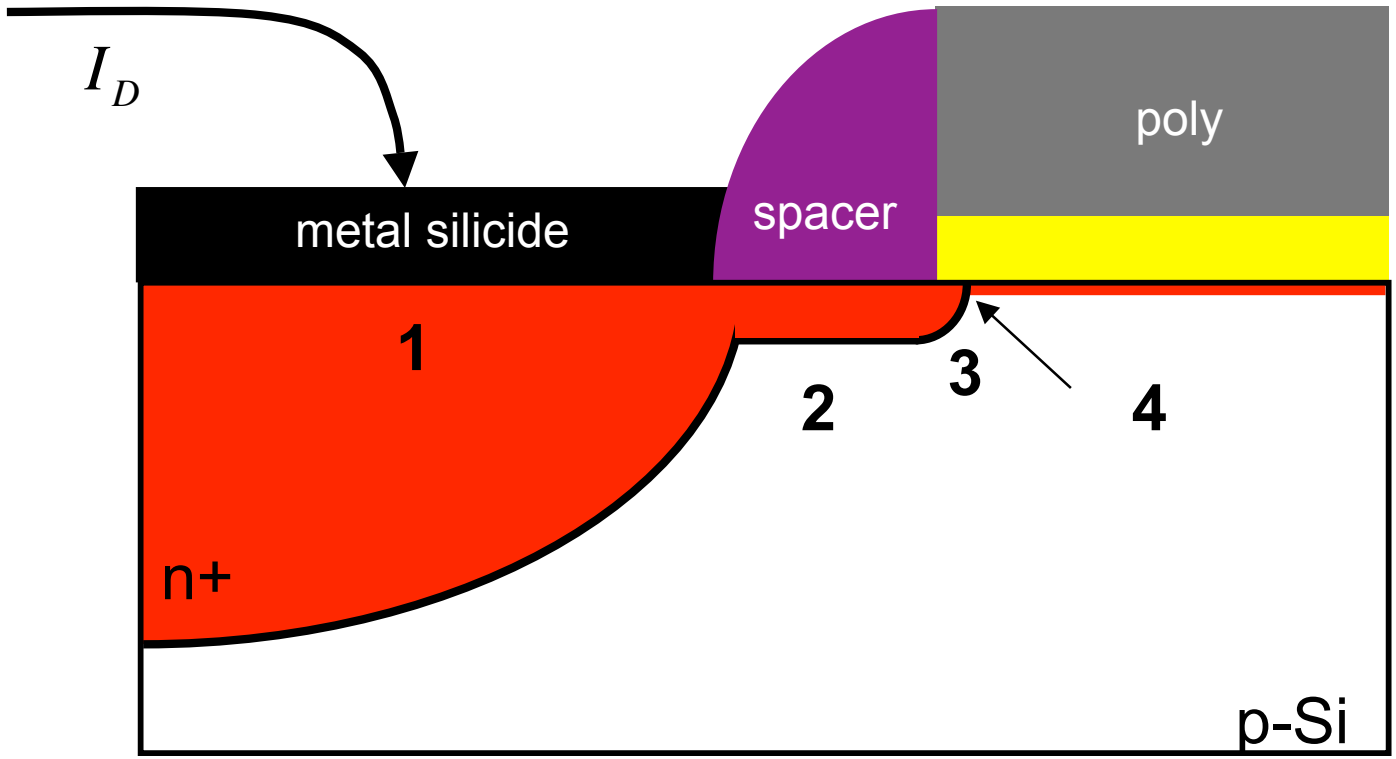


$$V_{GS} = V'_{GS} - I_D R_S$$

$$V_{DS} = V'_{DS} - I_D\left(R_S + R_D\right)$$



physical origin of R_{SD}

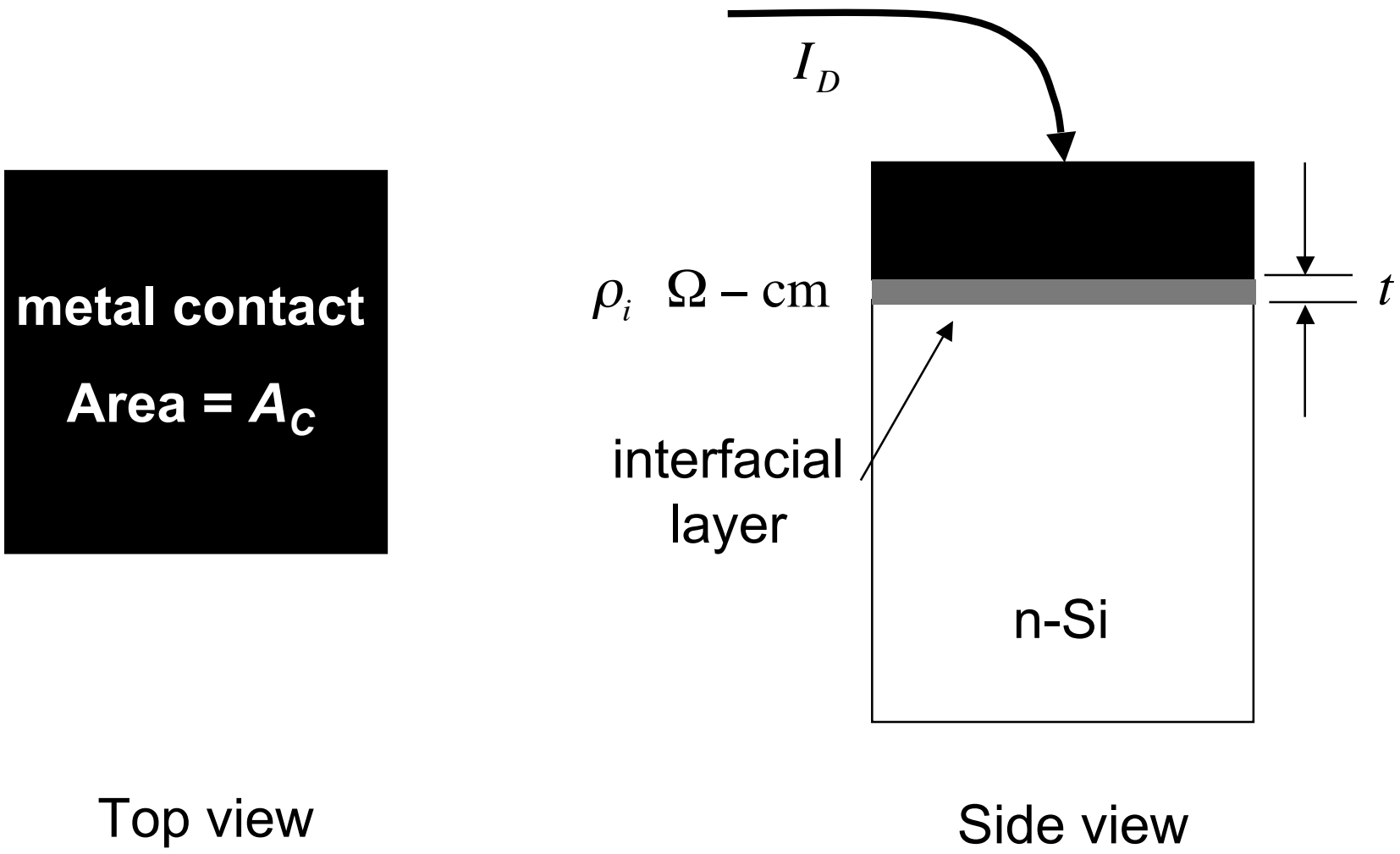


1) metal-semiconductor contact resistance
2) extension resistance
3) tip resistance
4) spreading resistance

outline

1) Effect on I-V
2) Series resistance components
3) **Metal-semiconductor resistance**
4) Other series resistance components
5) A look at the ITRS
6) effective channel length

metal-semiconductor contact resistance



metal-semiconductor contact resistance

$$R_{C0} = \frac{\rho_i t}{A_C} = \frac{\rho_C}{A_C}\,\Omega$$

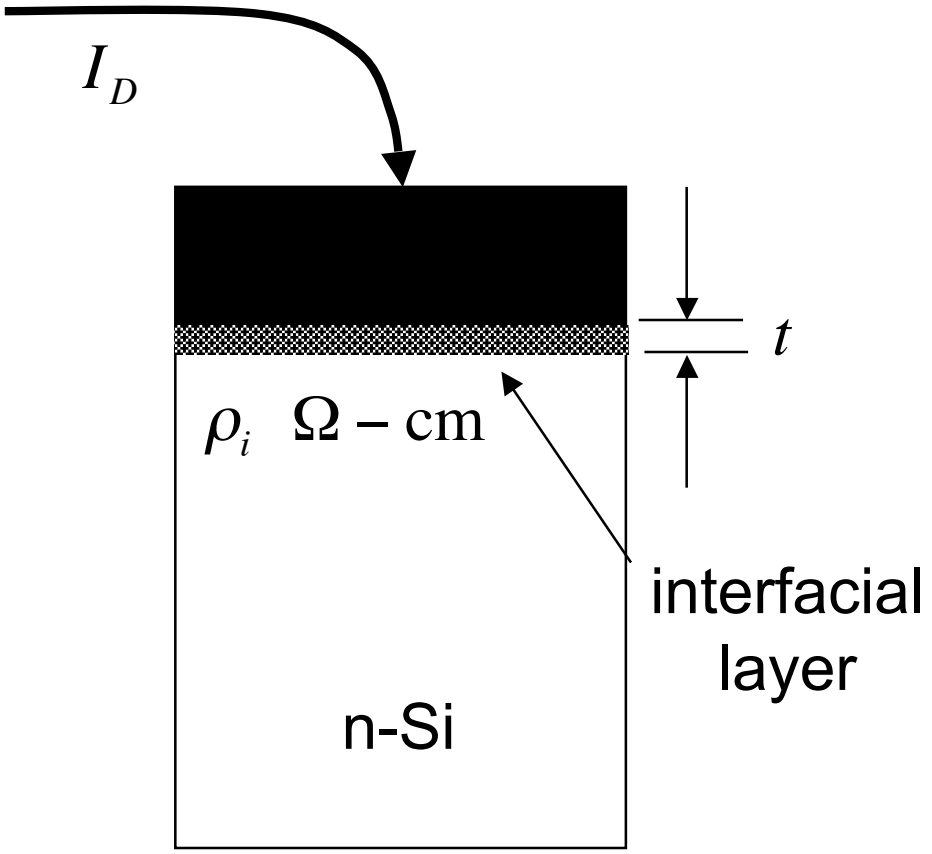
$$10^{-8} < \rho_C < 10^{-6}\ \Omega\text{-cm}^2$$

"interfacial contact resistivity"

$$A_C = 0.15\,\mu m \times 1.0\,\mu m$$

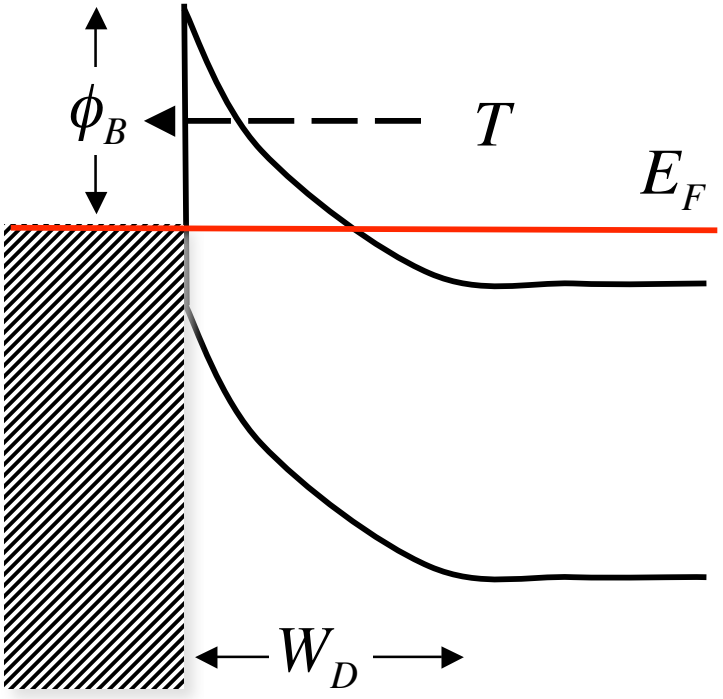
$$\rho_C = 10^{-7}\,\Omega\text{-cm}^2$$

$$R_{C0} = 66\,\Omega\text{-}\mu\text{m}$$



Side view

what determines the M-S contact resistance?



$$G_C \sim T$$

$$\rho_C \sim 1/T$$

$$T \sim e^{-\phi_B/\phi_0}$$

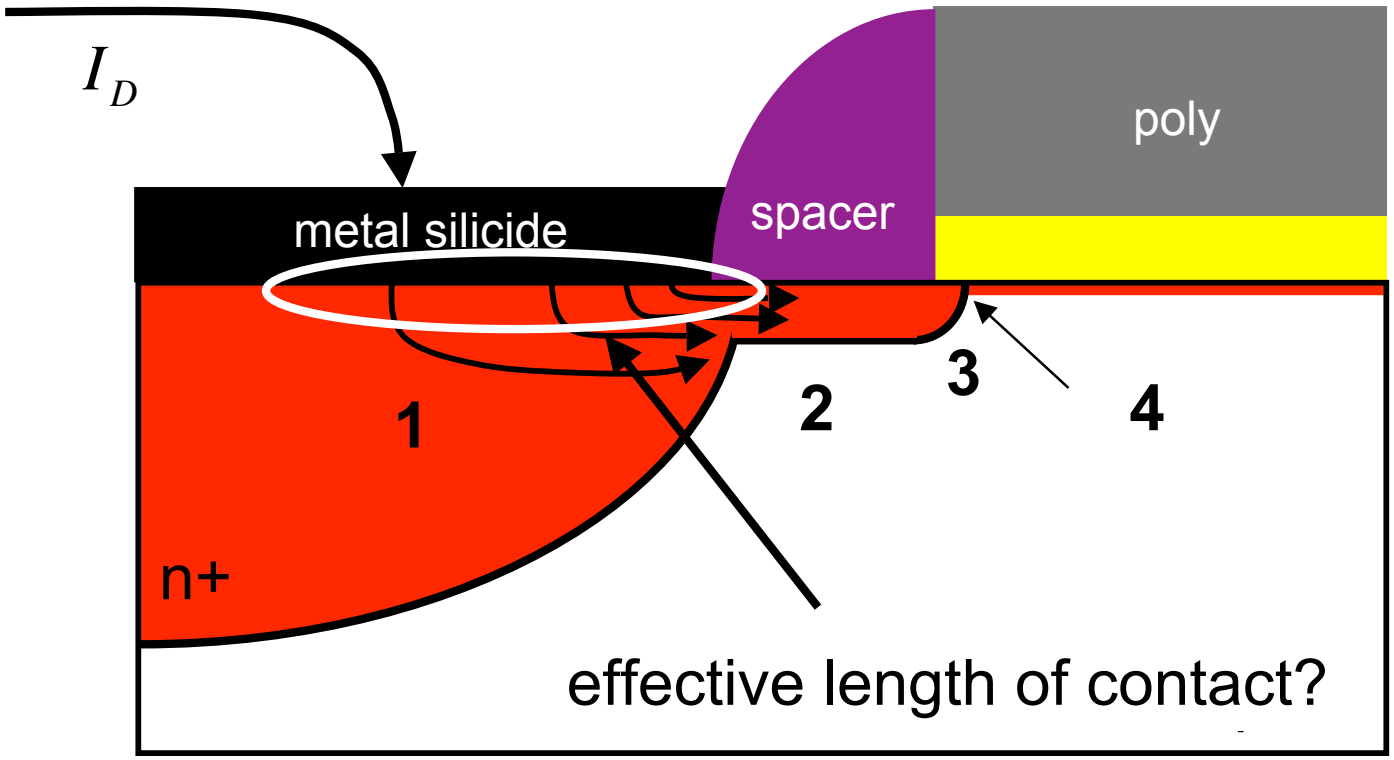
$$T \sim e^{-W_D/W_0}$$

$$W_D \sim 1/\sqrt{N_D}$$

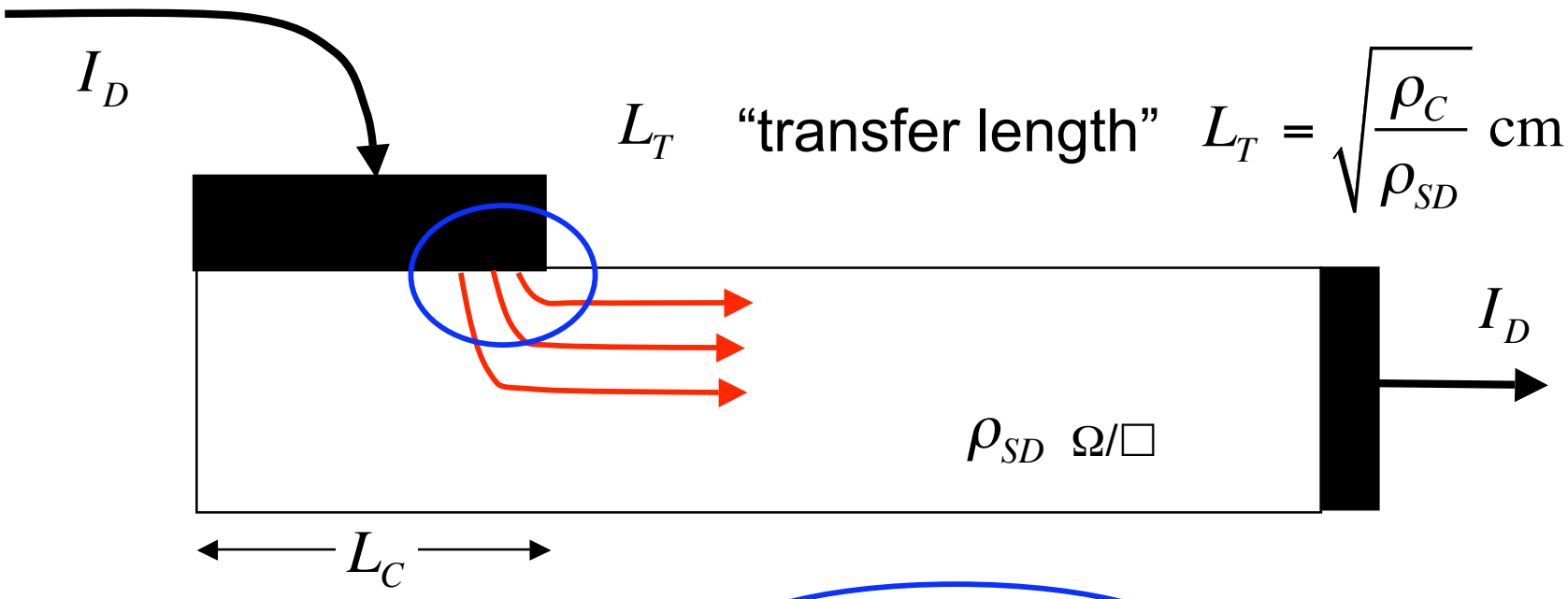
$$\rho_C \propto \exp\left[\frac{4\pi\phi_B}{qh}\sqrt{\frac{m^*\varepsilon_{Si}}{N_D}}\right]$$

(eqn. 5.11) of Taur and Ning)

lateral current flow



lateral current flow (ii)

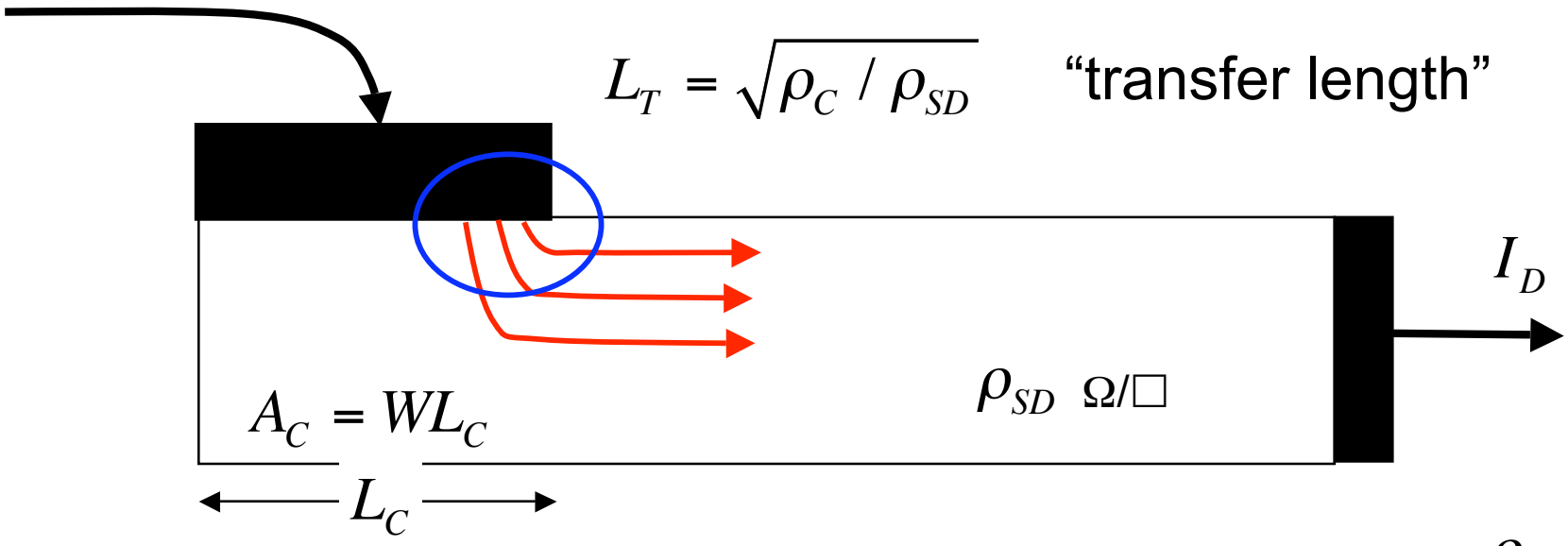


$A_C = WL_C$

(*W* into page)

$A_C(\text{eff}) < WL_C$

lateral current flow (iii)



$$R_{C0} = \frac{\sqrt{\rho_C \rho_{SD}}}{W} \coth\left(L_C / L_T\right)$$

Eqn. (5.8) Taur and Ning

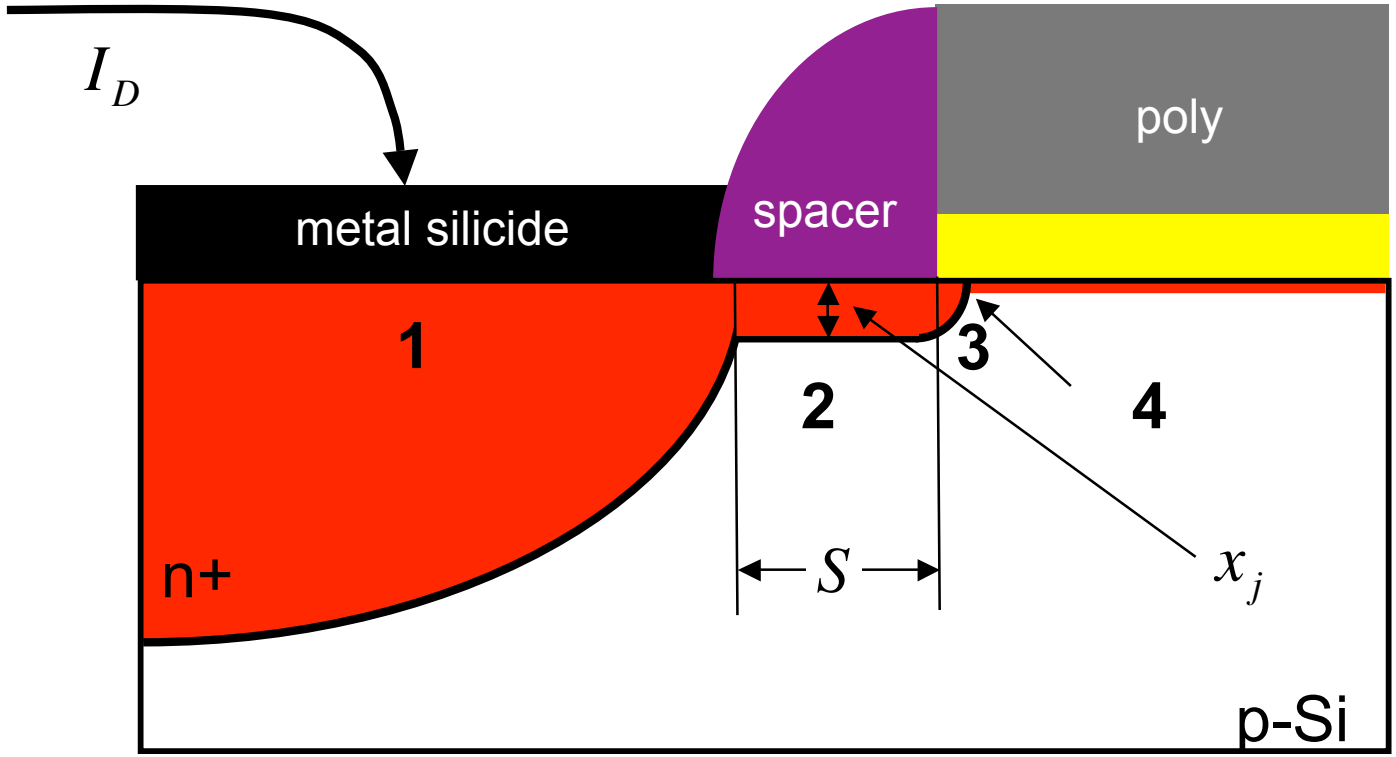
i) $L_C << L_T$: $R_{C0} = \dfrac{\rho_C}{L_C W}$

ii) $L_C >> L_T$: $R_{C0} = \dfrac{\rho_C}{L_T W}$

outline

1) Effect on I-V
2) Series resistance components
3) Metal-semiconductor resistance
4) **Other series resistance components**
5) A look at the ITRS
6) effective channel length

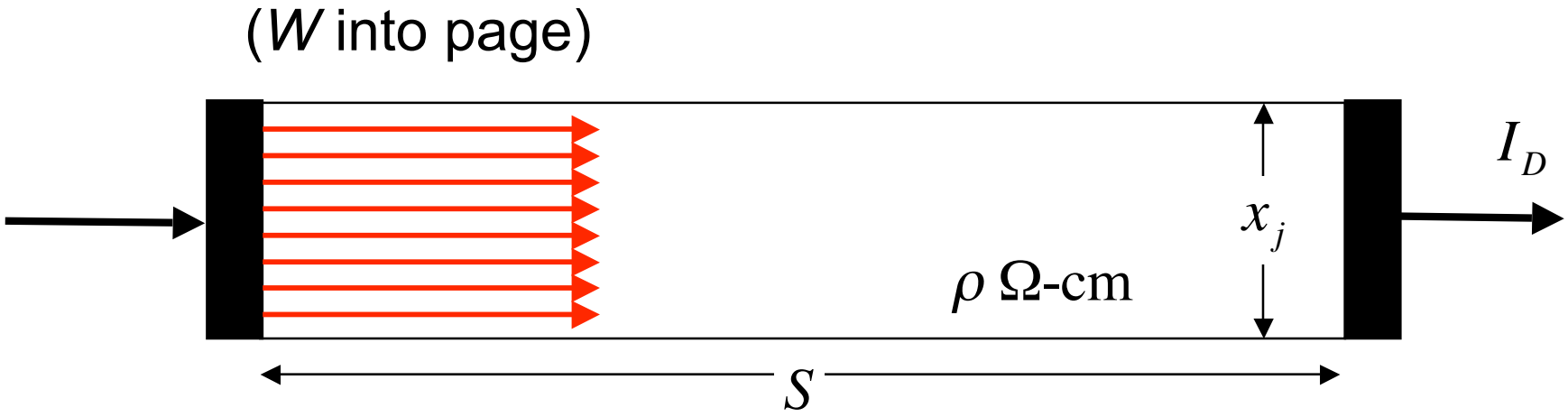
physical origin of R_{SD}



1) metal-semiconductor contact resistance
2) **extension resistance**
3) tip resistance
4) spreading resistance

resistance of the S/D extension

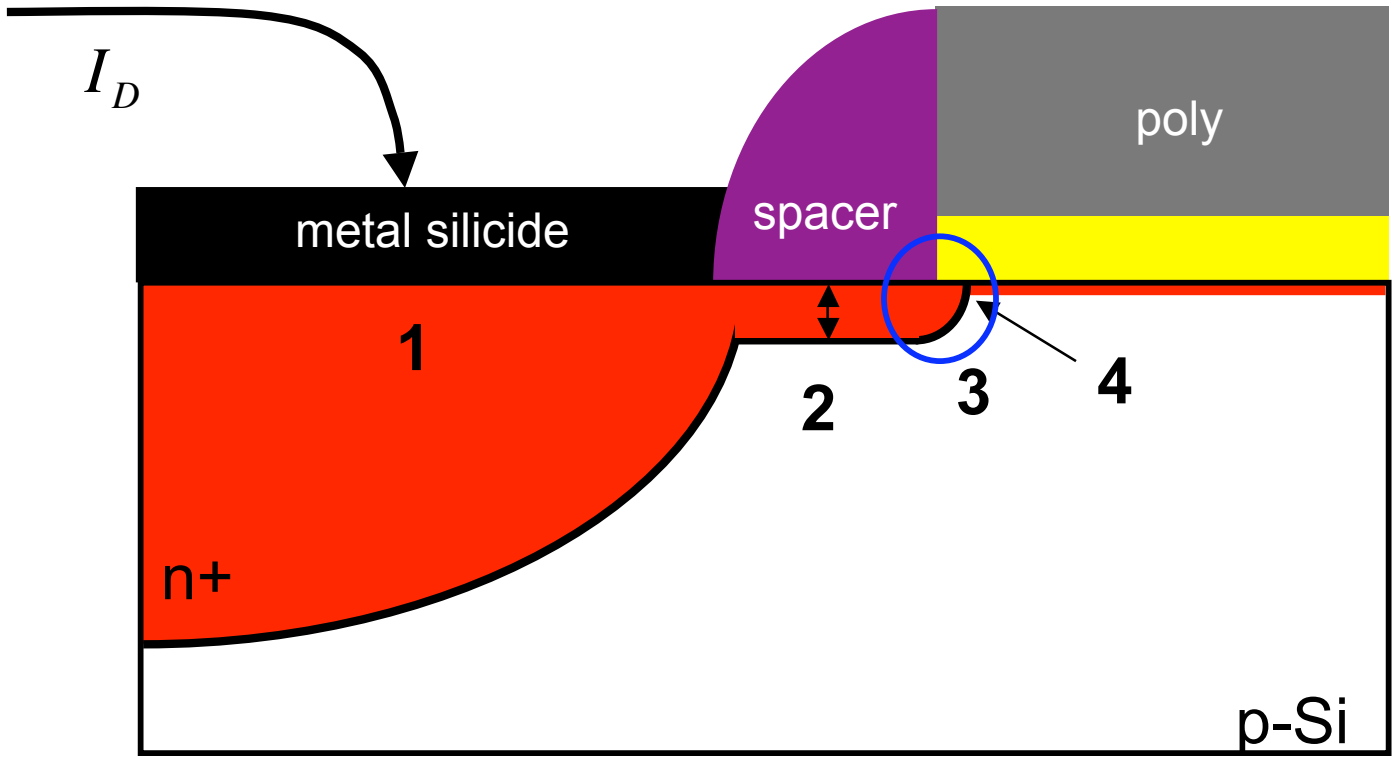
$$\rho = 1/\left(N_D q \mu_n\right)$$



$$R_{EXT} = \rho \frac{S}{x_j W} = \left(\frac{\rho}{x_j}\right) \frac{S}{W} = \rho_{EXT} \frac{S}{W}$$

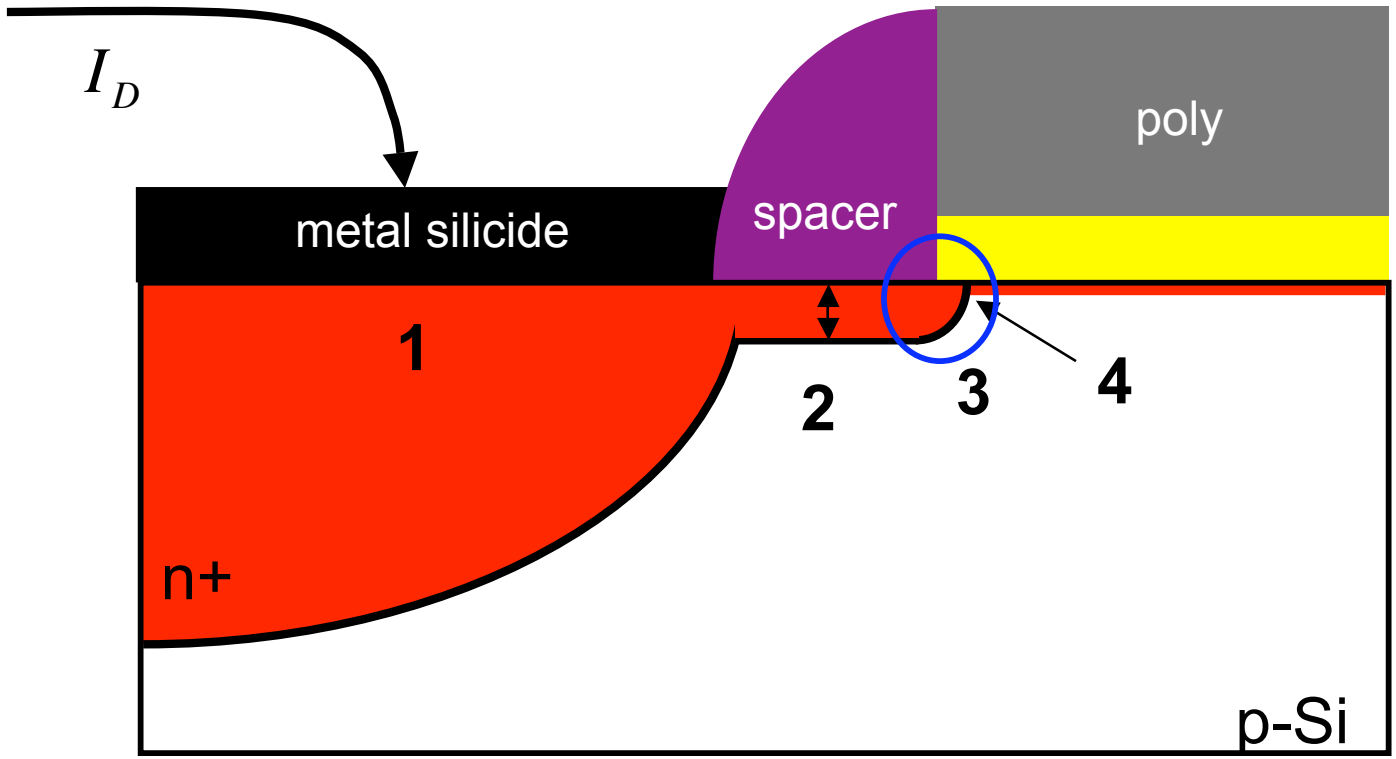
ρ_{EXT} Ω/□ sheet resistance of the S/D extensions

physical origin of R_{SD}



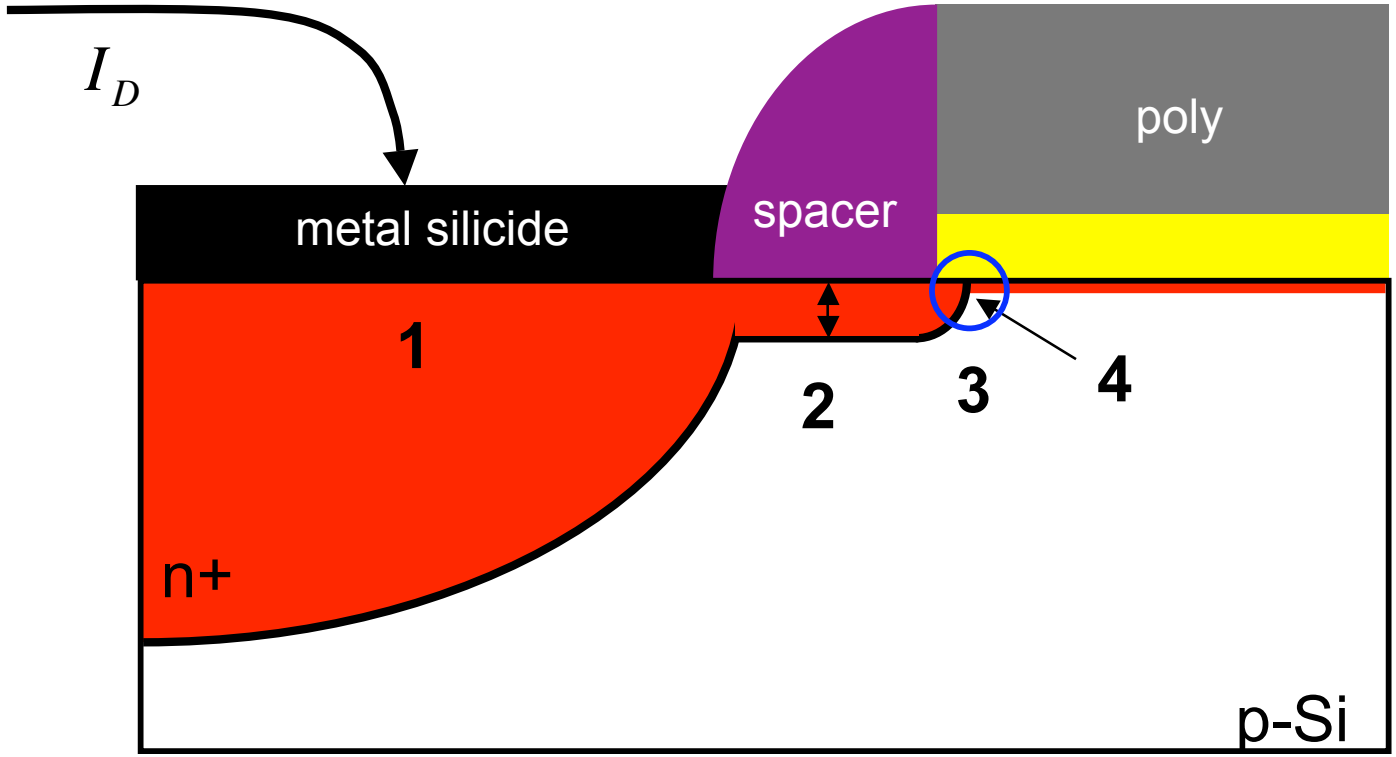
1) metal-semiconductor contact resistance
2) extension resistance
3) tip resistance
4) spreading resistance

physical origin of R_{SD}



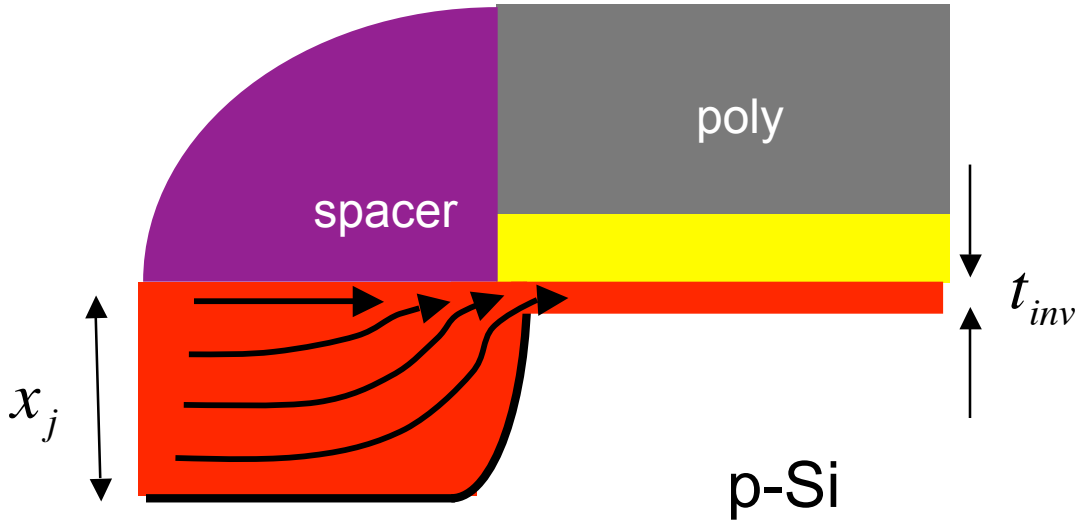
-tip resistance is controlled by the steepness of the junction
-steepness measured in nm/dec
-tip resistance is a significant part of R_{SD}

physical origin of R_{SD}



1) metal-semiconductor contact resistance
2) extension resistance
3) tip resistance
4) **spreading resistance**

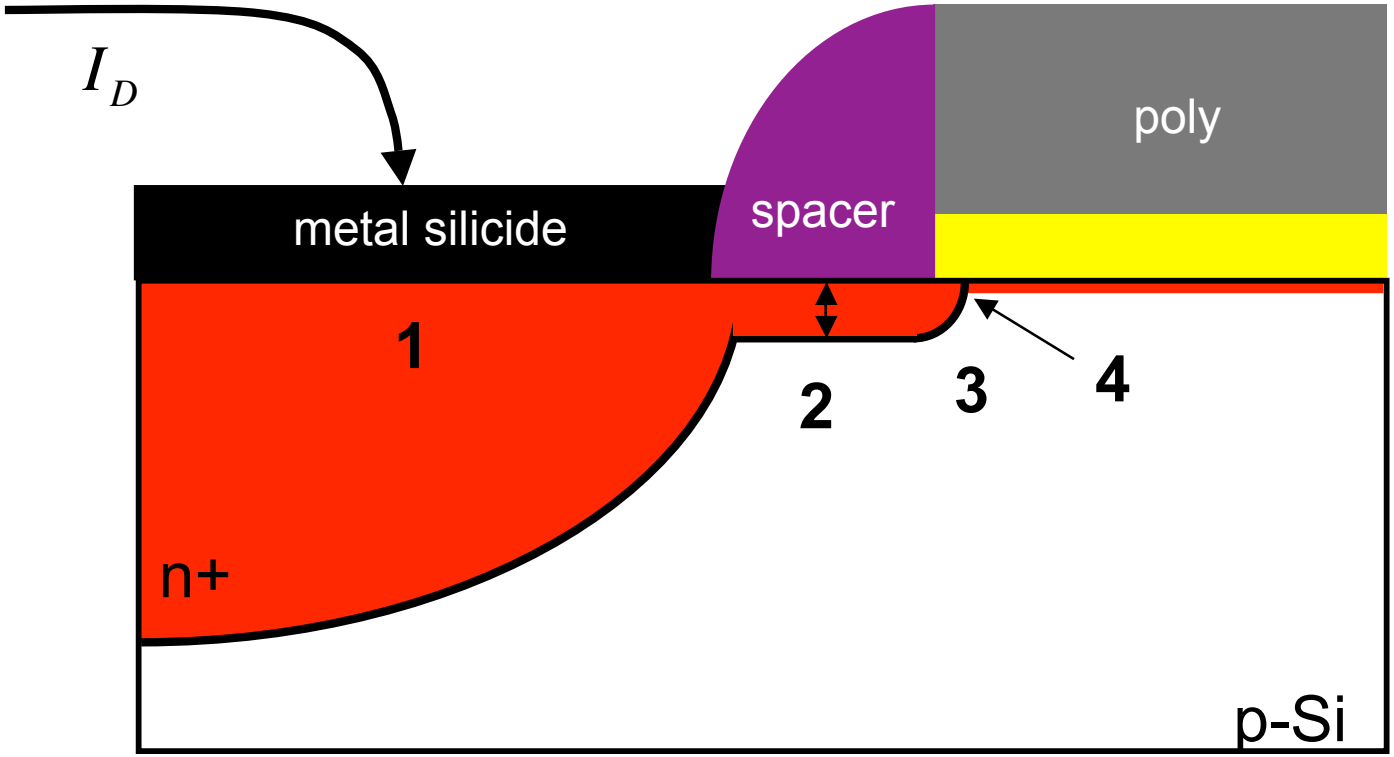
spreading resistance



$$R_{SPR} = \frac{2\rho}{\pi W} \ln\left(0.75 \frac{x_j}{t_{inv}}\right)$$

Eqn. (5.6) of Taur and Ning

components of R_{SD}



$$R_S = R_D = R_{C0} + R_{EXT} + R_{TIP} + R_{SPR}$$

summary: components of R_{SD}

$$R_S = R_D = R_{C0} + R_{EXT} + R_{TIP} + R_{SPR}$$

1) $$R_{C0} = \frac{\rho_C}{A_C(\text{eff})} \qquad A_C(\text{eff}) = W\left(\frac{L_T}{\coth(L_C / L_T)}\right)$$

$$L_T = \sqrt{\rho_C / \rho_{SD}}$$

2) $$R_{EXT} = \rho_{EXT}\frac{S}{W}$$

3,4) $R_{TIP} + R_{SPR}$ ‘link-up resistance’

outline

1) Effect on I-V
2) Series resistance components
3) Metal-semiconductor resistance
4) Other series resistance components
5) **A look at the ITRS**
6) Effective channel length

R_{SD} and the ITRS

12 Process Integration, Devices, and Structures

Table 40a High-Performance Logic Technology Requirements—Near-term (continued)

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
R_{sd}: Effective Parasitic series source/drain resistance [12]									
Planar Bulk (Ω-μm)	180	170	140	140	120	105	80	70	
UTB FD (Ω-μm)				155	140	125	110	90	75
DG (Ω-μm)							110	100	90

[12] Rsd is the maximum allowable parasitic series source plus drain resistance for a MOSFET of one micron width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow and red coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.

R_{SD} and the ITRS (ii)

Table 69a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term Years

Grey cells indicate the requirements projected only for near, intermediate, or long-term years.

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Drain extension X_j (nm) for bulk MPU/ASIC [F]	11	9	7.5	7.5	7	6.5	5.8	4.5	
Maximum allowable parasitic series resistance for bulk NMOS MPU/ASIC × width (Ω–μm) [G]	180	170	140	140	120	105	80	70	
Maximum drain extension sheet resistance for bulk MPU/ASIC (NMOS) (Ω/sq) [G]	653	674	640	740	677	650	548	593	
Extension lateral abruptness for bulk MPU/ASIC (nm/decade) [H]	3.5	3.1	2.8	2.5	2.2	2.0	1.8	1.5	
Contact X_j (nm) for bulk MPU/ASIC [I]	35.2	30.8	27.5	25.3	22	19.8	17.6	15.4	
Allowable junction leakage for bulk MPU/ASIC (μA/μm)	0.06	0.15	0.2	0.2	0.22	0.28	0.32	0.34	
Sidewall spacer thickness (nm) for bulk MPU/ASIC [J]	35.2	30.8	27.5	25.3	22	19.8	17.6	15.4	
Maximum silicon consumption for bulk MPU/ASIC (nm) [K]	17.6	15.4	13.8	12.7	11.0	9.9	8.8	7.7	
Silicide thickness for bulk MPU/ASIC (nm) [L]	21	19	17	15	13	12	11	9	
Contact silicide sheet R_s for bulk MPU/ASIC (Ω/sq) [M]	7.5	8.6	9.6	10.5	12.1	13.5	15.1	17.3	
Contact maximum resistivity for bulk MPU/ASIC (Ω-cm^2) [N]	1.6E-07	1.3E-07	9.5E-08	8.3E-08	6.2E-08	4.7E-08	3.2E-08	2.5E-08	

R_{SD} and the ITRS (ii)

[G] The maximum allowable parasitic series resistance for NMOS devices comes from the PIDS device design. The allowable resistance for PMOS is taken to be 2.2 times the NMOS values. The maximum drain extension sheet resistance is modeled by **allocating 15% of the allowable source and drain parasitic resistances to the drain extensions**. …The drain extension sheet resistance value must be optimized together with the contact resistance and junction lateral abruptness (which affects spreading resistance), in order to meet the overall parasitic resistance requirements. This is a relatively crude model and the resultant sheet resistance values should only be used as a guide.

[H] **Channel abruptness** in nm per decade drop-off in doping concentration) = 0.11 * Physical Gate Length based on Short Channel effect. This lateral abruptness is consistent with a 3 decade fall off of doping over the lateral extent of the junction, which is taken to be 60% of the vertical junction depth. …

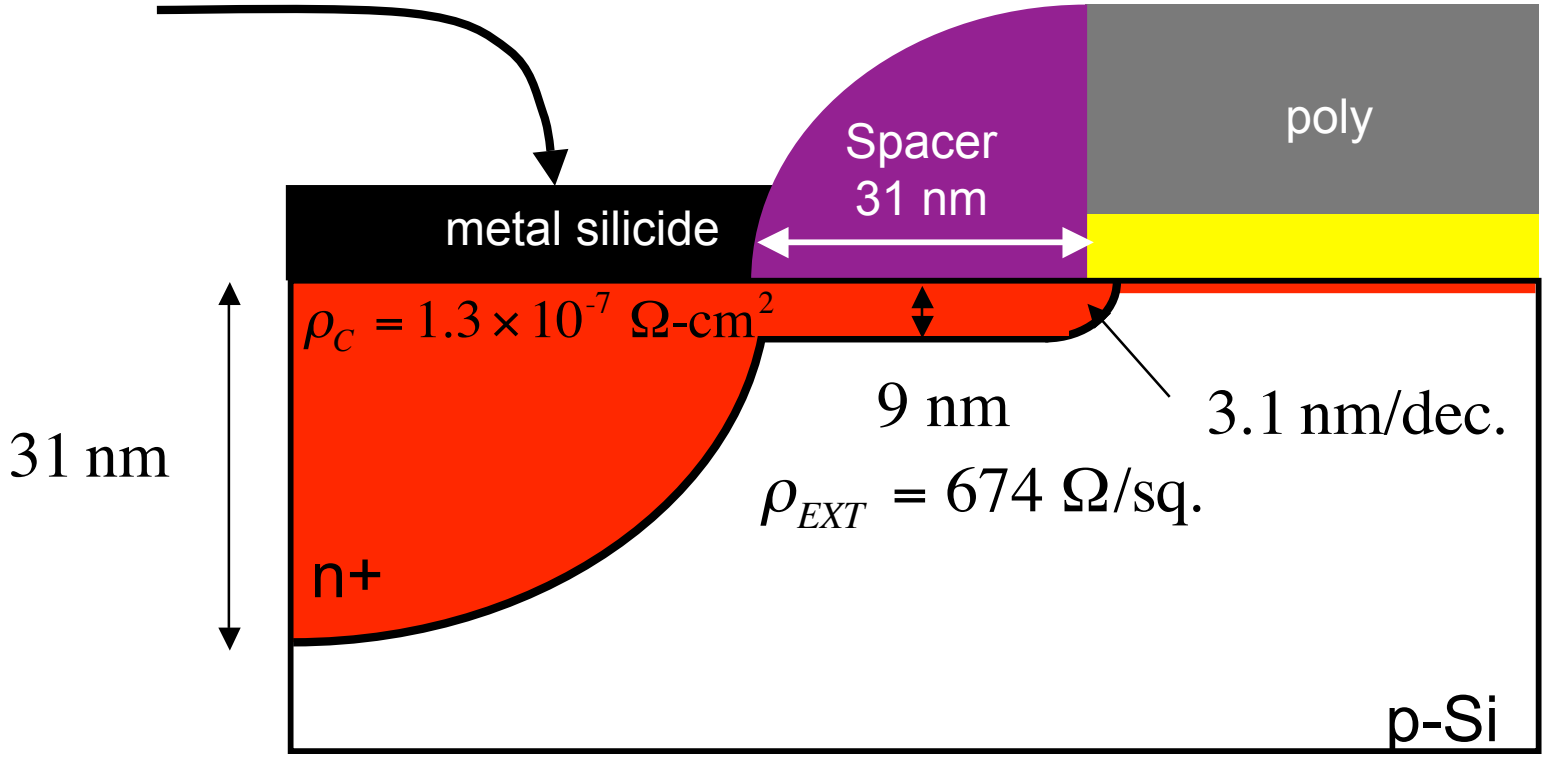
R_{SD} and the ITRS (iii)

[I] **Contact Junction Depth** = 1.1*Physical Gate Length (with a range of +/-33%) for Bulk devices. Junction depths for NMOS and PMOS are the same.

[J] **Spacer thickness** (width) is taken as the same as the Contact Junction Depth, namely 1.1 × Lgate, for bulk devices…

[N] The Si/Silicide **maximum interfacial contact resistivity** values were calculated assuming that 100% of the PIDS total allowed MOSFET Source/Drain resistance is allocated to the contact resistivity. It further assumes that the transistor contact length is taken to be twice the MPU half pitch, where length is in the direction of current flow. …These values should be appropriately modified if different transistor contact lengths are assumed… The values of contact resistivity, drain extension sheet resistance, and drain extension lateral abruptness must be co-optimized in order to meet the overall parasitic resistance requirements.

structure of 70nm node MOSFET



components of R_S at the 70 nm node

$$R_S = R_D = R_{C0} + R_{EXT} + R_{TIP} + R_{SPR}$$

$$L_T = \sqrt{\rho_C / \rho_{SD}} = \sqrt{1.3 \times 10^{-7} / 674} = 139 \text{ nm}$$

$$L_C = 2 \times 78 = 156 \text{ nm}$$

$$A_C(\text{eff}) = W\left(\frac{L_T}{\coth(L_C / L_T)}\right) = 0.83 L_T W = 1.15 \times 10^{-9} \text{ cm}^2$$

$$R_{C0} = \frac{\rho_C}{A_C(\text{eff})} = \frac{1.3 \times 10^{-7}}{1.15 \times 10^{-9}} = 113\ \Omega - \mu m \qquad \left(R_{SD}(\text{ITRS}) = 170\ \Omega\right)$$

components of R_S at the 70 nm node (ii)

$$R_S = R_D = R_{C0} + R_{EXT} + R_{TIP} + R_{SPR}$$

$$R_{EXT} = \rho_{EXT}\frac{S}{W} = 674 \times \frac{31\,\text{nm}}{1000\,\text{nm}} = 21\,\Omega - \mu m$$

$$R_{SD}(\text{ITRS}) = 170\ \Omega$$

$$2R_{EXT} \approx 25\% \text{ of } R_{SD}(\text{ITRS})$$

components of R_S at the 70 nm node (iii)

$$R_S = R_D = R_{C0} + R_{EXT} + R_{TIP} + R_{SPR}$$

$$R_S = R_D = 113 + 21 + R_{TIP} + R_{SPR}$$

$$R_{SD}(\text{ITRS}) = 170\ \Omega$$

also significant, but hard to estimate

How do these components scale?

scaling of R_{ON}

$$R_{ON} = \frac{V_{DD}}{I_{ON}} \rightarrow \frac{V_{DD}/\kappa}{I_{ON}/\kappa} \qquad R_{ON} \rightarrow R_{ON}$$

In practice, R_{ON} is ***decreasing***

need R_S < 10% R_{ON}

How does R_S scale?

scaling of R_S

$$R_S = R_{C0} + R_{EXT} + R_{TIP} + R_{SPR}$$

$$R_{C0} = \frac{\rho_C}{A_C(\text{eff})} \rightarrow \frac{\rho_C}{A_C(\text{eff})/\kappa^2} \qquad R_{C0} \rightarrow \kappa^2 R_{C0}$$

$$R_{EXT} = \rho_{EXT}\frac{S}{W} \rightarrow \kappa\,\rho_{EXT}\frac{S/\kappa}{W/\kappa} \qquad R_{EXT} \rightarrow \kappa R_{EXT}$$

ρ / x_j

R_S increases with scaling!

scaling of R_{ON}

$$R_{ON} = \frac{V_{DD}}{I_{ON}} \rightarrow \frac{V_{DD}/\kappa}{I_{ON}/\kappa} \qquad R_{ON} \rightarrow R_{ON}$$

In practice, R_{ON} is ***decreasing***

need R_S < 10% R_{ON}

How does R_S scale?

outline

1) Effect on I-V
2) Series resistance components
3) Metal-semiconductor resistance
4) Other series resistance components
5) A look at the ITRS
6) **Effective channel length**

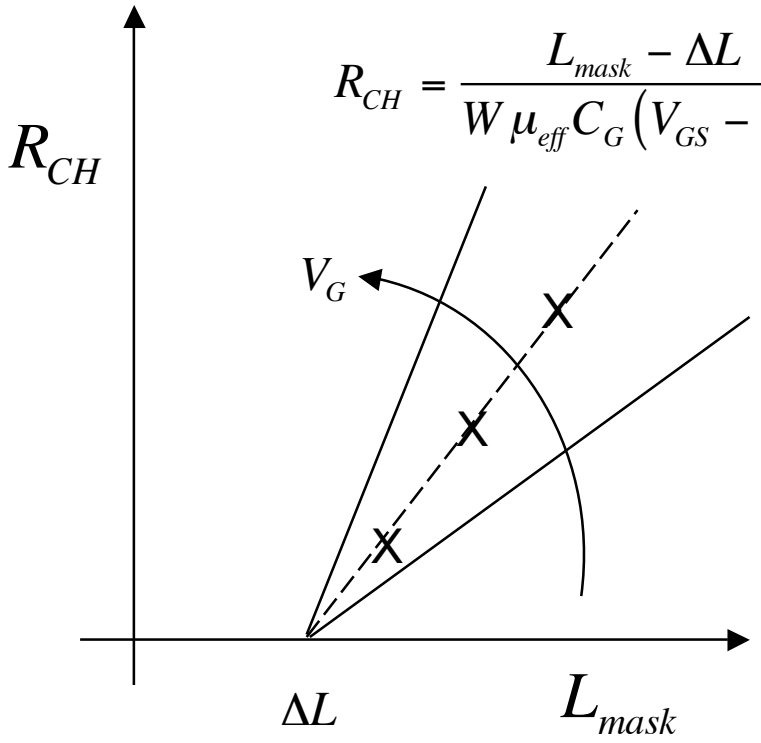
effective channel length

$$I_D = \frac{W}{L_{eff}} \mu_{eff} C_G \left(V_{GS} - V_T \right) V_{DS} = V_{DS} / R_{CH}$$

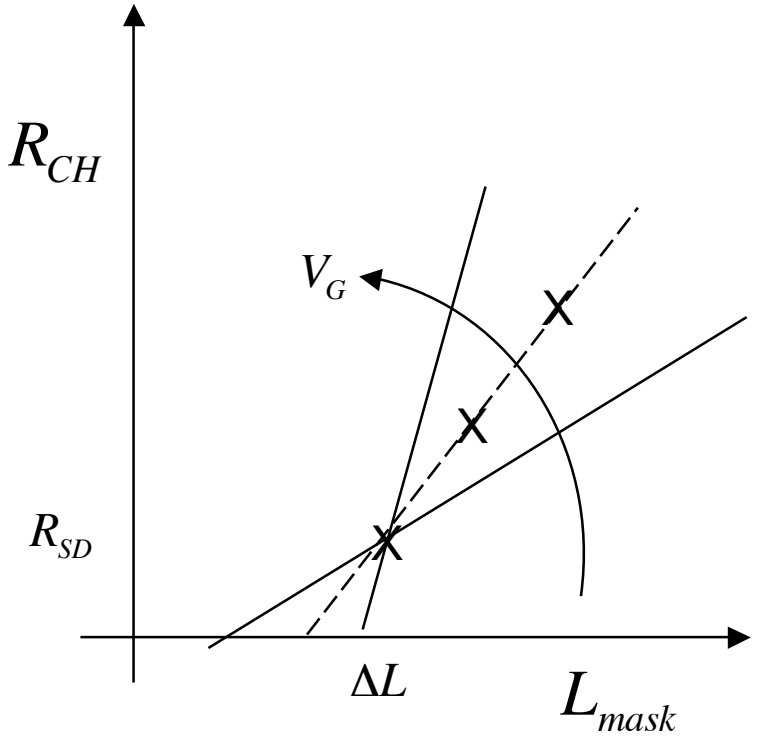
$$\frac{V_{DS}}{I_D} = R_{CH} = \frac{L_{eff}}{W \mu_{eff} C_G \left(V_{GS} - V_T \right)} = \frac{L_{mask} - \Delta L}{W \mu_{eff} C_G \left(V_{GS} - V_T \right)}$$

measuring Leff

$$R_{CH} = \frac{L_{mask} - \Delta L}{W \mu_{eff} C_G \left(V_{GS} - V_T \right)}$$



with series resistance



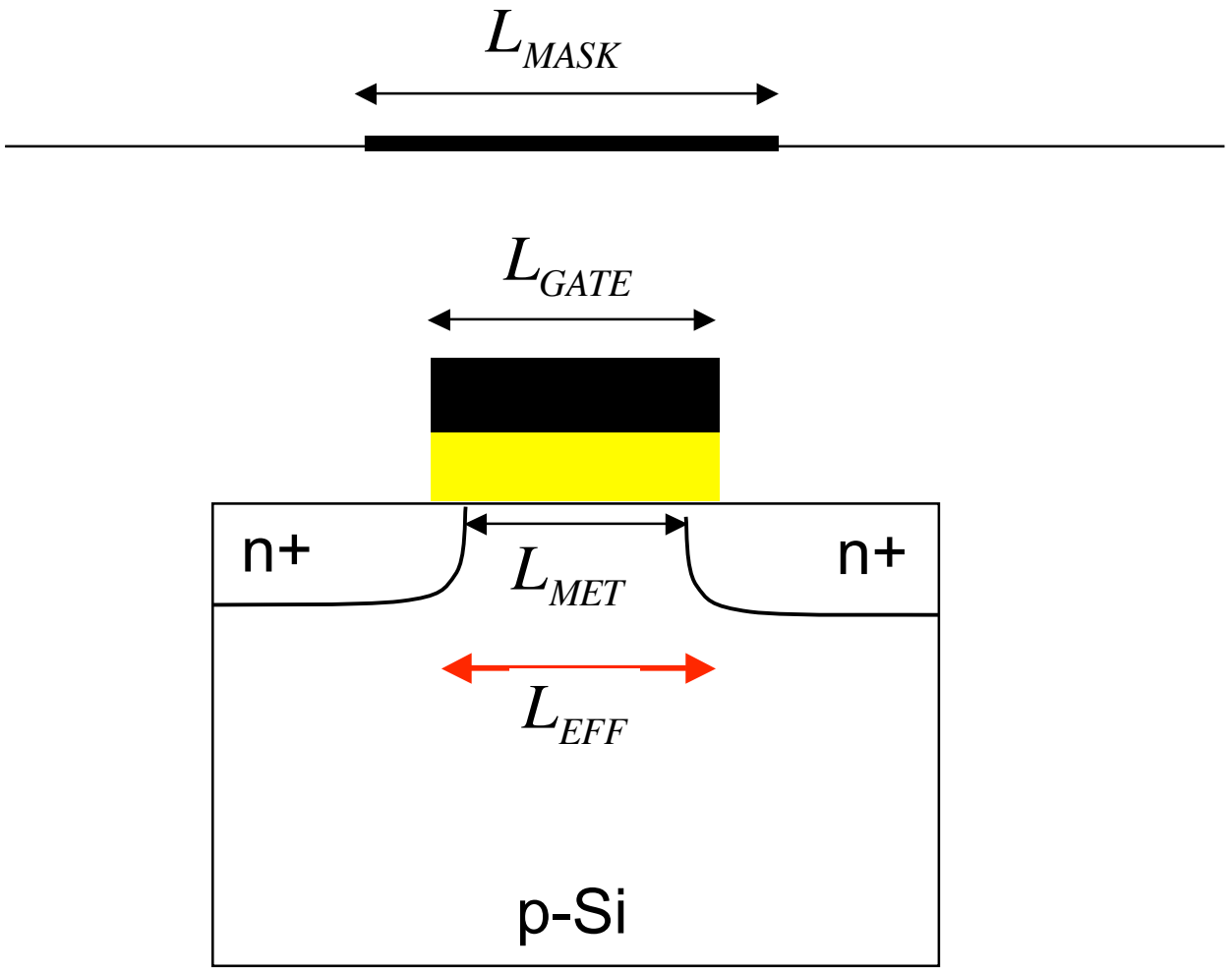
what is Leff?

"measure of gate-controlled current"

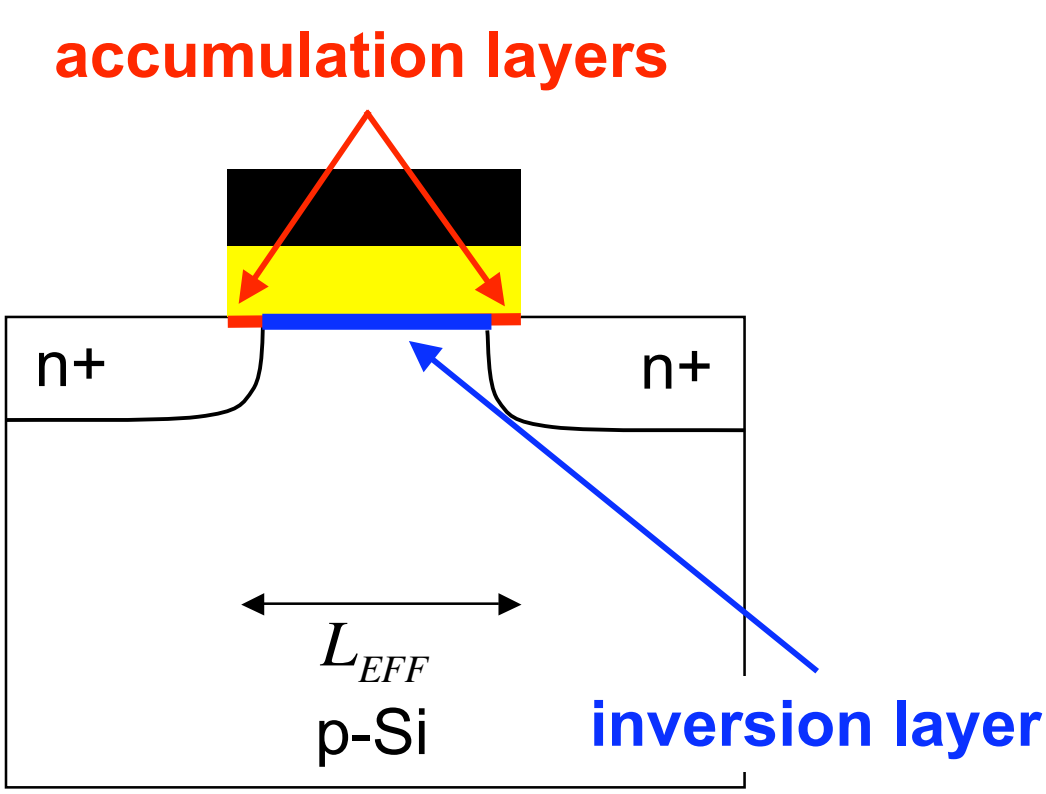
Y. Taur, *IEEE Trans. Electron Devices*, **47**, pp. 160-170, 2000

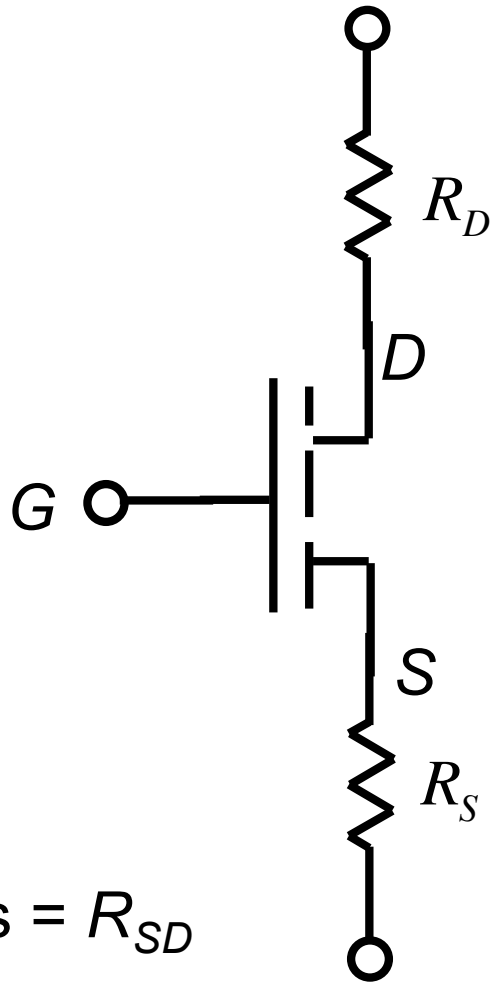
See also, Taur and Ning, pp. 202-221

various channel lengths



physical interpretation





gate voltage independent resistances = R_{SD}

physical interpretation

when sheet resistance underneath the accumulation layer is less than the sheet resistance of the accumulation layer, current spreads into the bulk n+ region and the channel ends.

outline

1) Effect on I-V
2) Series resistance components
3) Metal-semiconductor resistance
4) Other series resistance components
5) A look at the ITRS
6) Effective channel length