EE-612: Lecture 21: Gate resistance and Interconnects

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Lundstrom EE-612 F06
outline

1) Gate Resistance
2) Interconnects
3) ITRS
review: parasitic series $R$

Why did we not consider an $R_G$?
effect of a gate resistance (AC)

\[ V_G(t) = \left(1 - e^{-t/\tau}\right) \]

\[ \tau = R_G C_G \]

\[ 0.5 = \left(1 - e^{-\tau_G/\tau}\right) \]

\[ \tau_G = 0.69 R_G C_G \]
gate resistance

\[ R_G \]

\[ V_{DD} \]

\[ D \]

\[ S \]

\[ I_g \]

\[ L \]

\[ W \]
gate resistance (ii)

\[ R_G = \rho_G \frac{W}{L} \]

\[ R_G = \left( \frac{\rho_G}{L} \right) W = R_L W \]

\[ C_G = C_{ox} L W \]

\[ C_G = (C_{ox} L) W = C_L W \]
distributed gate resistance

The part of the channel closest to the contact turns on first.
distributed gate resistance (ii)

\[ \Delta V = I R_L dz \]

\[ \frac{\Delta V}{dz} = - \frac{\partial V}{\partial z} = I R_L \]

\[ \frac{\partial V}{\partial z} = -I R_L \quad (1) \]
distributed gate resistance (iii)

\[ R_L dz \quad I \quad I - \Delta I \quad R \quad R \]

\[ - \Delta V + \quad \Delta I \quad C_L dz \]

\[ \Delta I = C_L dz \frac{\partial V}{\partial t} \]

\[ \frac{\Delta I}{dz} = - \frac{\partial I}{\partial z} = C_L \frac{\partial V}{\partial t} \]

\[ \frac{\partial I}{\partial z} = - C_L \frac{\partial V}{\partial t} \quad (2) \]
distributed gate resistance (iii)

\[
\frac{\partial V}{\partial z} = -I R_L \quad (1)
\]

\[
\frac{\partial I}{\partial z} = -C_L \frac{\partial V}{\partial t} \quad (2)
\]

\[
\frac{\partial^2 V}{\partial z^2} = -R_L \frac{\partial I}{\partial z}
\]

\[
\frac{\partial^2 V}{\partial z^2} = R_L C_L \frac{\partial V}{\partial t}
\]

\[
\frac{\partial V(z,t)}{\partial t} = \frac{1}{R_L C_L} \frac{\partial^2 V(z,t)}{\partial z^2}
\]
distributed gate resistance (iii)

recall:
\[
\frac{\partial n(z,t)}{\partial t} = D_n \frac{\partial^2 n(z,t)}{\partial z^2}
\]

“minority carrier diffusion equation”

\[
\frac{\partial V(z,t)}{\partial t} = \frac{1}{R_L C_L} \frac{\partial^2 V(z,t)}{\partial z^2} = D_{\text{eff}} \frac{\partial^2 V(z,t)}{\partial z^2}
\]

\[D_{\text{eff}} = \frac{1}{R_L C_L}\]

units:
\[
\frac{1}{\Omega/\text{cm} \times \text{F/cm}} = \frac{\text{cm}^2}{\text{V/A} \times \text{C/V}} = \frac{\text{cm}^2}{\text{C/A}} = \frac{\text{cm}^2}{\text{sec}}
\]
distributed gate resistance (iv)

recall: \[ \tau_B = \frac{W_B^2}{2D_n} \] “base transit time”

\[ \tau_g = 0.5R_CLW^2 \]
distributed gate resistance and scaling

\[ \tau_g = 0.5 R_L C_L W^2 \]

\[ R_L = \frac{\rho_G}{L} \quad \rho_G \sim 2-10 \ \Omega/\text{sq.} \]
\[ C_L = C_{OX} L \]

behavior with scaling:

\[ R_L \rightarrow \frac{\rho_G}{L} \left( \frac{L}{\kappa} \right) = \kappa R_L \]
\[ C_L \rightarrow \left( \kappa C_{OX} \right) \left( \frac{L}{\kappa} \right) = C_L \]
\[ \tau_g \rightarrow \kappa \tau_g \]

device delay:

\[ \tau \rightarrow \frac{\tau}{\kappa} \]
outline

1) Gate Resistance
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interconnects

\[ V_{\text{IN}} \rightarrow V_{\text{OUT}} \rightarrow \text{fanout circuits} \]

\[ L_w \]
interconnect capacitance

\[ C_{Wire} = C_{ins} W_w L_w \]
\[ C_{ins} = \varepsilon_{ins} / t_{ins} \]

\[ C_{Wire} = (C_{ins} W_w) L_w = C_W (PP) L_W \]
interconnect capacitance (ii)

\[ C_{Wire} = \left[ C_W(PP) + C_W(FF) \right] L_W \]
interconnect capacitance (ii)

(see Fig. 5.21, Taur and Ning)
interconnect capacitance (ii)

\[ C_{\text{Wire}} = \left[ C_W(\text{PP}) + C_W(\text{FF}) + C(\text{WW}) \right] L_W \]

(see Fig. 5.22, Taur and Ning)

SiO$_2$ assumed

\[ C_W(\text{tot}) \]

\[ C_W(\text{PP}) \]

2 pF/cm

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interconnect delay

\[ \tau_w = 0.5 R_W C_w L_w^2 \]
interconnect scaling

\[ \tau_W = 0.5 R_W C_W L_W^2 \]

\[ C_W = C_W(\text{PP}) + C_W(\text{FF}) + C_W(\text{WW}) \]

\[ R_W = \frac{\rho_W}{W_w t_w} \]

\[ \rho_{Al} \approx 3 \times 10^{-6} \text{ } \Omega\text{-cm} \]

\[ \rho_{Cu} \approx \rho_{Al} / 1.5 \]

**scaling by factor, \( \kappa > 1 \)**

\[ C_W = C_{ins} W_w + C_W(\text{FF}) \rightarrow C_W \]

\[ R_W = \rho_W / (W_w t_w) \rightarrow \kappa^2 R_W \]

\[ J_W = I / (W_w t_w) \rightarrow \kappa J_W \text{ (A/cm}^2 \text{)} \] (electromigration)

\[ \tau_W = 0.5 R_W C_W L_W^2 \rightarrow \tau_W \] (device \( \tau \) is decreasing)
local interconnects

\[ L_w \rightarrow L_w / \kappa \quad \tau_w = 0.5 R_w C_w L_w^2 \rightarrow \tau_w \]

Is this an issue? Assume:

\[ C_w \approx 2\pi \varepsilon_{ins} \text{ F/cm} \quad \text{Eqn. (5.27) Taur and Ning} \]

\[ \tau_w \approx \pi \varepsilon_{ins} \rho_w \frac{L_w^2}{W_w t_w} \approx \left(3 \times 10^{-18} \text{ s}\right) \frac{L_w^2}{W_w t_w} \quad \text{Eqn. (5.29) (5.30)} \]

for \( W_w = t_w = 0.25 \mu m \) and \( L_w = 100 \mu m, \tau_w = 0.5 \text{ps} \)

for a 0.25 micron technology, an inverter delay is \( \sim 20 \text{ ps} \)

\textbf{local interconnect delays are not an issue}
global interconnects

\[ L_W \rightarrow L_W \quad \text{(approximately the size of the chip)} \]

\[ \tau_W = 0.5 R_W C_W L_W^2 \rightarrow \kappa^2 \tau_W \]

Is this an issue?

for a 0.25 micron technology:

\[ \tau_W \approx \pi \varepsilon_{\text{ins}} \rho_w \frac{L_W^2}{W_w t_w} \approx (3 \times 10^{-18} \text{ s}) \frac{L_W^2}{W_w t_w} \approx 1 \text{ ns} \]

\[ \tau_W >> \tau_{\text{Gate}} >> \tau_{\text{Device}} \]

global interconnect delays are a very big issue
global interconnect scaling solutions

\[ \tau_W = 0.5 R_W C_W L_W^2 \]

\[ C_W = C_W(PP) + C_W(FF) + C_W(WW) \]

(low-k dielectrics)

\[ R_W = \frac{\rho_W}{W_w t_w} \]

1) switch from Al metal to Cu \[ \rho_{Cu} \approx \rho_{Al} / 1.5 \]

2) increase cross-sectional area \[ A_W = W_w t_w \]
wiring hierarchy

$$\tau_W = 0.5 R_W C_W L_w^2$$

$$\tau_W = \frac{L_w}{2 / R_W C_W L_w}$$

$$\tau_W = \frac{L_W}{\nu_{Diff}}$$

$$\nu_{Diff} = 2 D_{eff} / L_w$$

after Fig. 5.24, Taur and Ning
\[ \tau_W = 0.5 R_W C_W L_W^2 \]
\[ \tau_W = \frac{L_W}{\nu_{\text{Signal}}} \]

**RC line:**
\[ \nu_{\text{Signal}} = \frac{2D_{\text{eff}}}{L_W} \]

**RLC line:**
\[ \nu_{\text{Signal}} < \frac{c}{n} \]
outline

1) Gate Resistance
2) Interconnects
3) ITRS
interconnects at the 70 nm node (MPU)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal 1 pitch</td>
<td>156 nm</td>
</tr>
<tr>
<td>Metal 1 A/R</td>
<td>1.7</td>
</tr>
<tr>
<td>$J_{\text{MAX}}$</td>
<td>$1.37 \times 10^6$ A/cm²</td>
</tr>
<tr>
<td>No. of metal layers</td>
<td>11</td>
</tr>
<tr>
<td>Inter-level dielectric</td>
<td>$\kappa &lt; 2.7$</td>
</tr>
<tr>
<td>Total IC length (metal 1 +5)</td>
<td>1212 m/cm²</td>
</tr>
<tr>
<td>$L_W$ for $RC = \tau$:</td>
<td>43 µm</td>
</tr>
<tr>
<td>$\tau_W$ for $L_W = 1$ mm metal 1:</td>
<td>612 ps</td>
</tr>
</tbody>
</table>

ITRS (2005 edition)
interconnects trends

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