

EE-612: Lecture 21: Gate resistance and Interconnects

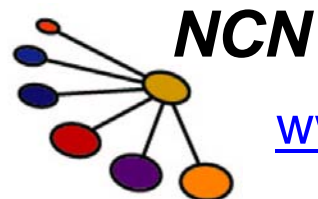
Mark Lundstrom

Electrical and Computer Engineering

Purdue University

West Lafayette, IN USA

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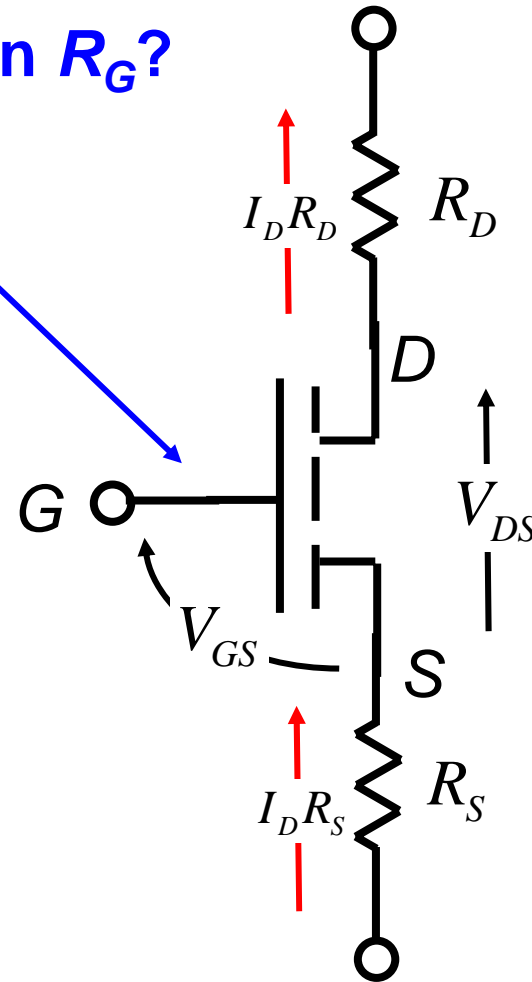
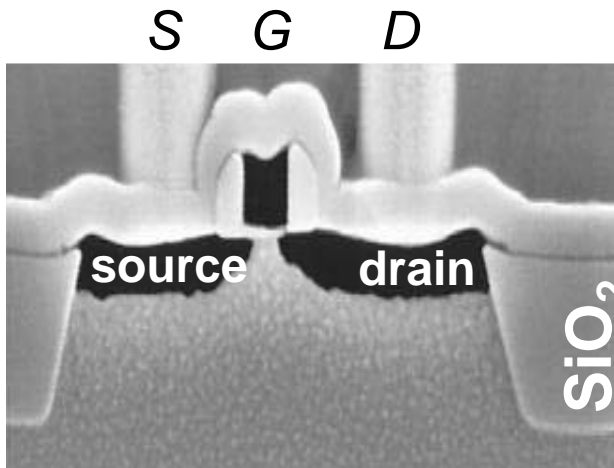
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outline

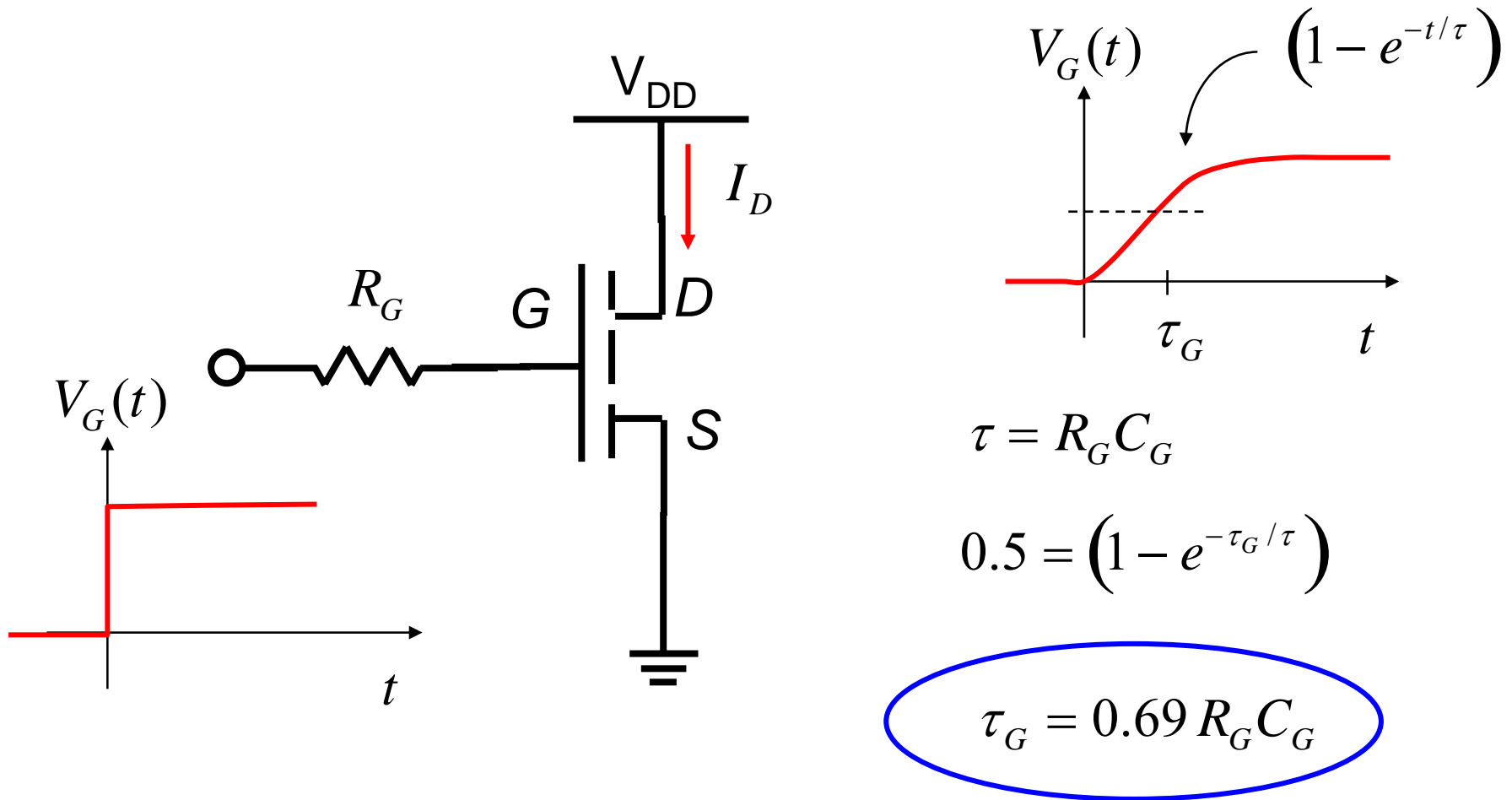
- 1) Gate Resistance
- 2) Interconnects
- 3) ITRS

review: parasitic series R

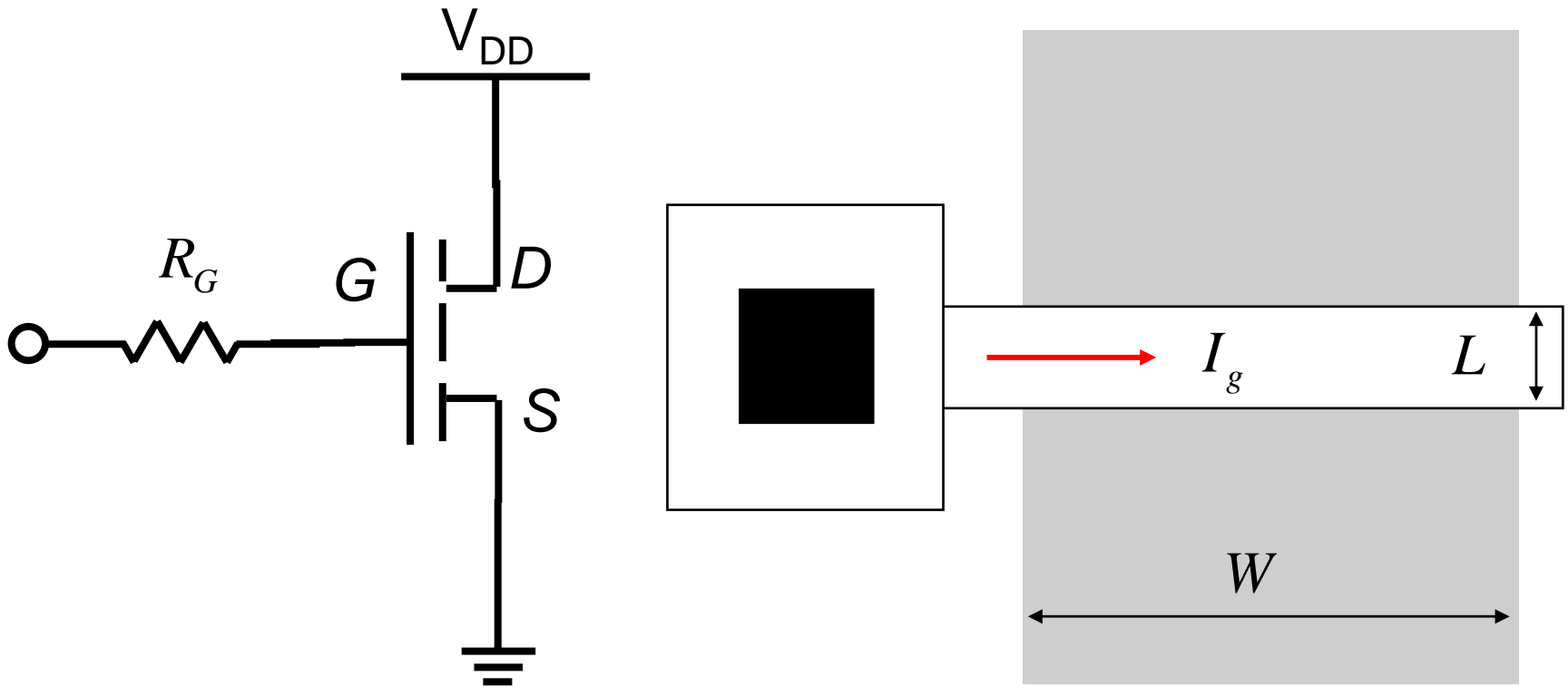
Why did we not consider an R_G ?



effect of a gate resistance (AC)



gate resistance



gate resistance (ii)

$$R_G = \rho_G \frac{W}{L}$$

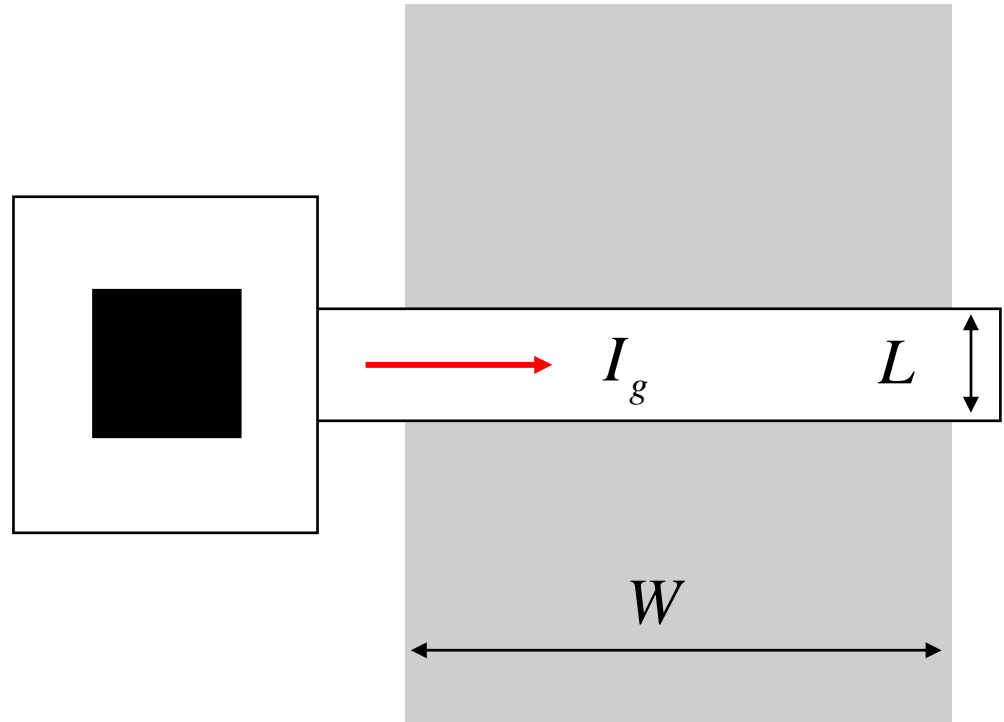
$$R_G = \left(\frac{\rho_G}{L} \right) W = R_L W$$

Ω / cm

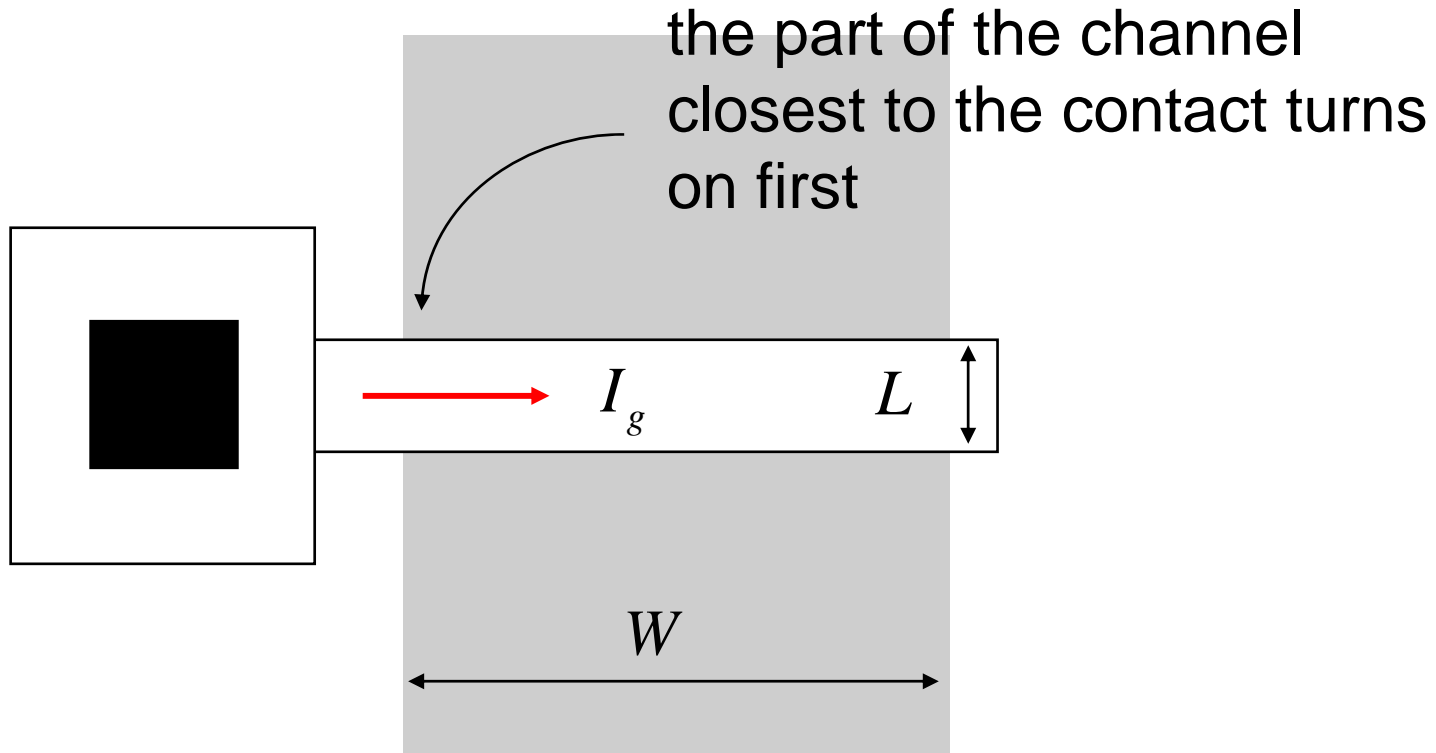
$$C_G = C_{OX} L W$$

$$C_G = (C_{OX} L) W = C_L W$$

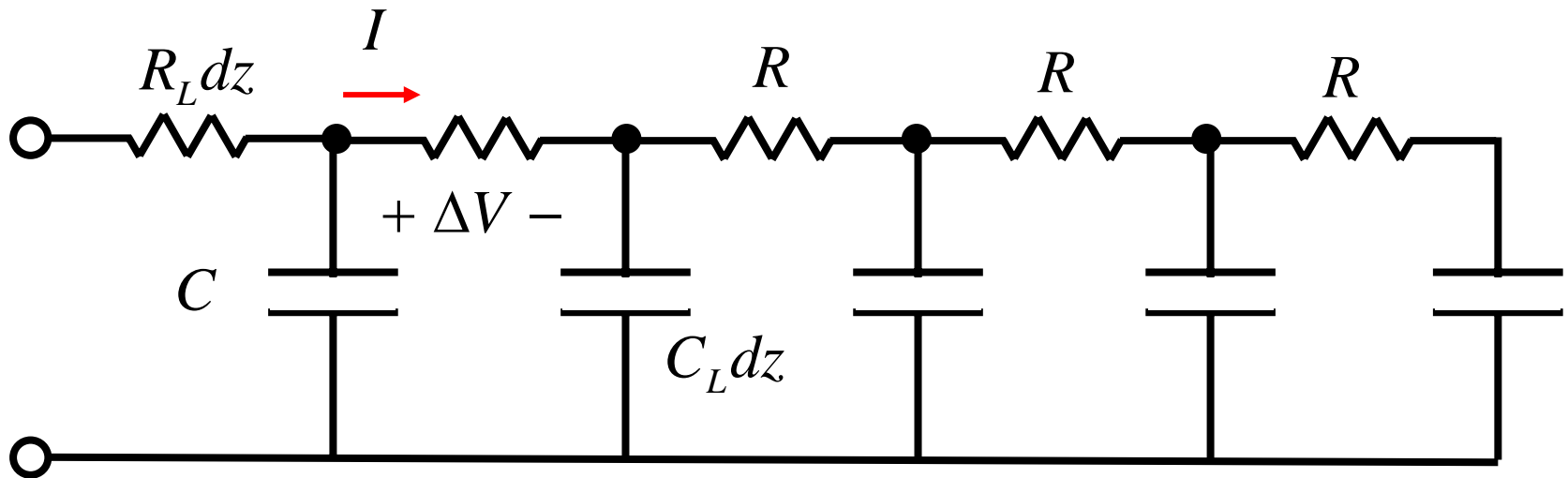
F / cm



distributed gate resistance



distributed gate resistance (ii)

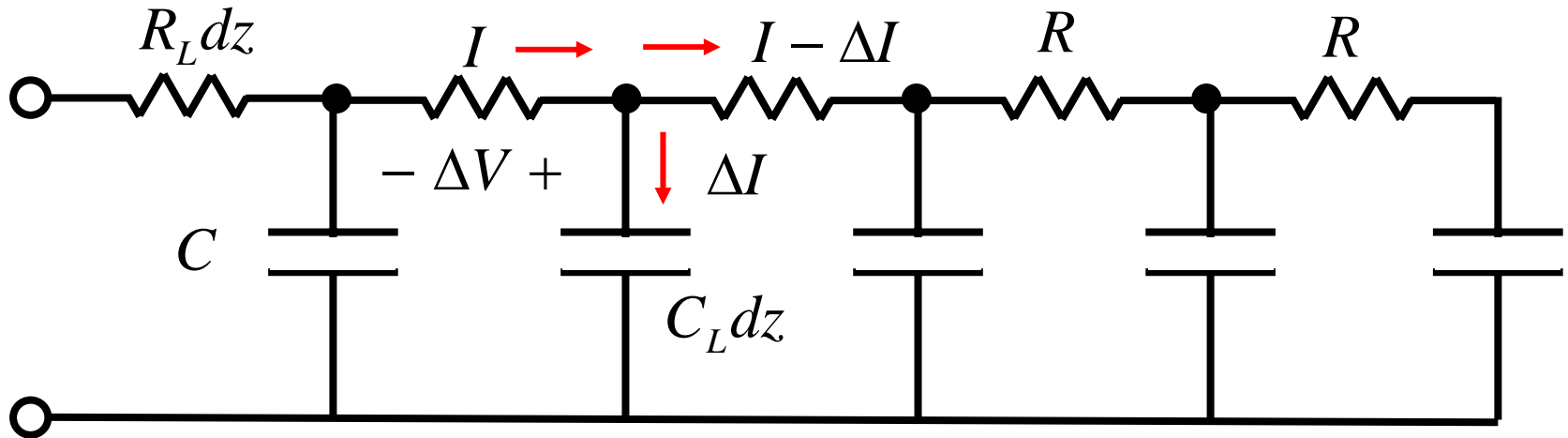


$$\Delta V = I R_L dz$$

$$\frac{\Delta V}{dz} = -\frac{\partial V}{\partial z} = I R_L$$

$$\frac{\partial V}{\partial z} = -I R_L \quad (1)$$

distributed gate resistance (iii)



$$\Delta I = C_L dz \frac{\partial V}{\partial t}$$

$$\frac{\Delta I}{dz} = - \frac{\partial I}{\partial z} = C_L \frac{\partial V}{\partial t}$$

$$\frac{\partial I}{\partial z} = - C_L \frac{\partial V}{\partial t} \quad (2)$$

distributed gate resistance (iii)

$$\frac{\partial V}{\partial z} = -I R_L \quad (1)$$

$$\frac{\partial^2 V}{\partial z^2} = -R_L \frac{\partial I}{\partial z}$$

$$\frac{\partial I}{\partial z} = -C_L \frac{\partial V}{\partial t} \quad (2)$$

$$\frac{\partial^2 V}{\partial z^2} = R_L C_L \frac{\partial V}{\partial t}$$

$$\frac{\partial V(z,t)}{\partial t} = \frac{1}{R_L C_L} \frac{\partial^2 V(z,t)}{\partial z^2}$$

distributed gate resistance (iii)

recall:
$$\frac{\partial n(z,t)}{\partial t} = D_n \frac{\partial^2 n(z,t)}{\partial z^2}$$

“minority carrier diffusion equation”

$$\frac{\partial V(z,t)}{\partial t} = \frac{1}{R_L C_L} \frac{\partial^2 V(z,t)}{\partial z^2} = D_{eff} \frac{\partial^2 V(z,t)}{\partial z^2}$$

$$D_{eff} = \frac{1}{R_L C_L}$$

units:
$$\frac{1}{\Omega/\text{cm} \times \text{F}/\text{cm}} = \frac{\text{cm}^2}{\text{V}/\text{A} \times \text{C}/\text{V}} = \frac{\text{cm}^2}{\text{C}/\text{A}} = \frac{\text{cm}^2}{\text{sec}}$$

distributed gate resistance (iv)

recall: $\tau_B = W_B^2 / 2D_n$ “base transit time”

$$\tau_g = 0.5R_L C_L W^2$$

distributed gate resistance and scaling

$$\tau_g = 0.5 R_L C_L W^2$$

$$\left. \begin{array}{l} R_L = \rho_G / L \quad \rho_G \sim 2 - 10 \text{ } \Omega/\text{sq.} \\ C_L = C_{OX} L \end{array} \right\} \tau_g = 0.5 \rho_G C_{OX} W^2$$

behavior with scaling:

$$R_L \rightarrow \rho_G / (L / \kappa) = \kappa R_L$$

$$C_L \rightarrow (\kappa C_{OX}) (L / \kappa) = C_L$$

$$\tau_g \rightarrow \kappa \tau_g$$

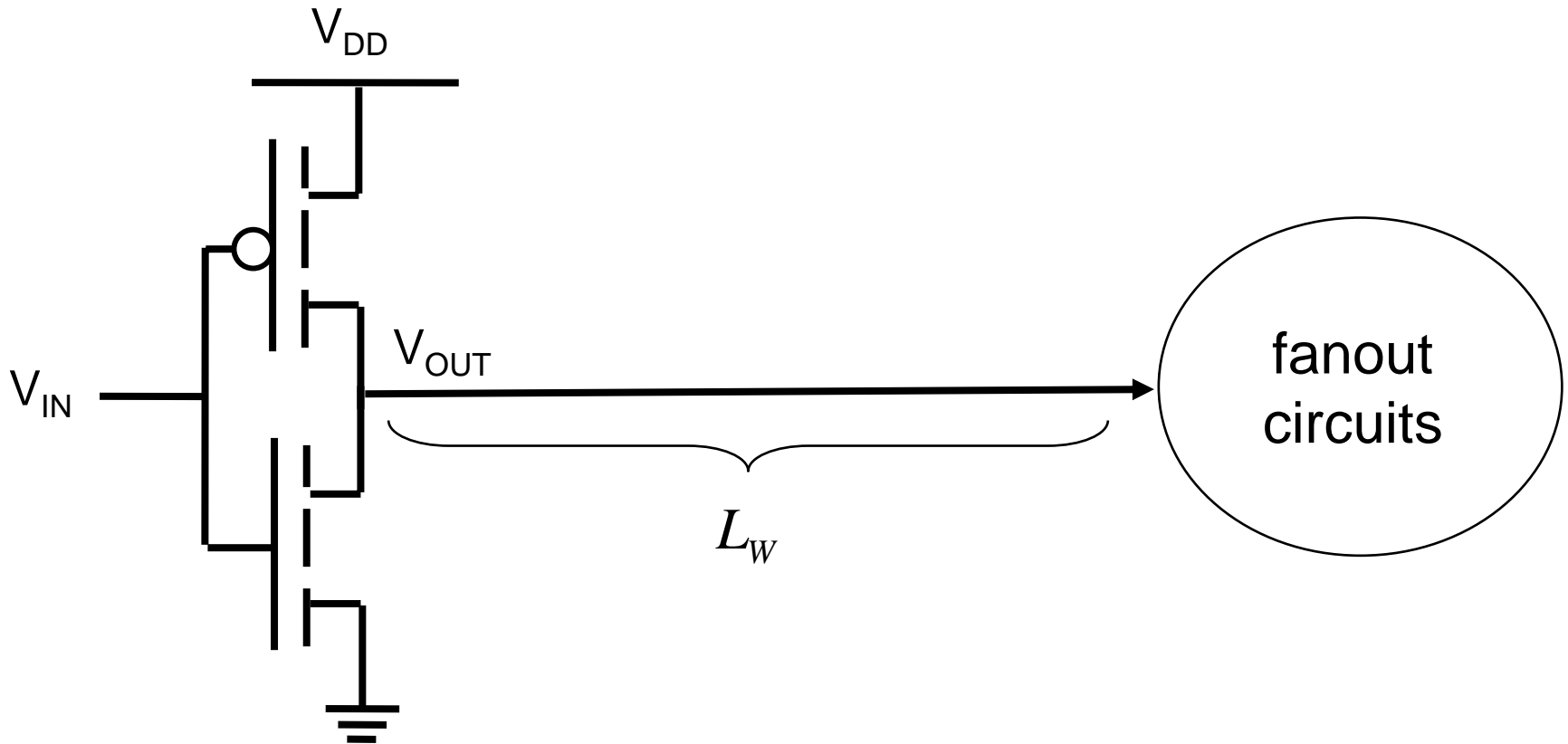
device delay:

$$\tau \rightarrow \tau / \kappa$$

outline

- 1) Gate Resistance
- 2) Interconnects**
- 3) ITRS

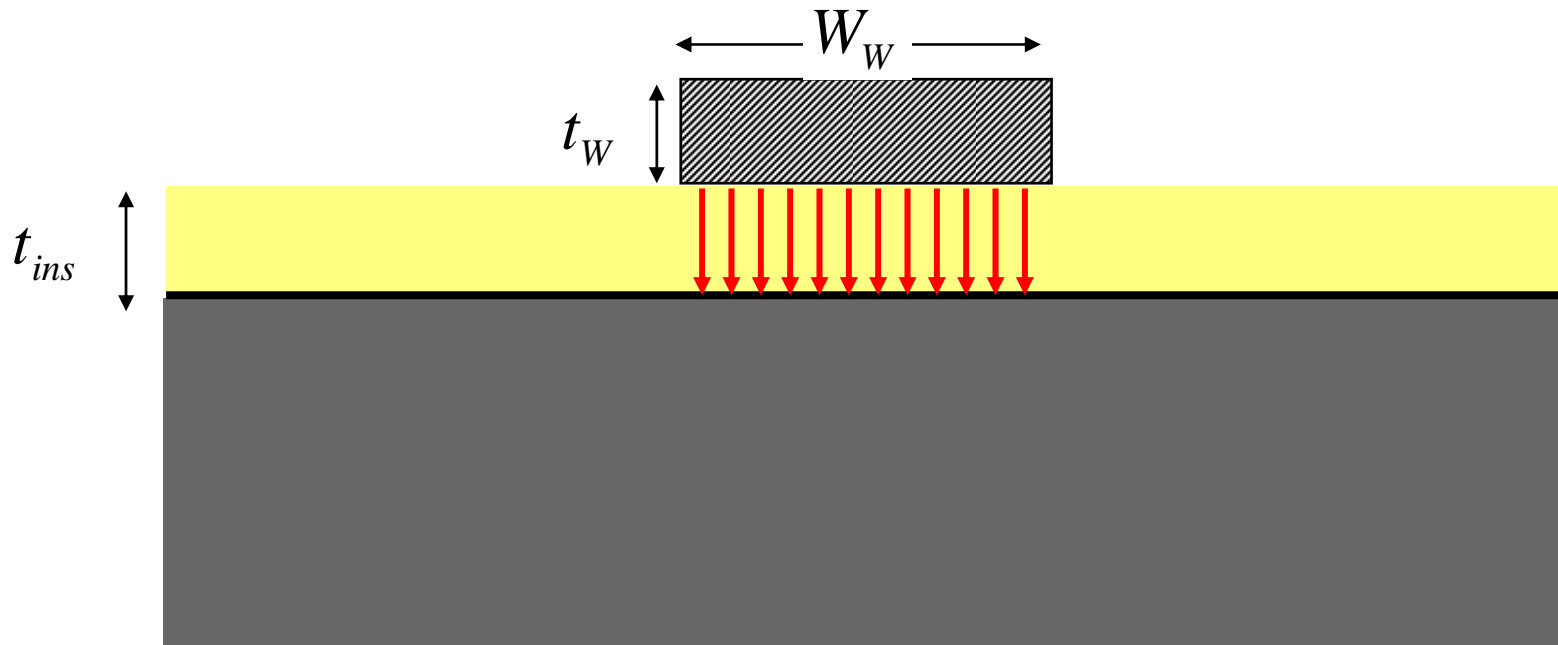
interconnects



interconnect capacitance

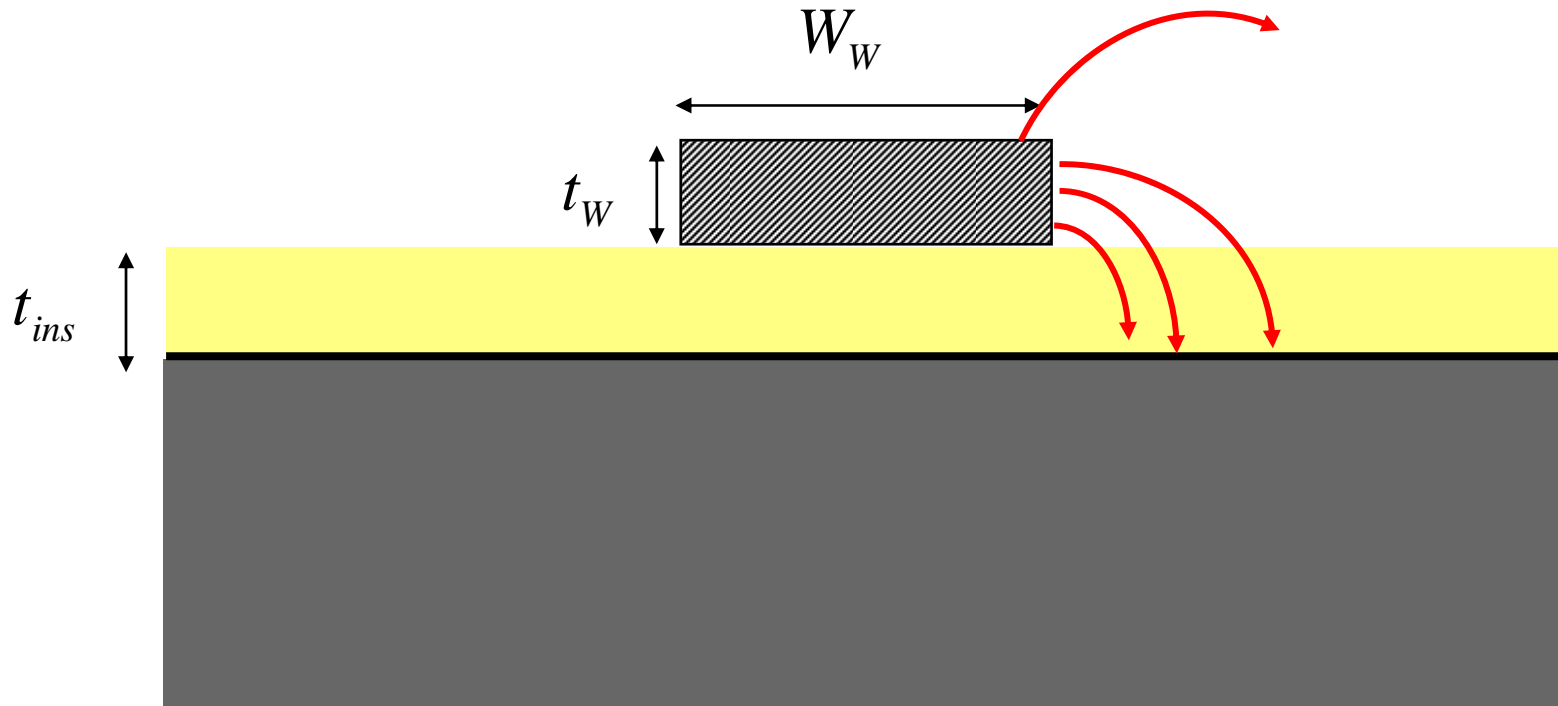
$$C_{Wire} = C_{ins} W_w L_w \quad C_{ins} = \epsilon_{ins} / t_{ins}$$

$$C_{Wire} = (C_{ins} W_w) L_w = C_W (PP) L_w$$

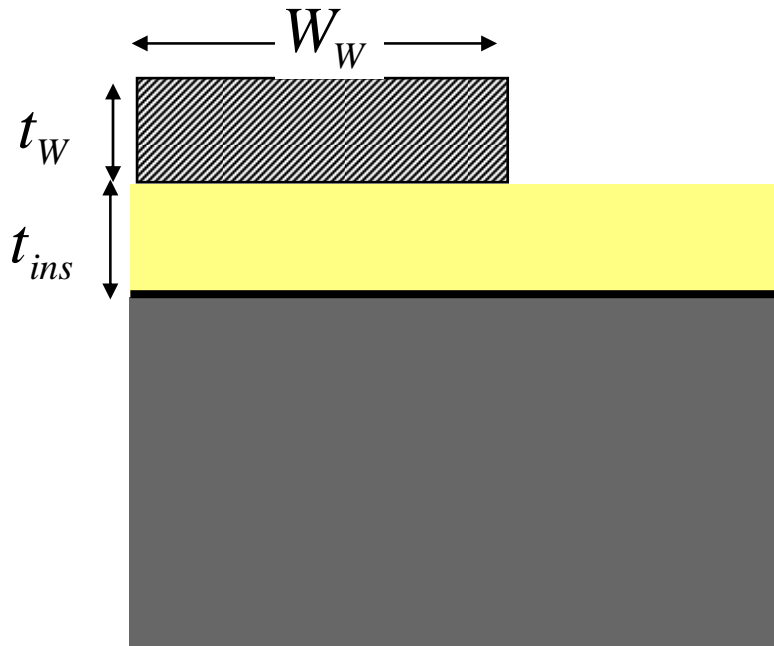


interconnect capacitance (ii)

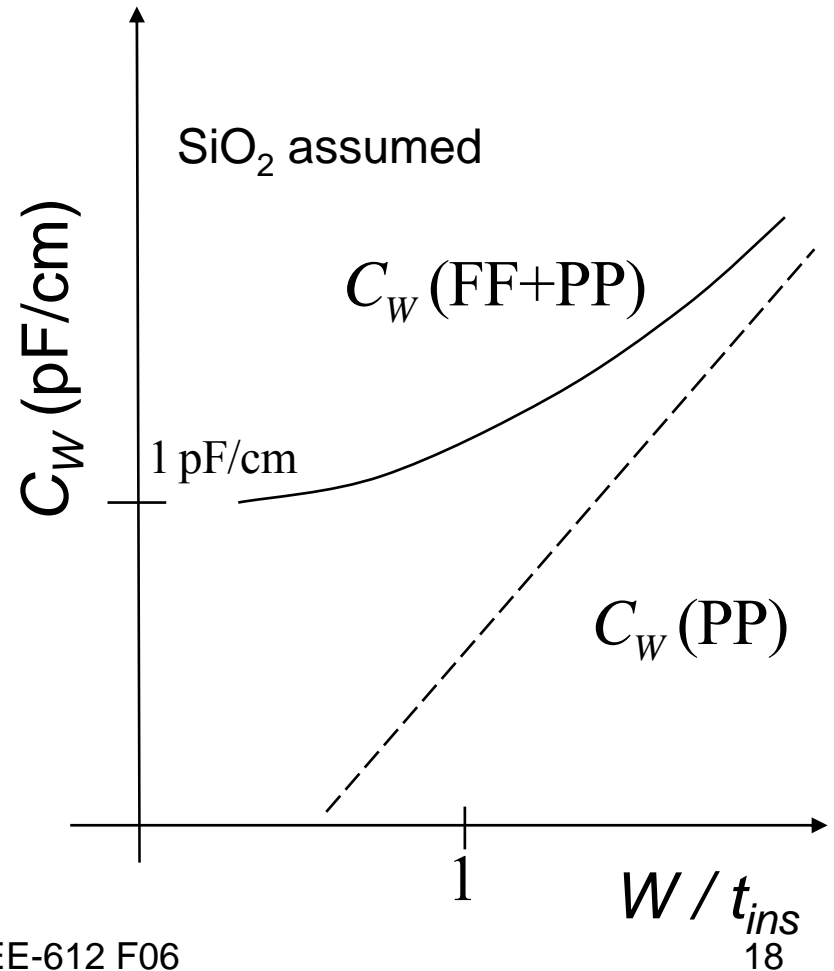
$$C_{Wire} = [C_W (PP) + C_W (FF)] L_W$$



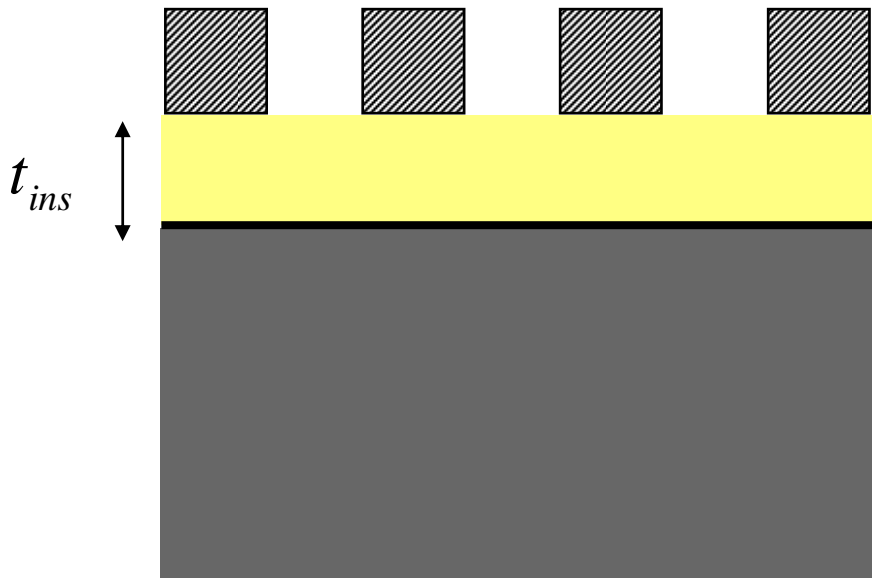
interconnect capacitance (ii)



(see Fig. 5.21, Taur and Ning)

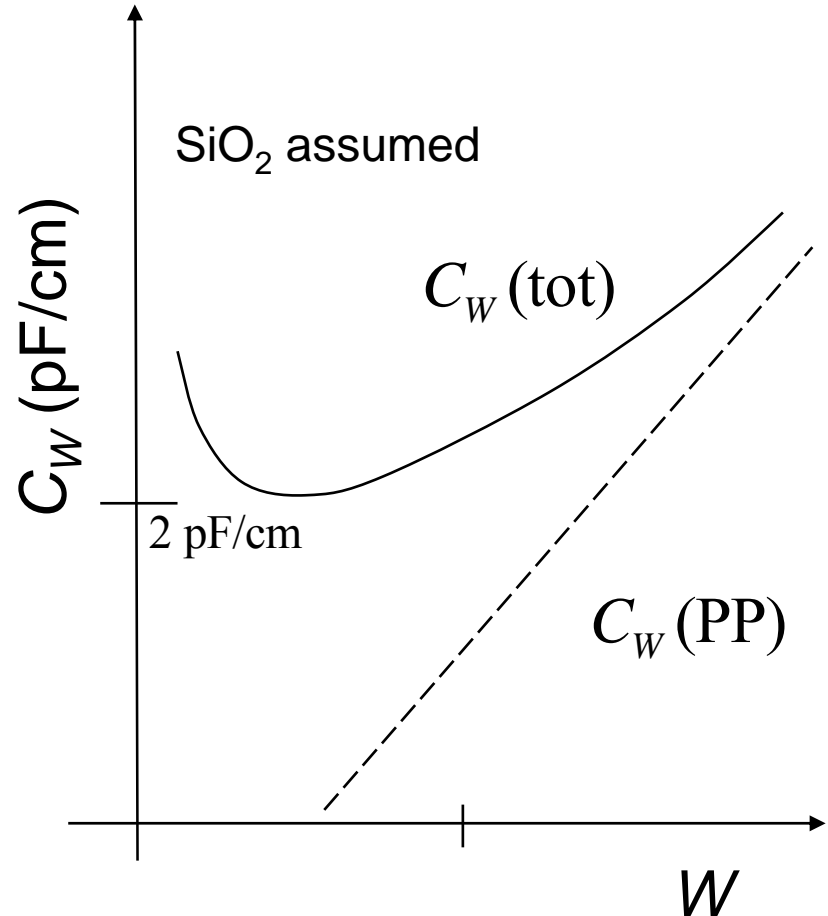


interconnect capacitance (ii)

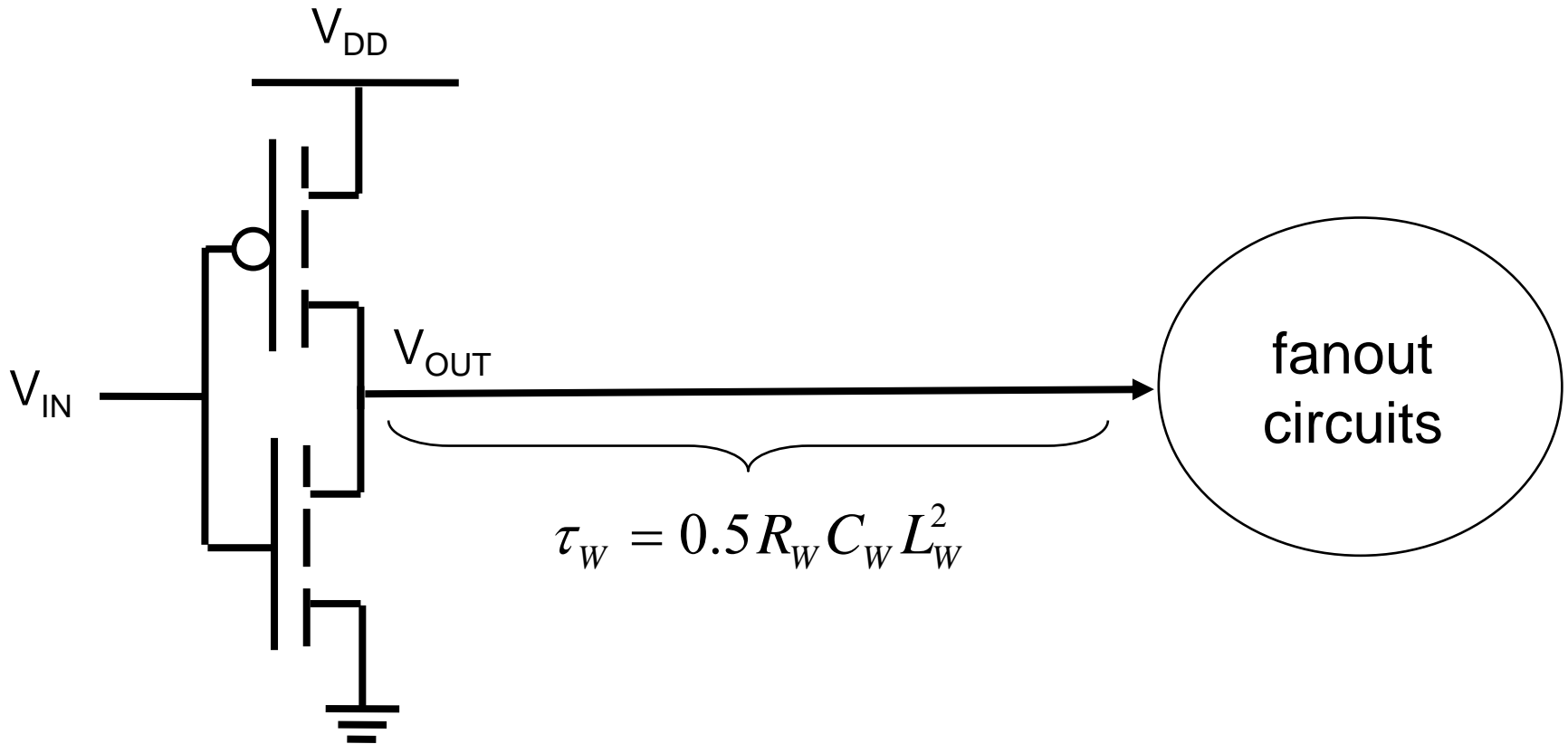


$$C_{Wire} = [C_W (PP) + C_W (FF) + C (WW)] L_W$$

(see Fig. 5.22, Taur and Ning)



interconnect delay



interconnect scaling

$$\tau_W = 0.5 R_W C_W L_W^2$$

$$C_W = C_W(\text{PP}) + C_W(\text{FF}) + C_W(\text{WW})$$

$$R_W = \frac{\rho_W}{W_w t_w}$$

$$\rho_{Al} \approx 3 \times 10^{-6} \text{ } \Omega\text{-cm}$$

$$\rho_{Cu} \approx \rho_{Al} / 1.5$$

scaling by factor, $\kappa > 1$

$$C_W = C_{ins} W_w + C_W(\text{FF}) \rightarrow C_W$$

$$R_W = \rho_W / (W_w t_w) \rightarrow \kappa^2 R_W$$

$$J_W = I / (W_w t_w) \rightarrow \kappa J_W \text{ (A/cm}^2\text{)} \quad \text{(electromigration)}$$

$$\tau_W = 0.5 R_W C_W L_W^2 \rightarrow \tau_W \quad \text{(device } \tau \text{ is decreasing)}$$

local interconnects

$$L_W \rightarrow L_W / \kappa \quad \tau_W = 0.5 R_W C_W L_W^2 \rightarrow \tau_W$$

Is this an issue? Assume:

$$C_W \approx 2\pi \epsilon_{ins} \text{ F/cm} \quad \text{Eqn. (5.27) Taur and Ning}$$

$$\tau_W \approx \pi \epsilon_{ins} \rho_w \frac{L_W^2}{W_w t_w} \approx (3 \times 10^{-18} \text{ s}) \frac{L_W^2}{W_w t_w} \quad \text{Eqn. (5.29) (5.30)}$$

for $W_w = t_w = 0.25 \mu\text{m}$ and $L_W = 100 \mu\text{m}$, $\tau_W = 0.5 \text{ps}$

for a 0.25 micron technology, an inverter delay is $\sim 20 \text{ps}$

local interconnect delays are not an issue

global interconnects

$L_W \rightarrow L_W$ (approximately the size of the chip)

$$\tau_W = 0.5 R_W C_W L_W^2 \rightarrow \kappa^2 \tau_W$$

Is this an issue?

for a 0.25 micron technology:

$$\tau_W \approx \pi \epsilon_{ins} \rho_w \frac{L_W^2}{W_w t_w} \approx (3 \times 10^{-18} \text{ s}) \frac{L_W^2}{W_w t_w} \approx 1 \text{ ns}$$

$$\tau_W \gg \tau_{Gate} \gg \tau_{Device}$$

global interconnect delays are a very big issue

global interconnect scaling solutions

$$\tau_W = 0.5 R_W C_W L_W^2$$

$$C_W = C_W(\text{PP}) + C_W(\text{FF}) + C_W(\text{WW})$$

(low-k dielectrics)

$$R_W = \frac{\rho_W}{W_w t_w}$$

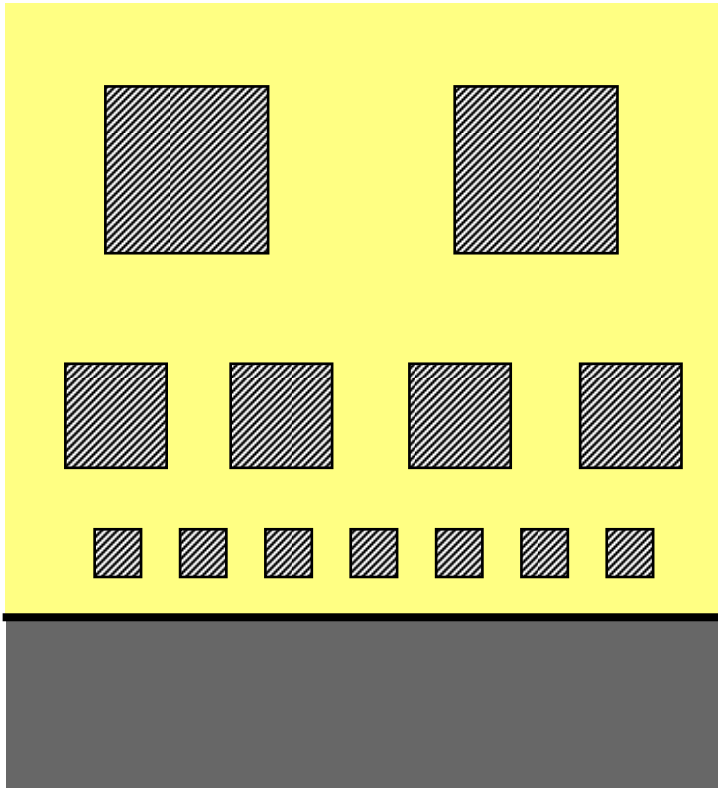
1) switch from Al metal to Cu

$$\rho_{Cu} \approx \rho_{Al} / 1.5$$

2) increase cross-sectional area

$$A_W = W_w t_w$$

wiring hierarchy



$$\tau_W = 0.5 R_W C_W L_W^2$$

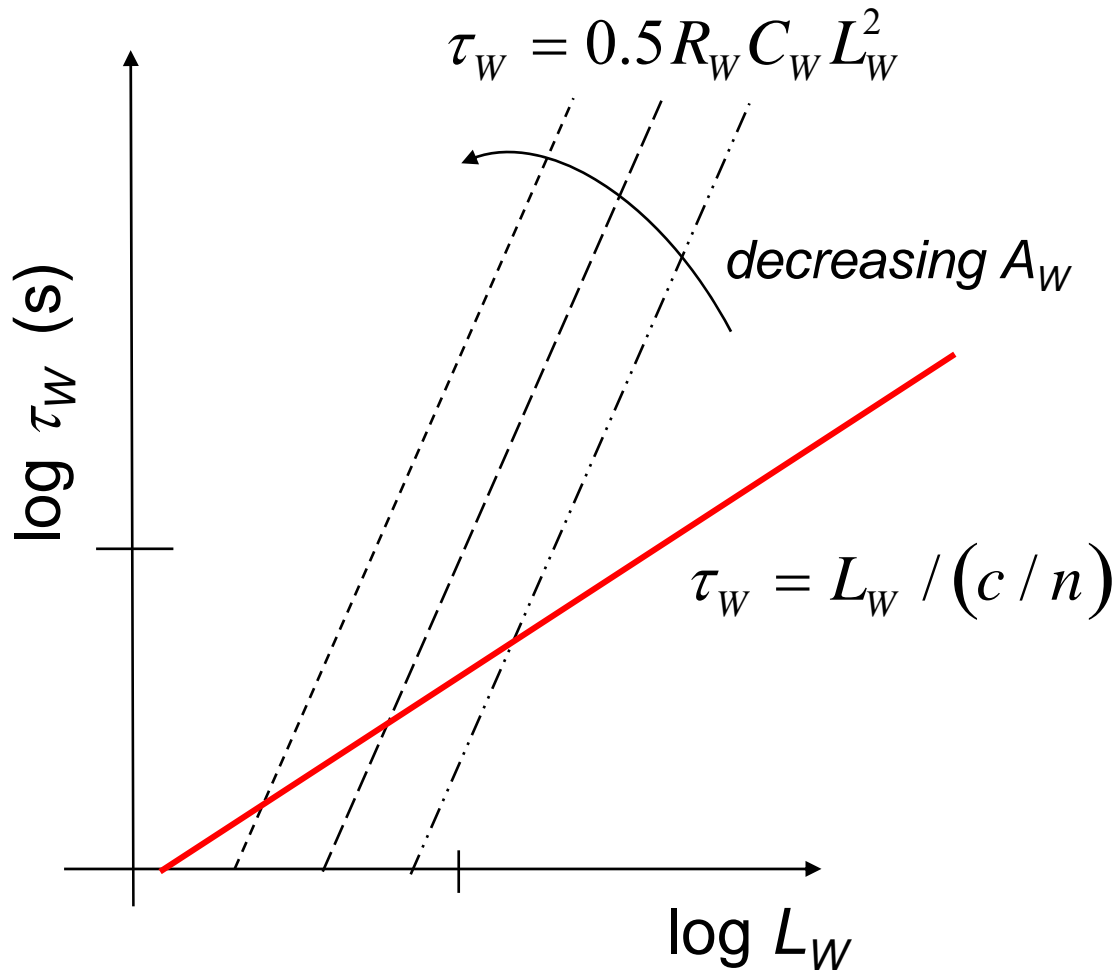
$$\tau_W = \frac{L_W}{2 / R_W C_W L_W}$$

$$\tau_W = \frac{L_W}{v_{Diff}}$$

$$v_{Diff} = 2D_{eff} / L_W$$

after Fig. 5.24, Taur and Ning

inductance



$$\tau_W = L_W / v_{Signal}$$

RC line:

$$v_{Signal} = 2D_{eff} / L_W$$

RLC line:

$$v_{Signal} < c / n$$

outline

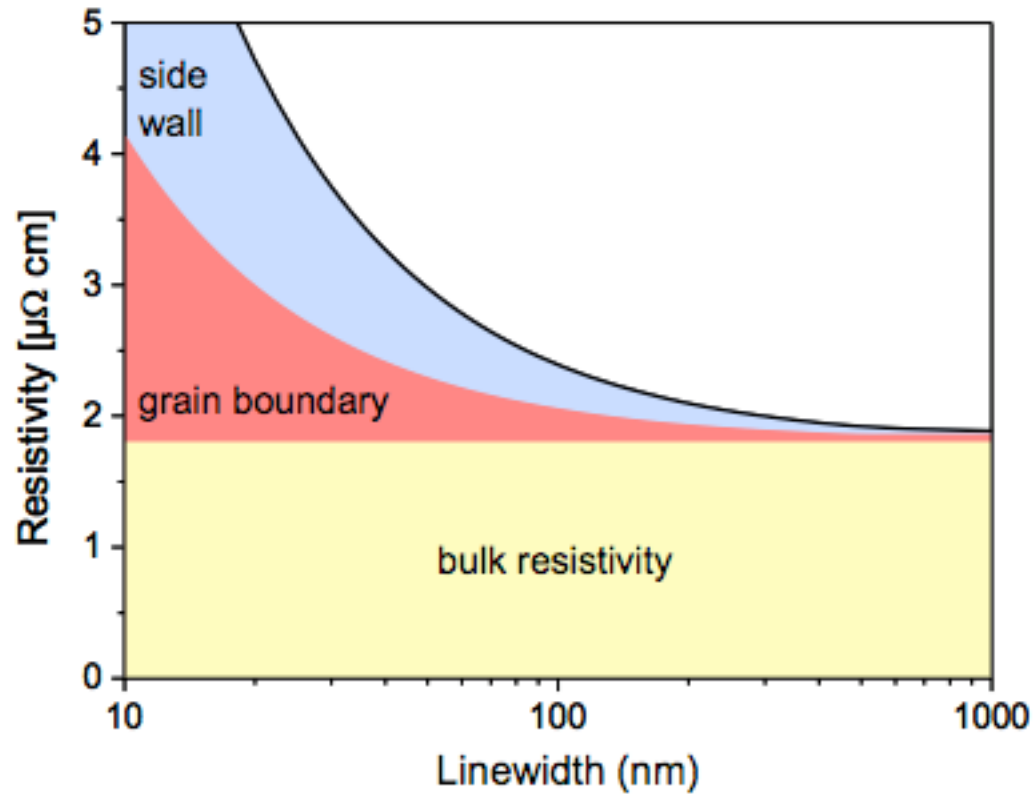
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interconnects at the 70 nm node (MPU)

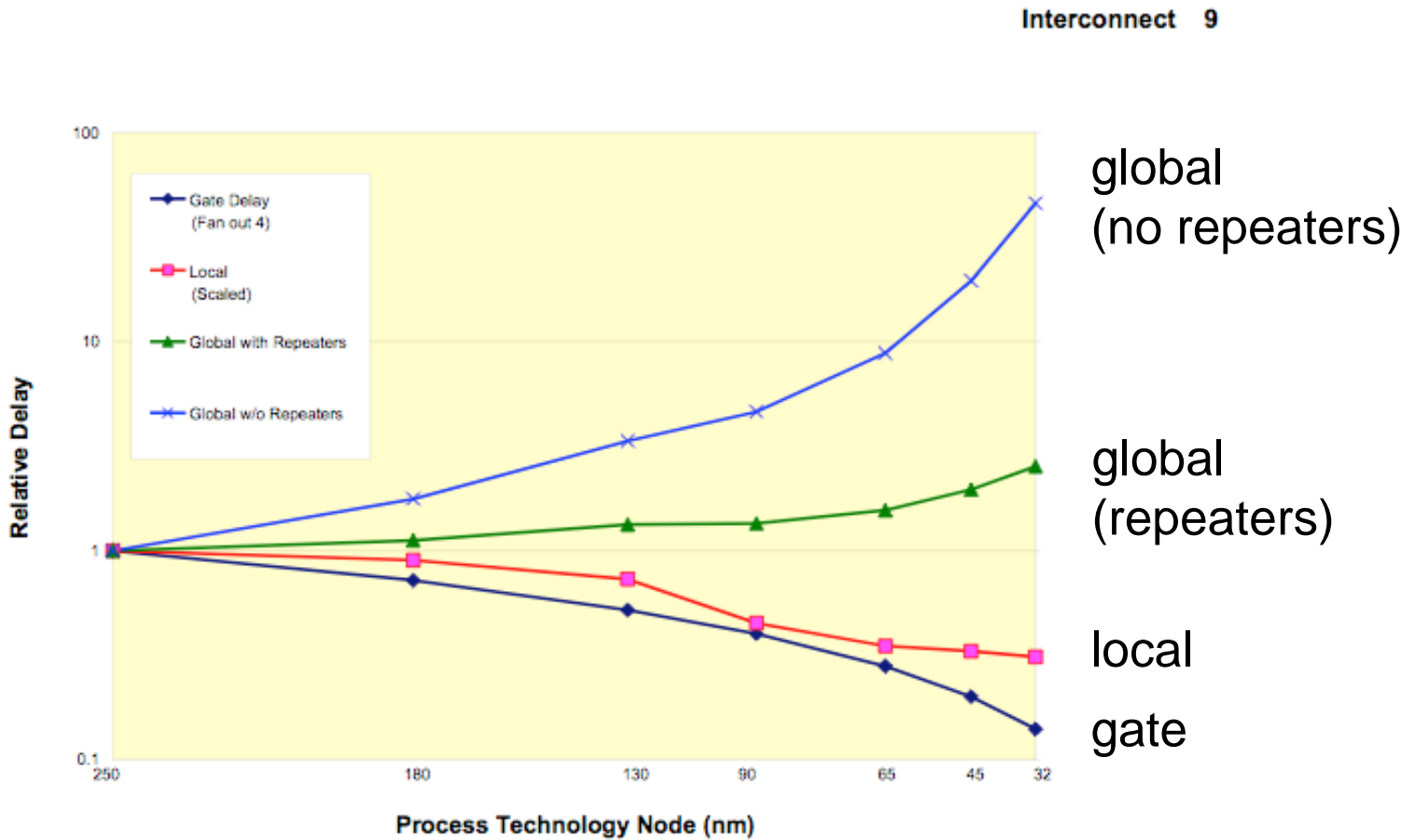
Metal 1 pitch:	156 nm
Metal 1 A/R:	1.7
J_{MAX}	1.37×10^6 A/cm ²
No. of metal layers:	11
Inter-level dielectric:	$\kappa < 2.7$
Total IC length (metal 1 +5):	1212 m/cm ²
L_W for $RC = \tau$:	43 μ m
τ_W for $L_W = 1$ mm metal 1:	612 ps

interconnects trends

8 Interconnect



interconnects trends



outline

- 1) Gate Resistance
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