EE-612:
Lecture 23:
CMOS Process Flow

Mark Lundstrom
Electrical and Computer Engineering
Purdue University
West Lafayette, IN USA
Fall 2006

NCN

www.nanohub.org

PURDUE UNIVERSITY

For a basic, CMOS process flow for an STI (shallow trench isolation process), see: http://www.rit.edu/~lffeee/AdvCmos2003.pdf

The author is indebted to Dr. Lynn Fuller of Rochester Institute of Technology for making these materials available. What follows is a condensed version of the more complete presentation (listed above) by Dr. Fuller. I regret any errors that I may have introduced by shortening these materials. -

Mark Lundstrom 10/19/06

RIT's Advanced CMOS Process

Dr. Lynn Fuller

webpage: http://www.rit.edu/~lffeee/

Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041

email: LFFEEE@rit.edu
microE webpage: http://www.microe.rit.edu

9-20-06 AdvCmos2006.ppt

INTRODUCTION

Advanced Processes Used:

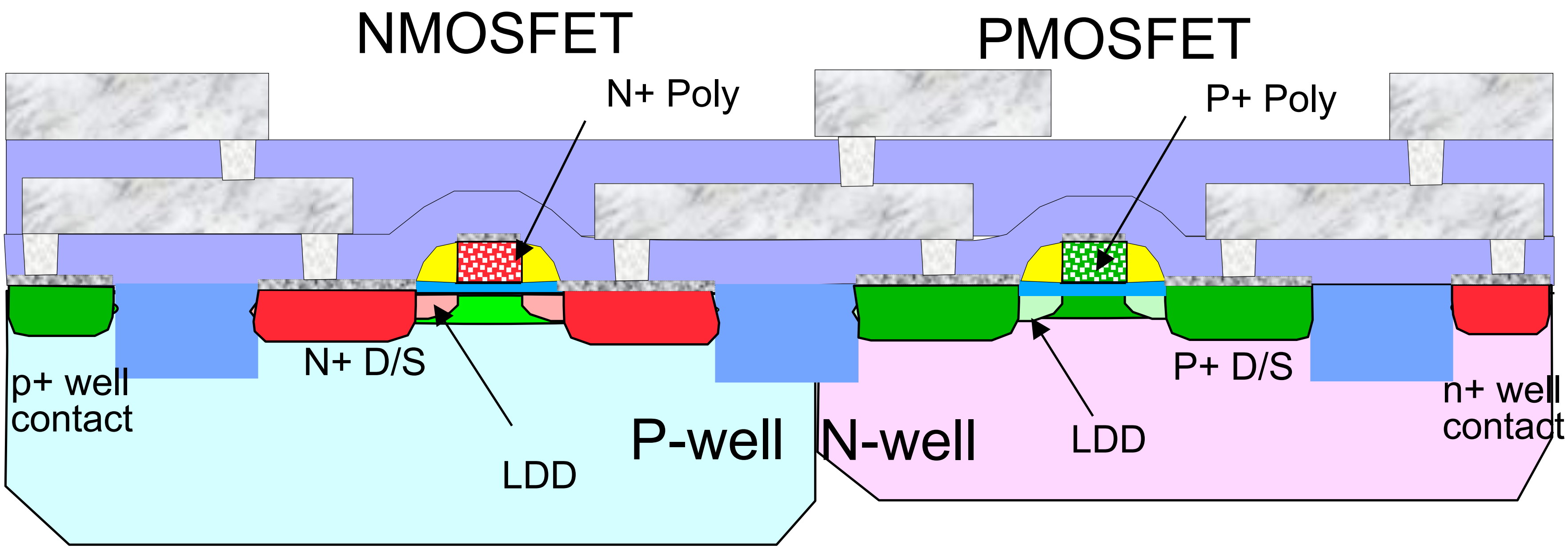
Shallow Trench Etch with Endpoint
Trench PECVD TEOS fill and CMP
Silicide $TiSi_2$, Recipes for Rapid Thermal Processor
Dual Doped Gate, Ion Implant and Mask Details
Anisotropic Poly Etch
100 Å Gate Oxide Recipe with N_2O
Nitride Spacer, New Anisotropic Nitride Etch
Plasma Etch of Contacts and Vias
Aluminum Metal, W Plugs Deposition, CMP of Oxide
Canon and ASML Masks
Canon and ASML Stepper Jobs
MESA Process, Products, Instructions, Parameters

RIT ADVANCED CMOS VER 150

RIT Advanced CMOS

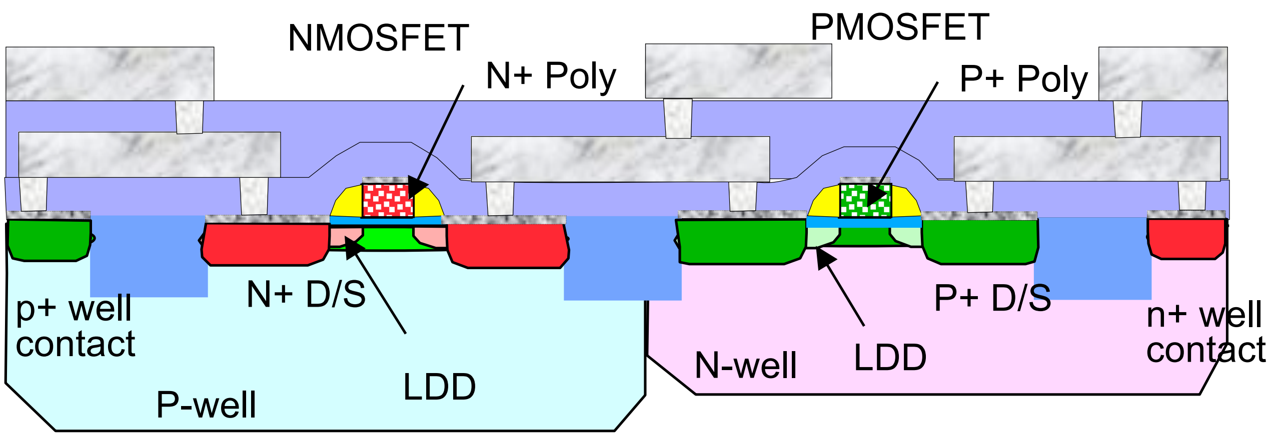
150 mm Wafers
Nsub = 1E15 cm-3 or 10 ohm-cm, n or p
Nn-well = 1E17 cm-3
Xj = 2.5 µm
Np-well = 1E17 cm-3
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox = 4000 Å
Dual Doped Gate n+ and p+
Tox = 100 Å
Lmin= 0.5 µm
LDD/Nitride Side Wall Spacers
TiSi2 Silicide
Tungsten Plugs, CMP, 2 Layers Aluminum

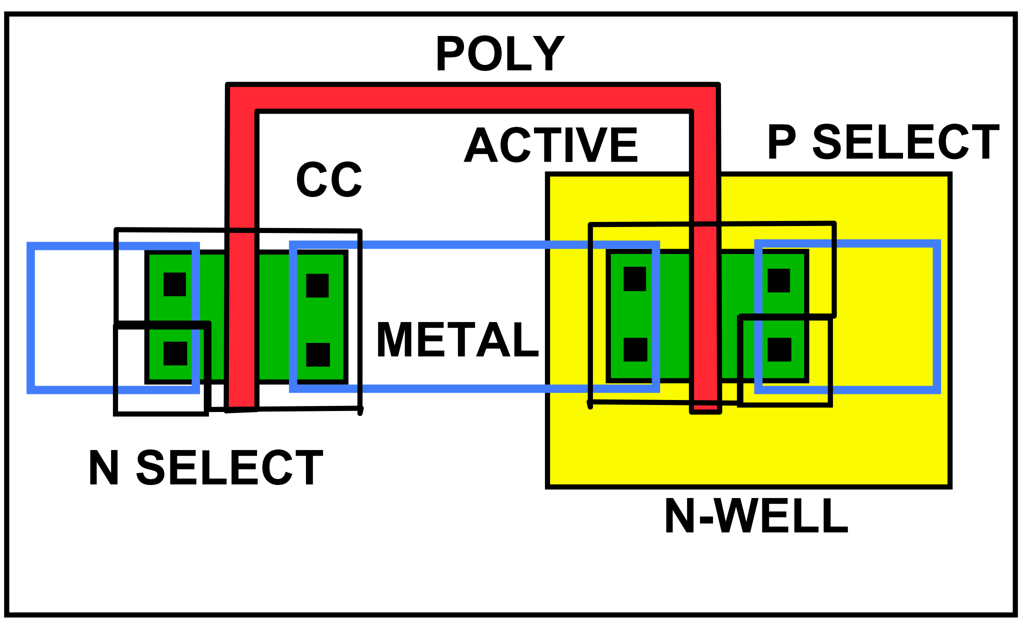
RIT ADVANCED CMOS

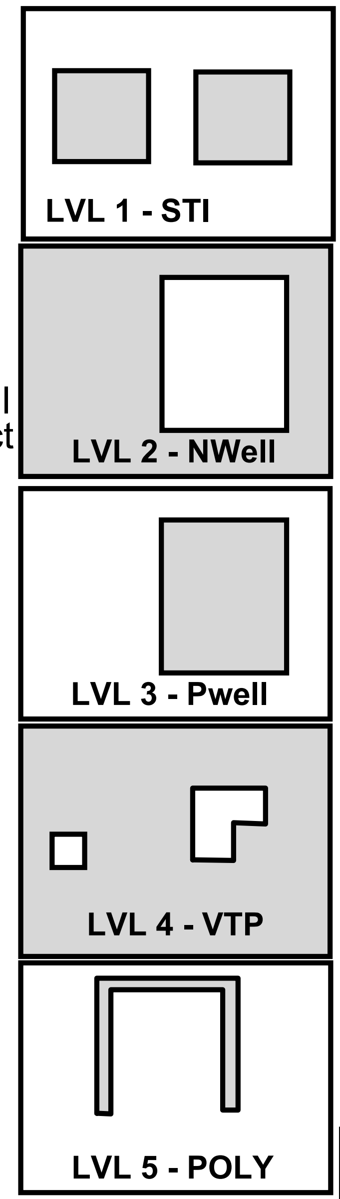


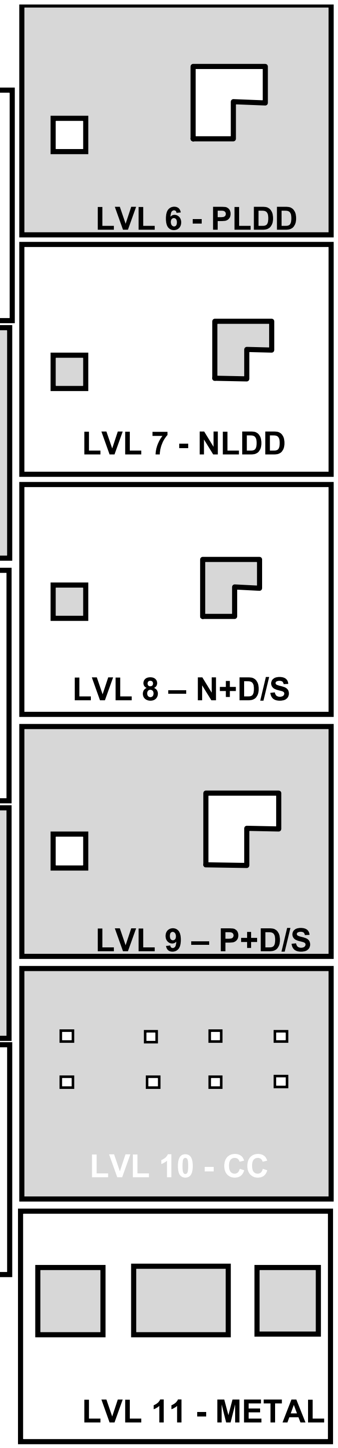
Rochester Institute of Technology
Microelectronic Engineering

RIT ADVANCED CMOS PROCESS









11 PHOTO LEVELS

ADV-CMOS 150 PROCESS

CMOS Versions 150, one level Metal

1. ID01
2. DE01
3. CL01
4. OX05--- pad oxide 500 A
5. CV02- 1500 Å
6. PH03 –1- STI
7. ET29 etch shallow trench, 4000A
8. ET07-ash
9. CL01
10. OX05 – pad oxide, 500 A
11. PH03 -2- N-Well
12. IM01 3E13, P31, 170KeV
13. ET07
14. PH03 -3-P-Well
15. IM01 - 8E13, B11, 80KeV
16. ET07
17. CL01
18. CV03 Trench Fill TEOS
19. CM01STI CMP
20. CL02 Decontamination Clean
21. CL01

21.1 OX08 Densify

22. ET19
23. OX06 well drive, 6hr 1100C
24. PH03 -4 -NVT
25. IM01 Implant NVT
26. ET07
27. PH03 – 5 - PVT adjust
28. IM01 Implant PVT
29. ET07
30. ET06 Etch Pad Oxide
31. CL01
32. ET06 Pre Gate Oxide Etch
33. OX06 gate oxide
34. CV01 poly dep 4000Å
35. PH03 - 6 - poly
36. ET08 poly etch
37. ET07
38. CL01
39. OX05 Poly ReOx
40. PH03 –7- p LDD
41. IM01 p LDD
42. ET07
43. PH03 –8- n LDD
44. IM01 n LDD
45. ET07
46. CL01
47. CV02 nitride spacer dep
48. ET39 spacer etch
49. PH03 – 8 - N+D/S
50. IM01 – N+D/S
51. ET07
52. PH03 – 9- P+ D/S
53. IM01 – P+ D/S
54. ET07
55. CL01
56. OX08 – DS Anneal
57. ET06
58. ME03 Ti Dep
59. RT01
60. ET11 Ti Etch
61. RT02
62. CV03 – LTO
63. PH03 – 10 CC
64. ET10
65. ET07
66. CL01
67. ME01 Aluminum
68. PH03 -11- metal
69. ET15 plasma Al Etch
70. ET07
71. SI01
72. SEM1
73. TE01
74. TE02
75. TE03
76. TE04

(Revision 9-20-06)

STARTING WAFER

N-type or P-type Substrate 10 ohm-cm

RCA CLEAN

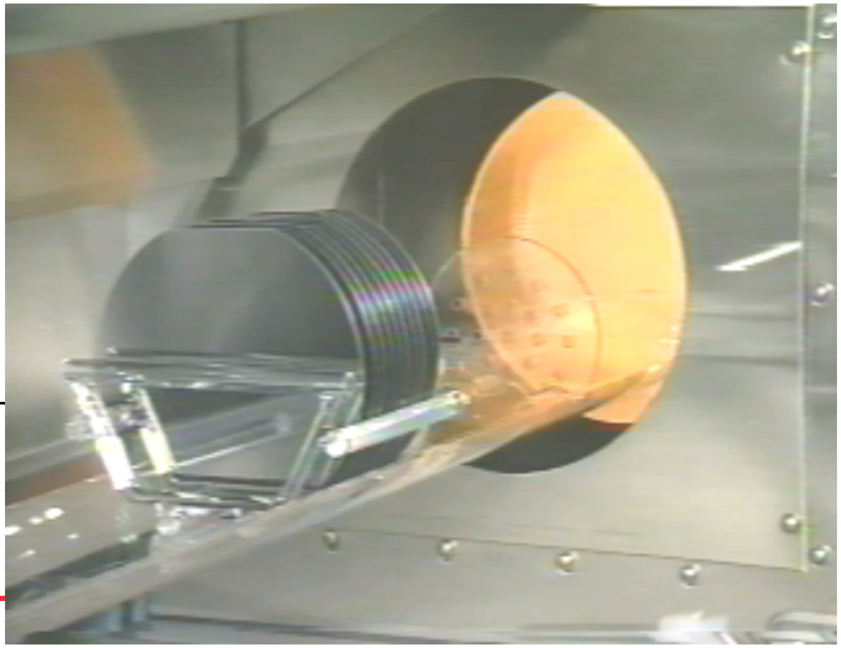
1. **APM or SC1**
   NH_4OH - 1part
   H_2O_2 - 3parts
   H_2O - 15parts
   70 °C, 15 min.
2. DI water rinse, 5 min.
3. H_20 - 50
   HF - 1
   60 sec.
4. DI water rinse, 5 min.
5. **HPM or SC2**
   HCL - 1part
   H_2O_2 - 3parts
   H_2O - 15parts
   70 °C, 15 min.
6. DI water rinse, 5 min.
7. SPIN/RINSE DRY

Rochester Institute of Technology
Microelectronic Engineering

RCA CLEAN AND PAD OXIDE GROWTH

Pad Oxide, 500A
Bruce Furnace 04 Recipe 250
~45 min at 1000 °C

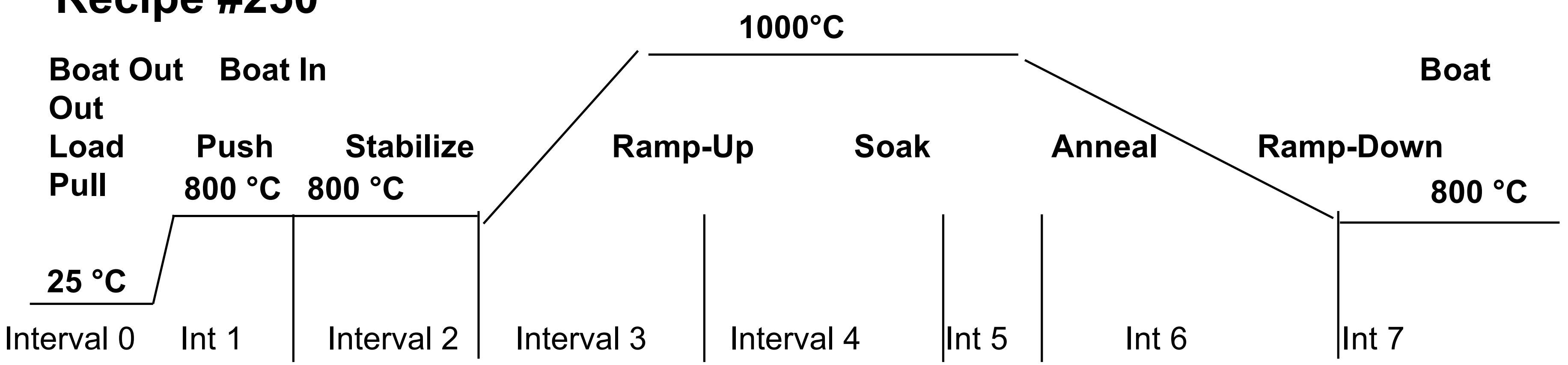
Substrate 10 ohm-cm



Rochester Institute of Technology
Microelectronic Engineering

BRUCE FURNACE RECIPE 250 500Å DRY OXIDE

Recipe #250



Any	**12 min**	**15 min**	**20 min**	**40min**	**5min**	**40 min**	**12 min**
0 lpm	**10 lpm**	**10 lpm**	**5 lpm**	**10 lpm**	**15 lpm**	**10 lpm**	**5 lpm**
none	**N2**	**N2**	**O2**	**O2**	**N2**	**N2**	**N2**

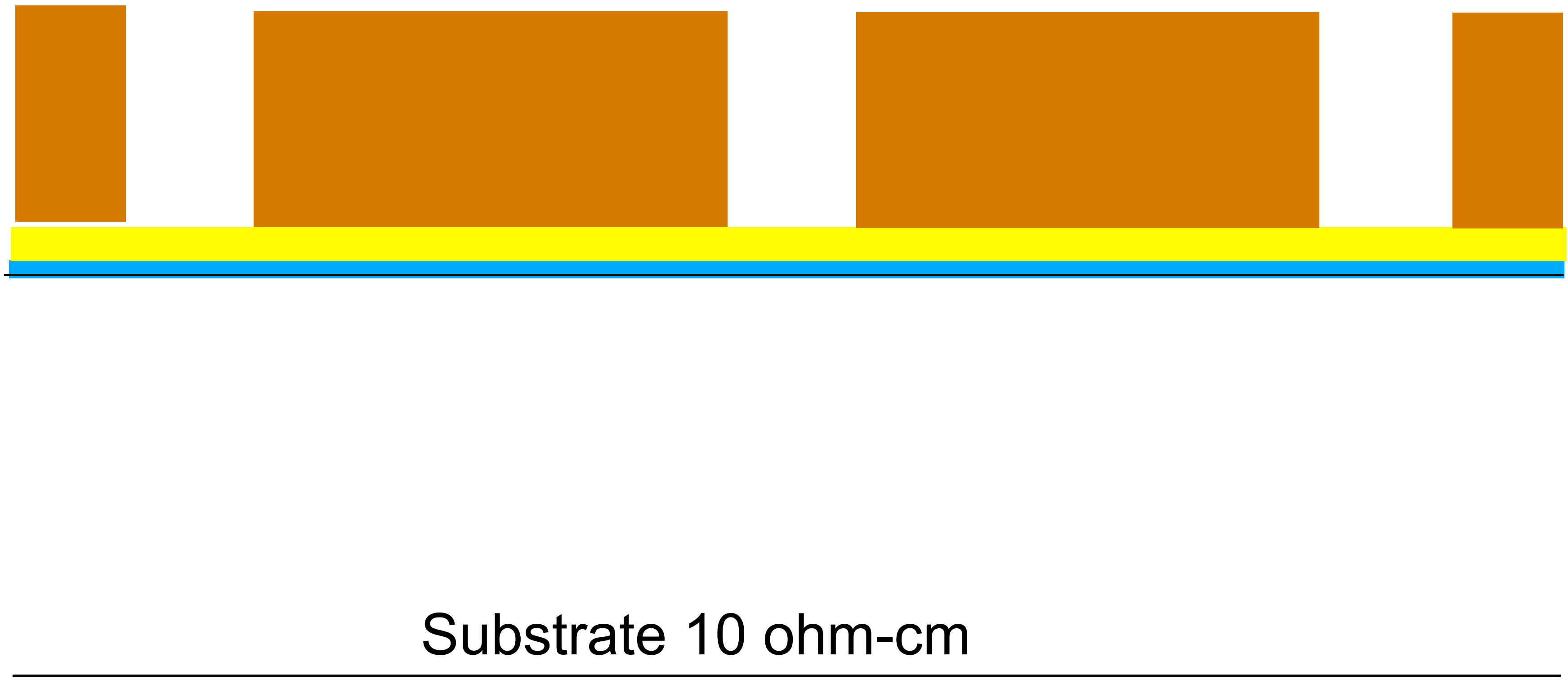
DEPOSIT SILICON NITRIDE

Recipe Nitride 810
Nitride, 1500A
LPCVD, 810C, ~30min

Substrate 10 ohm-cm

Rochester Institute of Technology
Microelectronic Engineering

LEVEL 1 PHOTO - STI



PLASMA ETCH NITRIDE/OXIDE/SILICON

STI Etch: SF_6 plasma

LAM 490 Etcher, Etch Rate ~1000 Å/min for Nitride

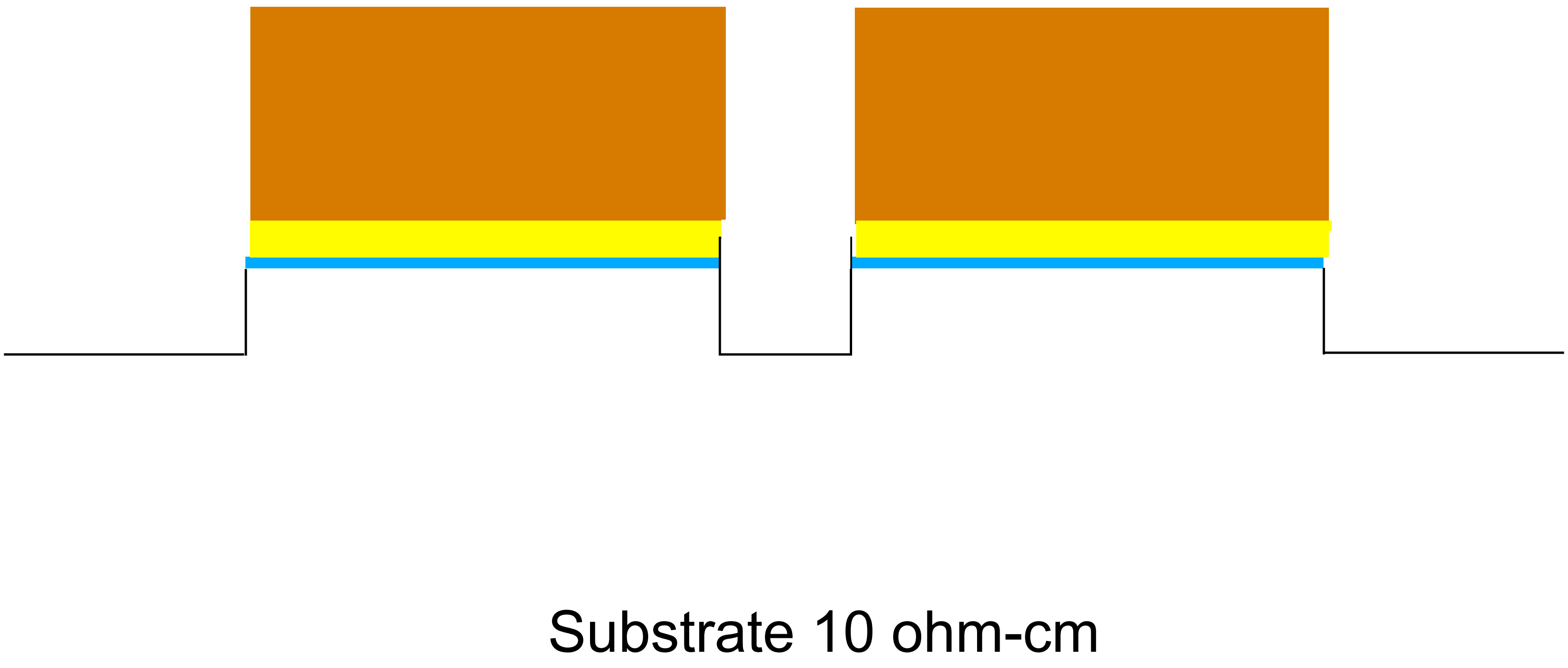
~ 500 Å/min for Oxide

~ 5000 Å/min for silicon

Substrate 10 ohm-cm

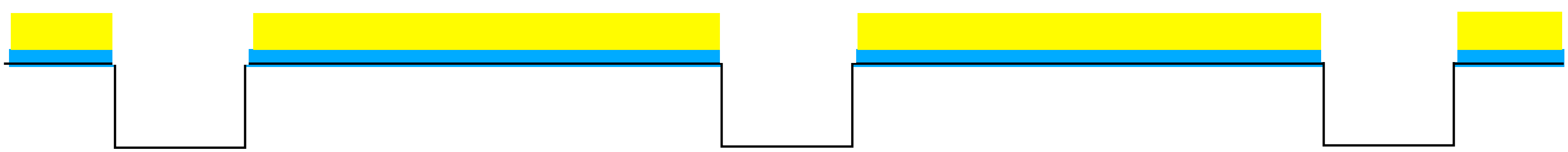
Rochester Institute of Technology
Microelectronic Engineering

CONTINUE THE ETCH THRU PAD OXIDE AND INTO THE SILICON



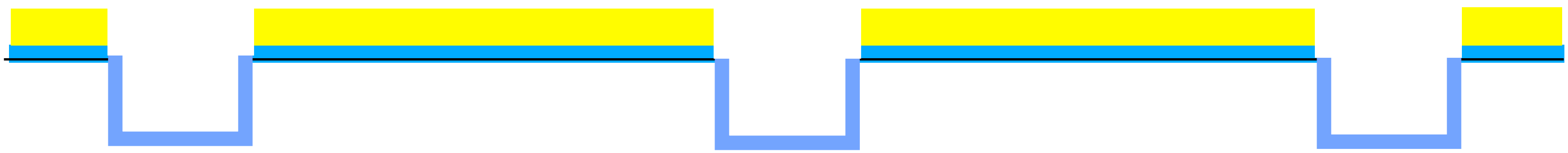
Rochester Institute of Technology
Microelectronic Engineering

STRIP RESIST AND RCA CLEAN



Substrate 10 ohm-cm

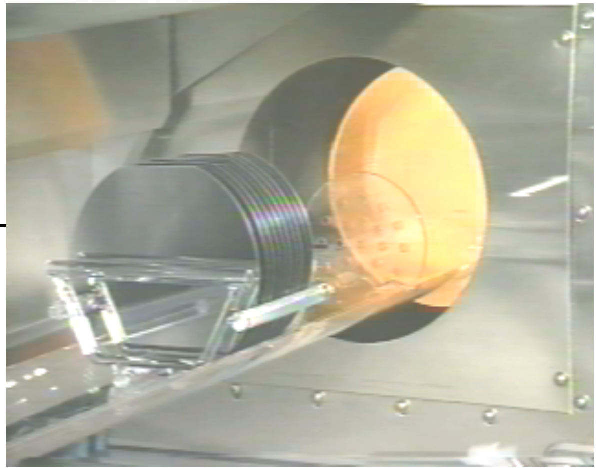
GROW TRENCH LINER OXIDE



Pad Oxide, 500A

Bruce Furnace 04 Recipe 250

Substrate 10 ohm-cm



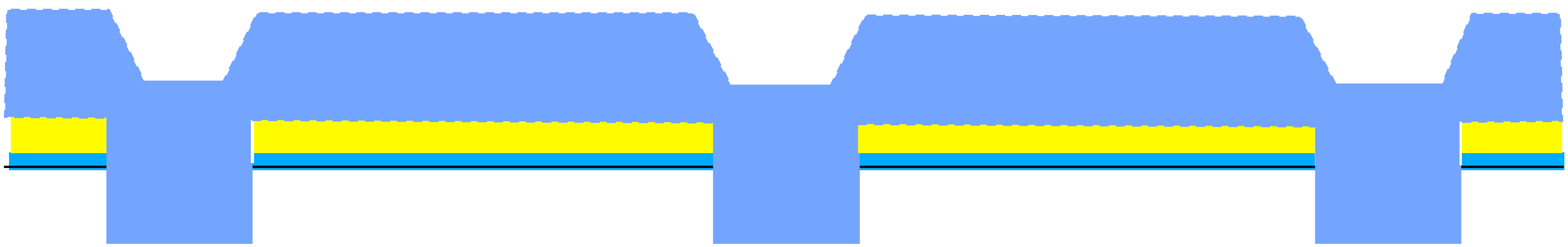
Rochester Institute of Technology
Microelectronic Engineering

APPROACH FOR WELL FORMATION IN ADVANCED CMOS PROCESS

The preferred Adv-CMOS process calls for ion implanting the well through the filled trenches. This requires exact trench depths, exact CMP stop, and high energy implants requiring thick photoresists (~1.7μm).

(At RIT, we choose well implant before fill and CMP)

DEPOSIT LTO TRENCH FILL

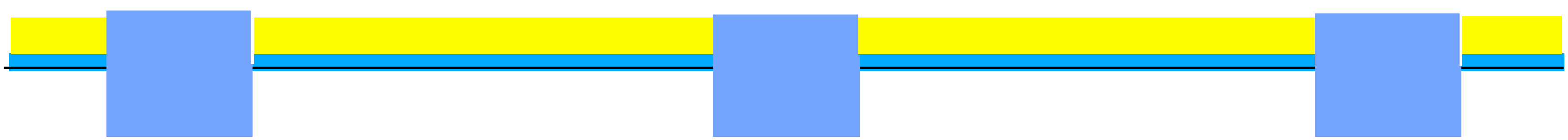


Substrate 10 ohm-cm

Fill 4000 Å trench
Deposit 6000 Å LTO

Recipe A6-FAC 0.6M TEOS
390 °C, 60 sec

AFTER CMP



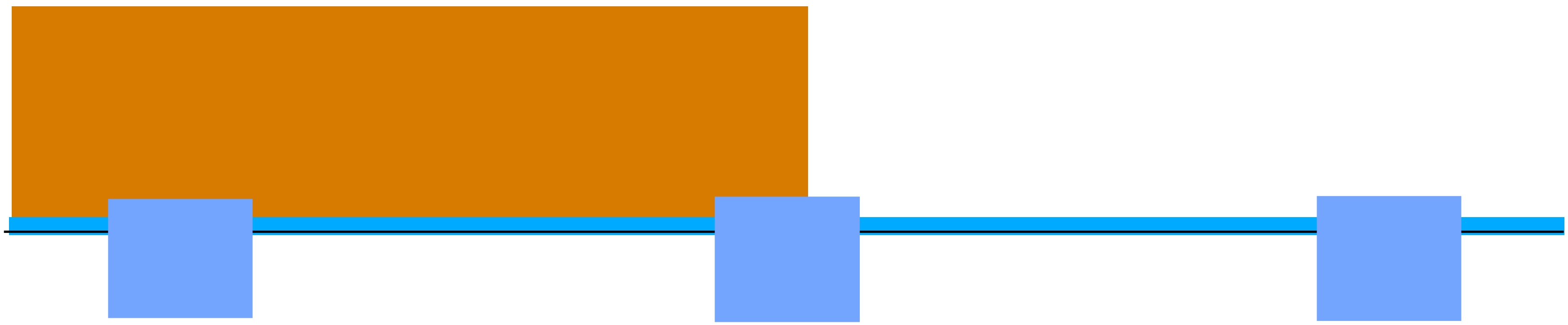
Substrate 10 ohm-cm

HOT PHOSPHORIC ACID NITRIDE ETCH

30s Dip in 5:1 BHF, Rinse
Hot Phosphoric Acid
Wet Nitride Etch.
Etch Rate ~80 Å/min
Etch ~20 min.

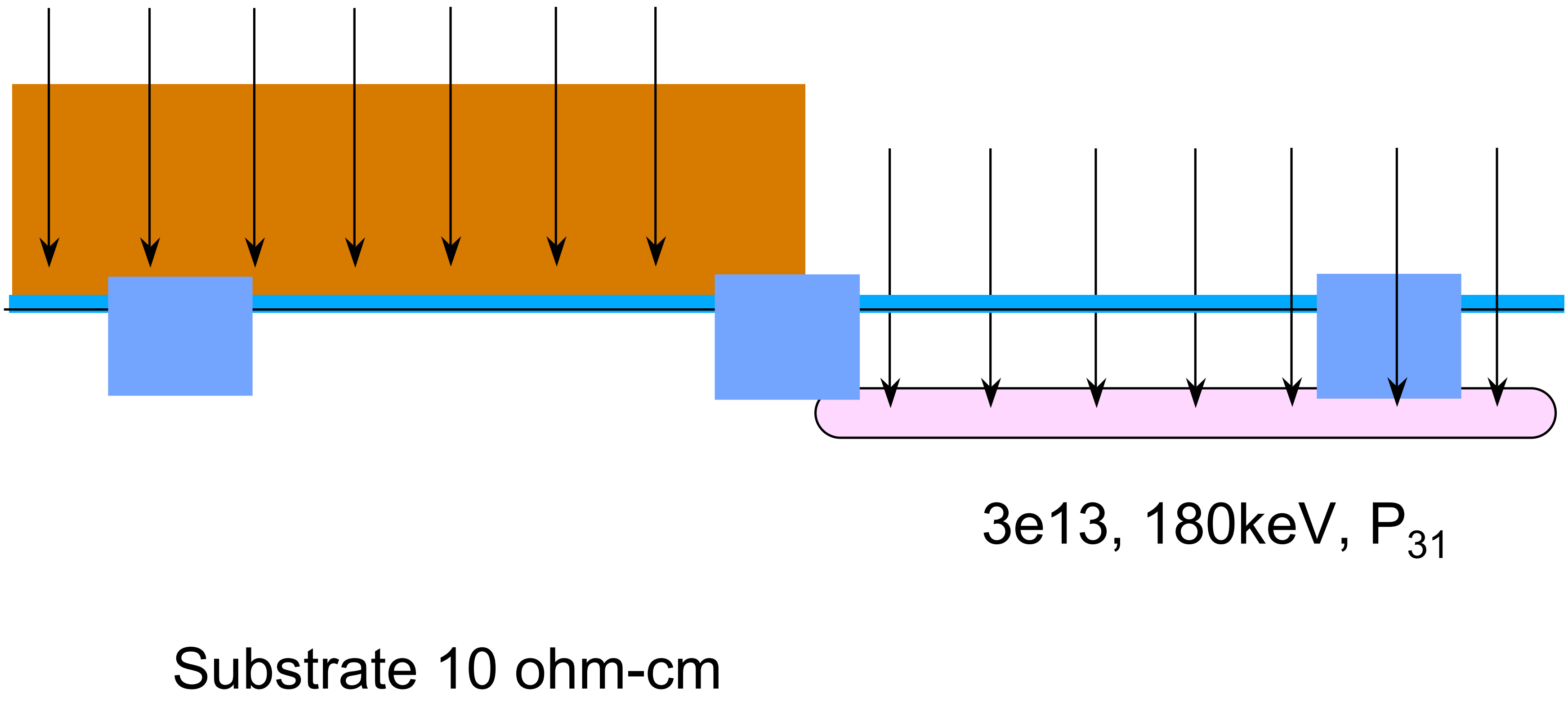
Substrate 10 ohm-cm

PHOTO 2 N-WELL



Need thicker resist
Use COATMTL.RCP (2000rpm, 30 sec gives 1.3µm)
and DEVMTL.RCP (~75 seconds)

N-WELL IMPLANT



Trench Fill and CMP First

STRIP RESIST

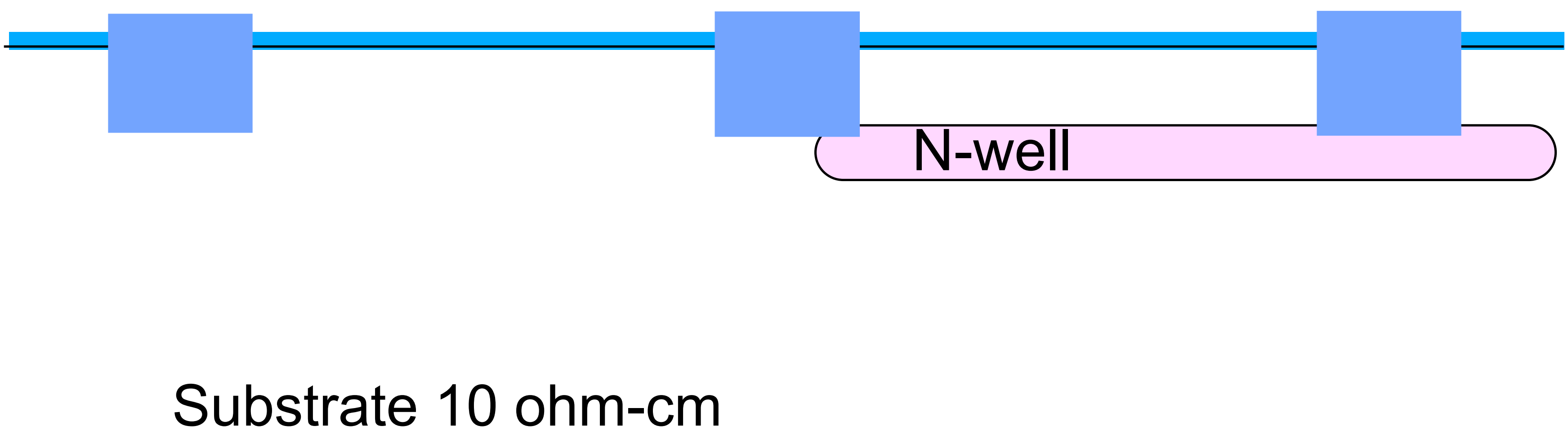
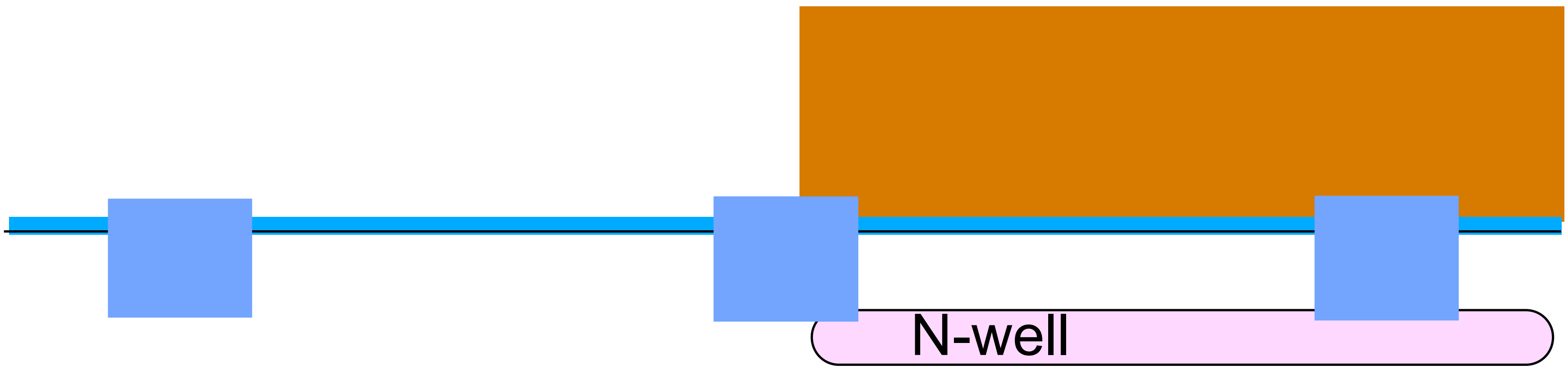
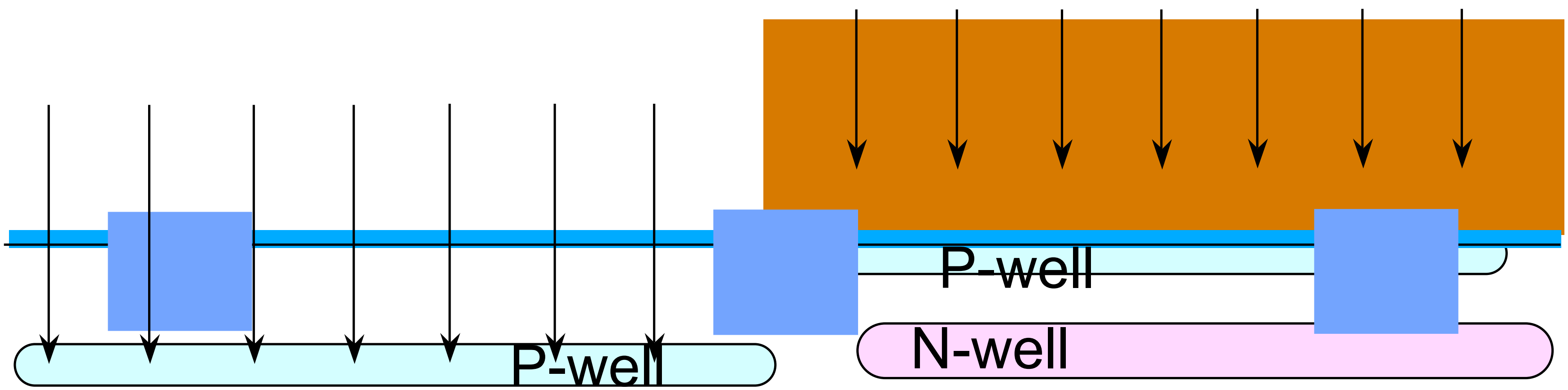


PHOTO 3 P-WELL



Need thicker resist
Use COATMTL.RCP (2000rpm, 30 sec gives 1.3µm)
and DEVMTL.RCP (~75 seconds)

ION IMPLANT P-WELL

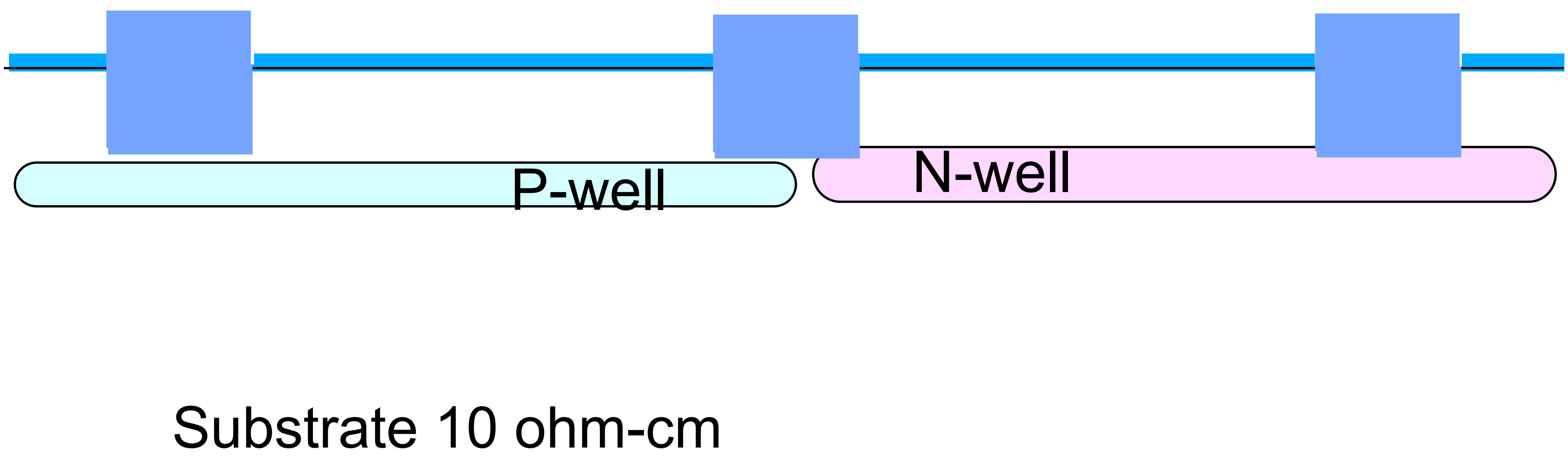


3e13, 150keV, B_{11}

Substrate 10 ohm-cm

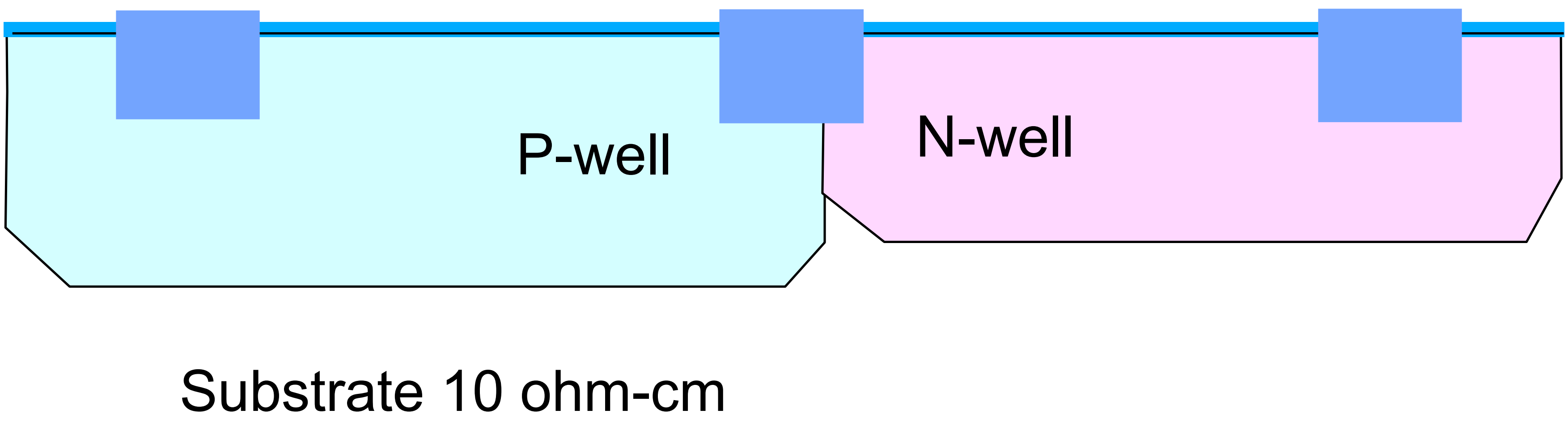
Trench Fill and CMP First

Strip Resist



WELL DRIVE

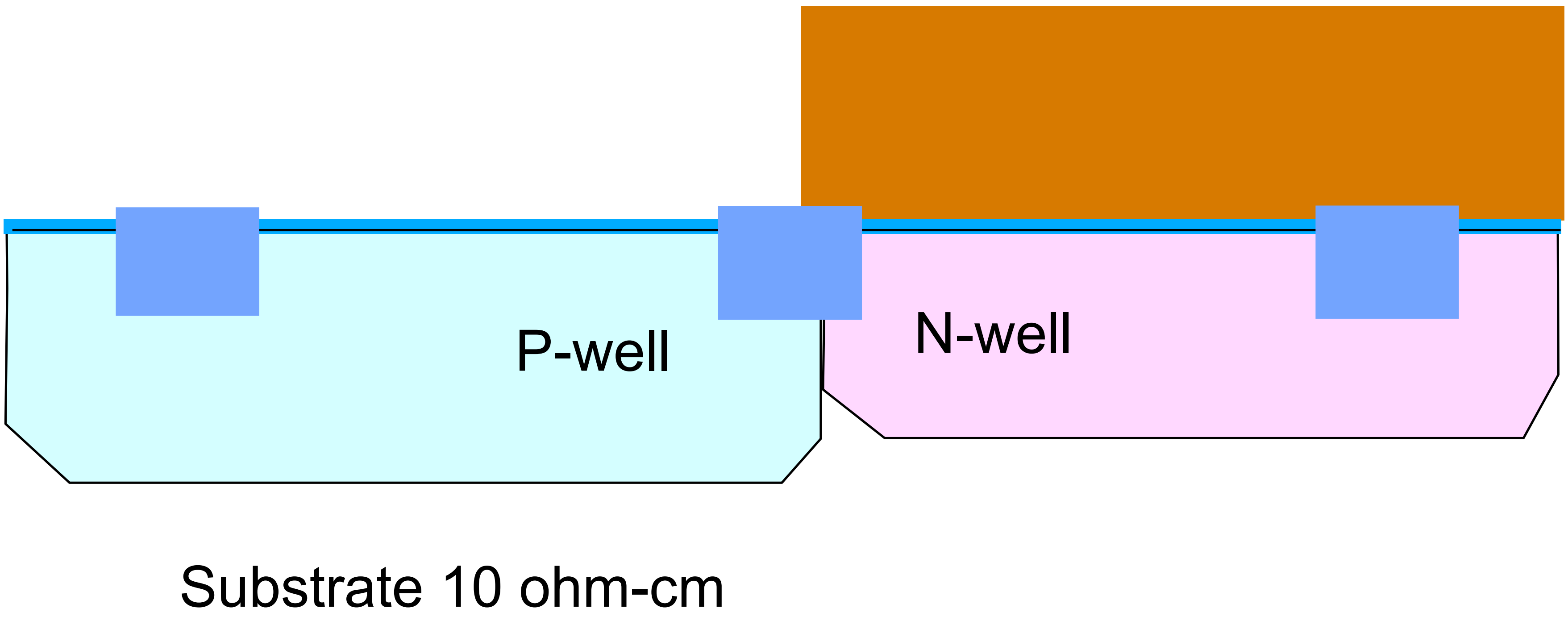
6 hrs, 1100 °C



WELL PARAMETERS

	Design Parameters
N well	
Dose (cm-2)	3E13
Energy (KeV)	
Surface Conc.	~1E17
N well Xj (µm)	~3.0
P well	
Dose (cm-2)	3E13
Energy (KeV)	
Surface Conc.	~1E17
P well Xj (µm)	~3.0

PHOTO - NMOS VT ADJUST



NMOS VT ADJUST IMPLANT

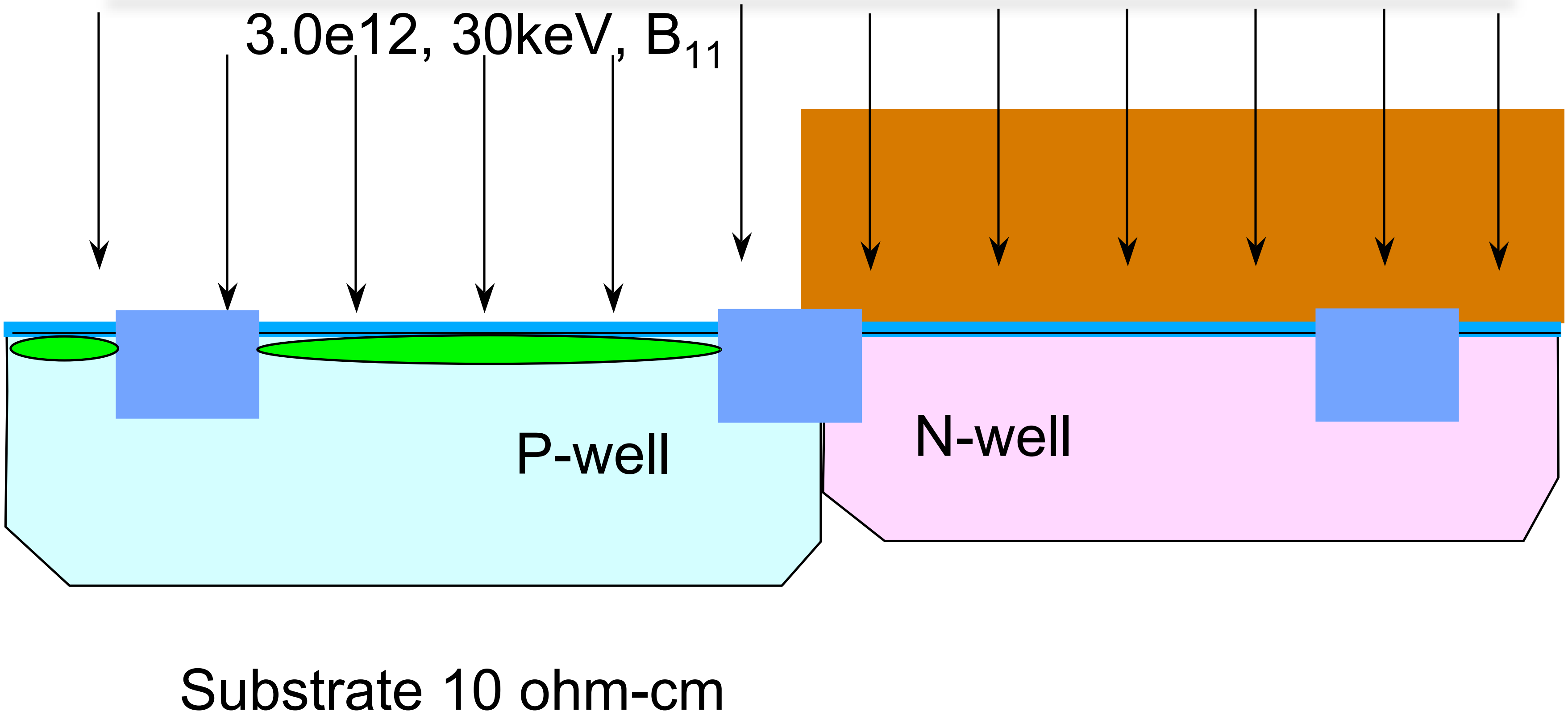
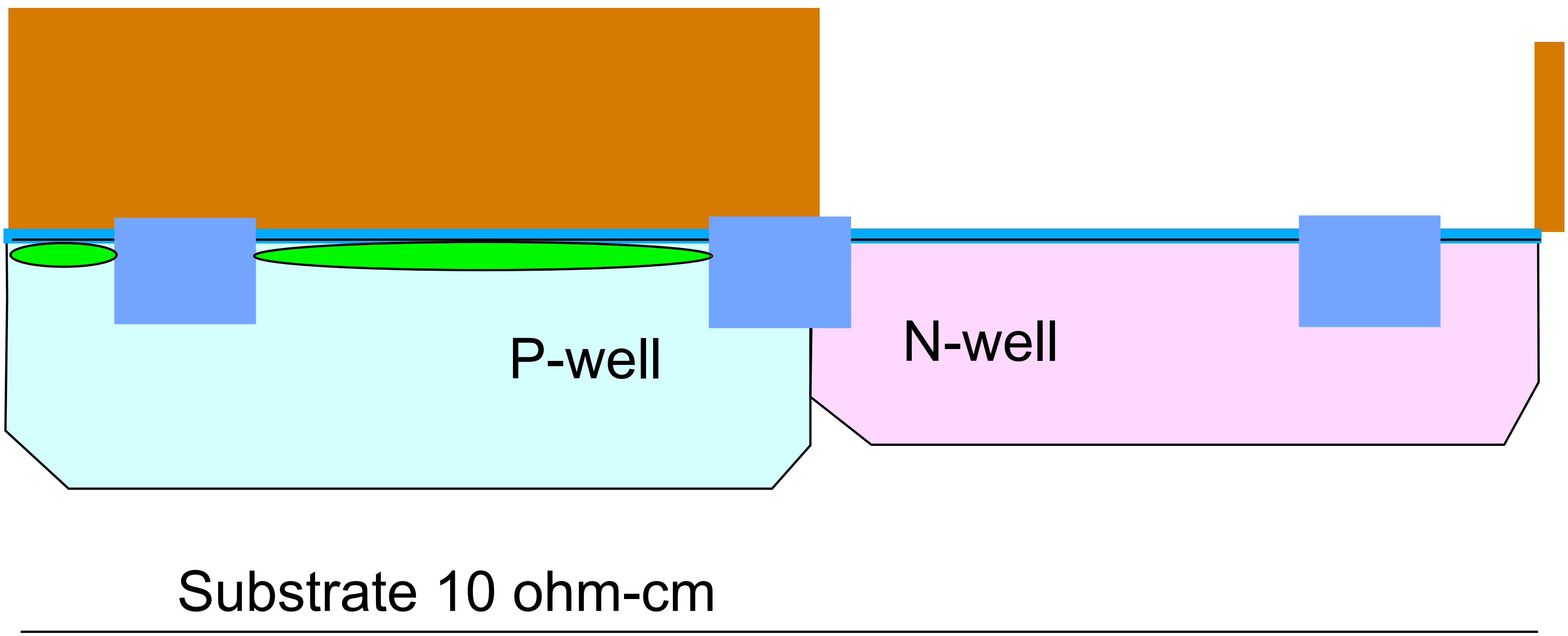
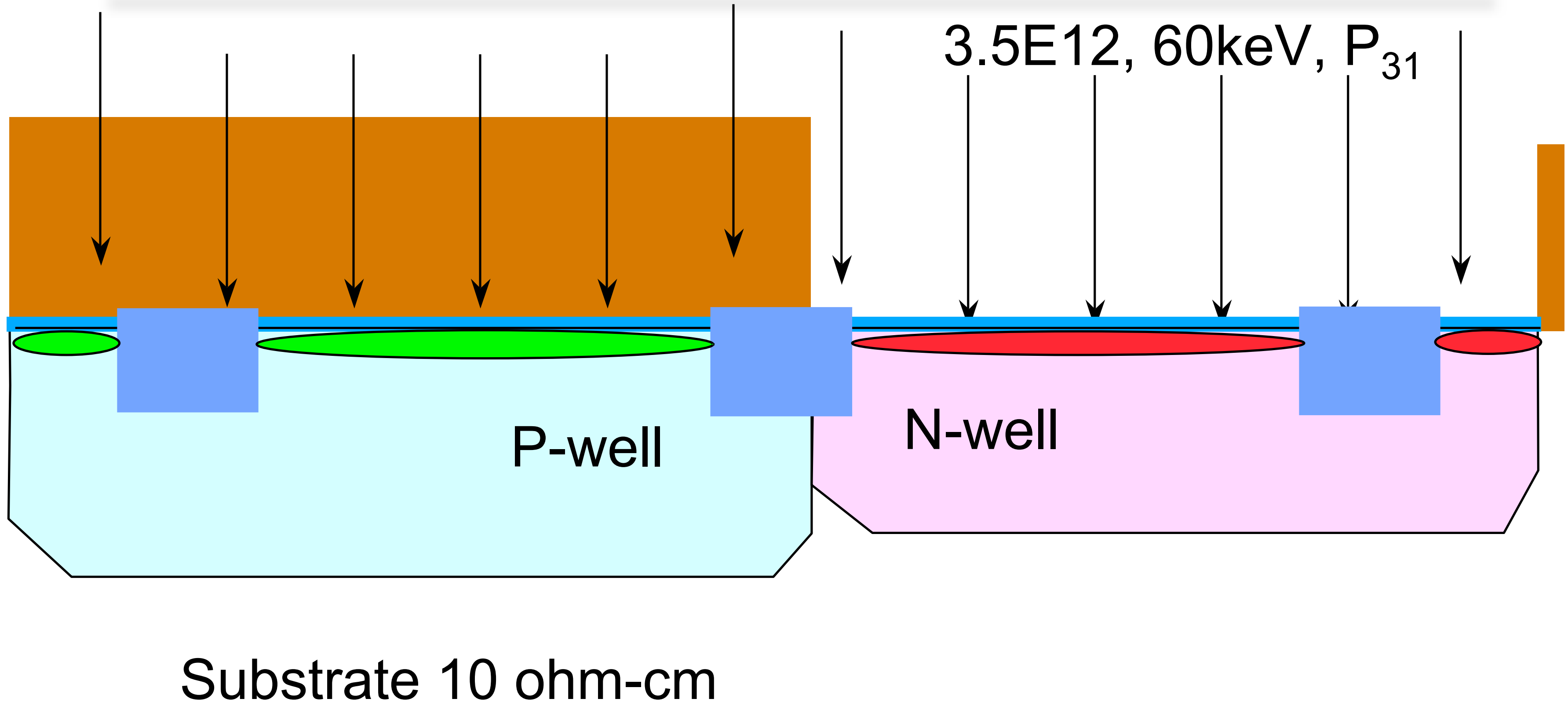


PHOTO PMOS VT ADJUST

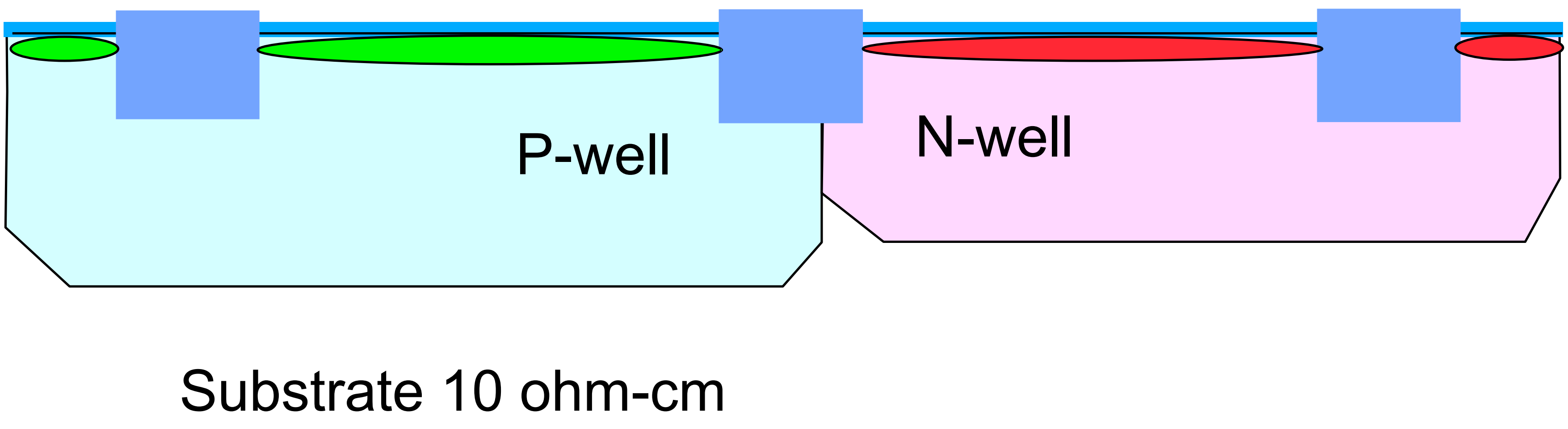


PMOS VT IMPLANT



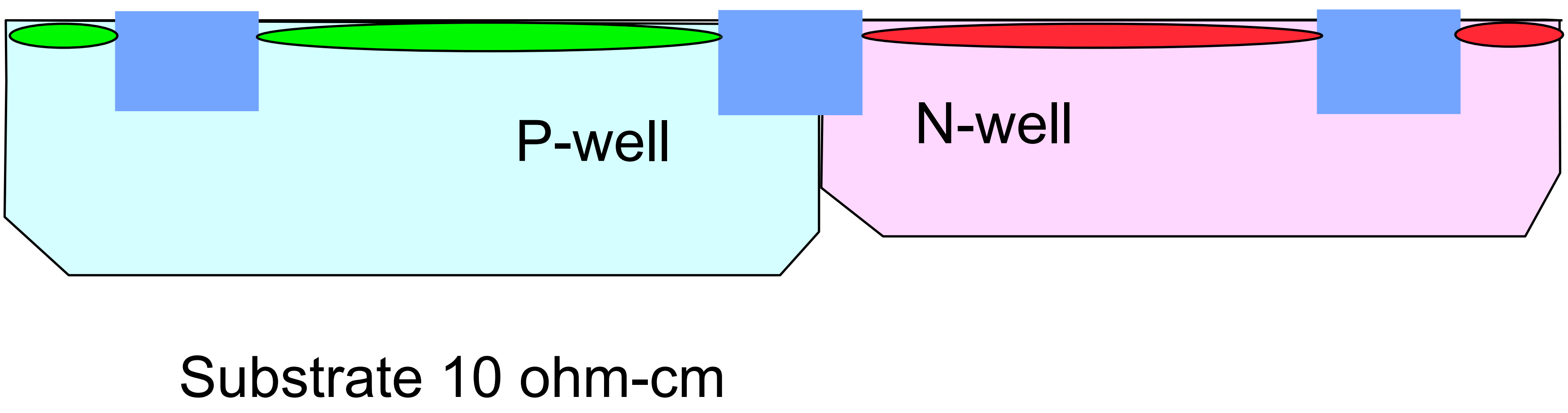
Rochester Institute of Technology
Microelectronic Engineering

STRIP RESIST



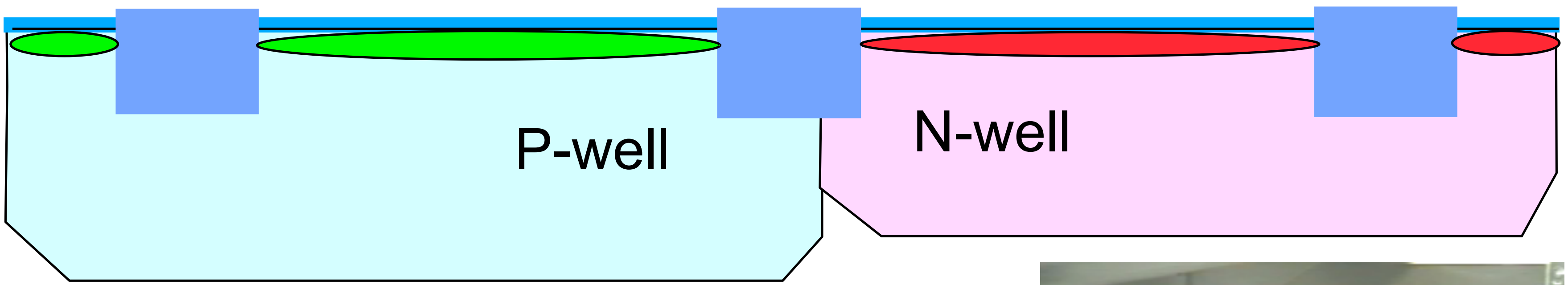
OXIDE ETCH

Etch in 10:1 BOE
45 seconds, Rinse, SRD

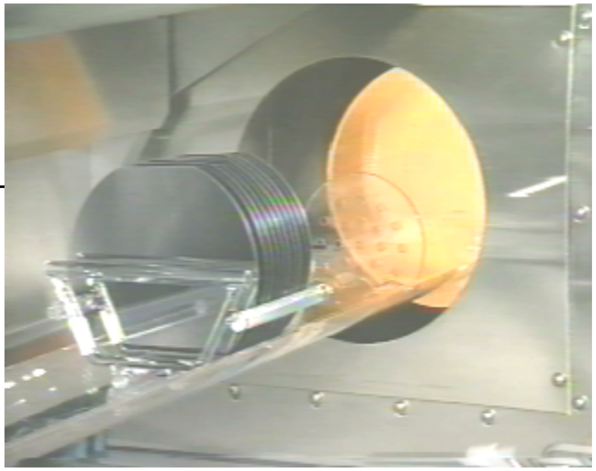


RCA CLEAN AND GROW GATE OXIDE

Just Prior to Gate Oxide Growth
Etch wafers in 50:1 HF, 1 min.
Grow Oxide, 100Å, Dry O_2
Bruce Furnace04 Recipe 213



Substrate 10 ohm-cm



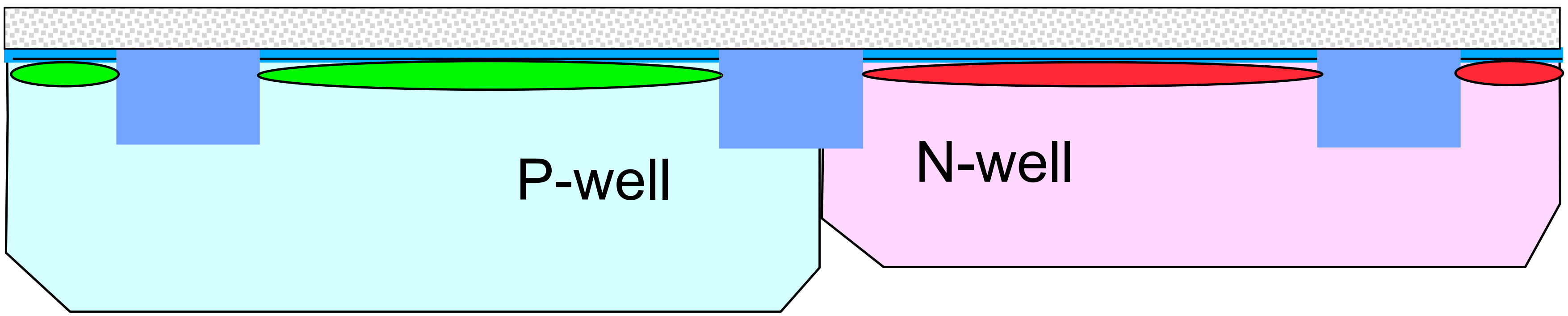
INCORPORATING NITROGEN IN THIN GATE OXIDES

In today's deep sub-micron transistors the pMOSFET normally has p+Poly for the gate material. The gate oxide is 100Å or less. The p+ dopant is normally Boron and **Boron diffuses quickly** (compared to Phosphorous) **through oxides**. Since the gate oxides are thin this could allow Boron to diffuse through the gate oxide and dope the channel causing the transistors to not function correctly.

If some nitrogen is incorporated in the gate oxide the diffusion of Boron is much lower. This project involved developing a gate oxide recipe that will result in **nitrogen incorporation in the gate oxide**. The recipe included 30 min anneal in N2, 30 min oxynitride growth in N2O and 30 min oxide growth in O2, all at 900 °C.

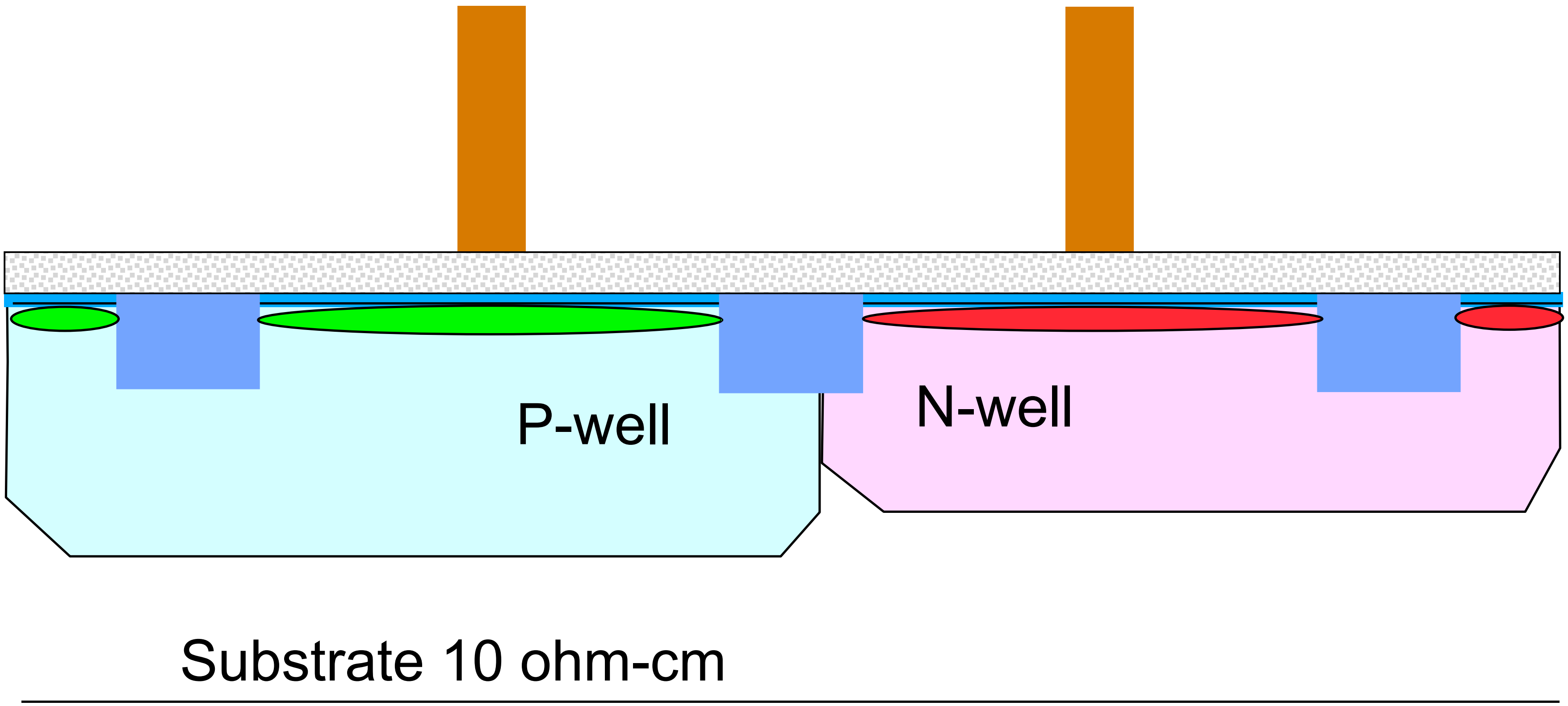
LPCVD POLY

Polysilicon, 4000A
LPCVD, 610C, ~55min
100 sccm of SiH4, 300 mTorr



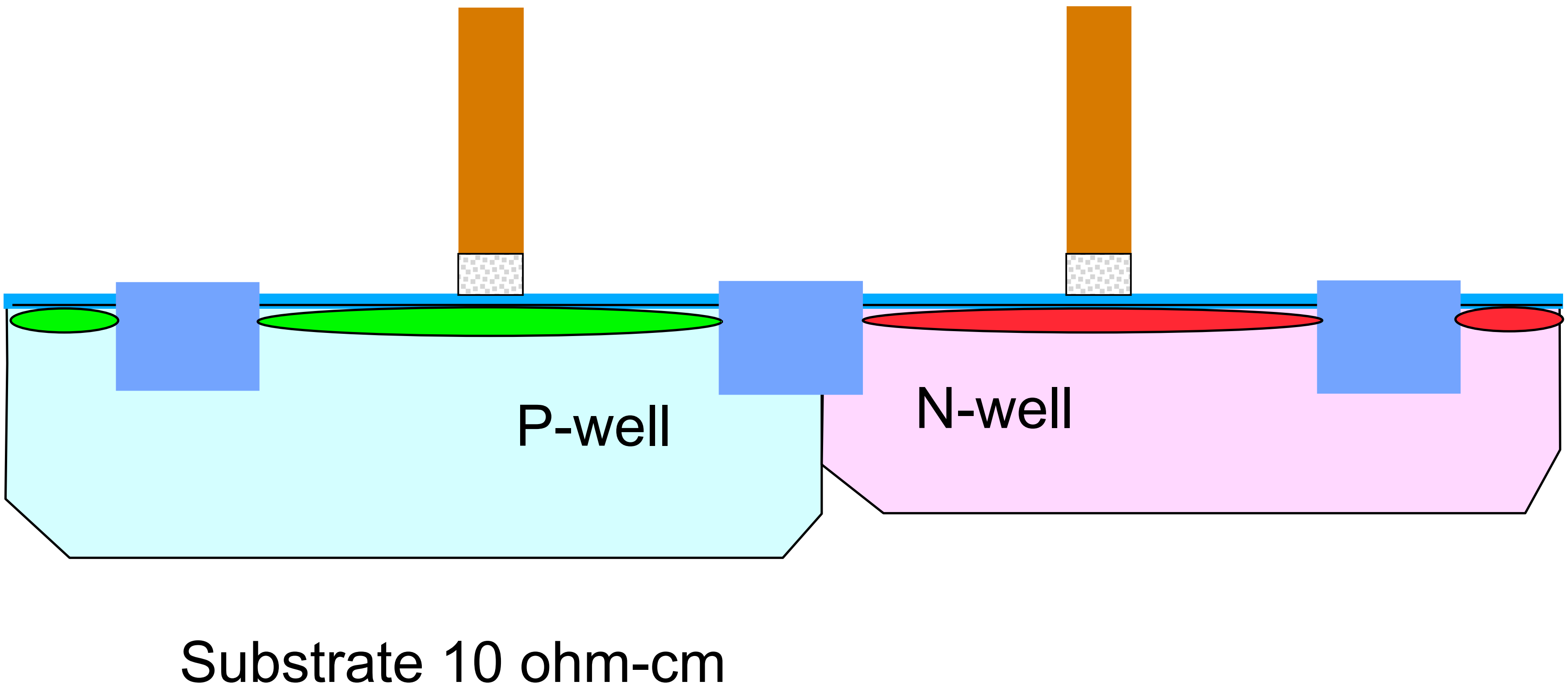
Substrate 10 ohm-cm

PHOTO 6 POLY GATE

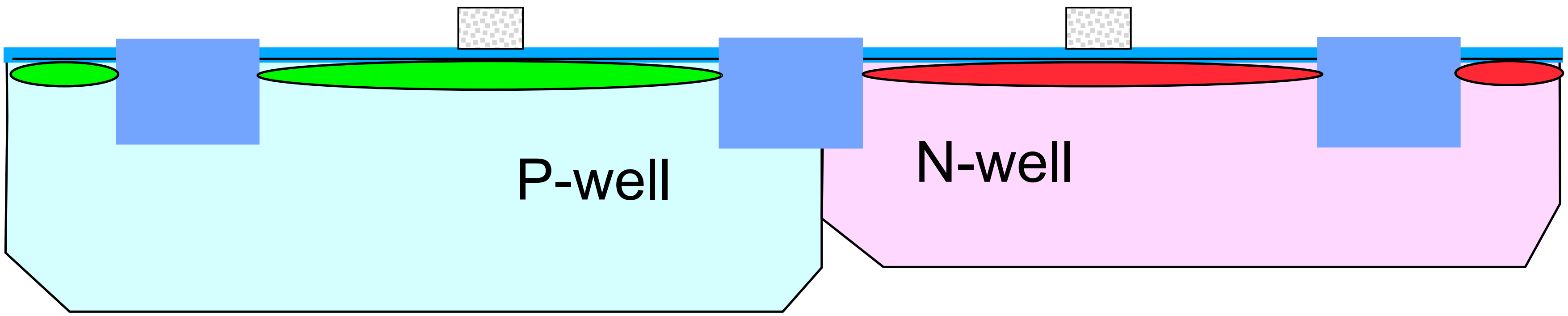


Rochester Institute of Technology
Microelectronic Engineering

POLY ETCH



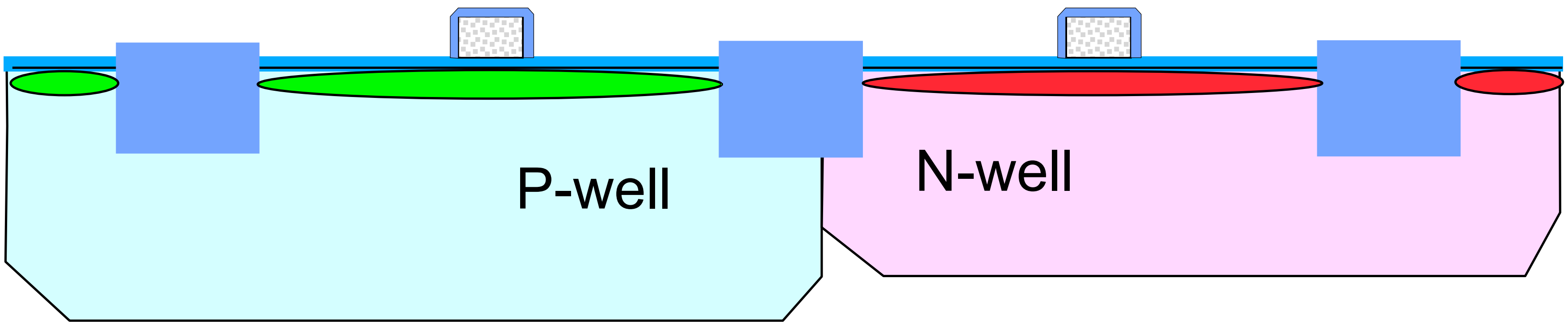
STRIP RESIST / RCA Clean



Include D1-D3
Strip Photresist in Branson Asher

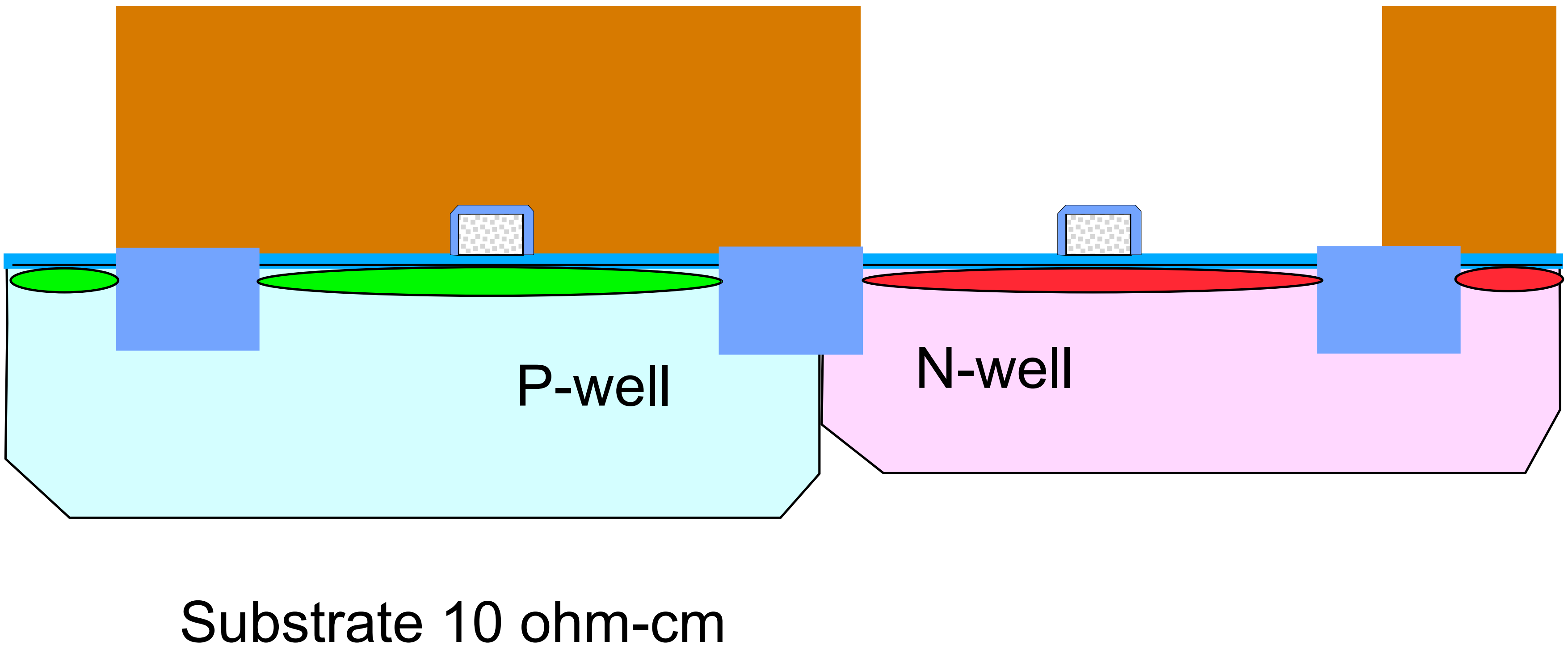
POLY REOX OXIDE

Oxide, 500A
Bruce Furnace 04 Recipe 250
~45 min at 1000 °C

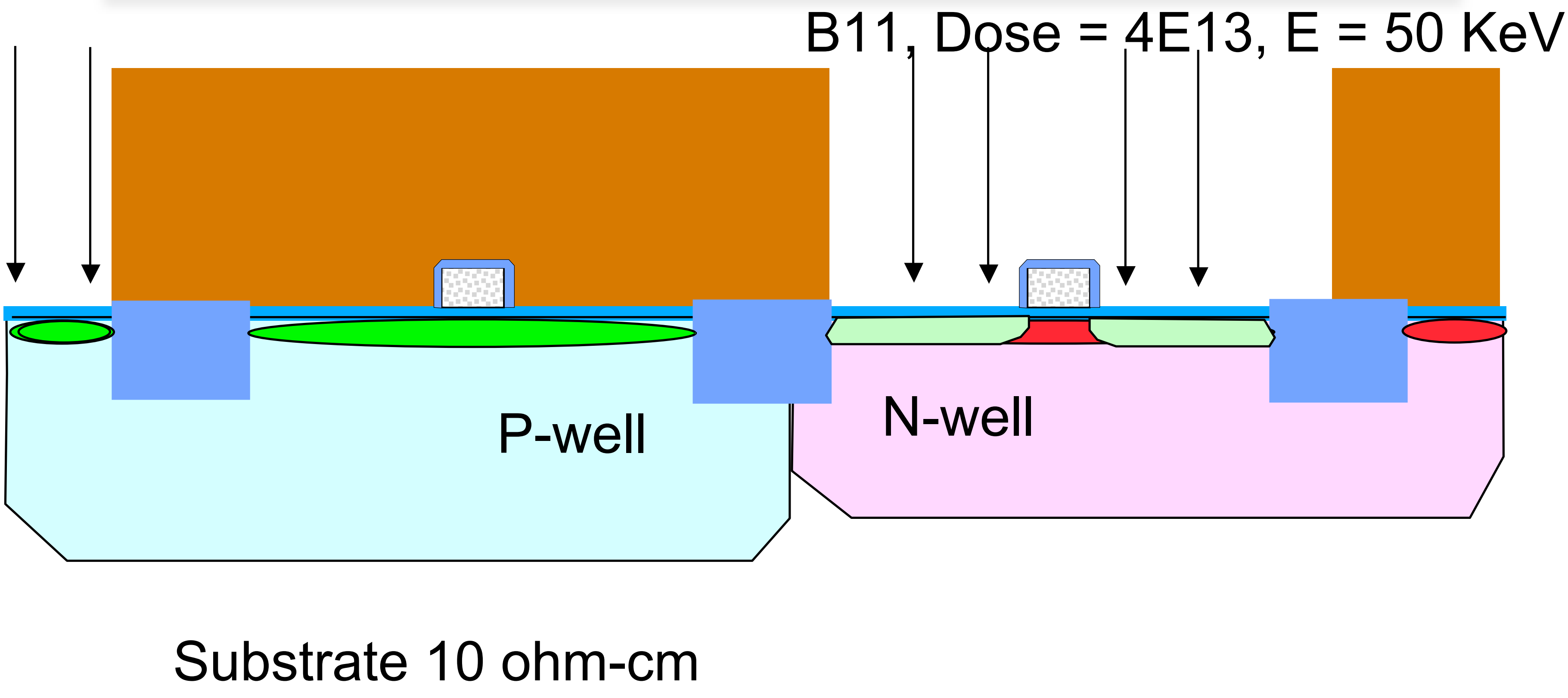


protects exposed edge of gate oxide

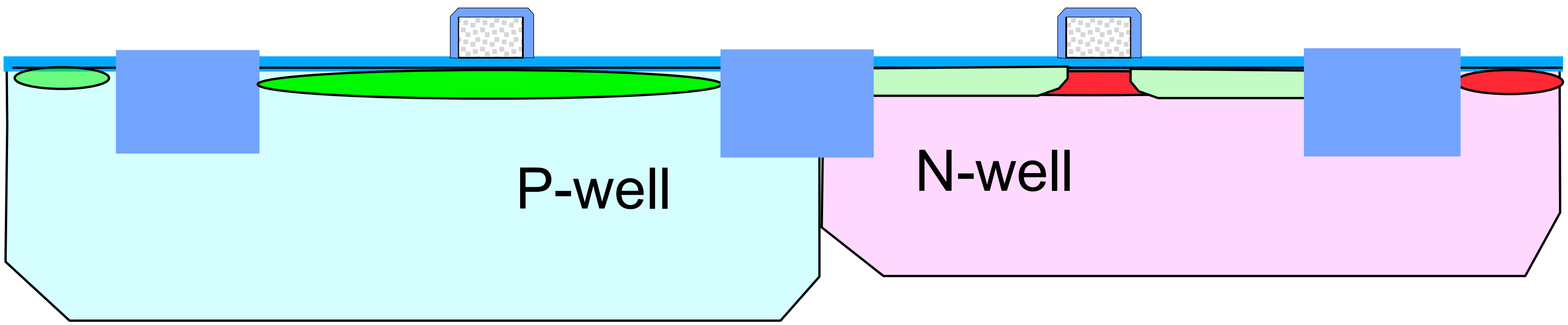
PHOTO 7 LDD P-TYPE IMPLANT



IMPLANT P-LDD

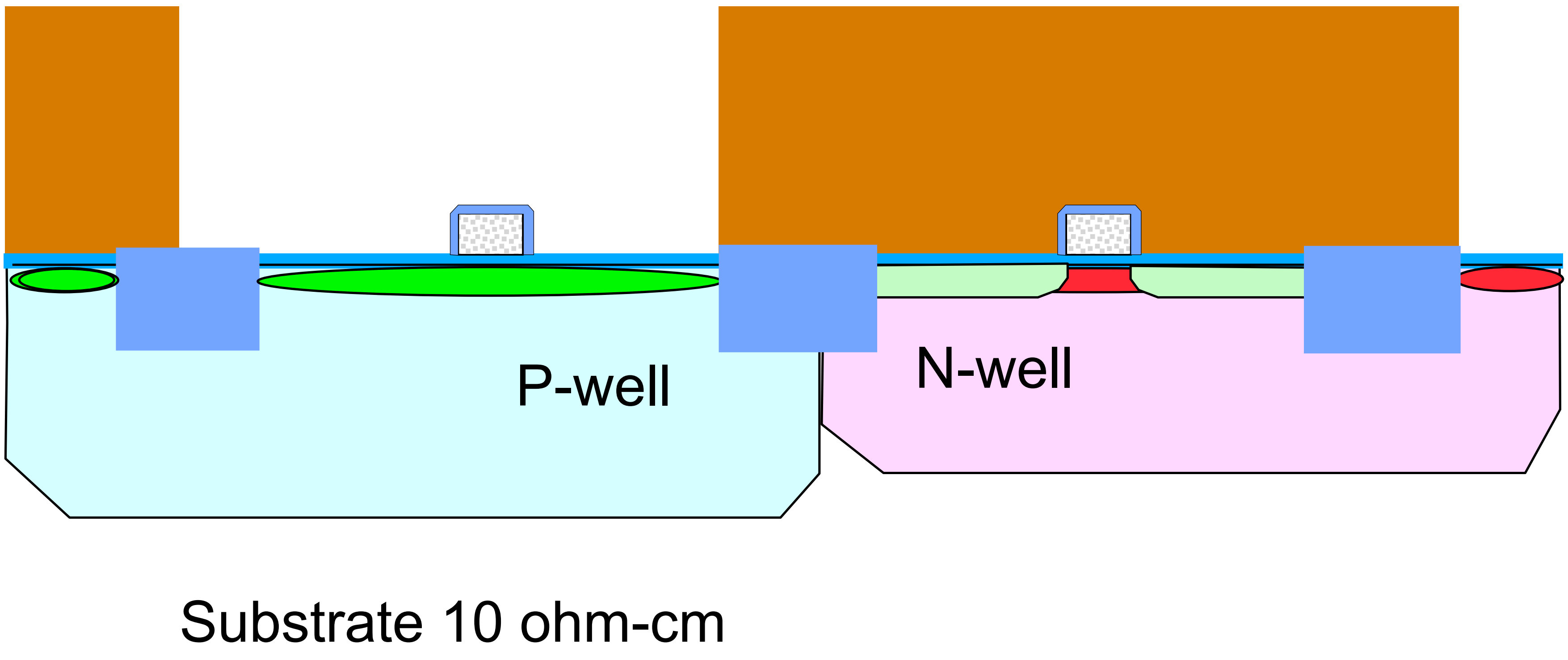


STRIP RESIST



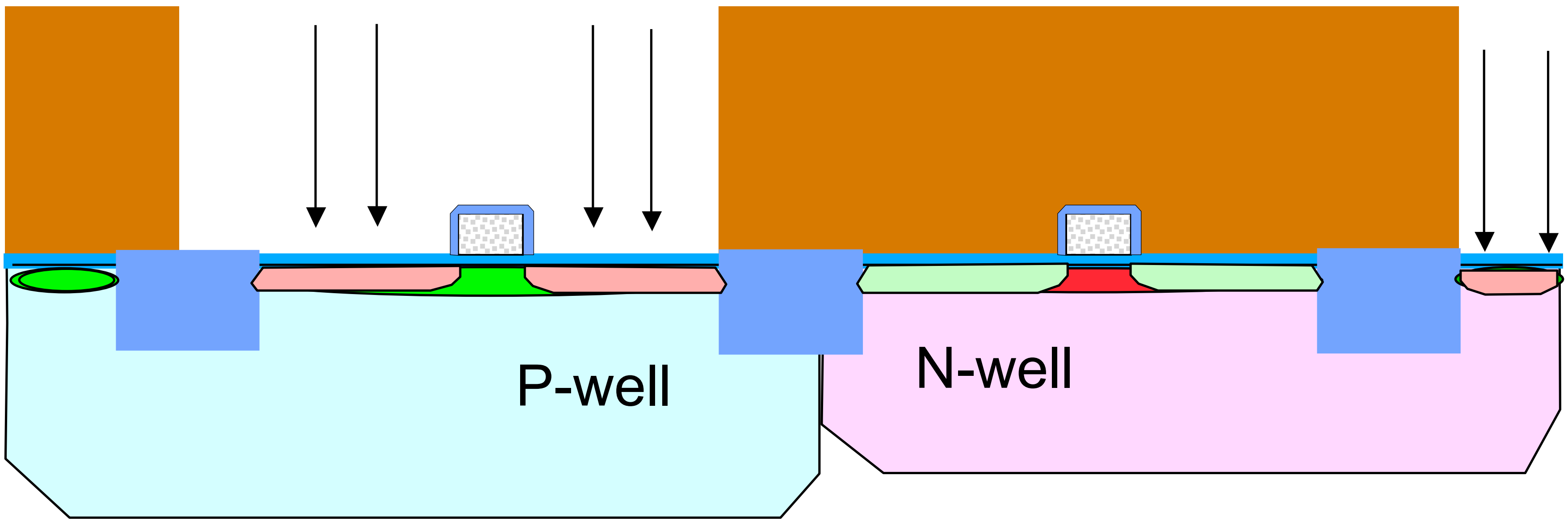
Include D1-D3
Strip Photresist in Branson Asher

PHOTO 8 LDD N-TYPE IMPLANT



IMPLANT N-LDD

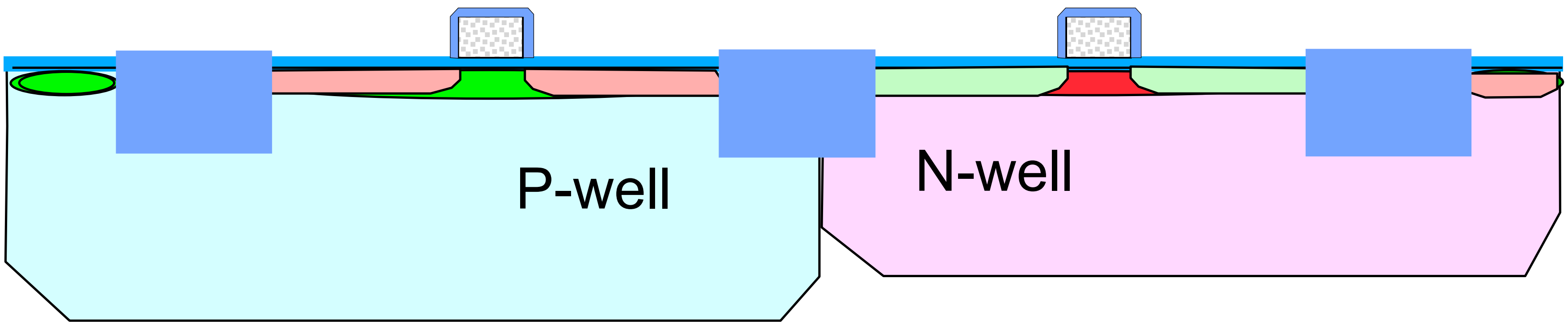
P31, Dose = 4E13, E = 60 KeV



Substrate 10 ohm-cm

Rochester Institute of Technology
Microelectronic Engineering

STRIP RESIST

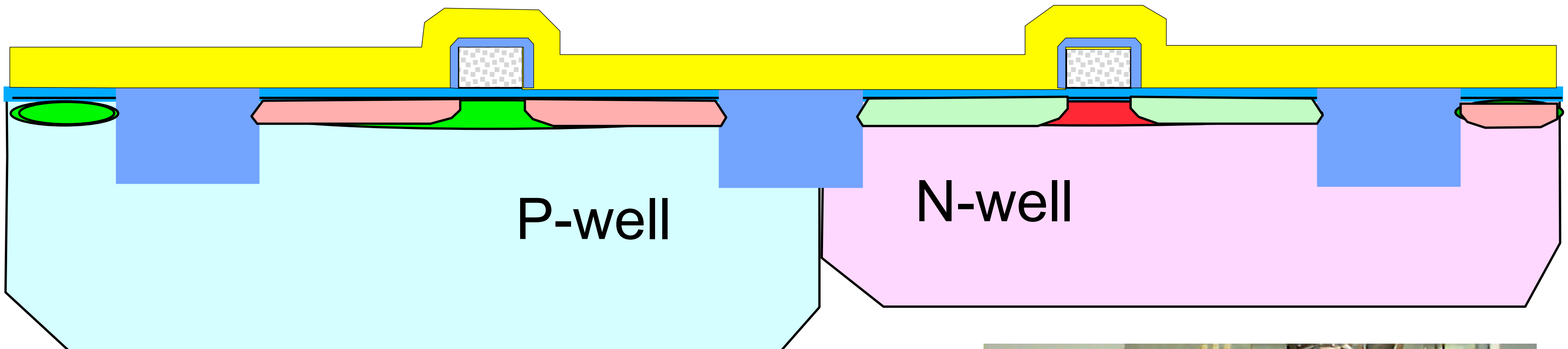


Include D1-D3
Strip Photresist in Branson Asher

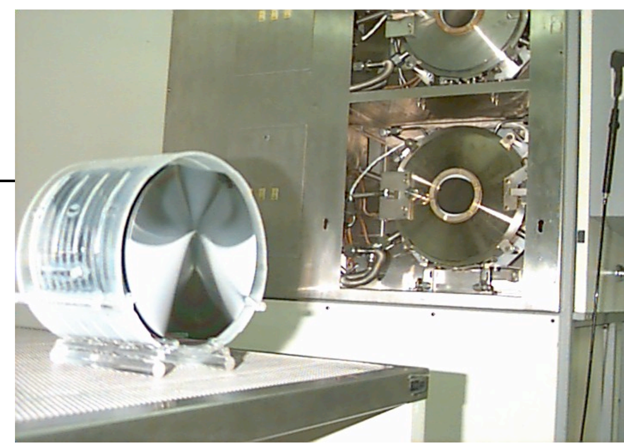
RCA CLEAN AND LPCVD NITRIDE

LPCVD Nitride 810°C
400 mTorr, NH3 flow = 150 sccm
Dichlorosilane flow = 60 sccm

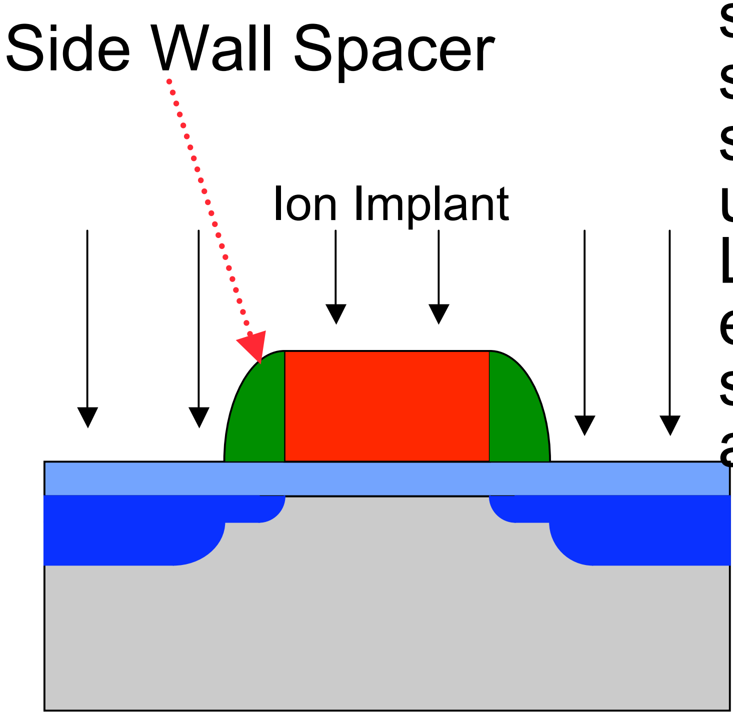
Target 3500 Å



ASM 6" LPCVD Tool



NITRIDE SIDE WALL SPACERS

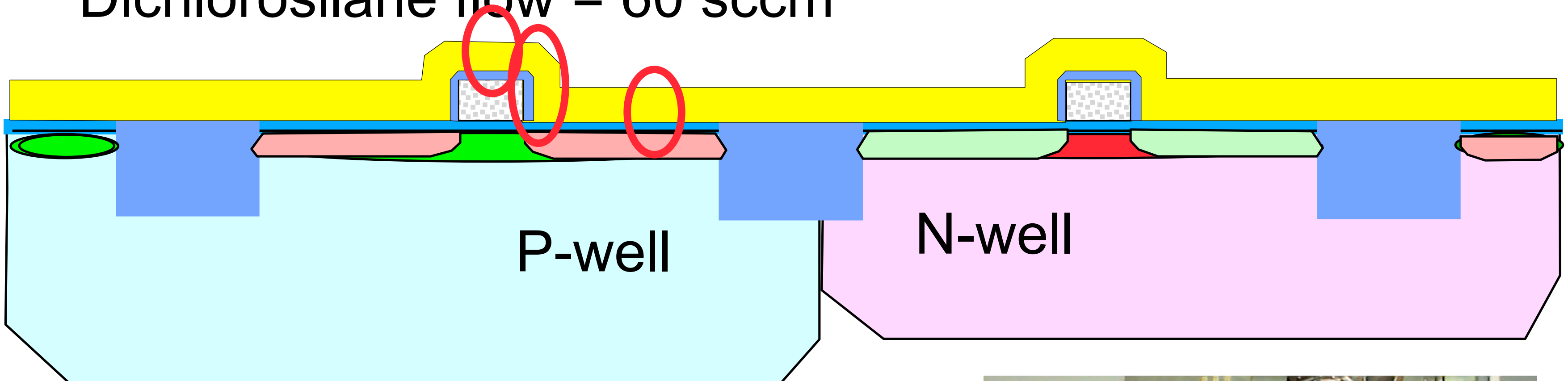


Nitride as a **side wall spacer** in deep sub micron transistor fabrication has some advantages over oxide side wall spacers. Nitride LPCVD is a more uniform and more conformal film than LTO. Nitride offers the possibility of end-point detection and higher selectivity during the plasma etch, while an oxide spacer does not.

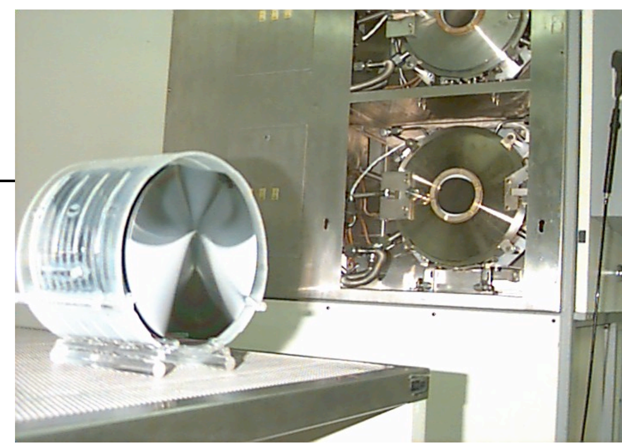
RCA CLEAN AND LPCVD NITRIDE

LPCVD Nitride 810°C
400 mTorr, NH_3 flow = 150 sccm
Dichlorosilane flow = 60 sccm

Target 3500 Å

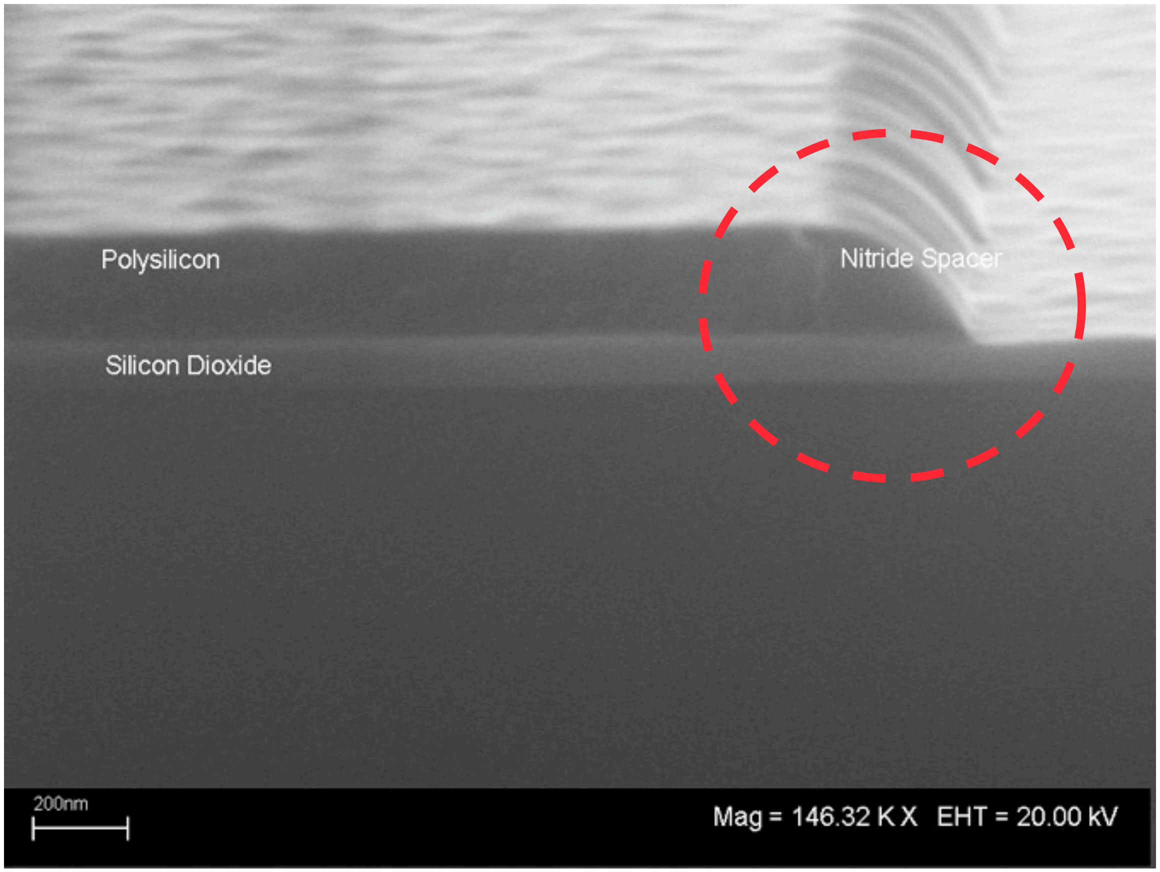


ASM 6" LPCVD Tool



Rochester Institute of Technology
Microelectronic Engineering

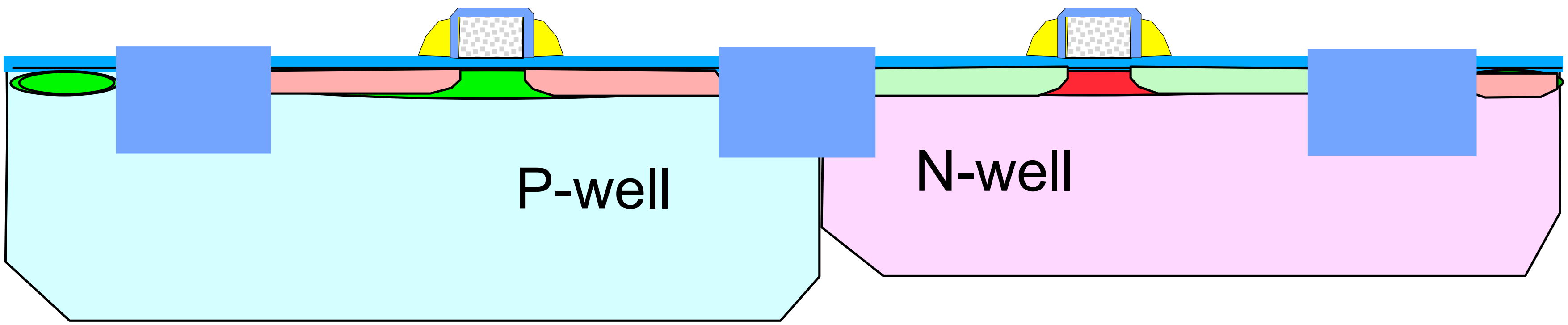
NITRIDE SIDE WALL SPACERS



Poly thickness = 2300 A
Oxide thickness = 1000A
Spacer Height = 2300 A
Spacer Width = 0.3 um

Special thanks to Dr. Sean Rommel for help in using the new LEO SEM

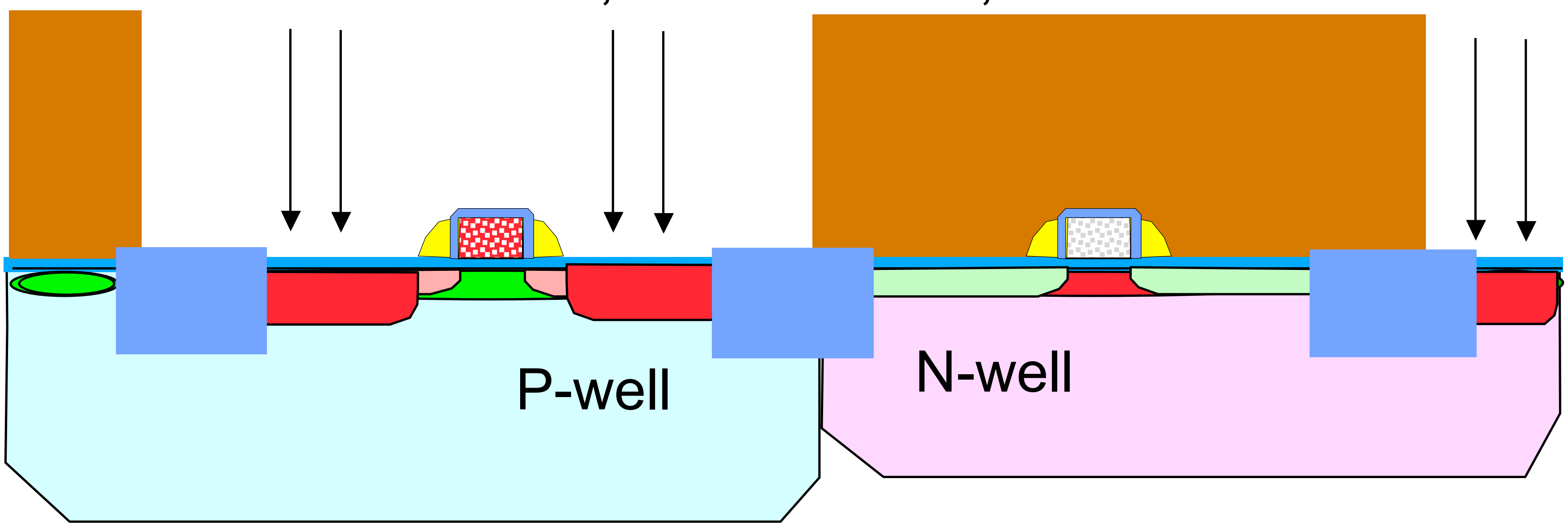
AFTER ETCH NITRIDE TO FORM SIDE WALL SPACERS



Rochester Institute of Technology
Microelectronic Engineering

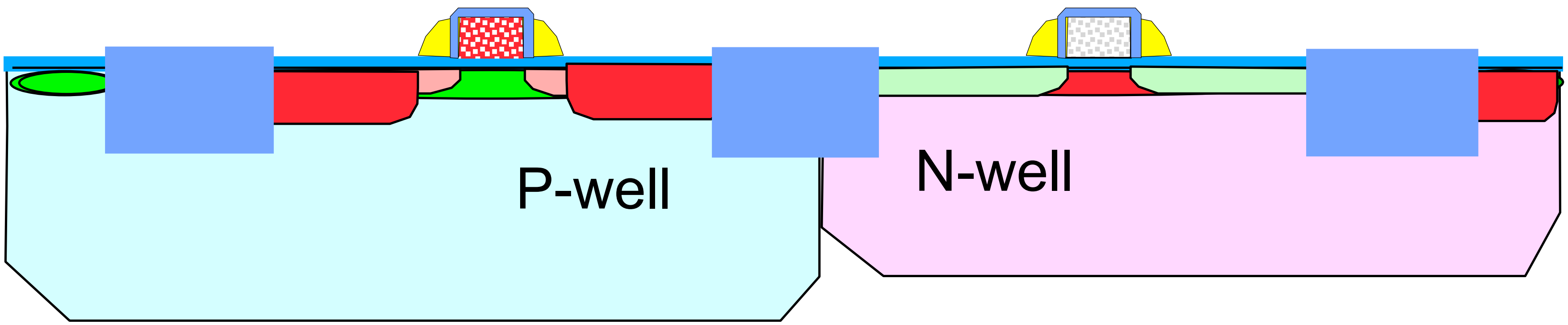
PHOTO 9 N+ D/S

P31, Dose = 4 E15, E = 60 KeV



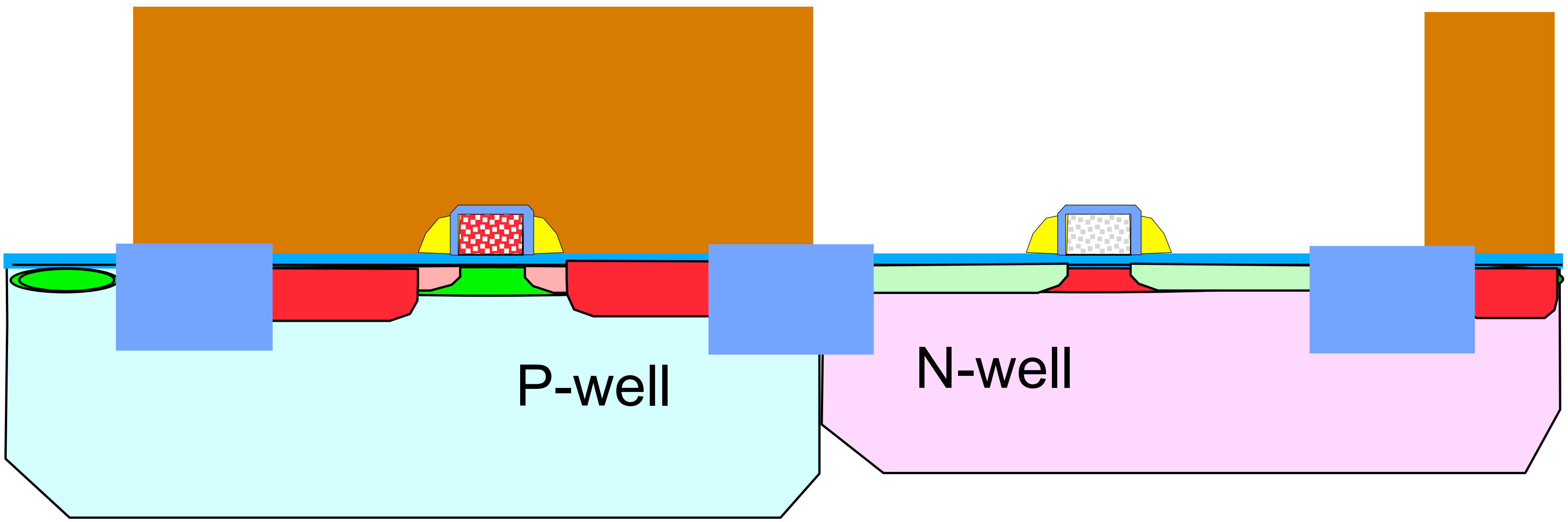
Rochester Institute of Technology
Microelectronic Engineering

STRIP RESIST

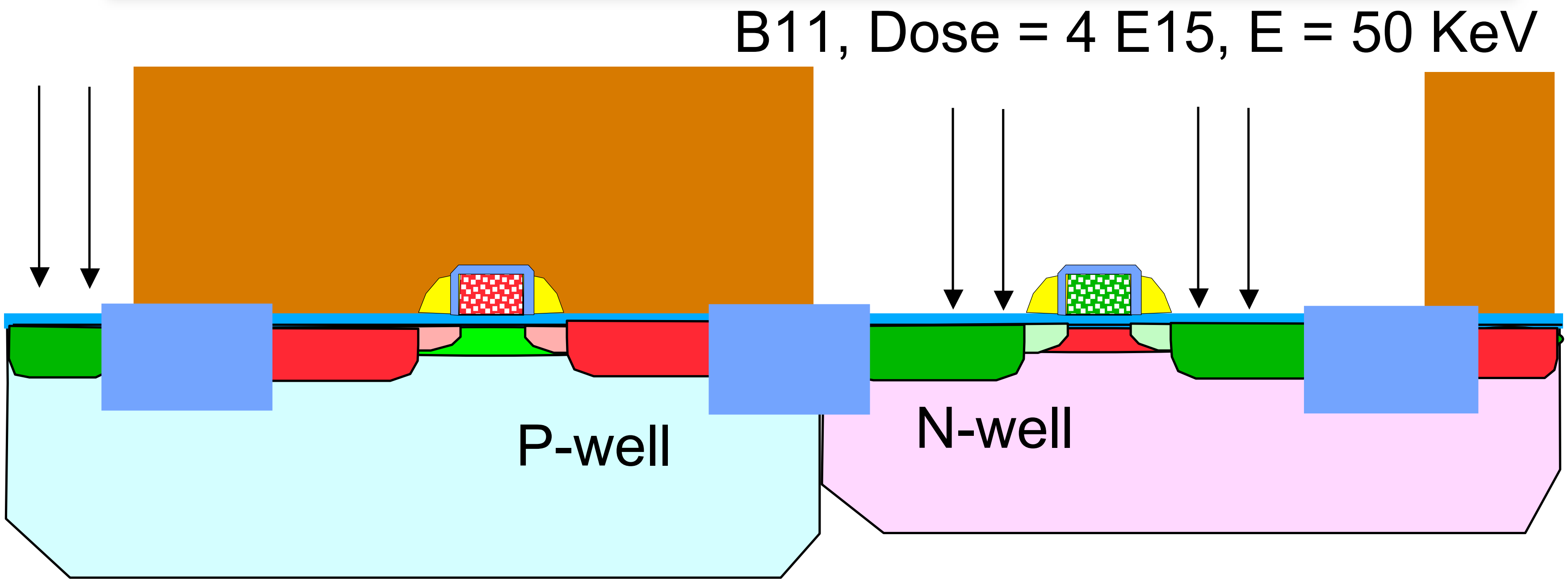


Include D1-D3
Strip Photresist in Branson Asher

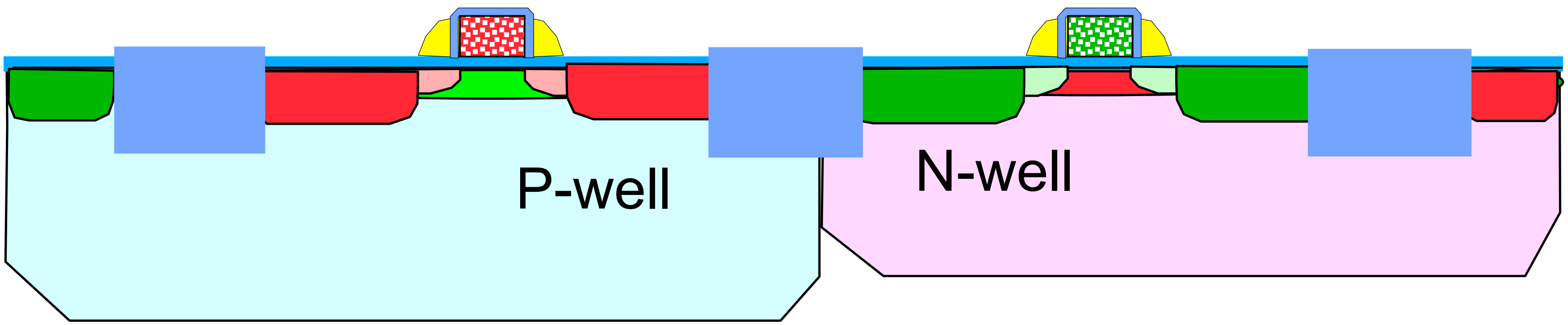
PHOTO 10 P+ D/S



IMPLANT P+ D/S

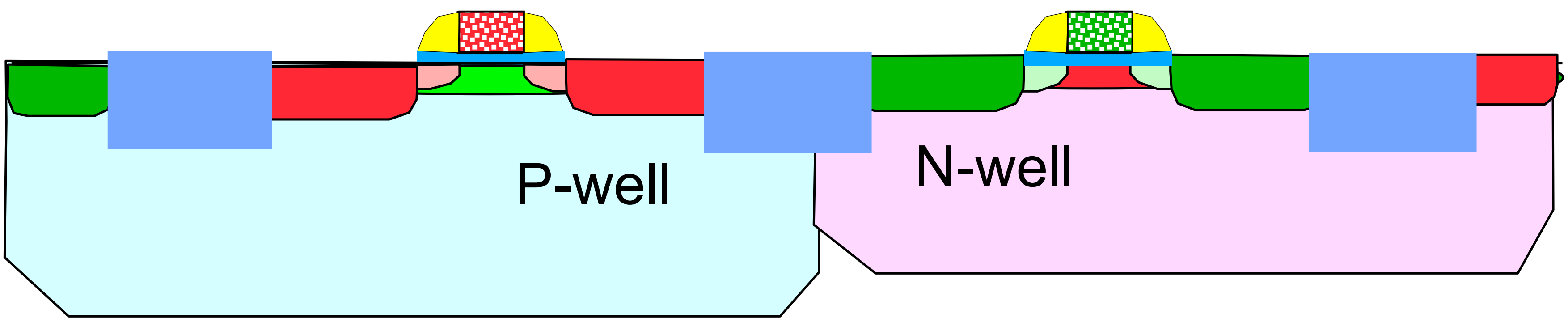


STRIP RESIST, RCA CLEAN



Include D1-D3
Strip Photresist in Branson Asher

ETCH OXIDE

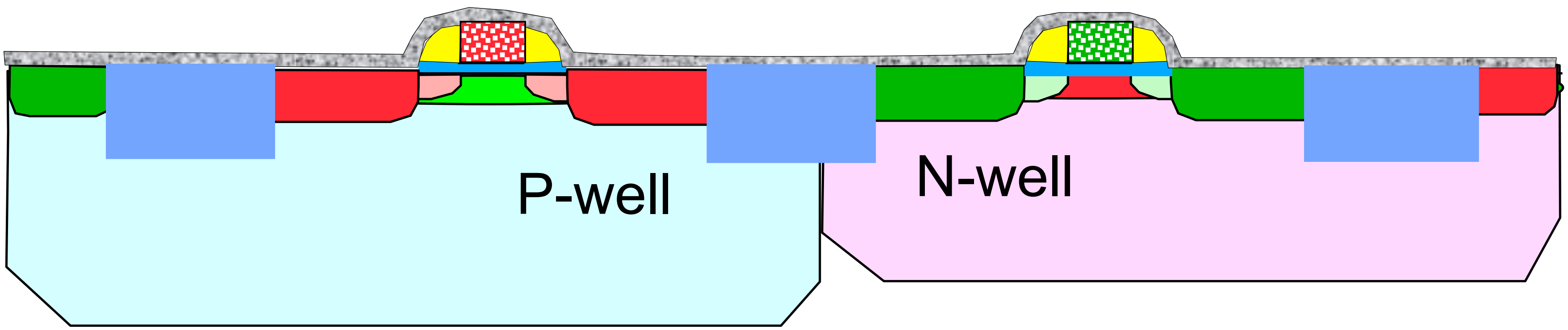


TiSi SALACIDE PROCESS

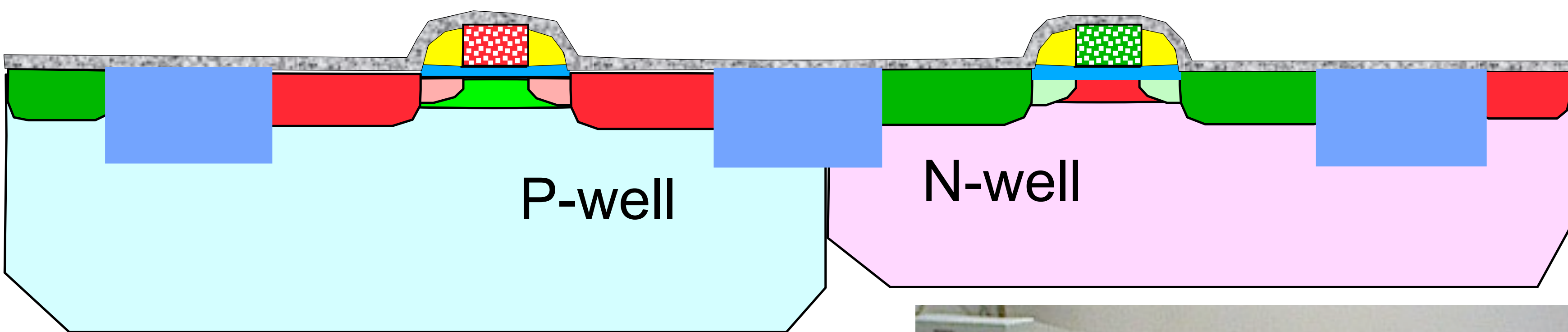
Forming a **metal silicide** helps reduce the resistance of the polysilicon interconnects and reduces the sheet resistance of the drain/source areas of the transistor. In deep sub-micron CMOS the nMOSFET transistor has n+ poly and the pMOSFET has p+ poly. Normally the poly is doped by ion implantation at the same time the drain and sources is implanted. In this case it is **essential to form a silicide to reduce the sheet resistance of the poly and to connect n+ and p+ poly where ever they meet**.

SALICIDE is an acronym for **self-aligned silicide** and can be achieved with the following process. Ti (or some other metal) is sputtered on the wafer. It is heated in vacuum or N2 atmosphere to form TiSi where ever the Ti metal is in contact with silicon but not where it is in contact with silicon dioxide. The wafer is etched in sulfuric acid and hydrogen peroxide mixture which removes the metal from the oxide regions leaving TiSi self aligned on the silicon areas. Further heat treating at a higher temperature can convert TiSi to **TiSi2 which has lower sheet resistance**.

AFTER Ti SPUTTER

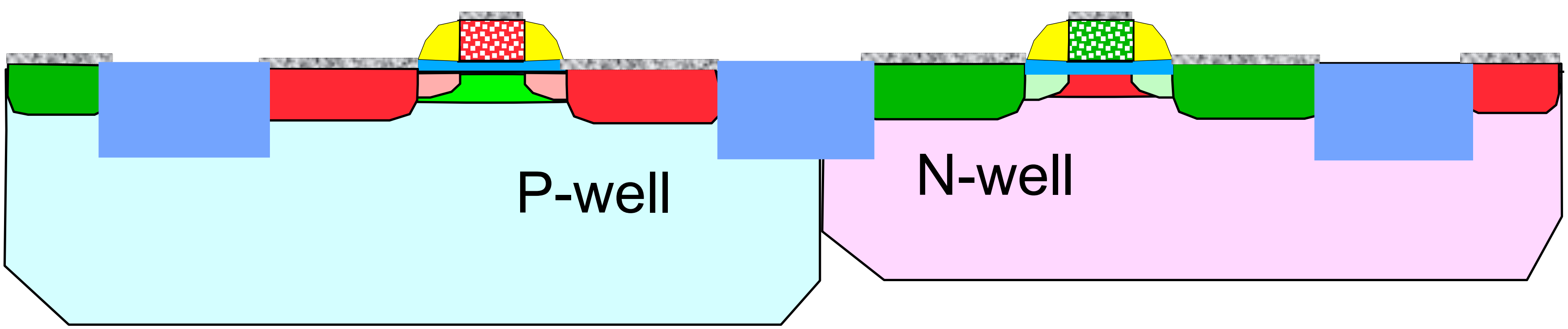


RTP TO FORM SILICIDE



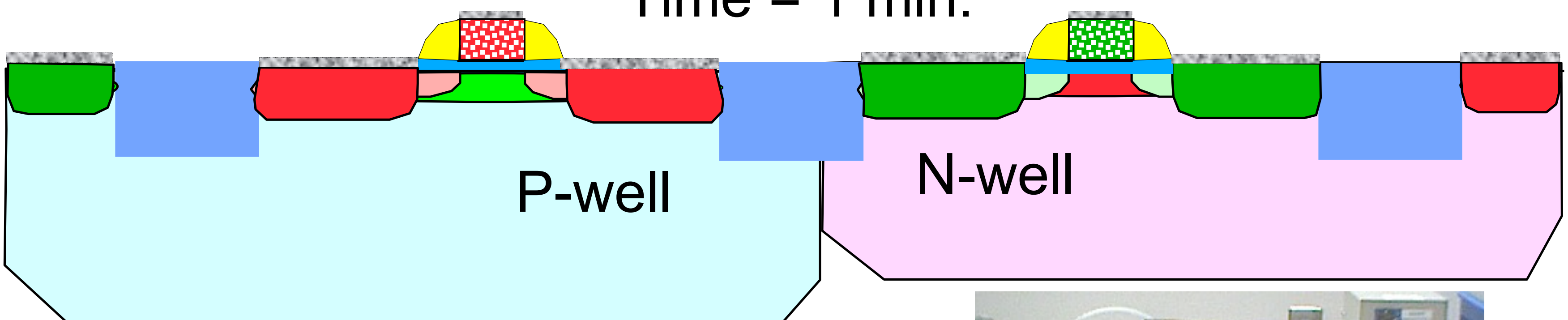
Rochester Institute of Technology
Microelectronic Engineering

ETCH REMOVE Ti



RTP TO FORM SILICIDE (TiSi2)

AG Associates 610
N2
Recipe TiSi2.RCP
Temp = ~800 C
Time = 1 min.



Industry moving to $CoSi_2$ and now $NiSi_2$ for lower sheet resistance and because is consumes less Si.

RCA CLEAN AND DEPOSIT LPCVD OXIDE

Target 4000 Å

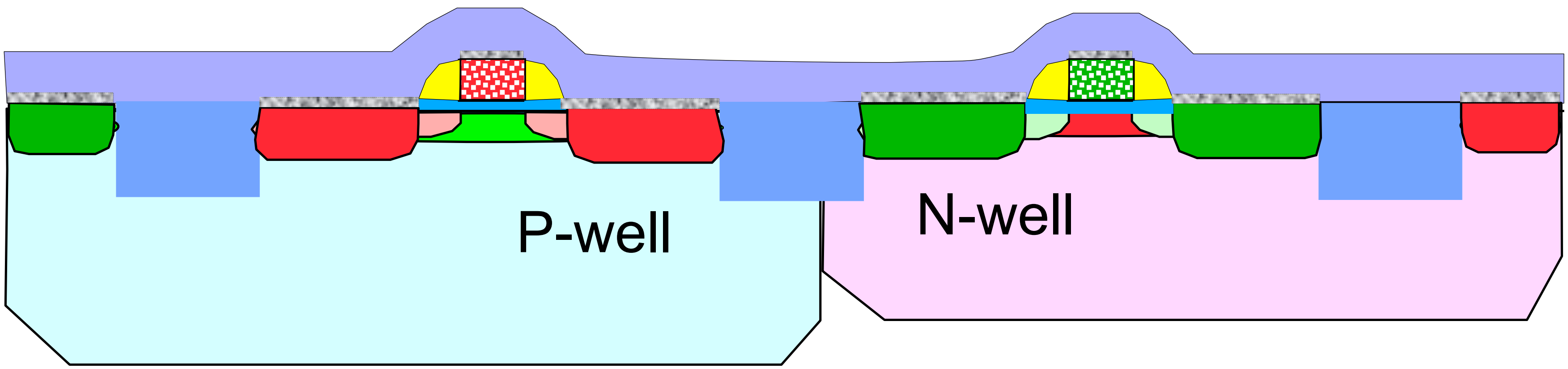
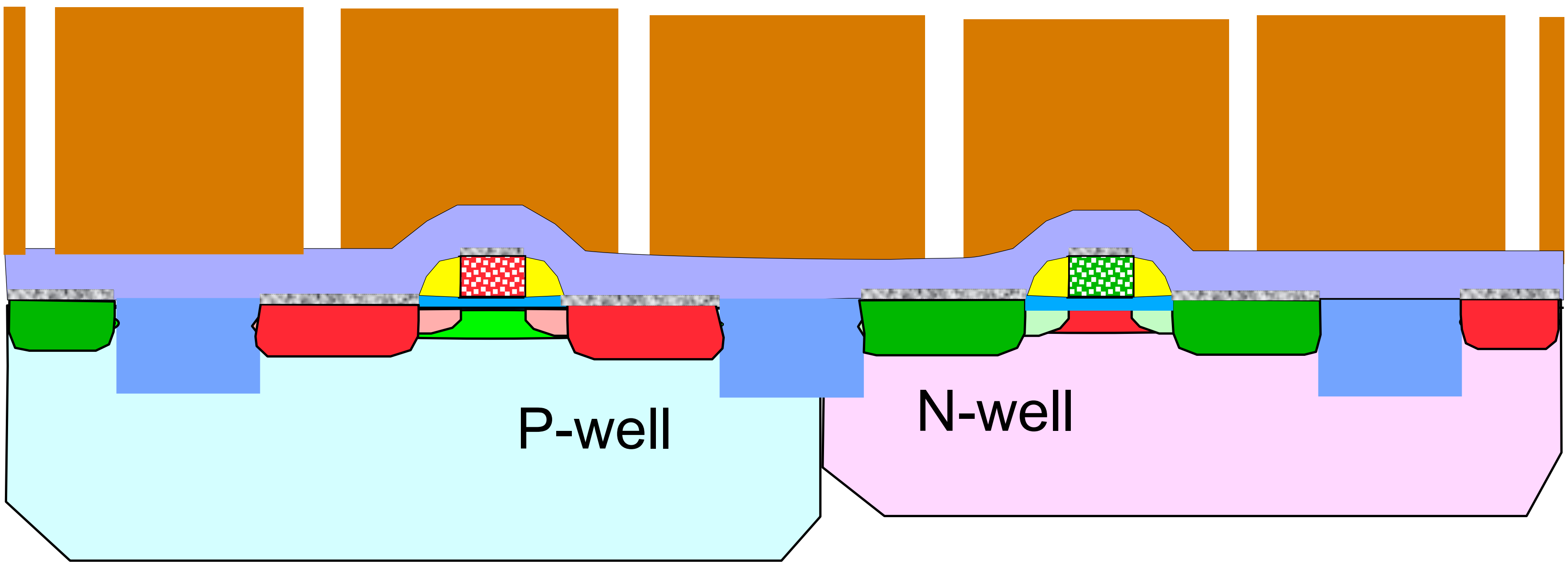
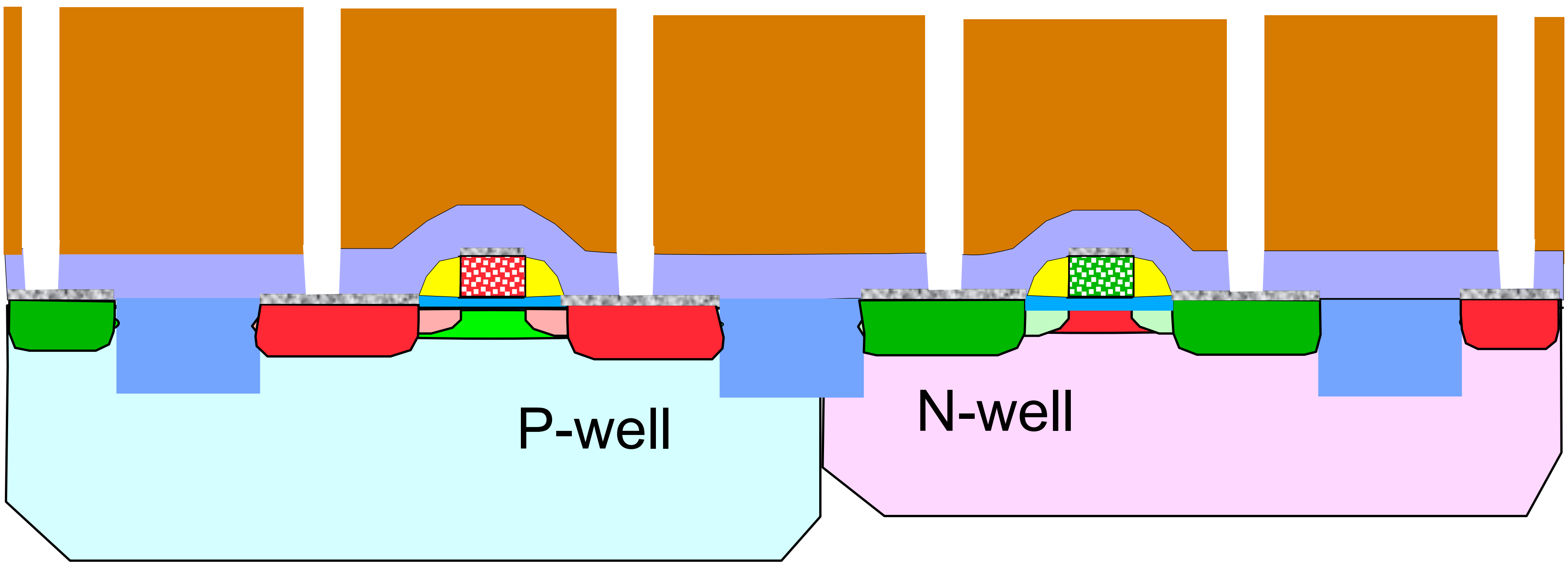


PHOTO 11 CONTACT CUTS

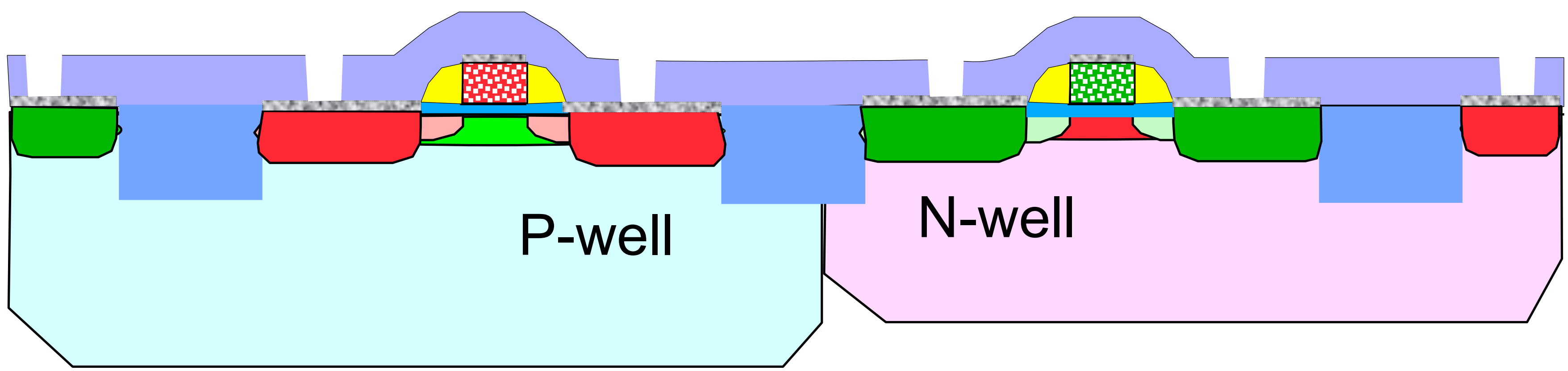


ETCH CONTACT CUTS



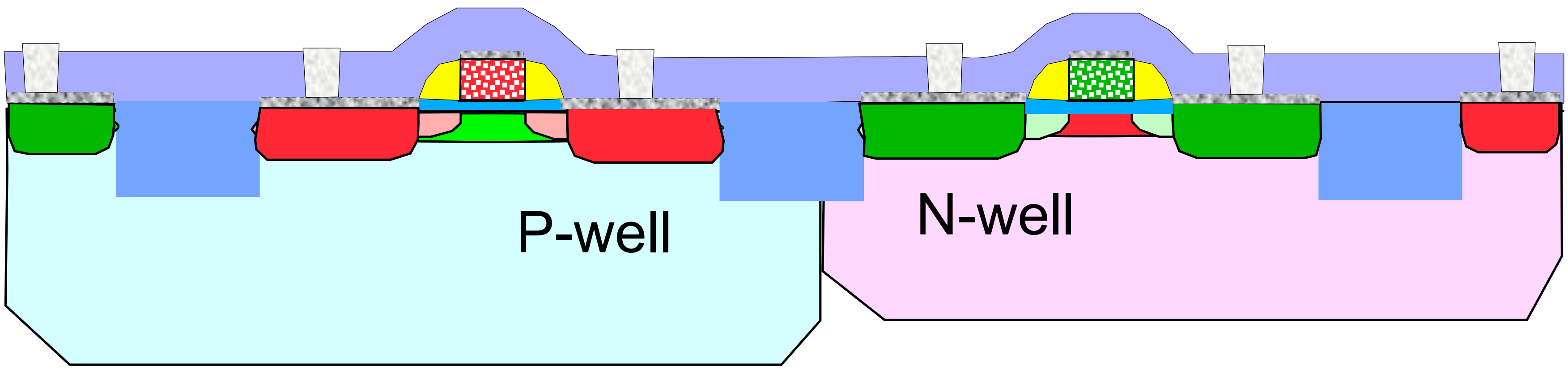
Wet Etch in BHF, 5 min, SRD

STRIP RESIST



Include D1-D3
Strip Photresist in Branson Asher

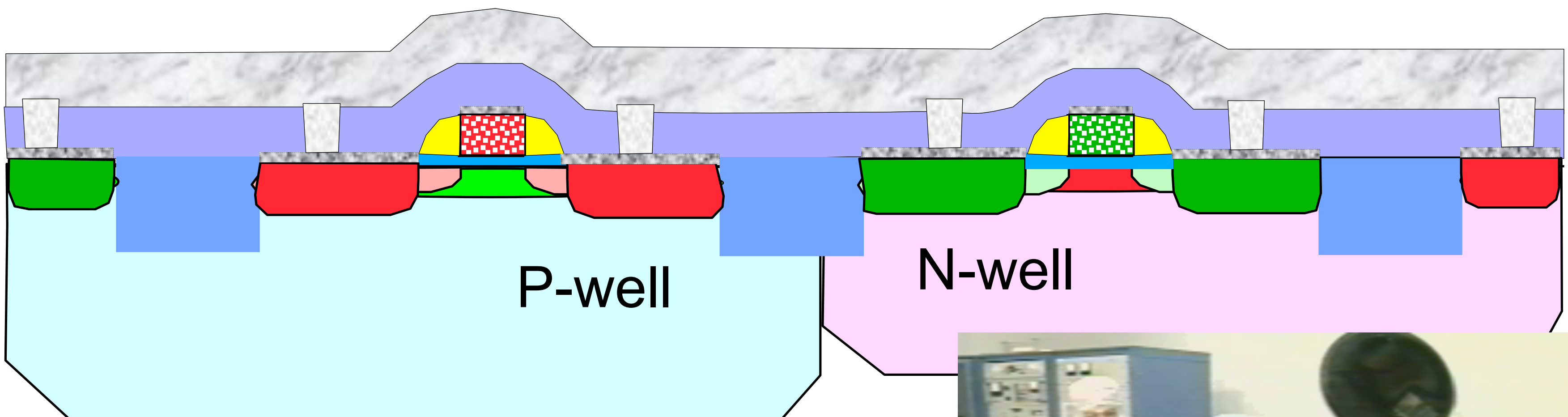
LPCVD TUNGSTEN PLUGS



DEPOSIT ALUMINUM

industry uses Cu instead of Al now.

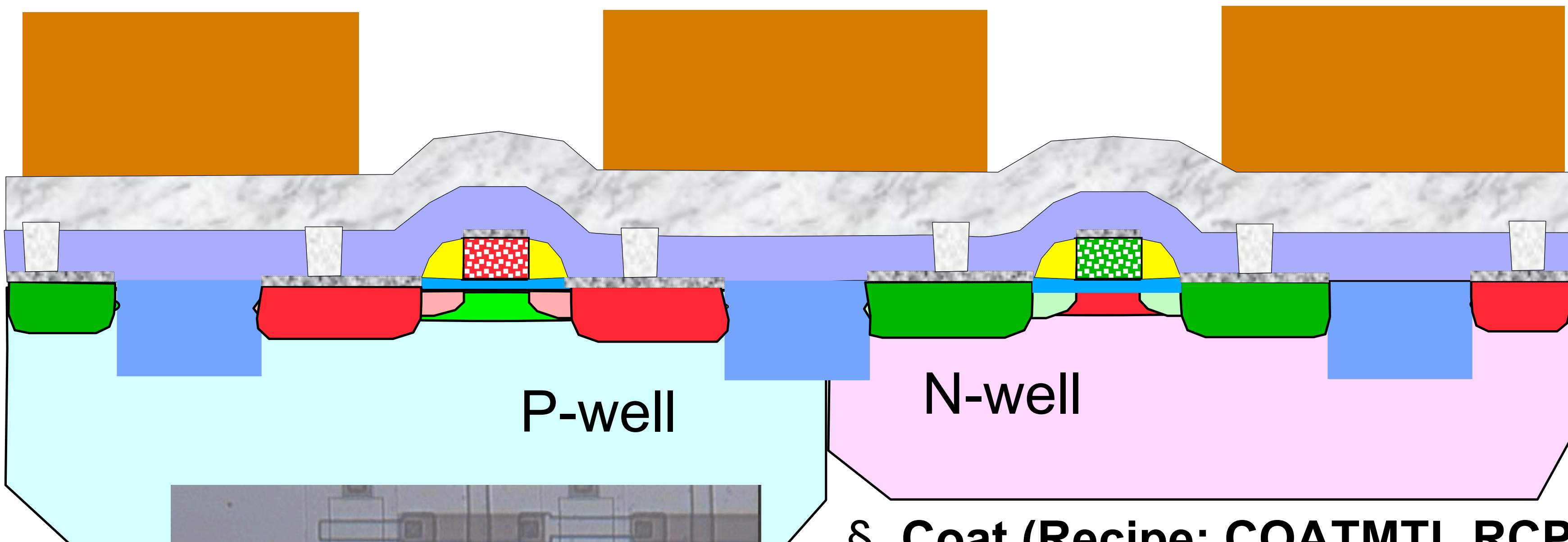
0.75 µm Aluminum

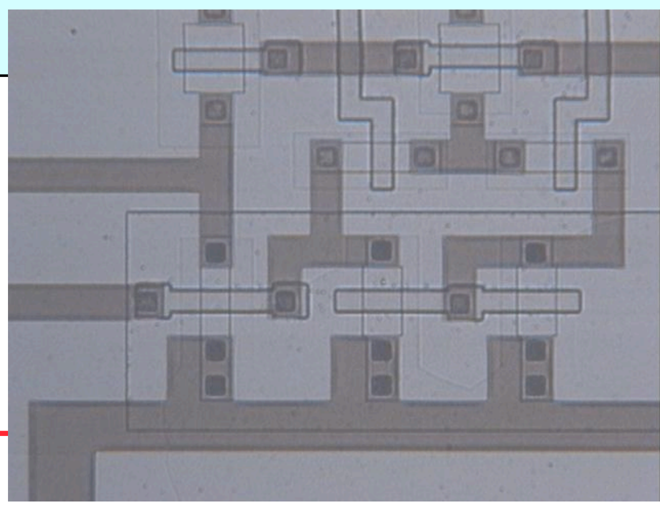


CVC 601 Sputter Tool

Rochester Institute of Technology
Microelectronic Engineering

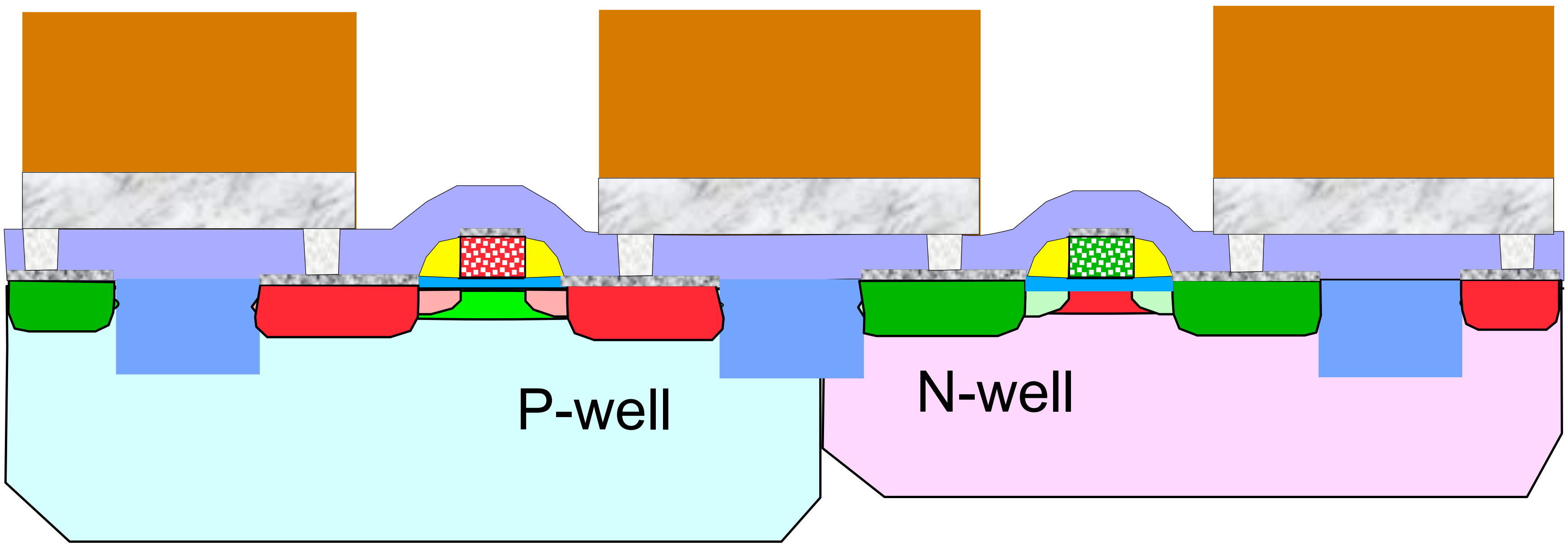
PHOTO 12 METAL ONE



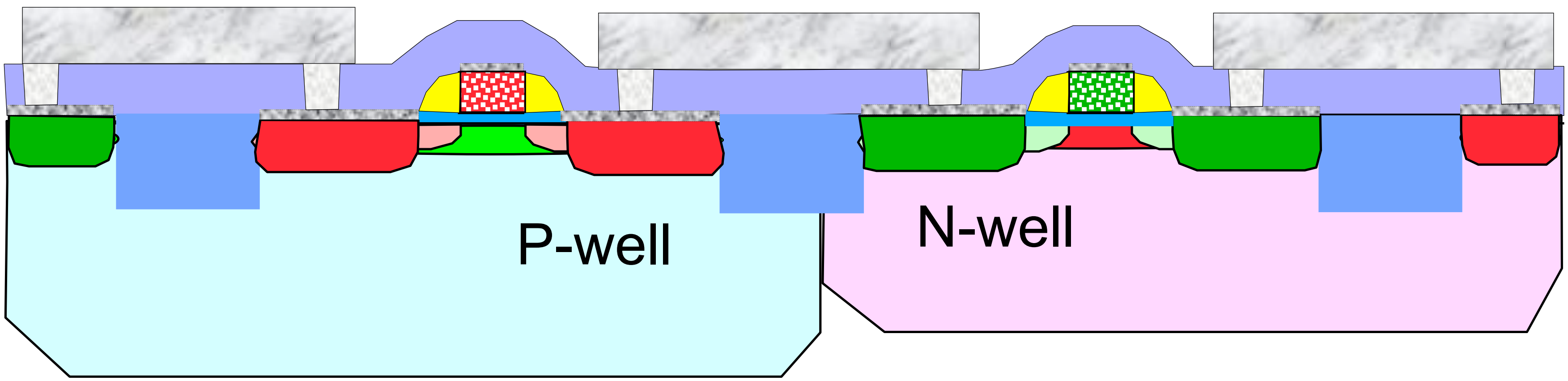


- **Coat (Recipe: COATMTL.RCP)**
  - 400RPM for 2 seconds
  - 2000RPM for 30 seconds
  - Thickness of 13127A
- **Exposure**
  - Energy: 140mJ/cm2
  - Focus: 0.24um
- **Develop (Recipe: DEVMTL.RCP)**
  - Dispense 7 seconds
  - Wait 68 seconds
  - Hard Bake 2 min.

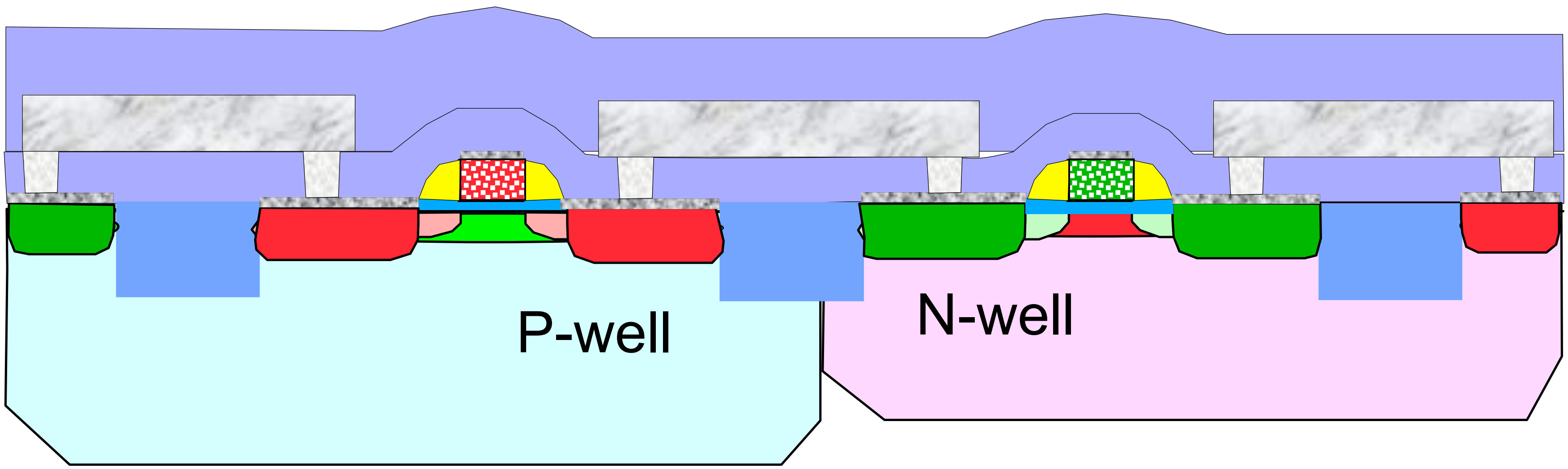
ALUMINUM ETCH



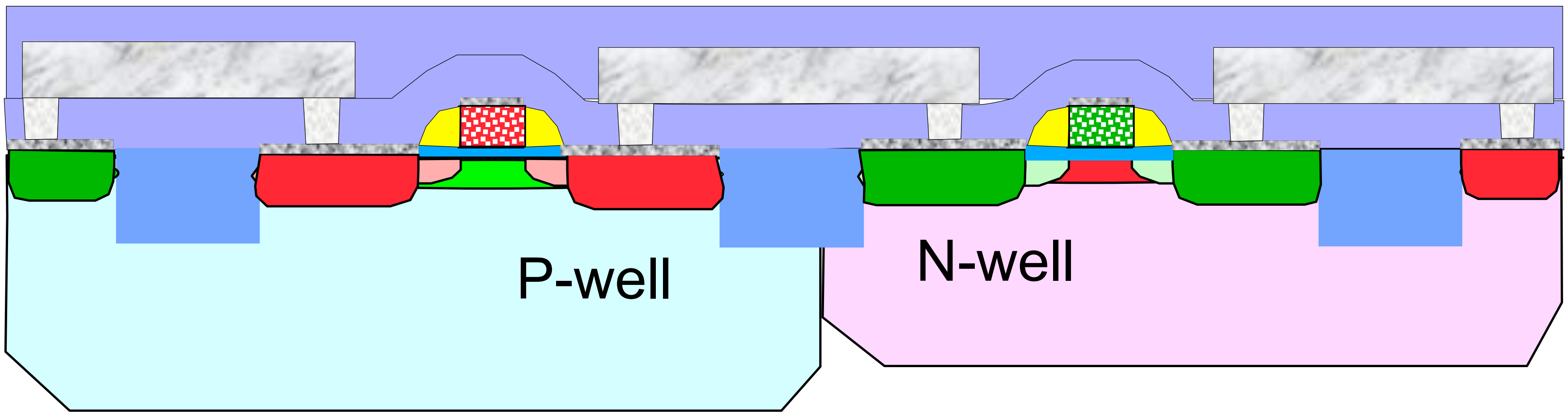
RESIST STRIP



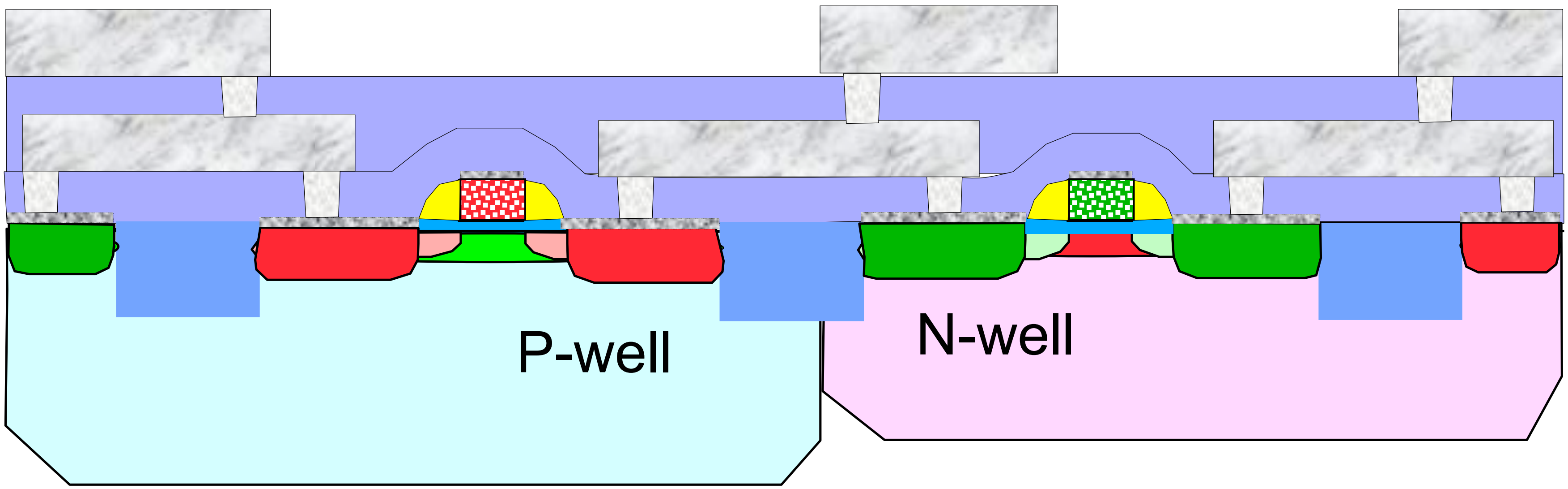
LTO



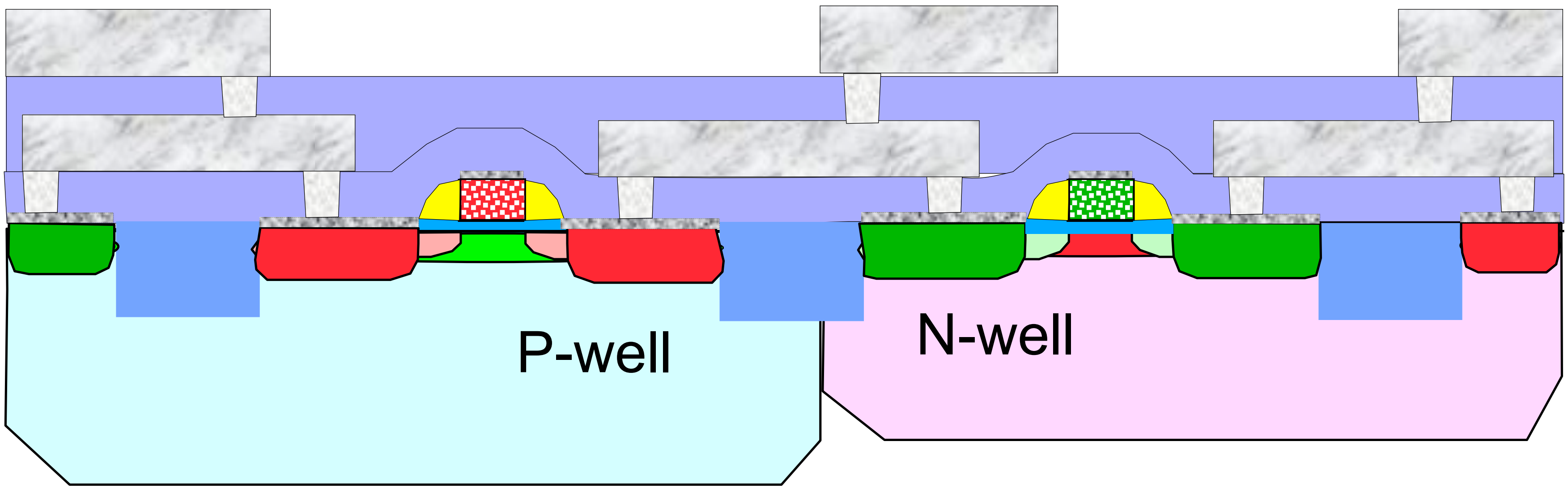
CMP



VIA, TUNGSTEN PLUGS, ALUMINUM, AL ETCH



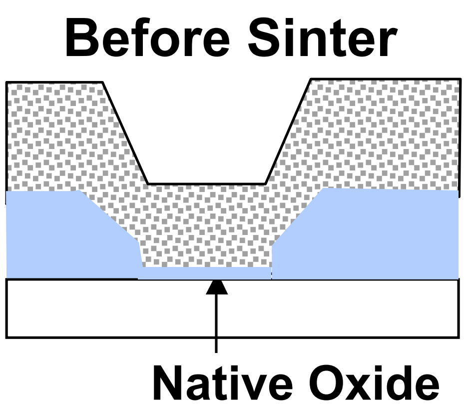
SINTER



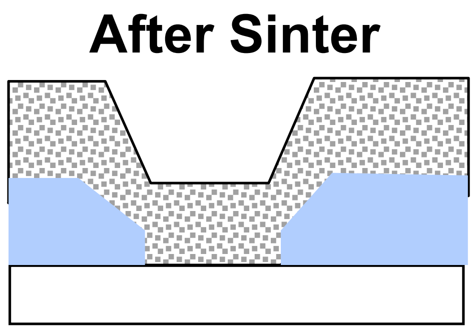
Bruce Furnace 02

Recipe 101: 450C, H_2N_2, 30min

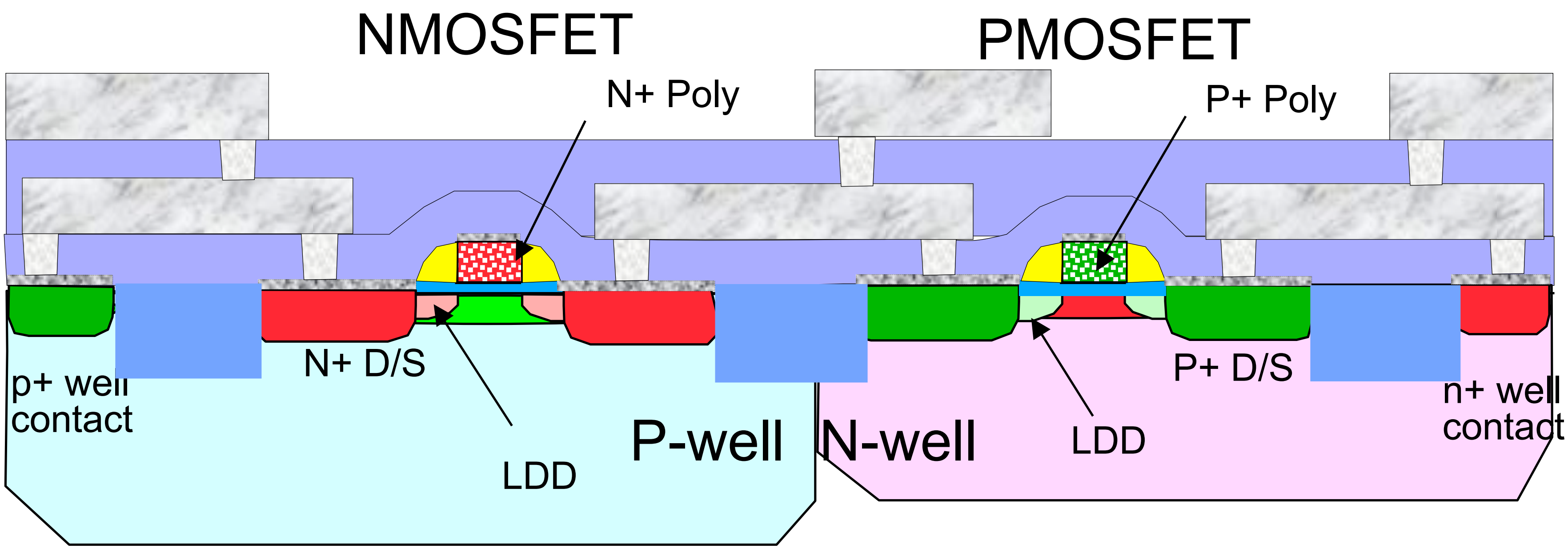
SINTER



Reduce Contact Resistance



ADV-CMOS 150


NMOSFET
PMOSFET
N+ Poly
P+ Poly
N+ D/S
P+ D/S
LDD
LDD
p+ well
contact
n+ well
contact
P-well
N-well

REFERENCES

1. Silicon Processing for the VLSI Era, Volume 1 – Process Technology, 2nd, S. Wolf and R.N. Tauber, Lattice Press.

2. The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.

HOMEWORK – RIT ADVCMOS2003

1. Why do we want the surface concentration under the shallow trench in the p-well to be above some given value?
2. Why are the well implant energies greater than 150 KeV?
3. When checking material thickness for the ability to block D/S implant, which implant type and which material is the most critical.
4. Why is a nitride spacer (instead of oxide) used.
5. What are the two main purposes of the silicide in this process?
6. Why is the gate doped N-type on the NMOS and P-type on the PMOS devices?
7. What is the poly sheet resistance?
8. What is the purpose of the N2O in the gate oxide growth recipe?

SUMMARY

Thanks again to Dr. Lynn Fuller for providing this material. Please visit the RI website for more information.

http://www.rit.edu/~lffeee/

Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041

email: LFFEEE@rit.edu

microE webpage: http://www.microe.rit.edu