Status Report
August 2010

Nanoelectronics • Architectures
MIND
MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

3-D Quantum Transport Modeling

NEMO 1-D + NEMO 3-D => OMEN

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NIST

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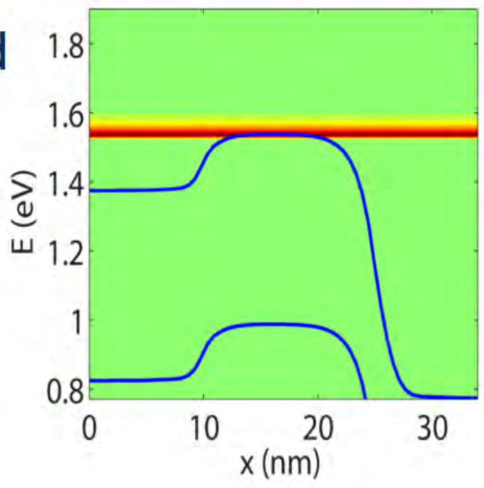
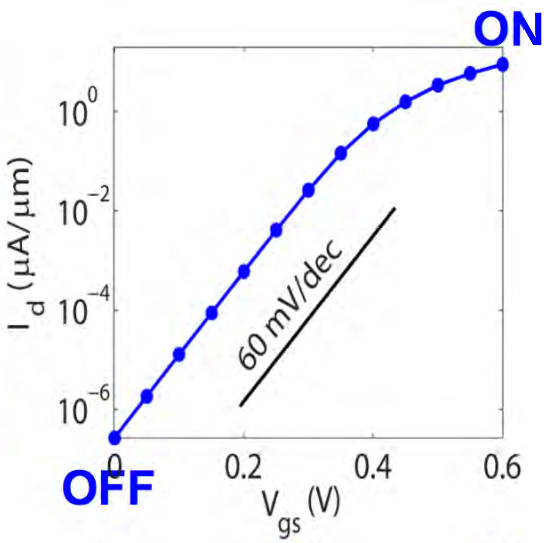
NSF Peta-Apps Award
NCN seed effort

MOSFET vs TFET: Injection Mechanism

Problem with V_{DD} Scaling:

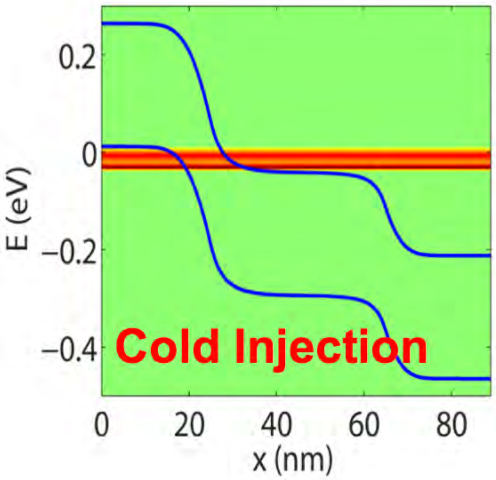
- Subthreshold Swing (SS) limited to 60 mV/dec
- Large I_{ON}/I_{OFF} ratio => large V_{DD}
- High Power Consumption
- V_{DD} scaling not possible:
  - either increase of I_{OFF}
  - or decreases of I_{ON}

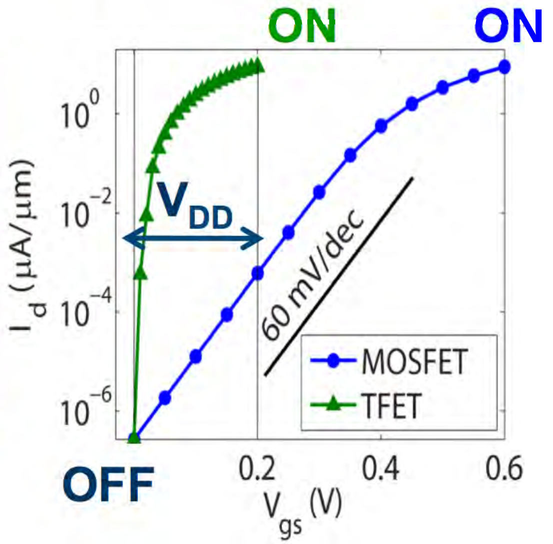




Solution: BTB Tunneling

- No lower limit on the SS
- Low Power Consumption
- Various designs and materials
- **Biggest Challenges:**
  - **High I_{ON}**
  - **Steep SS**
  - **Low I_{OFF}**





TFET: Open Questions

Assumptions:

- Any semiconductor material (Si, Ge, C, InAs, InSb, InAs/GaSb) equally viable
- Aim for 8-10nm technology
- Aim for CMOS augmentation
- Aim for low power

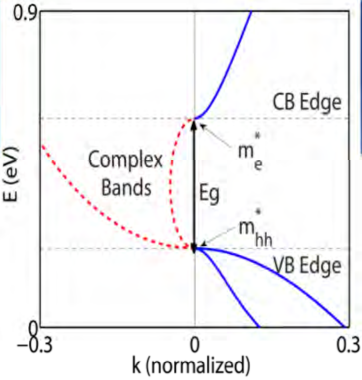
Open Questions

- Which geometry: SG, DG, GAA?
- Doping profiles?
- Lateral or Vertical Tunneling?
- Phonons – energy loss

Biggest Challenges:

➢**High I_{ON}**
➢**Steep SS**
➢**Low I_{OFF}**

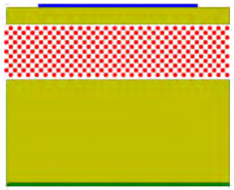
InSb
E_g=0.169eV
(Bulk)



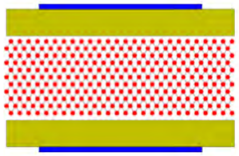
Graphene (C)
Tunable BG
Symmetric BS

Broken Gap
Heterostructure
150 meV

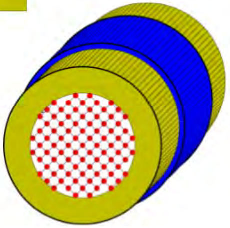
Single-Gate

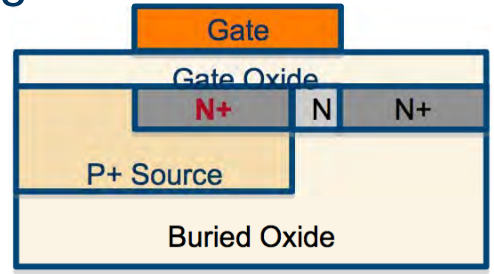


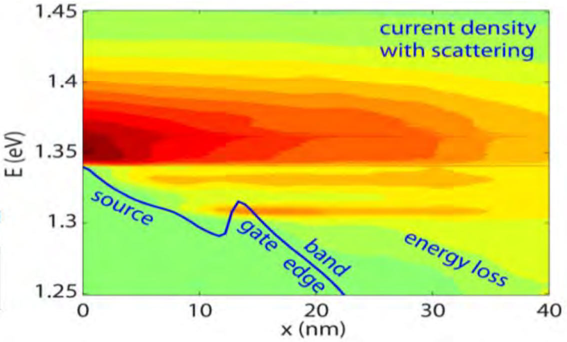
Double-Gate



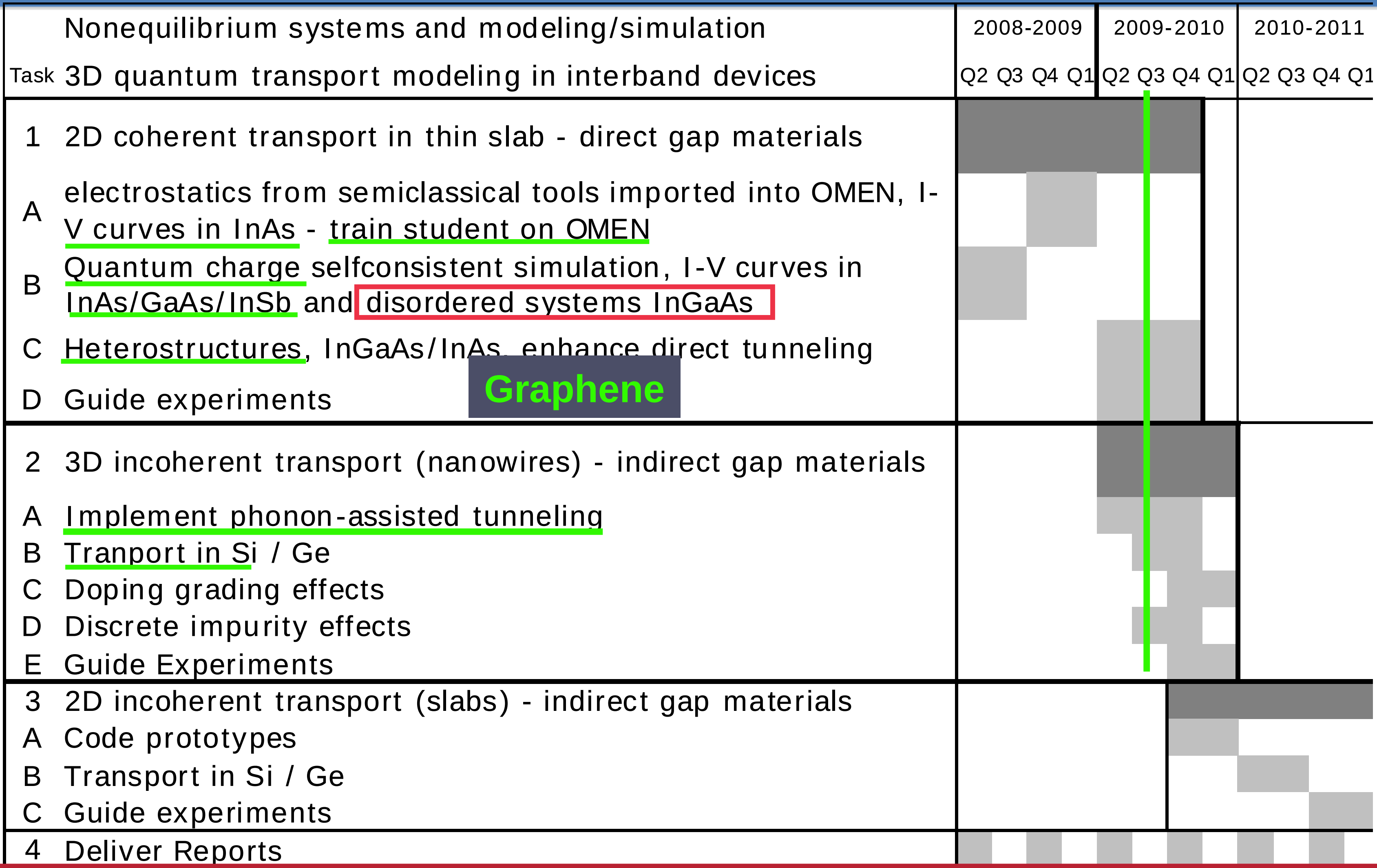
Gate-All-Around







Last Year’s Status



	Nonequilibrium systems and modeling/simulation	2008-2009				2009-2010				2010-2011			
Task	3D quantum transport modeling in interband devices	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1
1	2D coherent transport in thin slab - direct gap materials	■	■	■	■	■	■	■					
A	electrostatics from semiclassical tools imported into OMEN, I-V curves in InAs - train student on OMEN			▨	▨								
B	Quantum charge selfconsistent simulation, I-V curves in InAs/GaAs/InSb and disordered systems InGaAs	▨	▨										
C	Heterostructures, InGaAs/InAs, enhance direct tunneling					▨	▨	▨					
D	Guide experiments					▨	▨	▨					
2	3D incoherent transport (nanowires) - indirect gap materials					■	■	■	■				
A	Implement phonon-assisted tunneling					▨	▨	▨					
B	Tranport in Si / Ge						▨	▨					
C	Doping grading effects							▨	▨				
D	Discrete impurity effects						▨	▨					
E	Guide Experiments							▨	▨				
3	2D incoherent transport (slabs) - indirect gap materials							■	■	■	■	■	■
A	Code prototypes							▨	▨				
B	Transport in Si / Ge									▨	▨		
C	Guide experiments											▨	▨
4	Deliver Reports	▨		▨		▨		▨		▨		▨	

Graphene

Feedback from panel: Proceed to develop OMEN and connect further to experiments

This Year's Status

	Nonequilibrium systems and modeling/simulation	2008-2009				2009-2010				2010-2011			
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A	electrostatics from semiclassical tools imported into OMEN, I-V curves in InAs - train student on OMEN			░	░								
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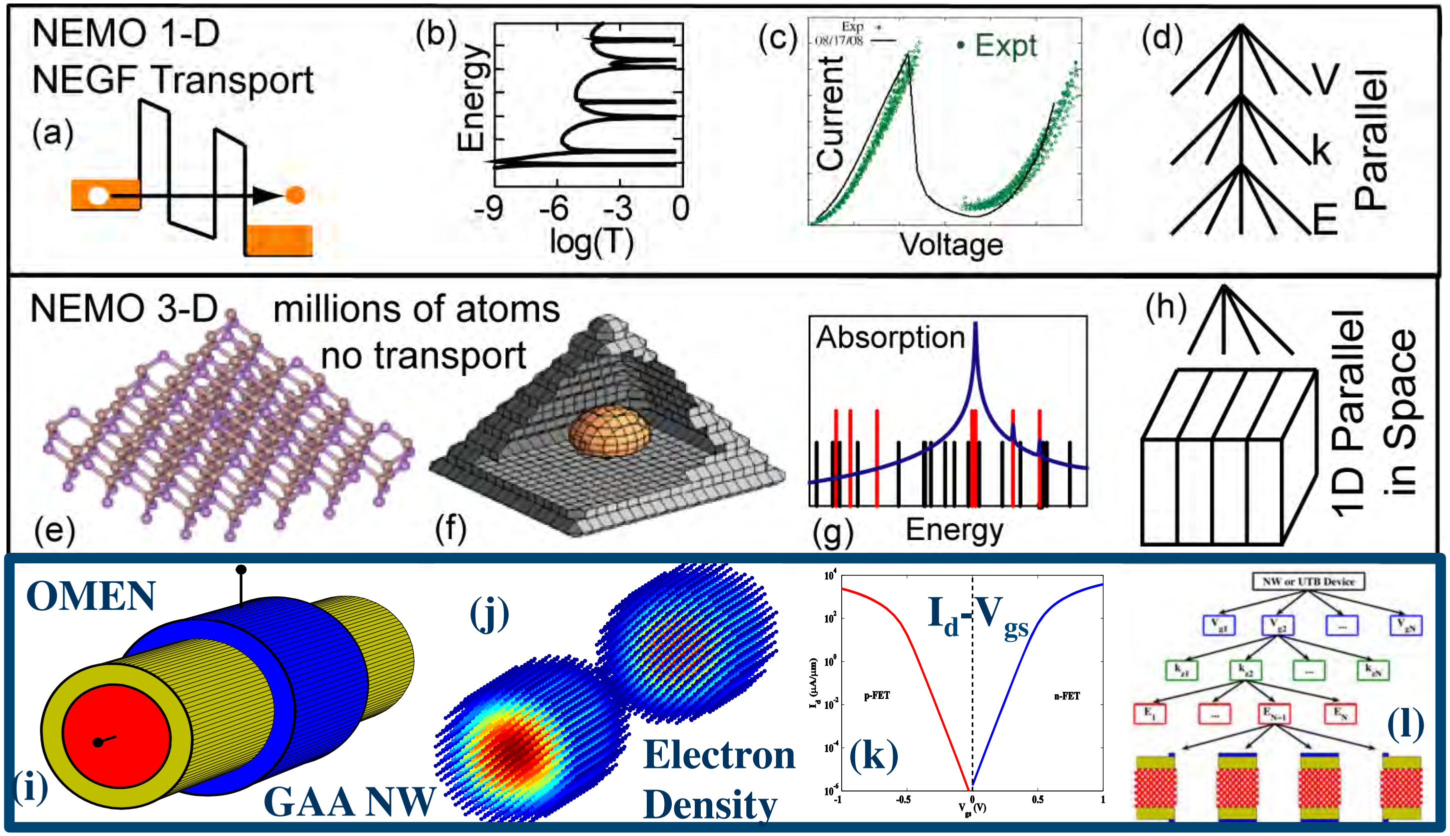
C	Guide experiments											░	░
4	Deliver Reports	░		░		░		░		░		░	

Graphene

Broken Gap Structures

**Comparison,
InAs, Graphene, InSb, GaSb/InAs**

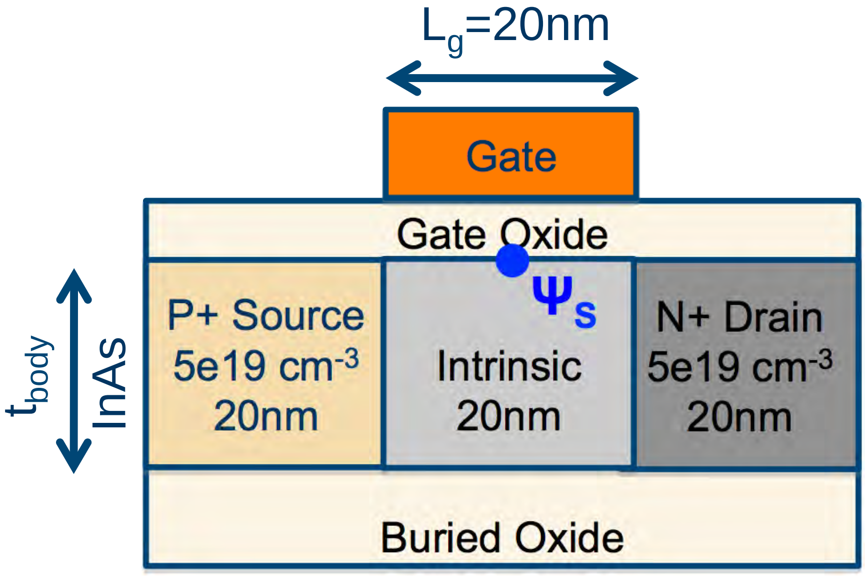
From NEMO 1-D to OMEN

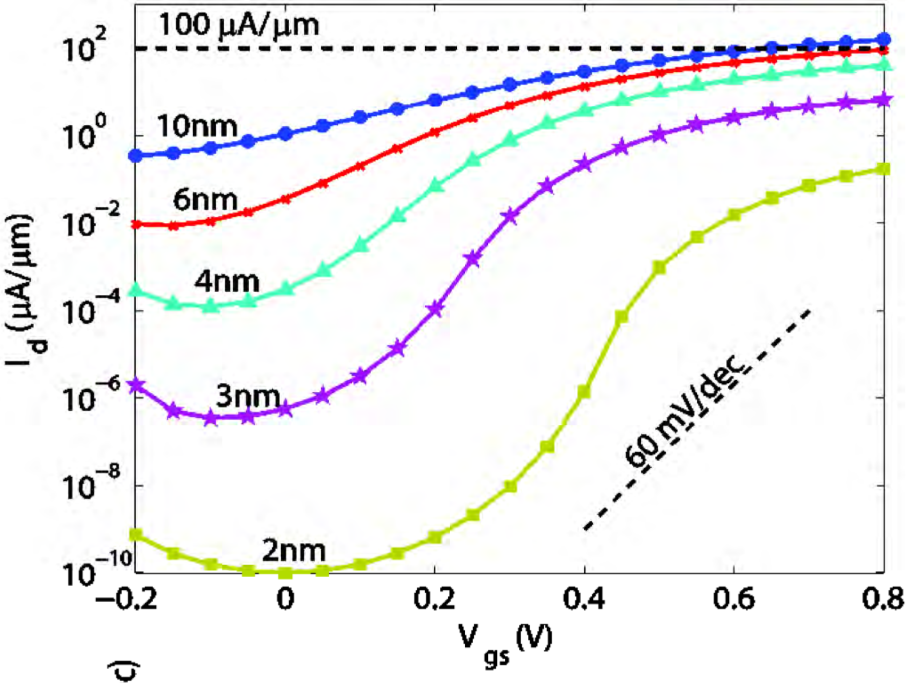


Features:

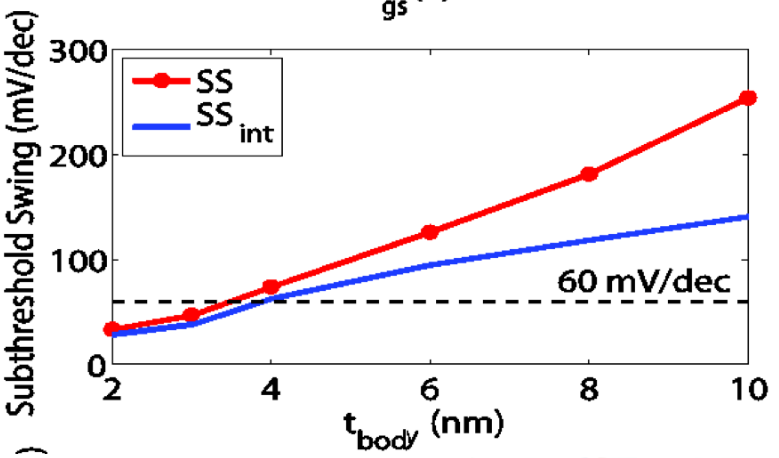
- **3D, Atomistic, and Full-Band Quantum Transport Simulator**
- **4 Levels of Parallelism (V, k, E, and DD)**

Lateral TFETs: Influence of Body Thickness





$$SS = \partial V_{gs}/\partial \log_{10} I_d = \partial V_{gs}/\partial \Psi_S \cdot SS_{int}$$

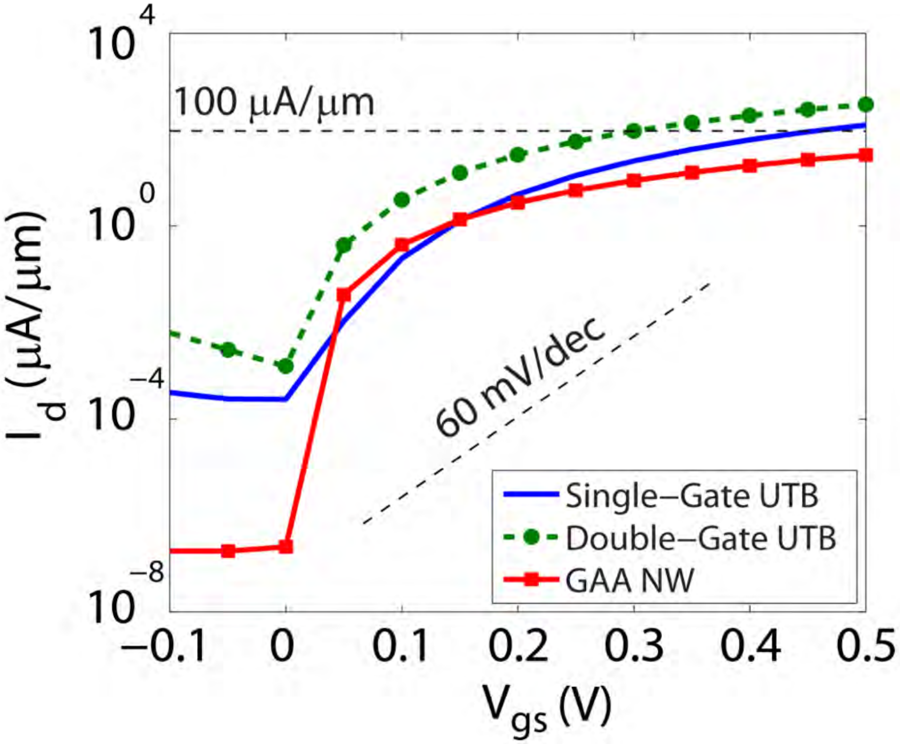


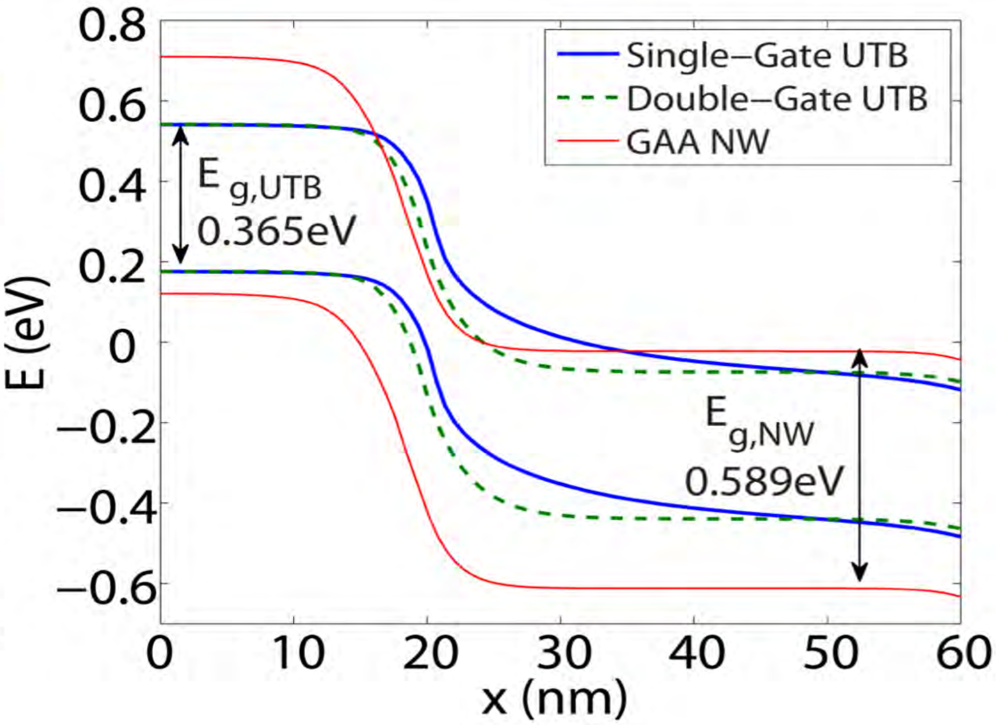
Body Thickness Variation (L_g=20nm)

- Poor electrostatic for t_{body}>4nm
- SS below 60 mV/dec for t_{body}<4nm
- Low ON-Current despite highly and abruptly doped source

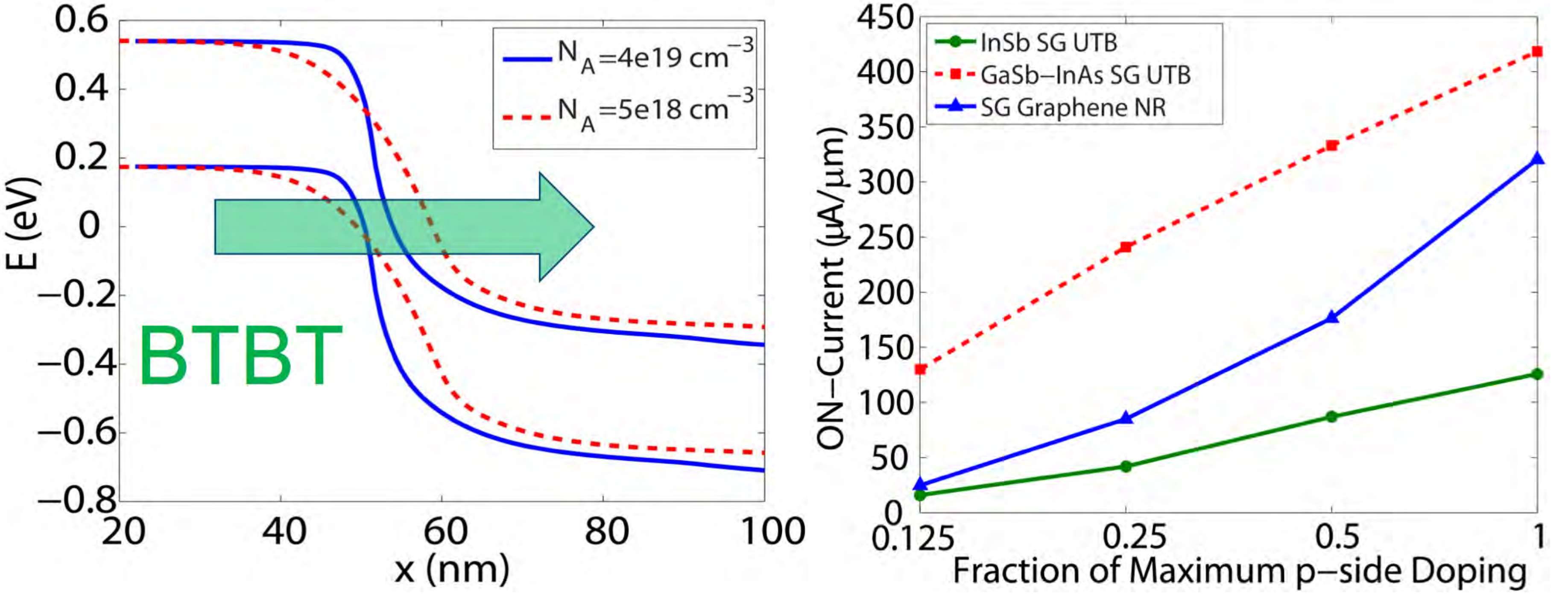
TFETs: InSb Devices

- Maximum Current of **330 μA/μm** for DG UTB @ **V_{DD}=0.5 V**
- **SS below 60 mV/dec**: GAA (9.2) < DG (20) < SG (34)
- Band Gap increase due to quantization





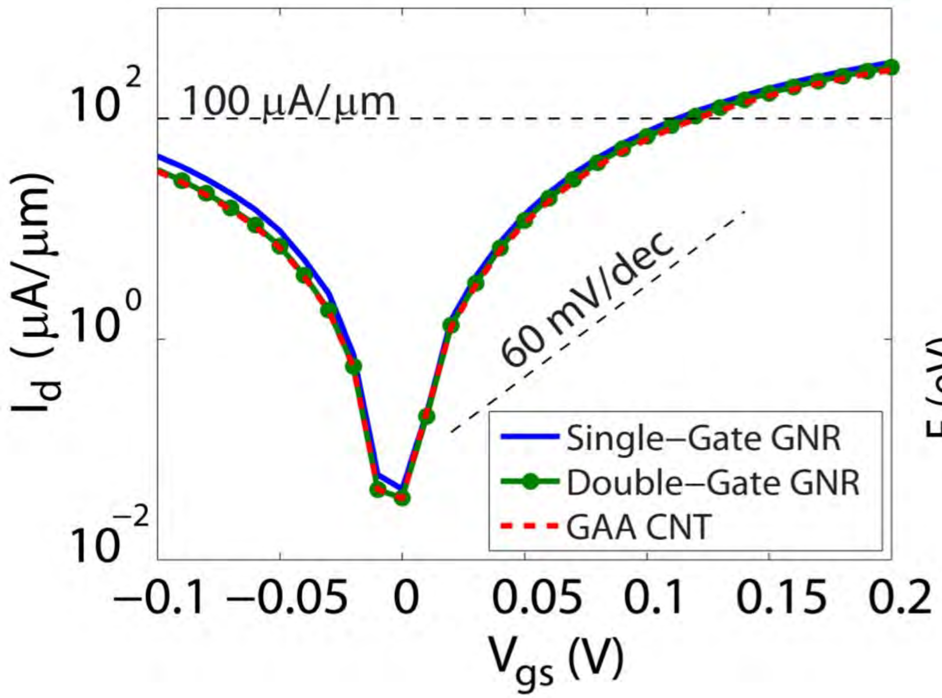
Lateral TFETs: Influence of Source Doping

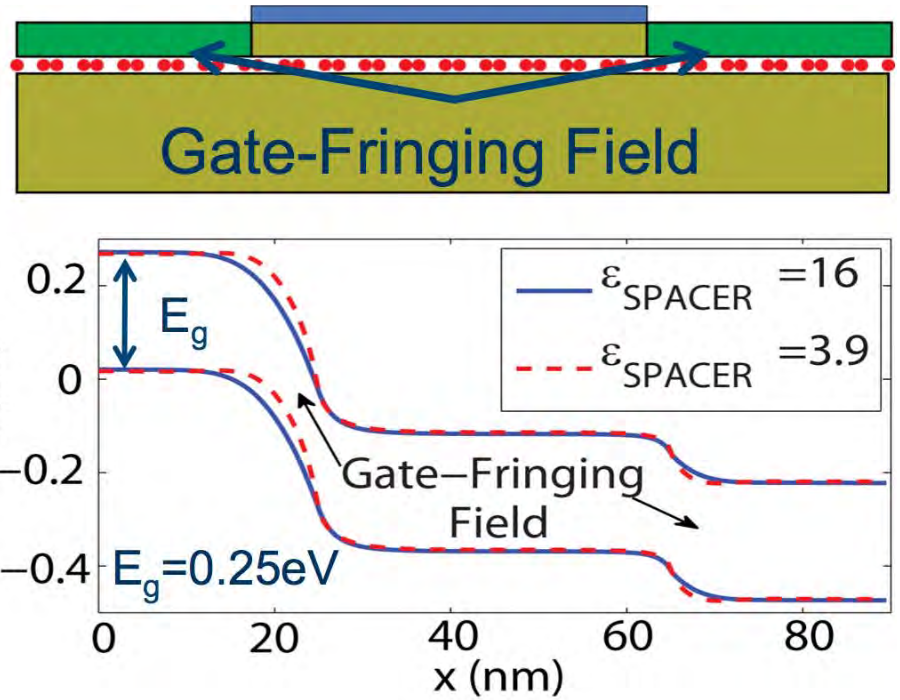


- **Assumption: abrupt doping at s-c interface**
- **Assumption: high source doping concentration**
- **Both conditions necessary**

- **High Tunneling Current => Large N_A**
- **Technology Limitation (hard to fabricate abrupt junction with high N_A)**

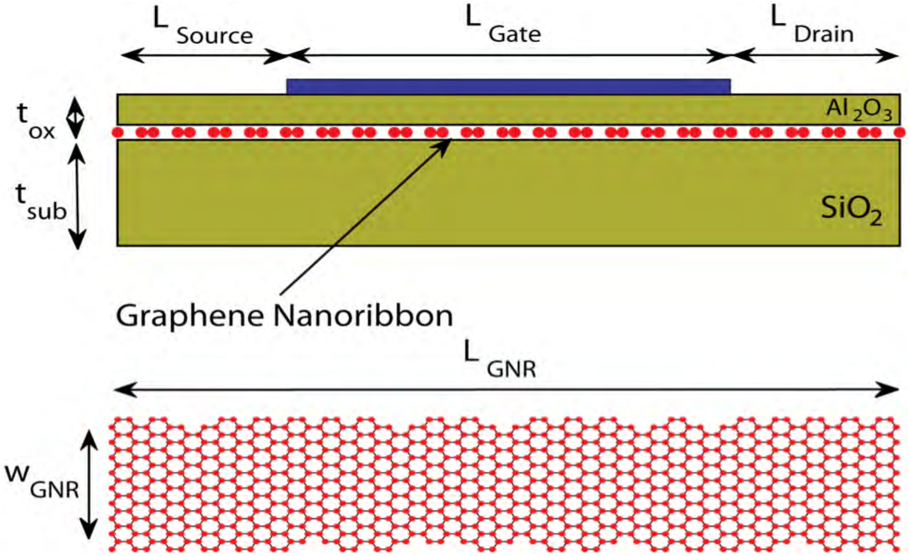
TFETs: Carbon-based Devices

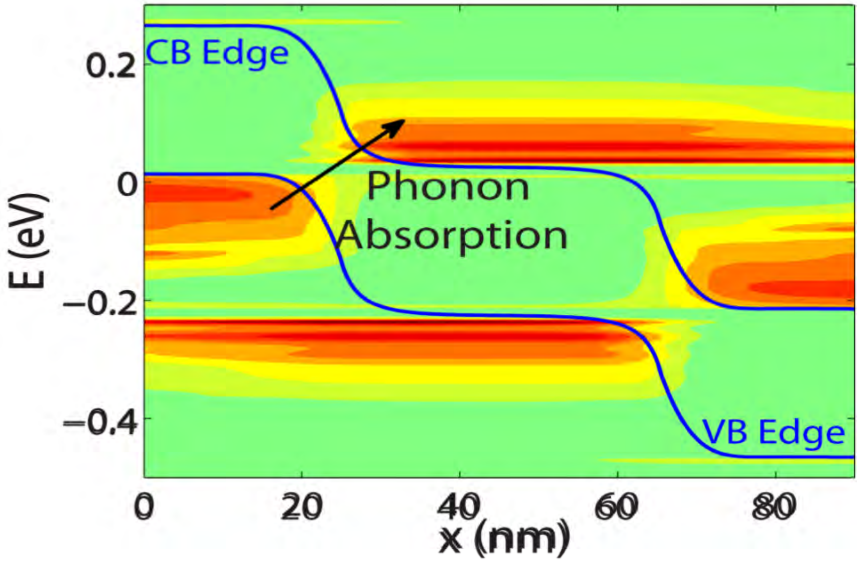


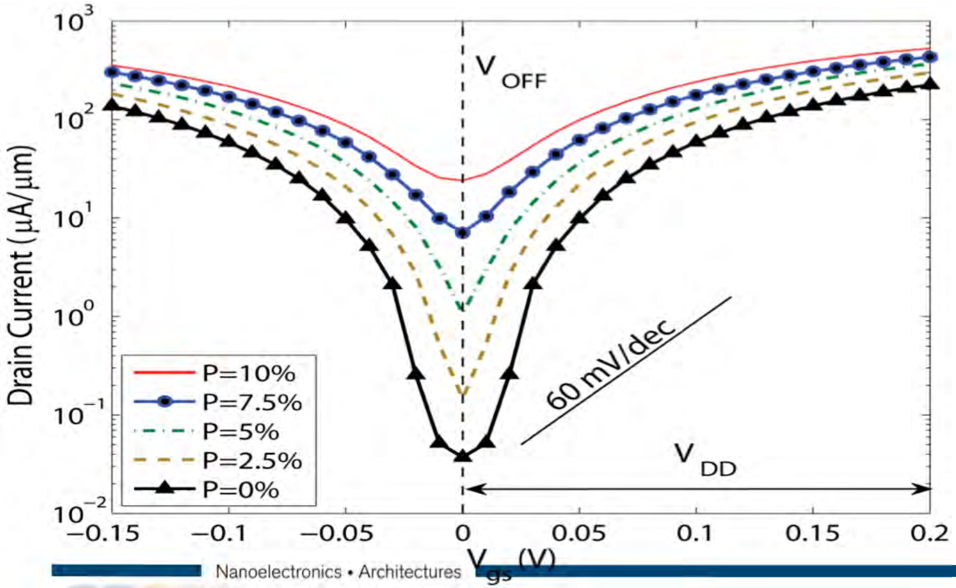


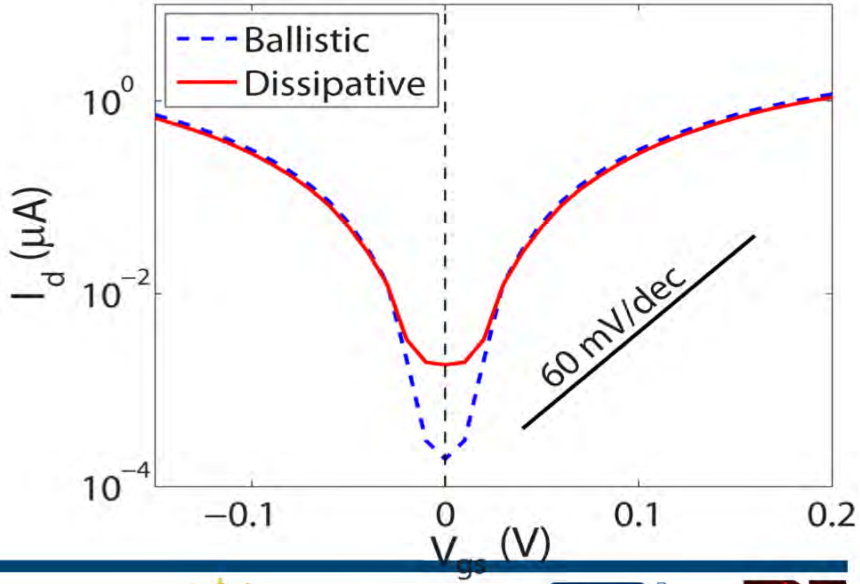
- •Maximum Current of **320 µA/µm** for SG GNR @ **V_{DD}=0.2 V**
- •Excellent electrostatic control in all cases => steep SS
- •Strong influence of Gate-Fringing Field

TFETs: Limitations of Graphene Nanoribbons

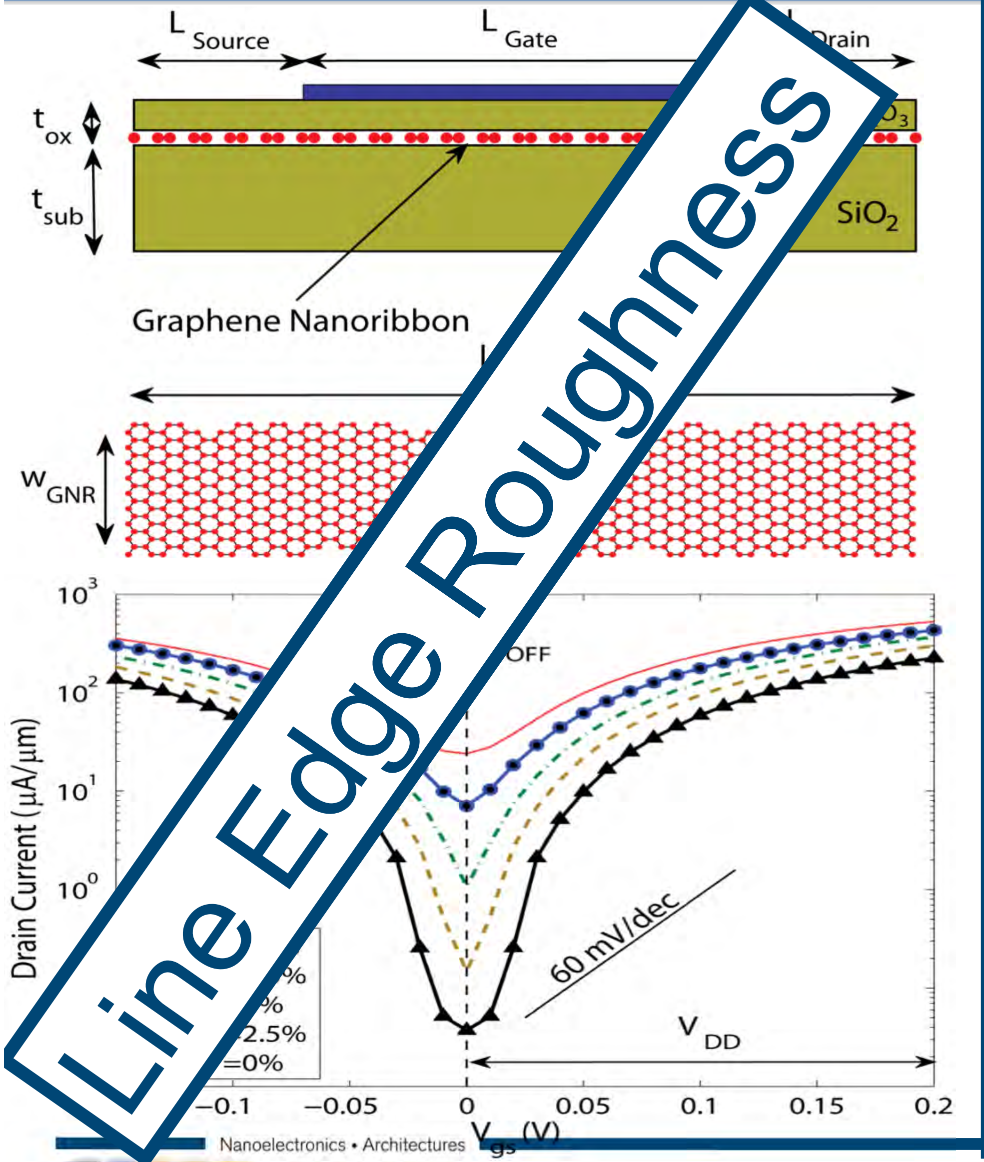




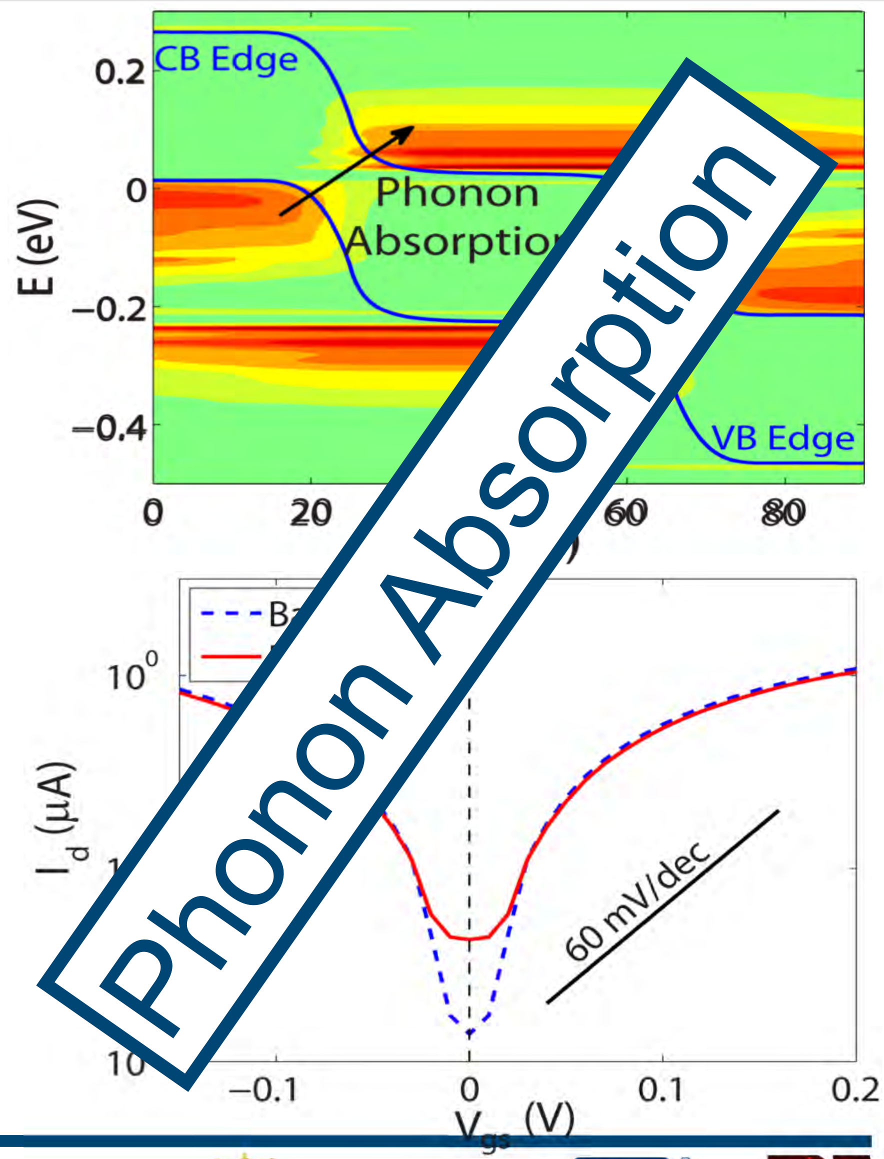




TFETs: Limitations of Graphene Nanoribbons



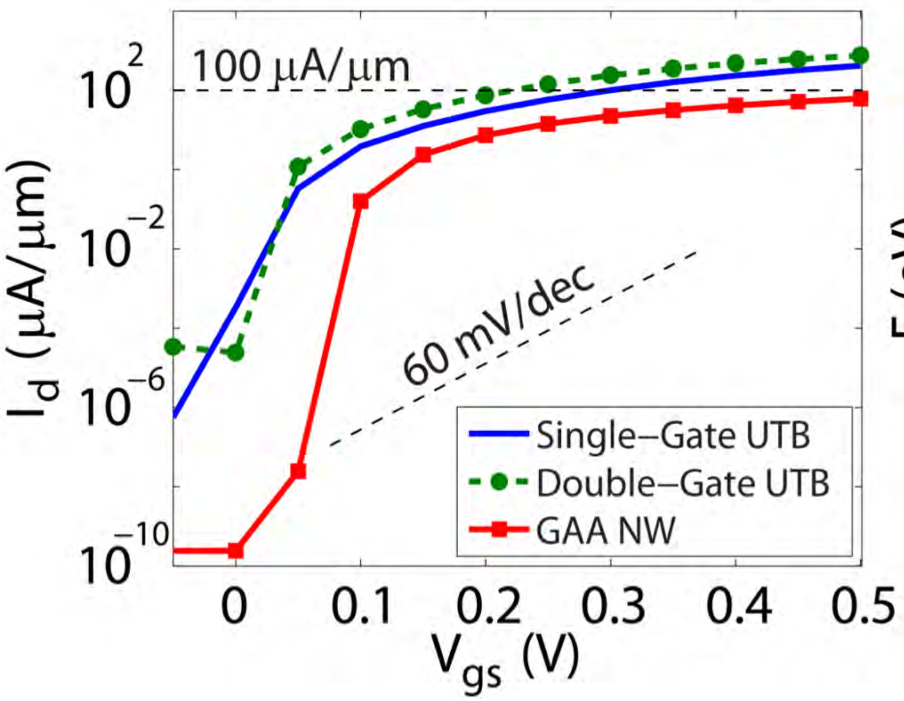
Line Edge Roughness

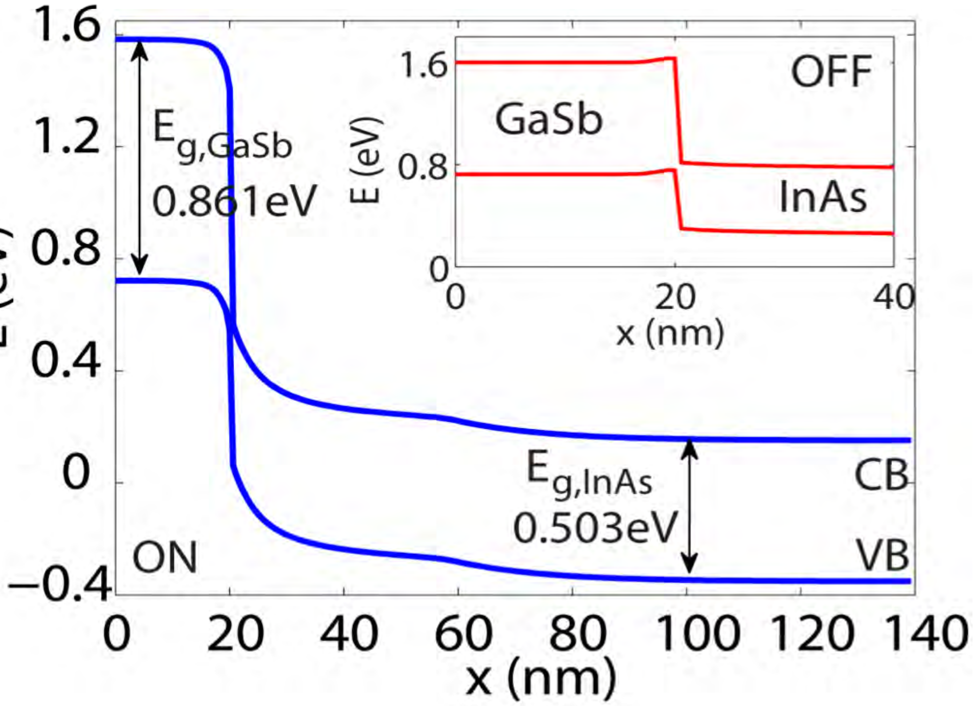


Phonon Absorption

TFETs: Broken-Gap Heterostructure Devices

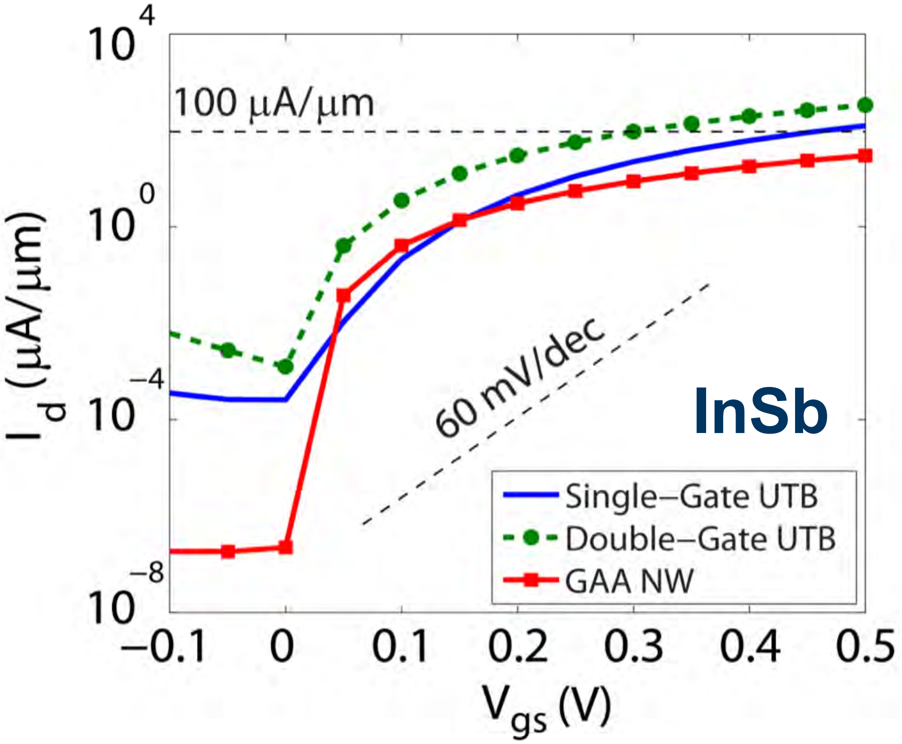
- Maximum Current of **900 µA/µm** for DG UTB @ **V_{DD}=0.5 V**
- **SS below 60 mV/dec**: GAA (7) < DG (11) < SG (17)
- Band Gap increase due to quantization (especially InAs)

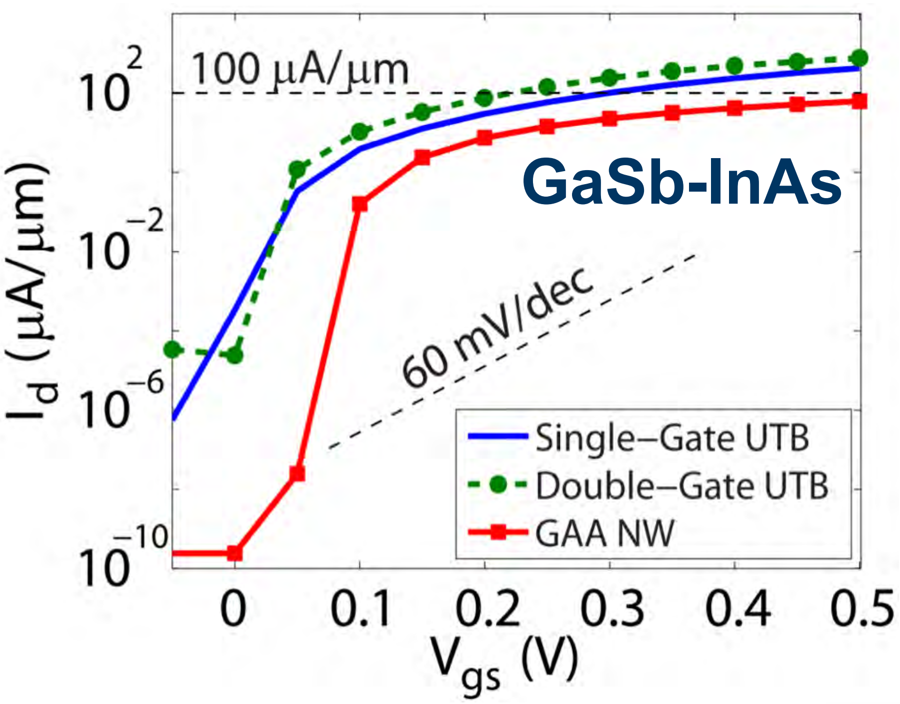




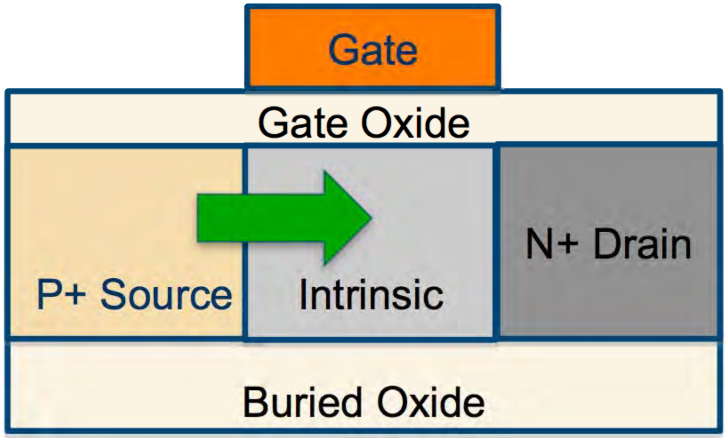
Lateral TFETs: InSb vs GaSb-InAs BG

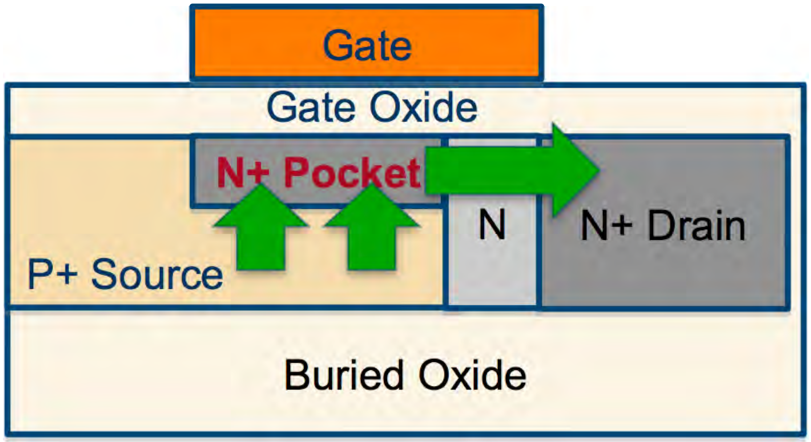
- InSb: maximum current of **330 μA/μm** @ **V_{DD}=0.5 V**
- GaSb-InAs: maximum current of **900 μA/μm** @ **V_{DD}=0.5 V**
- Assumptions: large source doping (**N_A=4e19 cm^{-3}**) and abrupt source-channel interface



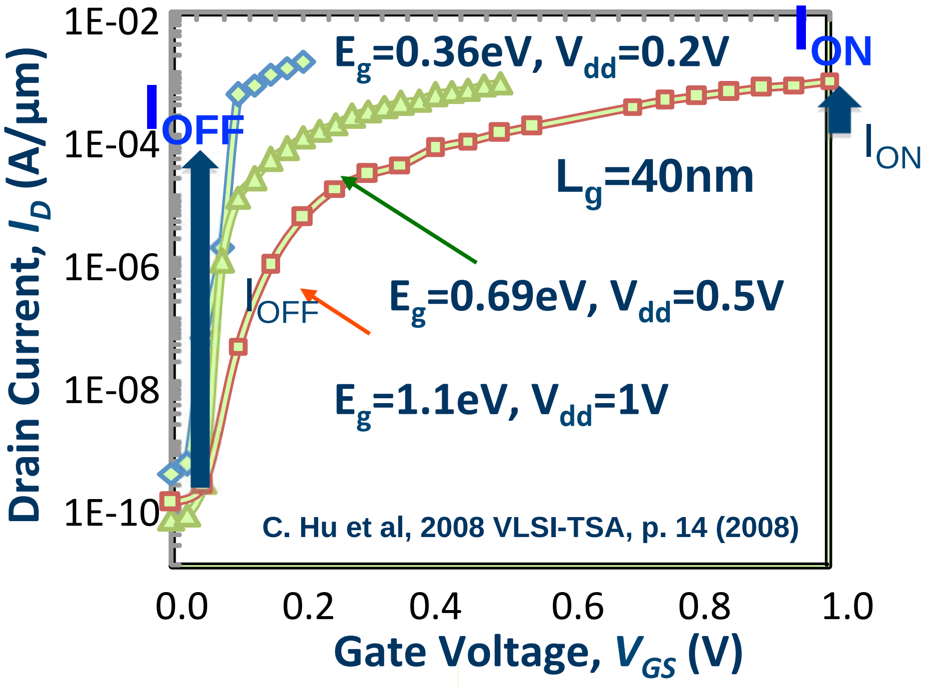


Lateral vs Vertical TFETs: Influence of the Tunneling Area





Source: Chenming Hu, *Green Transistor as a solution to the IC power crisis.*

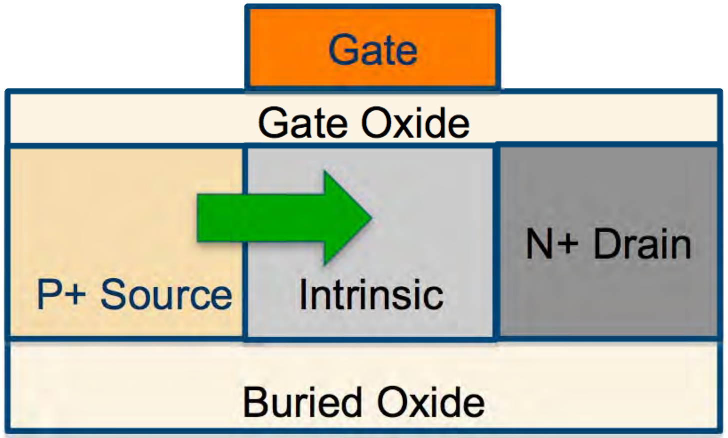


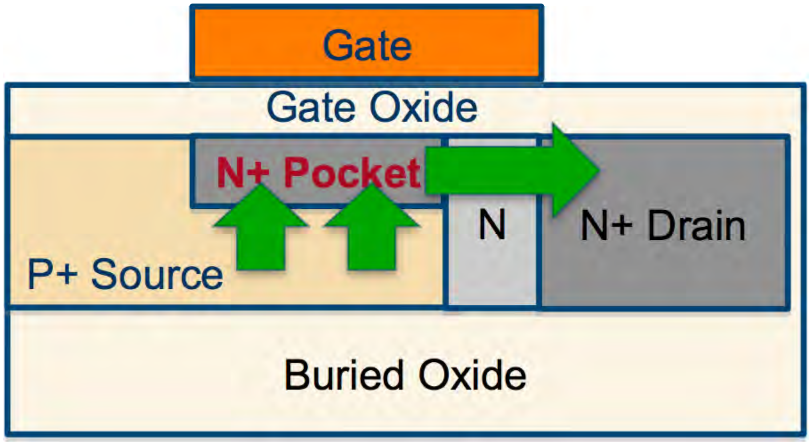
C. Hu et al, 2008 VLSI-TSA, p. 14 (2008)

InAs Vertical TFET Simulation @ UCB

- Drift-Diffusion and WKB approximation
- Tunneling only in pre-defined regions, along mesh lines, generally no angle
- High I_{ON} and low I_{OFF} predicted

Lateral vs Vertical TFETs: Influence of the Tunneling Area





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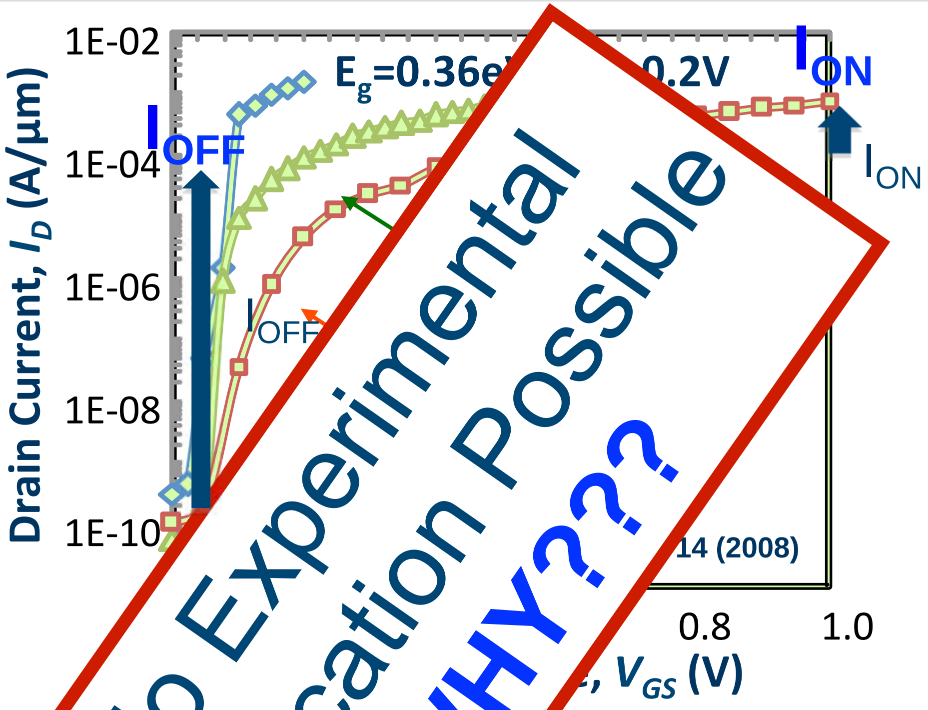


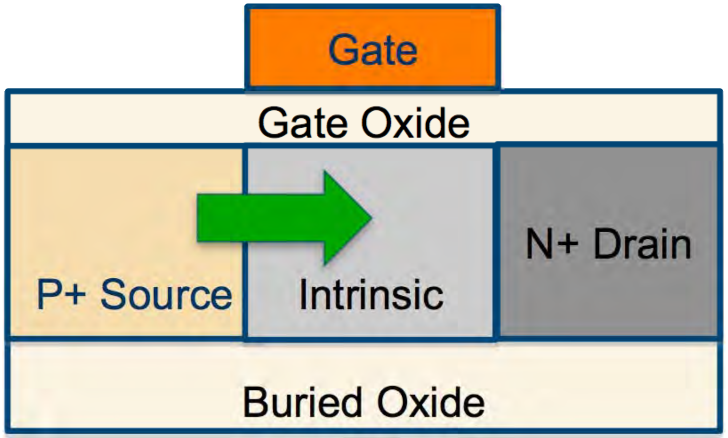
No Experimental Verification Possible

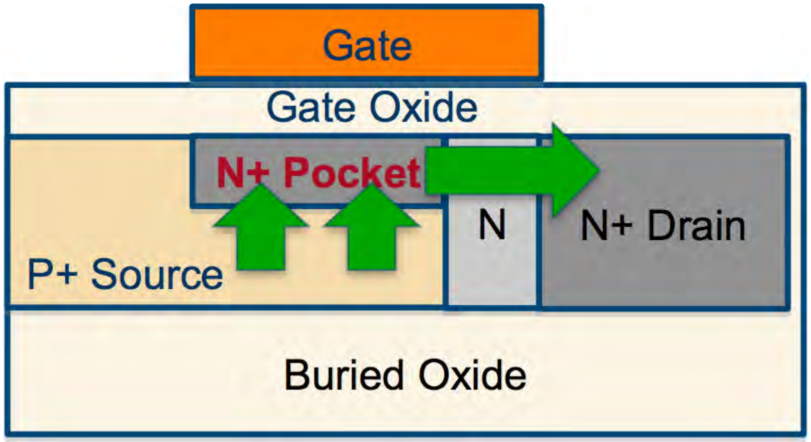
WHY???

mulation @ UCB

- WKB approximation
- Tun pre-defined regions, along m es, generally no angle
- High I_{ON} and low I_{OFF} predicted

Lateral vs Vertical TFETs: Influence of the Tunneling Area





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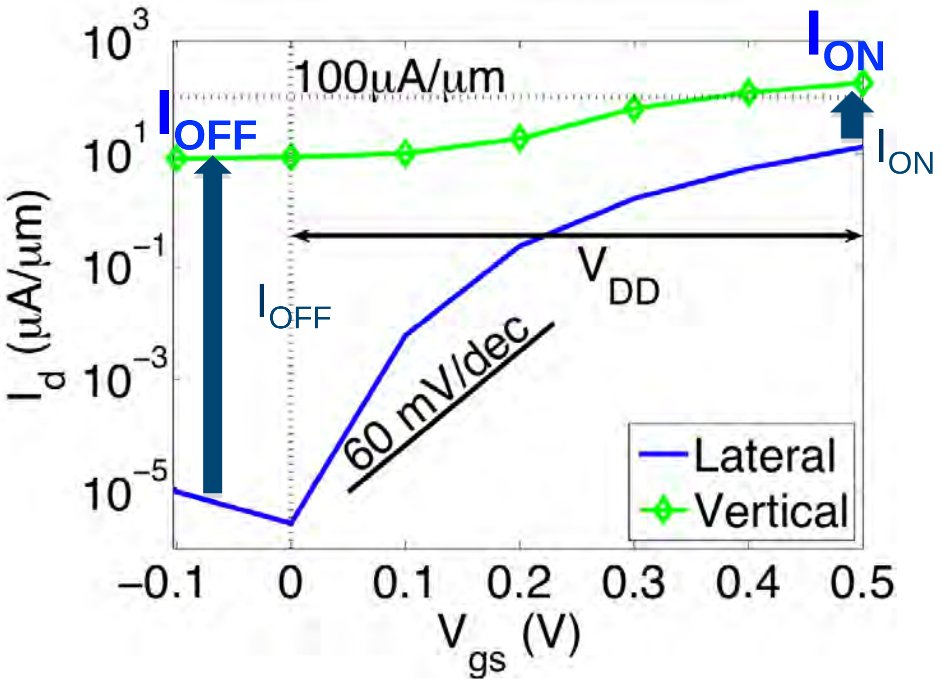
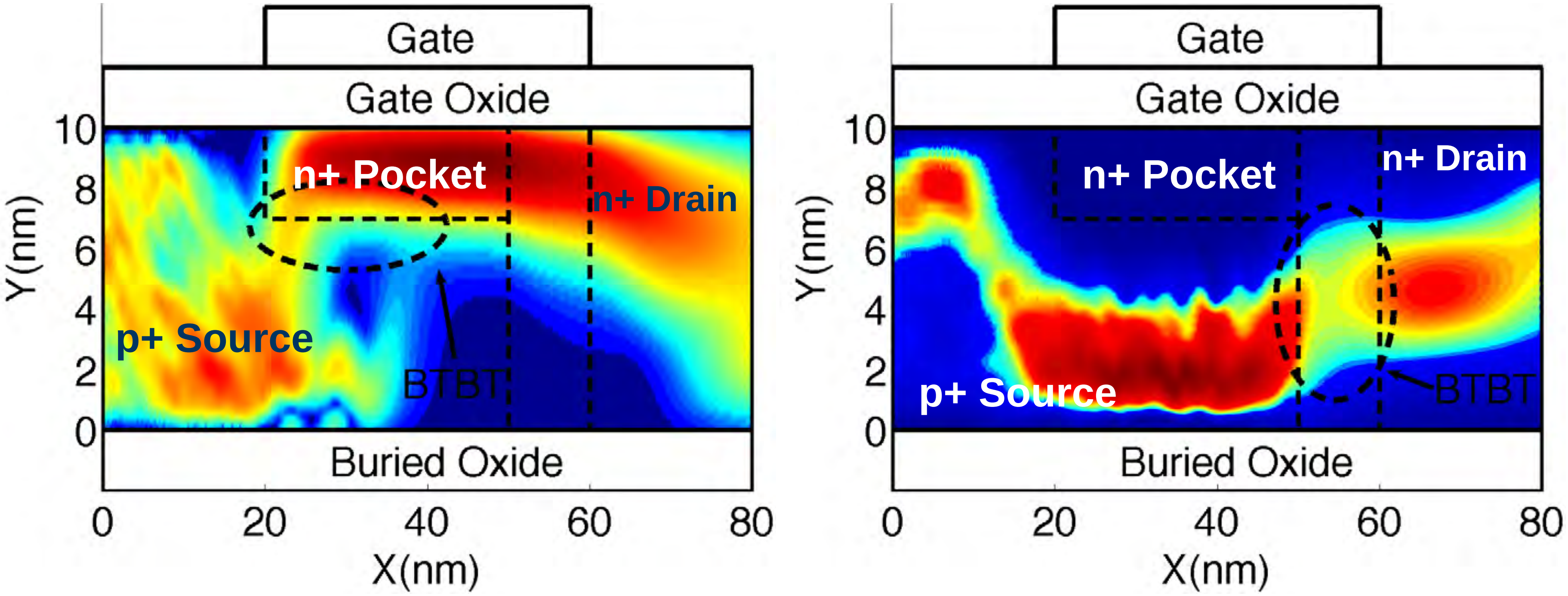


InAs Vertical TFET Sim. with OMEN

- Non-equilibrium FB quantum transport
- Tunneling present everywhere: vertical, horizontal, diagonal,…
- High I_{ON}, but high I_{OFF} too

Vertical TFET: Spatial Current Distributions



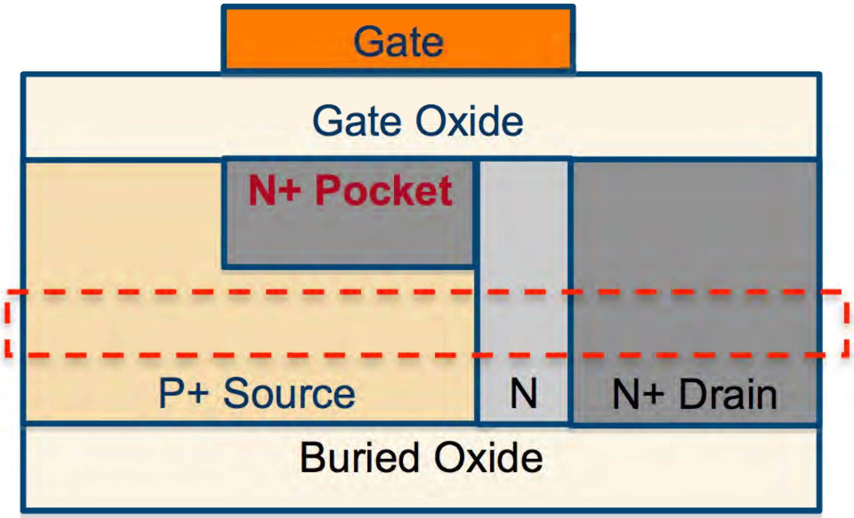
Vertical TFFET ON-Current

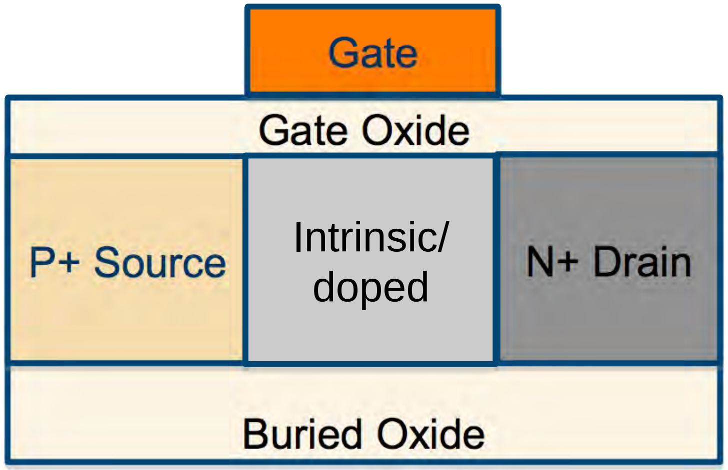
- Quasi-vertical tunneling between the n++ Pocket and the p+ Source close to the Gate
- Non-homogeneous tunneling, 2 main tunneling channels

Vertical TFET OFF-Current

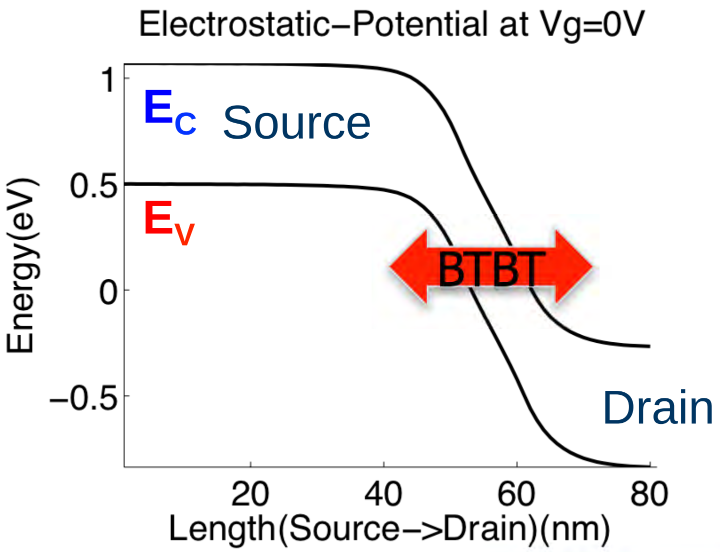
- Quasi-lateral tunneling between p+ Source and n+ Drain close to the Buried Oxide
- No electrostatic control over the tunneling region

Vertical TFET: OFF-State Current

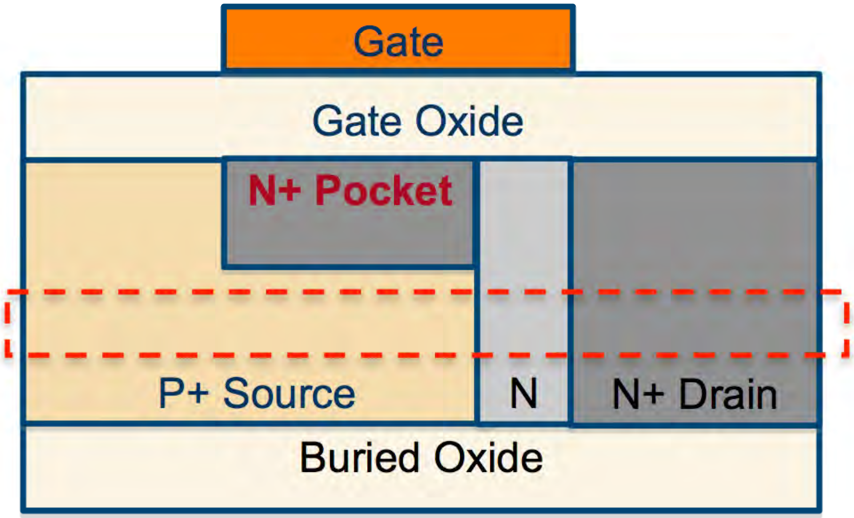


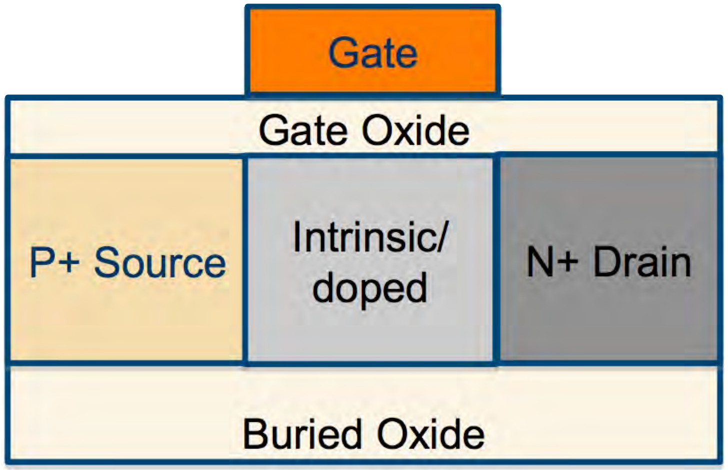


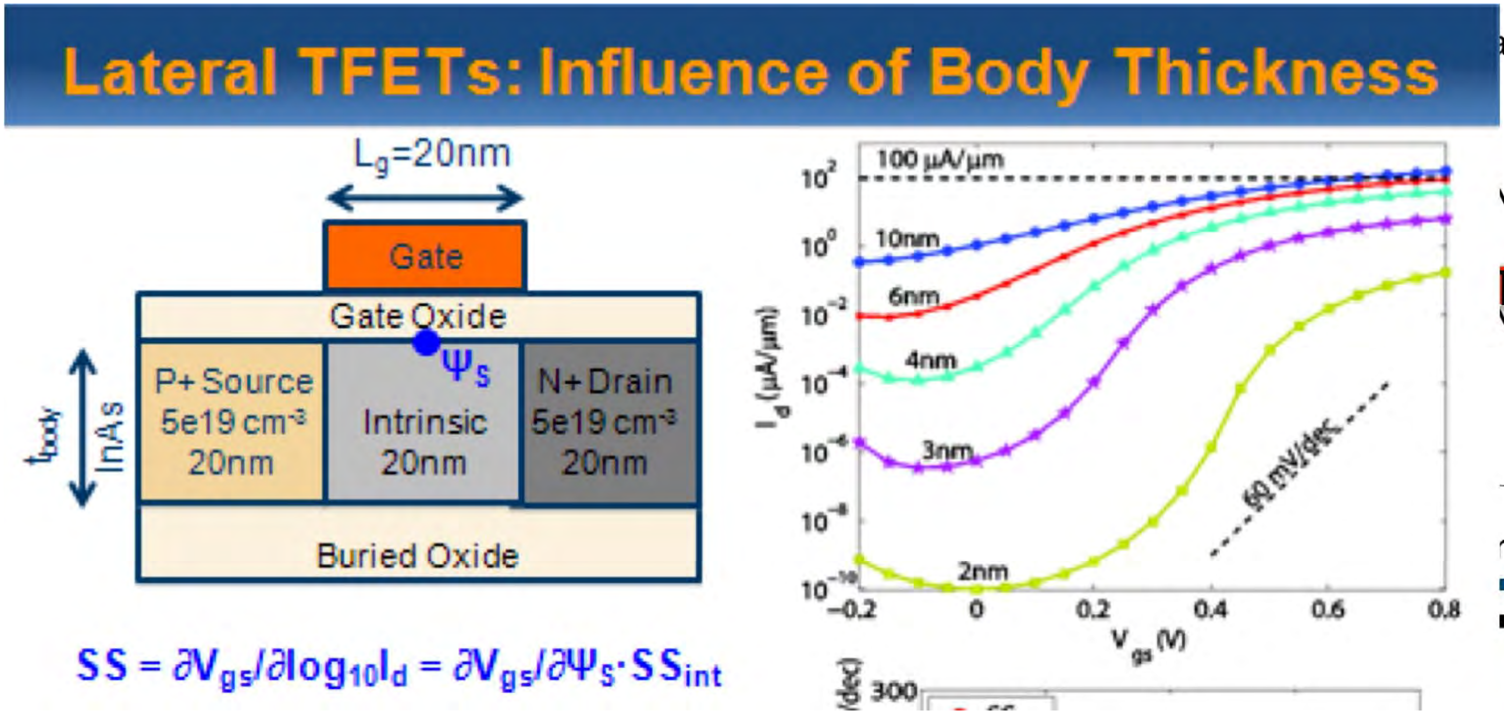
- **Region below the Pocket & p-i-n lateral TFET similar**
- **No electrostatic control away from the gate**
- **Source-to-drain tunneling leakage path**



Vertical TFET: OFF-State Current



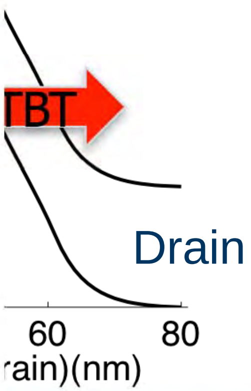




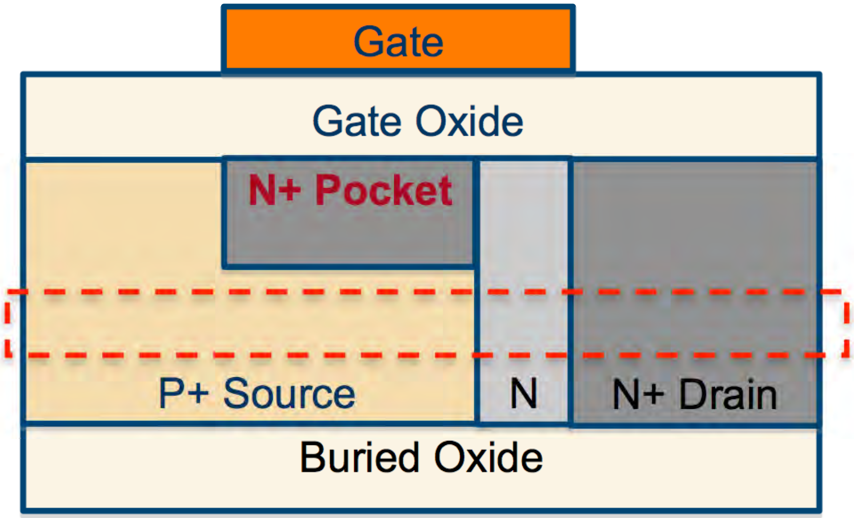
Lateral TFETs: Influence of Body Thickness

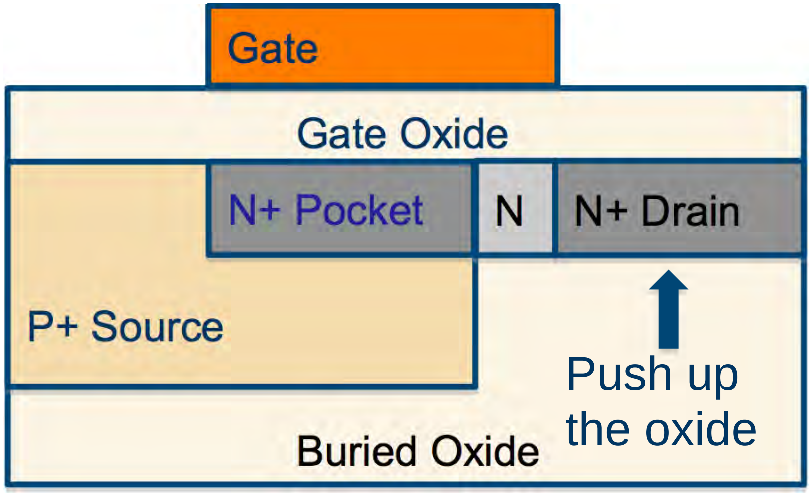
$$SS = \partial V_{gs}/\partial \log_{10} I_d = \partial V_{gs}/\partial \Psi_S \cdot SS_{int}$$

al at Vg=0V

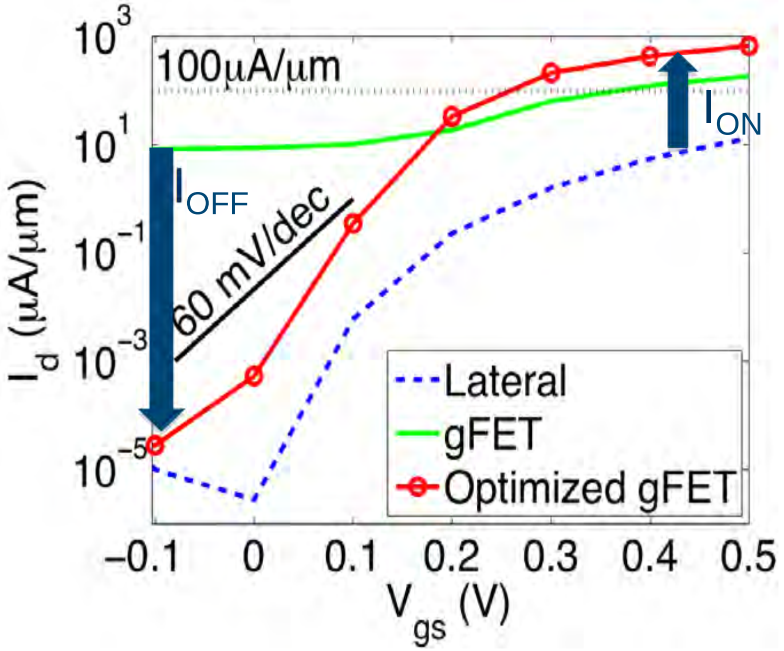


Improved Design





Push up the oxide

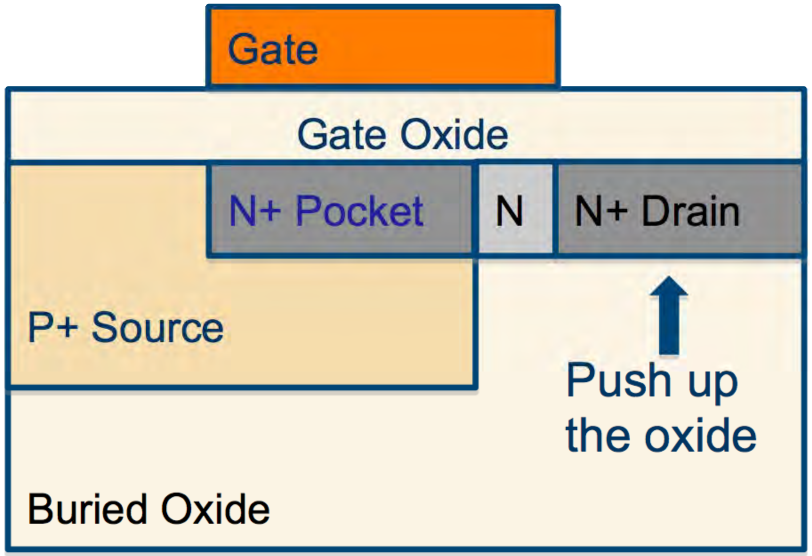


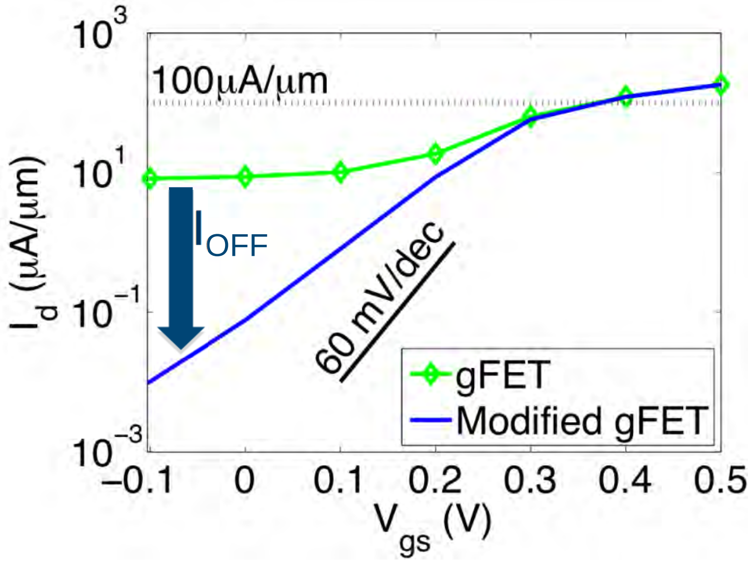
Results:

- decrease of the OFF-current by several orders of magnitude
- further optimizations required to obtain high performance device (not included in this patent form)

US Patent App. 12/858,465

Improved Design





Technical Solution:

- push up the buried oxide below the drain contact to block the lateral source-to-drain tunneling path
- alternative: use of a large band gap material on the drain side to obtain the same blocking effect

Results:

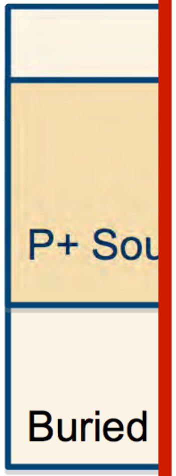
- decrease of the OFF-current by several orders of magnitude
- further optimizations required to obtain high performance device (not included in this patent form)

US Patent App. 12/858,465

Improved Design

Vertical TFET Conclusions

- Vertical TFET with structural problem
  => lateral tunneling leakage
- Commercial TCAD unable to predict internal deficiency
  => misleading consequences
- **OMEN** with global tunneling model as a more accurate solution
  => save time and money



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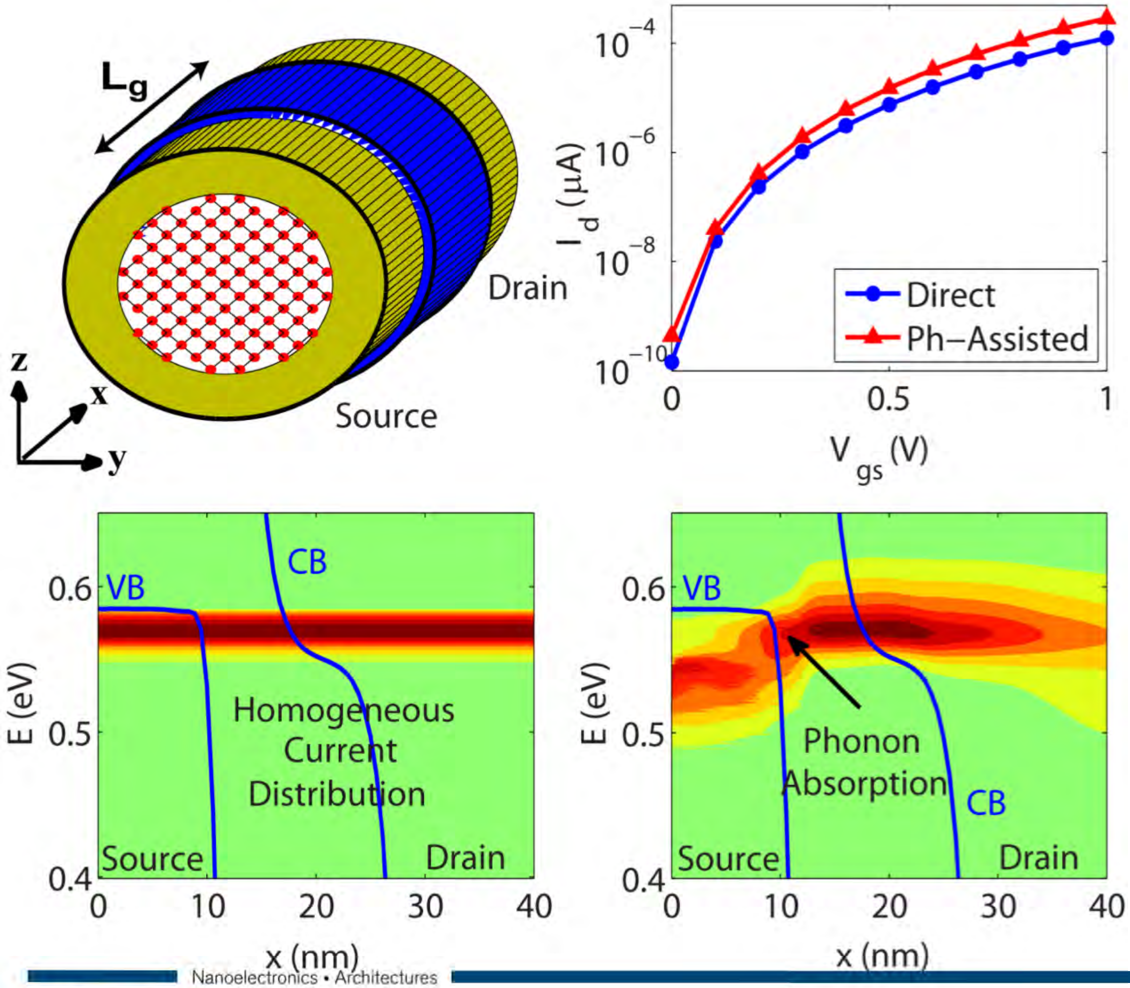
US Patent App. 12/858,465

TFETs: Phonon-Assisted Tunneling

Simulation of Si Nanowire TFETs: Effects of Electron-Phonon Scattering



Objective:

- Simulation of Phonon-Assisted Tunneling (PAT) in TFETs
- Design Si-Ge heterostructure devices for high ON-currents

Approach:

- Atomistic and full-band model
- NEGF up to self-consistent Born approximation
- Confined phonon dispersion

Result/Impact:

- First demonstration of PAT in 3-D nanowires with global tunneling model
- Si, Ge, and InAs nanowire TFETs simulated

Ongoing Work

- Same capability for UTB

Ballisticity of Si NW FETs

Objective:

- Electron-Phonon in Si NW FETs, extract v_{inj}, μ_{PH}, and B factor

Approach:

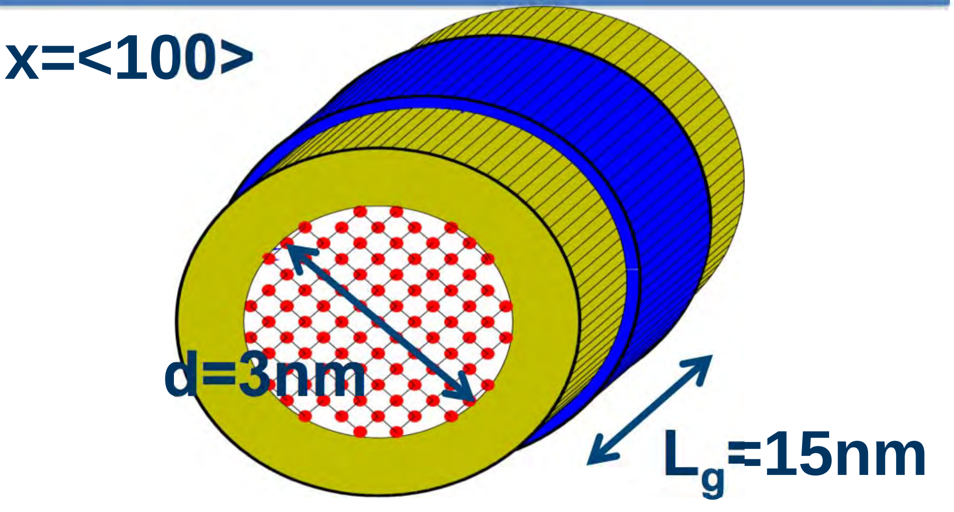
- Accurate description of the semiconductor material properties
- Atomistic Representation of the NWs
- Quantized phonon dispersion
- Quantum transport with NEGF

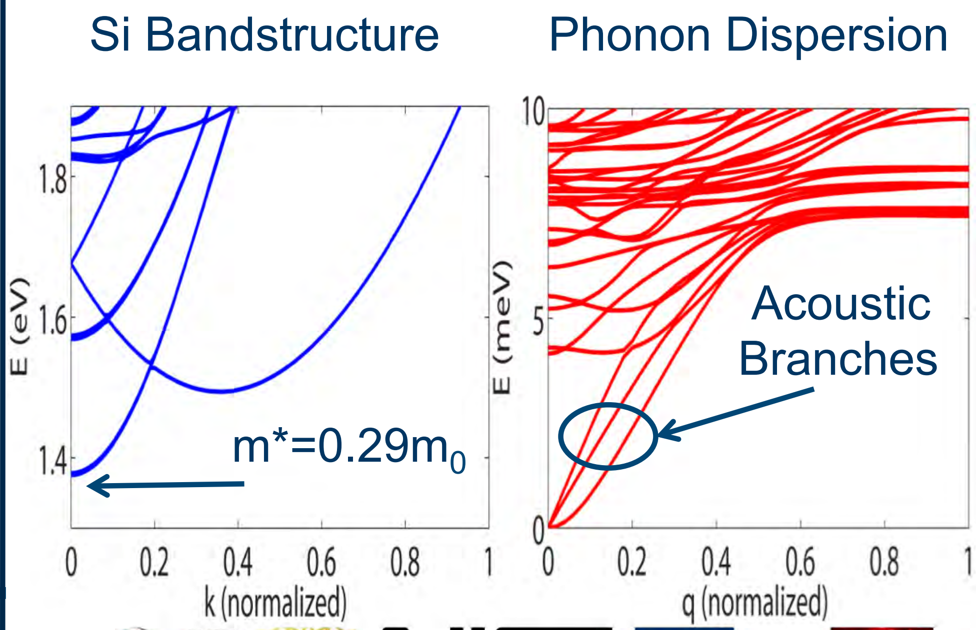
Results and Impacts:

- Reduction of the drain current and injection velocity, modification of the electrostatics
- First demonstration of FB + El-Ph

Ongoing Work:

- Mobility extraction in n/p NW FET
- Experimental data to verify the model





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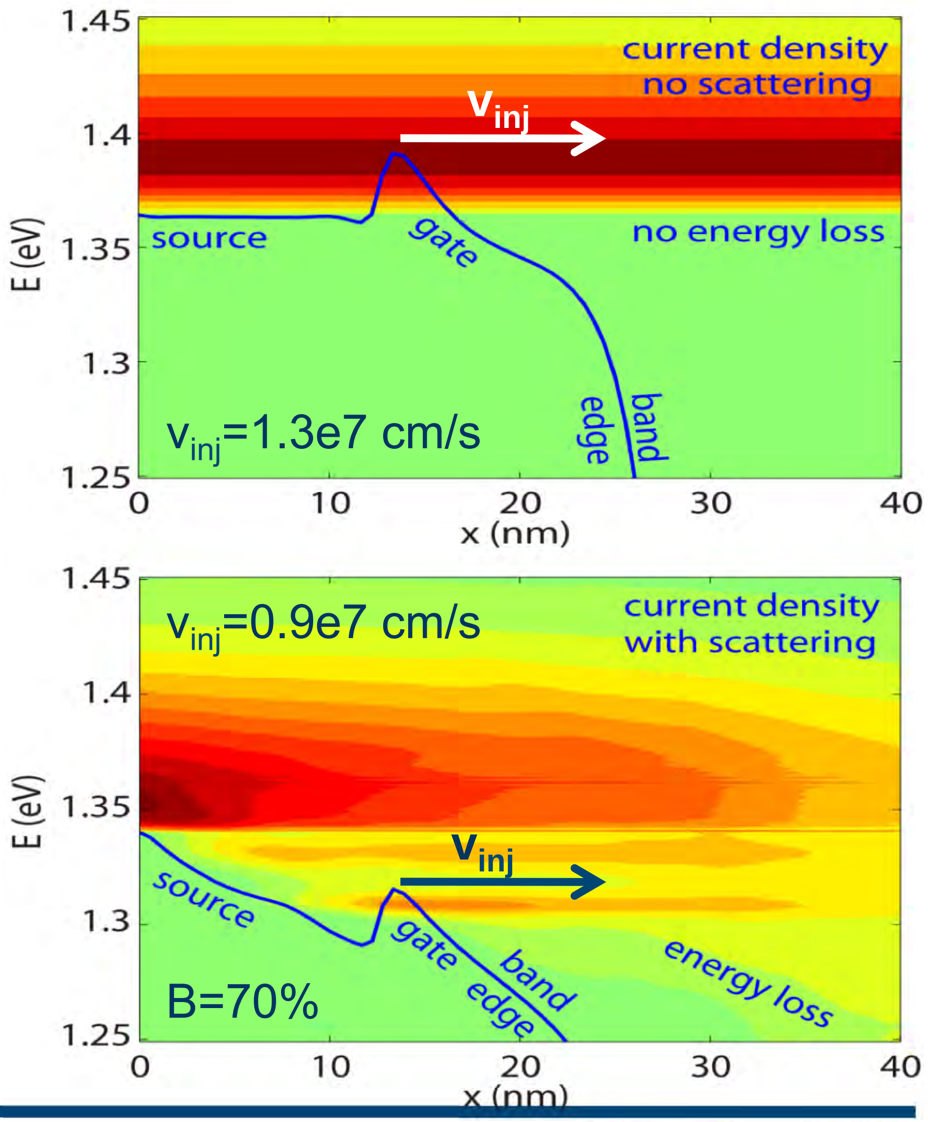
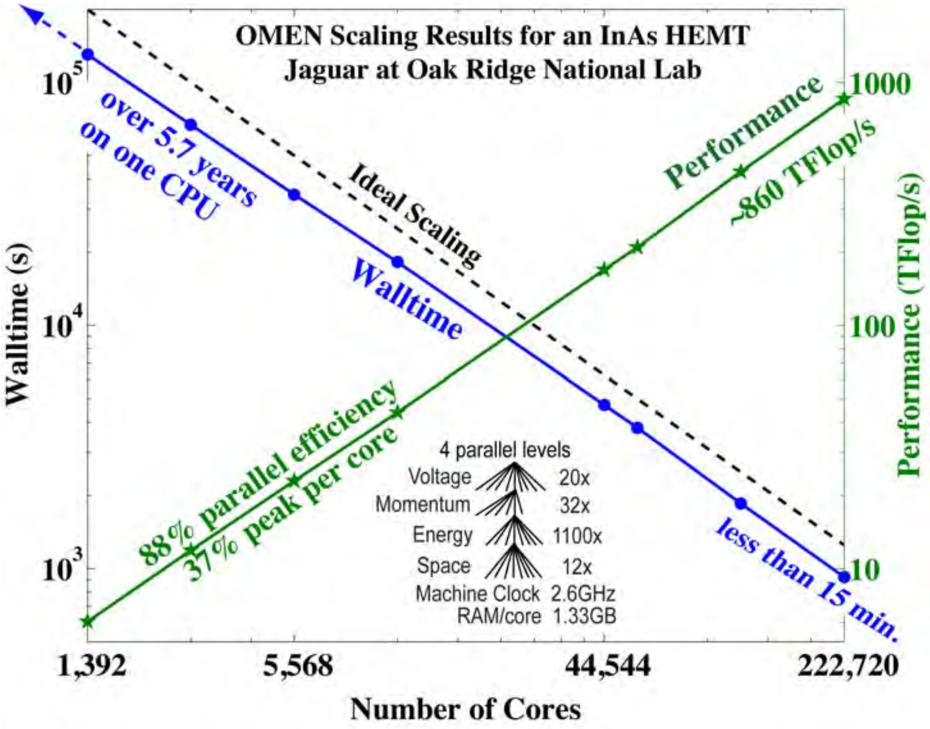
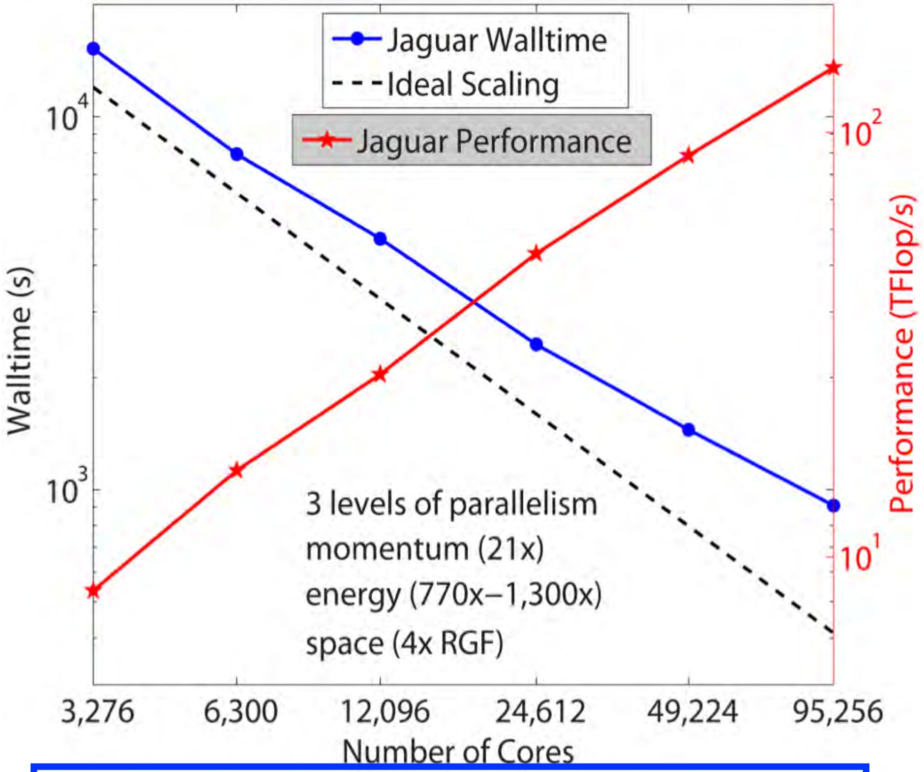


Computational Load
Ballistic vs. Electron-Phonon Scattering

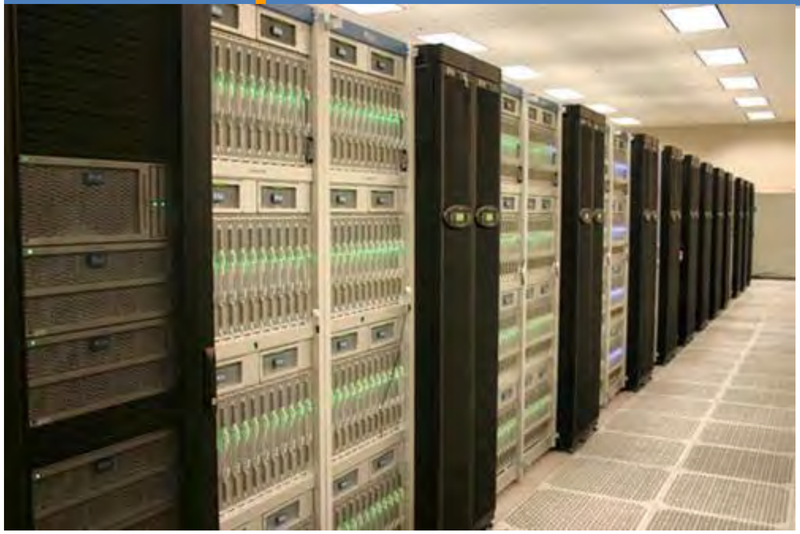




Ballistic Transport:
Ideal Scaling 222,720 cores
- >90% parallel efficiency on 95k cores
- >860 TFlop/s on 222k cores

Transport with Scattering:
>100-1,000x more intensive!
Much more communication!
1 bias point (20 for 222,720 cores)
- 58% parallel efficiency on 95k cores
- 142 TFlop/s on 95k cores

U.S. Science and Engineering Computational Resources



Ranger@TACC
~64,000 cores

SUN / AMD cores

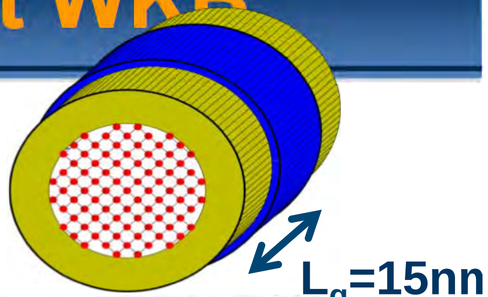
Kraken@NICS
~95,000 cores

Cray XT4 / AMD cores

Jaguar@ORNL
~225,000 cores

Cray XT5 / AMD cores

Calibration and Validation against WKB



Objective:

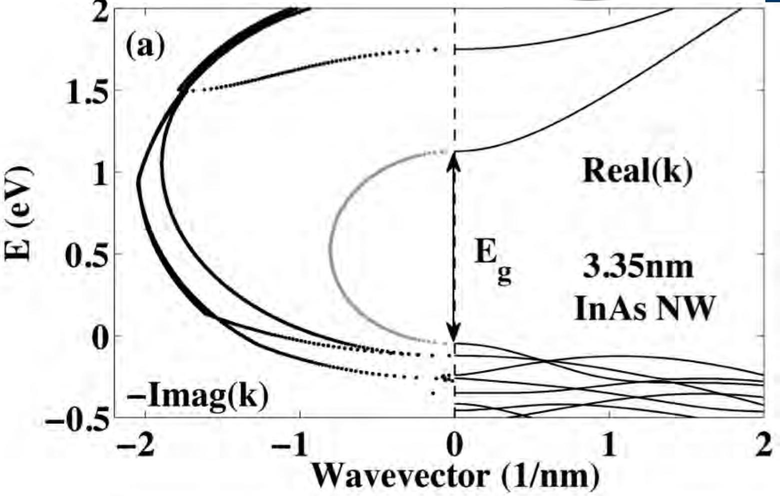
- Calibrate against the standard band-to-band tunneling model: WKB

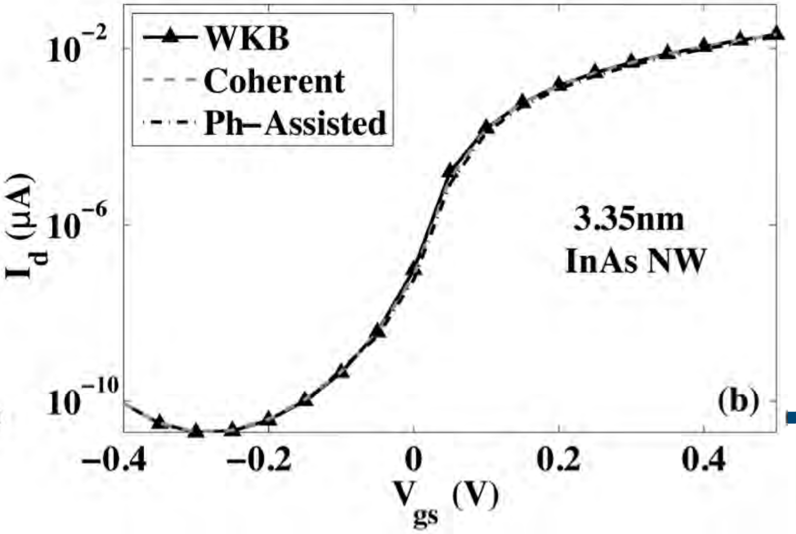
Approach:

- Select simple nanowire geometry
  - Adjust WKB (bandgap quantization)
- Select 2 material systems:
  - Expect agreement: direct gap InAs
  - Expect disagreement: indirect gap

Results and Impacts:

- Direct gap InAs – agreement!
  - But how does one get the right gap in WKB?
  - Indirect gap Si:
  - WKB overestimates current
  - Lateral BTBT show that one needs a non-local tunneling model





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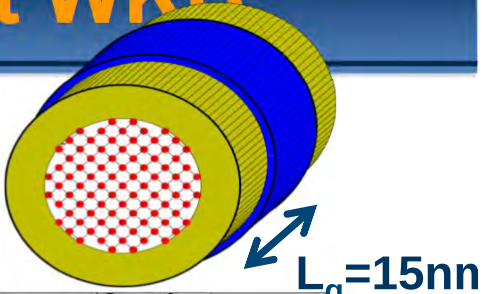

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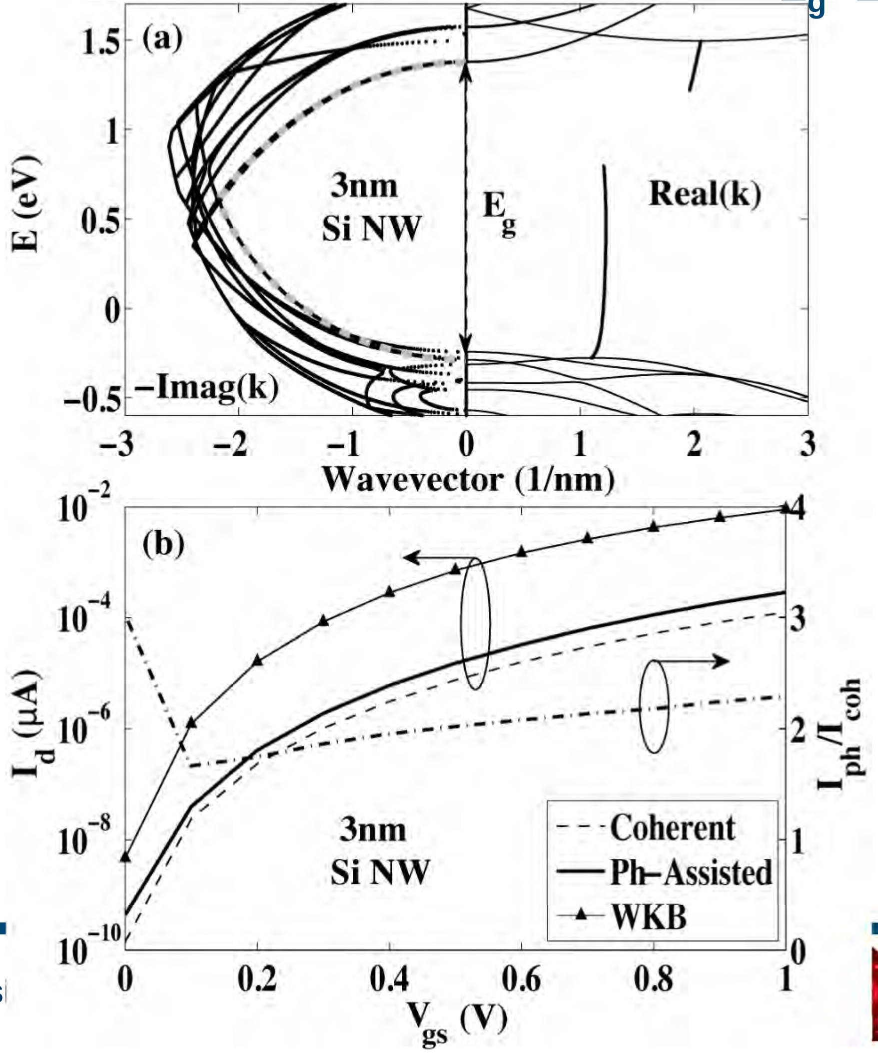


Status of Experimental Comparisons

- Existing experimental 2D and 3D geometries too large for OMEN
  - 2D devices up to 15nm body (5nm with scattering)
  - 3D devices up to 10nm diameter (4nm w/ scattering)

  Þ compare OMEN against traditional methods and understand their limitations

  Þ guide the design concepts at the ultimate limit
- Existing experimental 1D geometries / diodes require incoherent scattering
  - OMEN cannot handle scattering in layered diodes
  - Bandgap narrowing appears to be important
  - Explore with OMEN

Atomistic Nanoelectronic Transport Modeling

Objective:

- Creation of a new switch operating at low voltage with a low sub-threshold swing with enough on-current

OMEN Capabilities:

- Can perform coherent simulations on “large” devices (1D, 2D, 3D)
- Can perform incoherent/scattering transport over “small” devices (2D/3D)

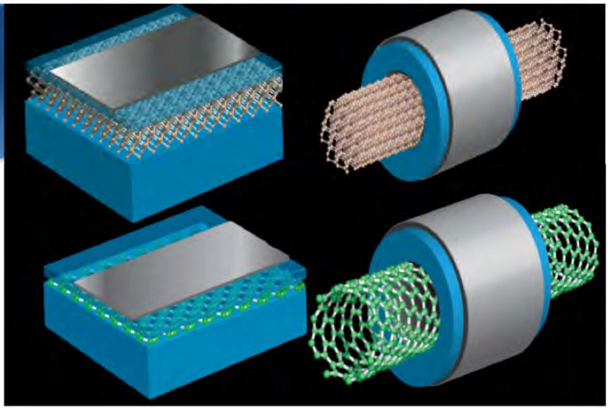
Some Insights / Opinions:

- The electrostatic gate control is a key element to switch a critical device domain as abruptly as possible
- Lateral homojunction BTBT cannot achieve this
  - Problems in regrowth of etched surfaces + high doping
- Standard vertical BTBT (mesa structure) cannot achieve this either
  - Gate control is too remote – cannot get a reliable steep SS
- Heterojunction BTBT with staggered band edges may help
  - Gate control and regrowth of new material system remain challenges

Where OMEN Modeling can help today:

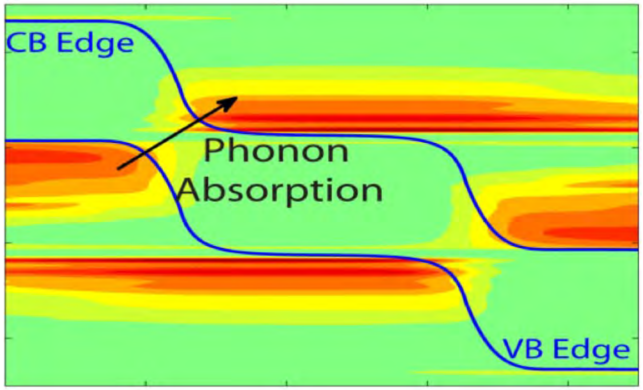
- Exploration of novel 2D and 3D geometry configurations to see if they can deliver strong gate control and large currents.
- Guide experiments in nano-scale device structures

Conclusion
OMEN is a New Physics-Based TCAD



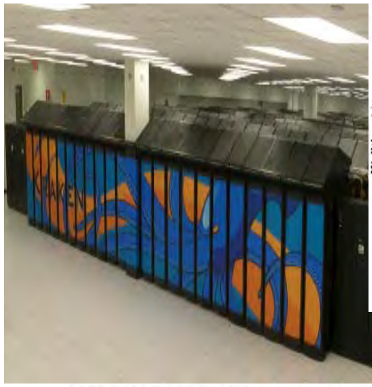
OMEN Simulation Approach

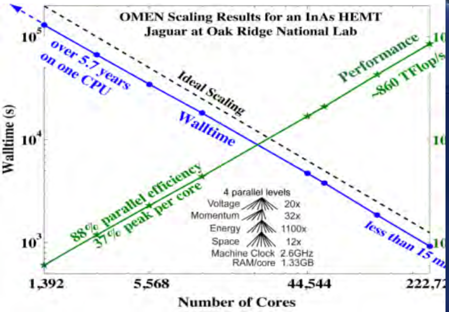
- 3D, full-band, atomistic, quantum transport
- UTB, NW, or HEMT structures BTBT
- Electron-phonon scattering
- 8 journal articles, 5 proceedings articles



Outlook and Near Term Challenges

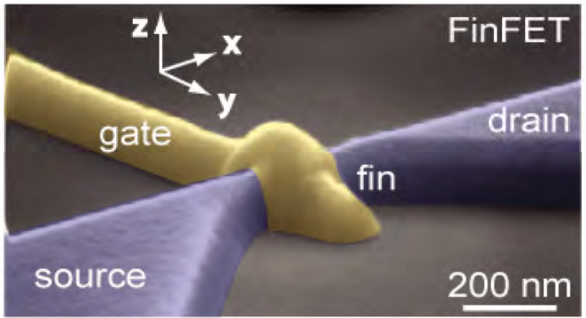
- explore design space for nano-scaled FETs sizes/materials/doping
- Explore doping effects, explicit impurities, bandgap narrowing
- Aid experiments





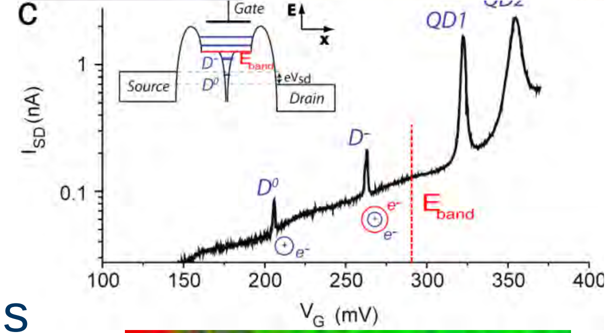
OMEN/NEMO on nanoHUB.org
Over 5,000 users

Long Term Vision and Needs



Boundary (new material / new device) is blurred

- Need an atomistic representation
- Can measure and model individual impurities!
- Need atomistic process models coupled to transport

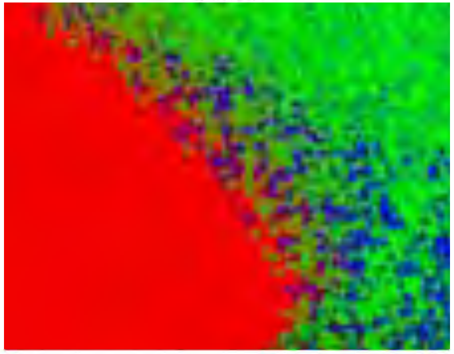


Contacts – begin to dominate intrinsic device

- Many electrons, many materials, scattering

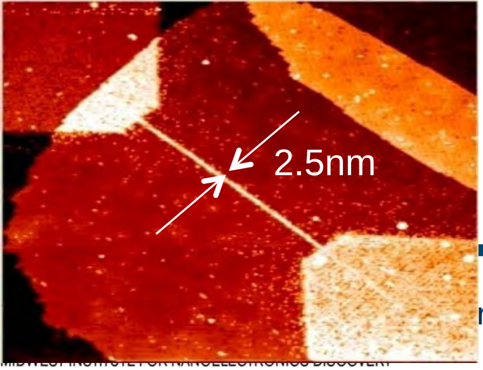
Non-local Interactions: Phonon-electron-spin-photons

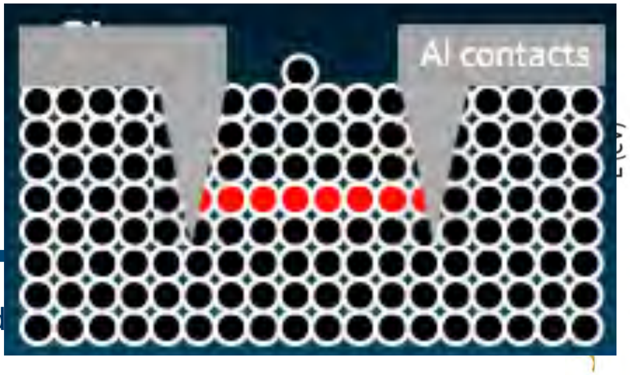
- Full matrix unfeasible => approximations
- Time dependence => noise, fluctuations, interactions
- Spin is in the basis! Not an afterthought!

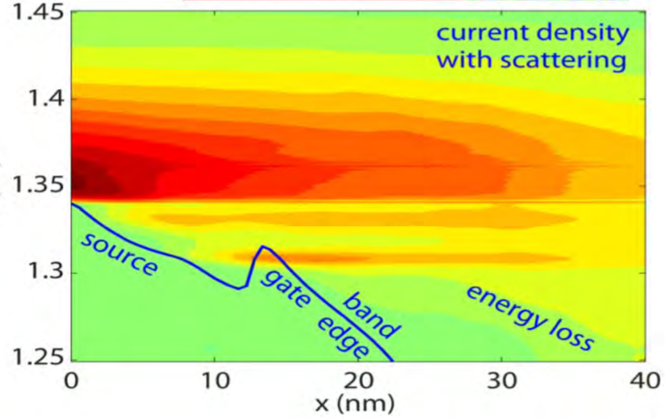


Thermoelectric cooling

Impurity channels – ultimate limit of electronics







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3. Samarth Agarwal, Gerhard Klimeck, Mathieu Luisier, "Leakage Reduction Design Concepts for Low Power Vertical Tunneling Field-Effect Transistors“, accepted to IEEE Electronic Device Lett. (2010) (acceptance March 12)Not Cited Yet
4. Mathieu Luisier, Gerhard Klimeck, "Numerical Strategies towards Peta-Scale Simulations of Nanoelectronics Devices“, Parallel Computing (PARCO), Vol. 36, pg. 117-128 (2010); doi:10.1016/j.parco.2010.01.003Cited by 2
5. Abhijeet Paul, Saumitra Mehrotra, Mathieu Luisier, Gerhard Klimeck, "Performance Prediction of Ultra-scaled SiGe/Si Core/Shell Electron and Hole Nanowire MOSFETs“, IEEE Electron Device Lett., Vol. 31 pg. 278-280 (2010);
6. Gerhard Klimeck, Mathieu Luisier, "Atomistic Modeling of Realistically Extended Semiconductor Devices with NEMO/OMEN“, IEEE Computing in Science and Engineering (CISE), Vol.12, pg. 28-35 (2010)Not Cited Yet
7. Mathieu Luisier, Gerhard Klimeck, "Atomistic Full-Band Simulations of Si Nanowire Transistors: Effects of Electron-Phonon Scattering“ Phys. Rev. B, Vol. 80, 155430 (2009); doi:10.1103/PhysRevB.80.155430
8. Mathieu Luisier, Gerhard Klimeck, "Performance analysis of statistical samples of graphene nanoribbon tunneling transistors with line edge roughness“ Applied Physics Lett., Vol. 94, 223505 (2009); doi:10.1063/1.3140505

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3. Neerav Kharche, Gerhard Klimeck, Dae-Hyun Kim, Jesús. A. del Alamo, Mathieu Luisier, "Performance Analysis of Ultra-Scaled InAs HEMTs“, IEDM 2009, Dec. 7-9, 2009.
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