EE-612:
Lecture 28:
Overview of SOI Technology

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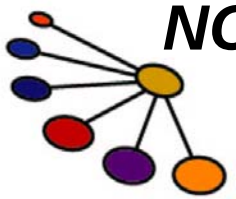

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outline

1) Basic structures and SOI advantages
2) SOI film technologies
3) Partially depleted SOI
4) Fully depleted SOI
5) Advanced SOI devices

acknowledgements

1) Professor Jerry Fossum

The approach and several of the figures were taken from a talk , "SOI MOSFET Physics Underlying the Good and Bad of SOI CMOS," that Prof. Fossum delivered at Purdue University, in March, 2000.

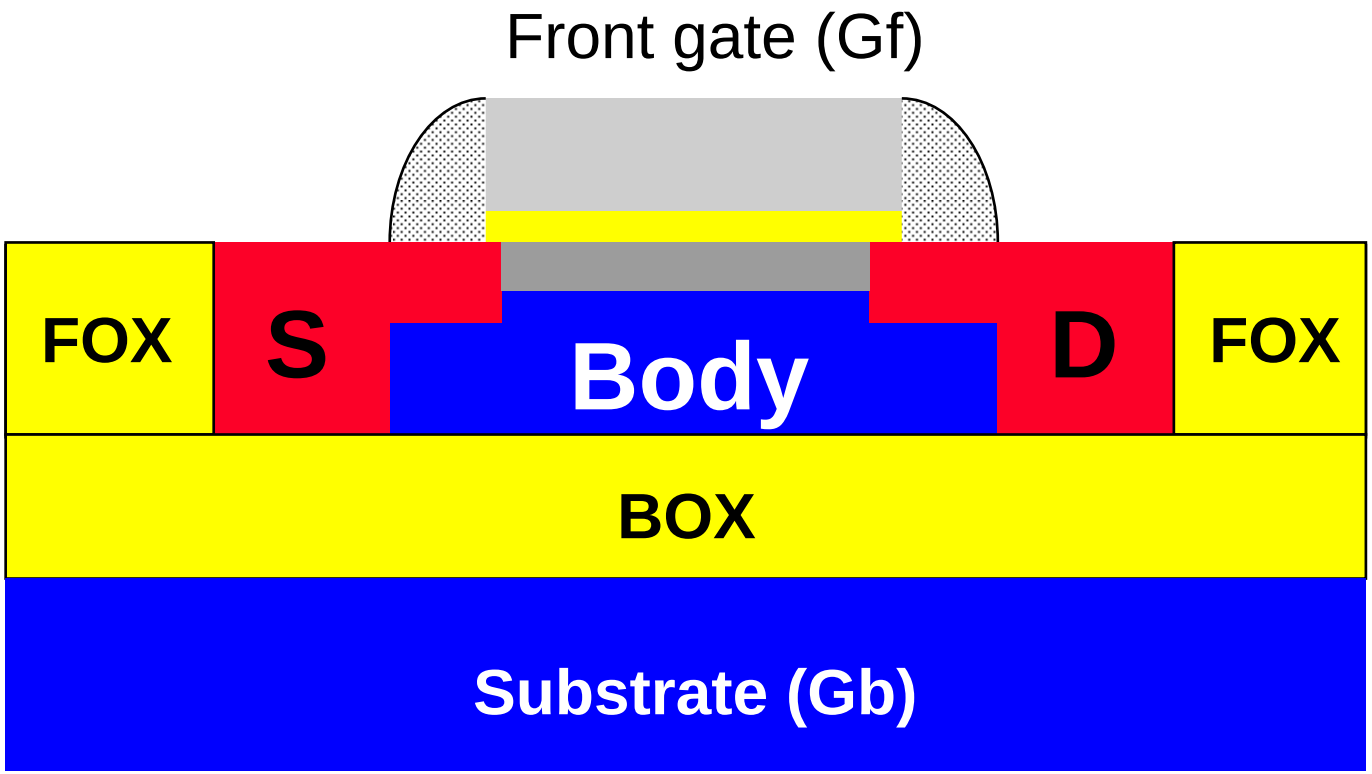
2) Jianan Yang

Several of the figures on SOI film technology are from Dr. Yang's Ph.D. thesis proposal

3) Professor Gerry Neudeck

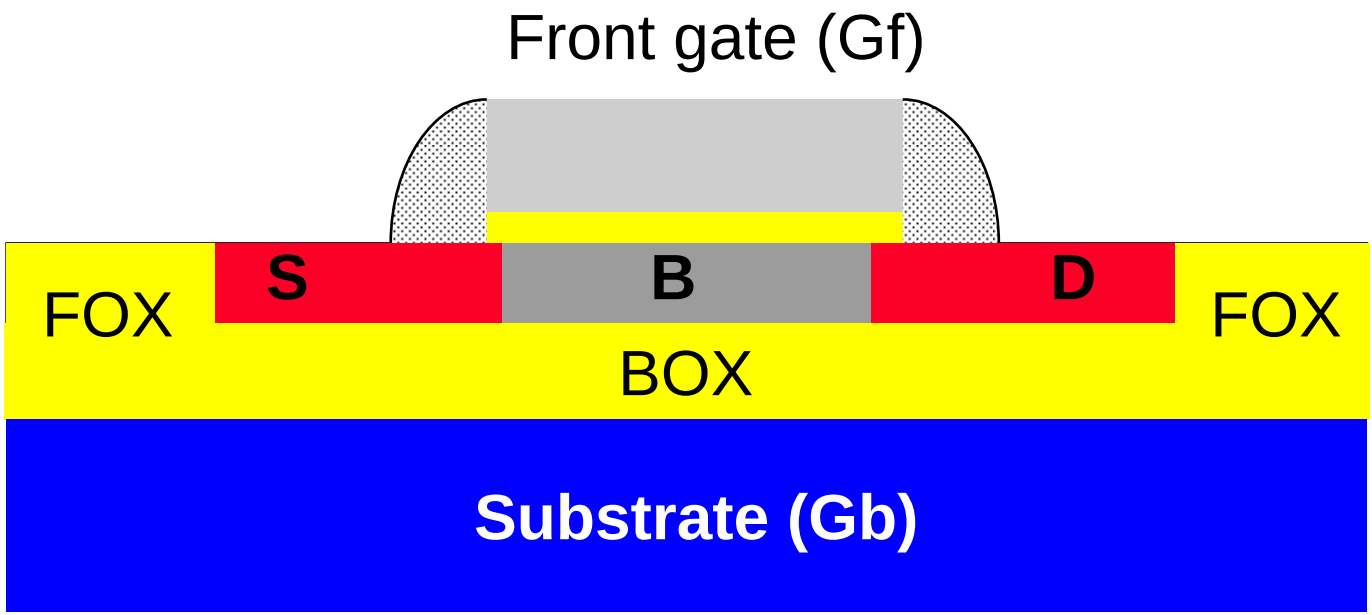
The SEG/ELO material was obtained from Prof. G. W. Neudeck.

basic structures



Partially depleted (PD) body
(similar to bulk MOSFET but the body **floats**)

basic structures



Fully depleted (FD) body

benefits of SOI

-Simple IC processing (isolation)

-Higher density

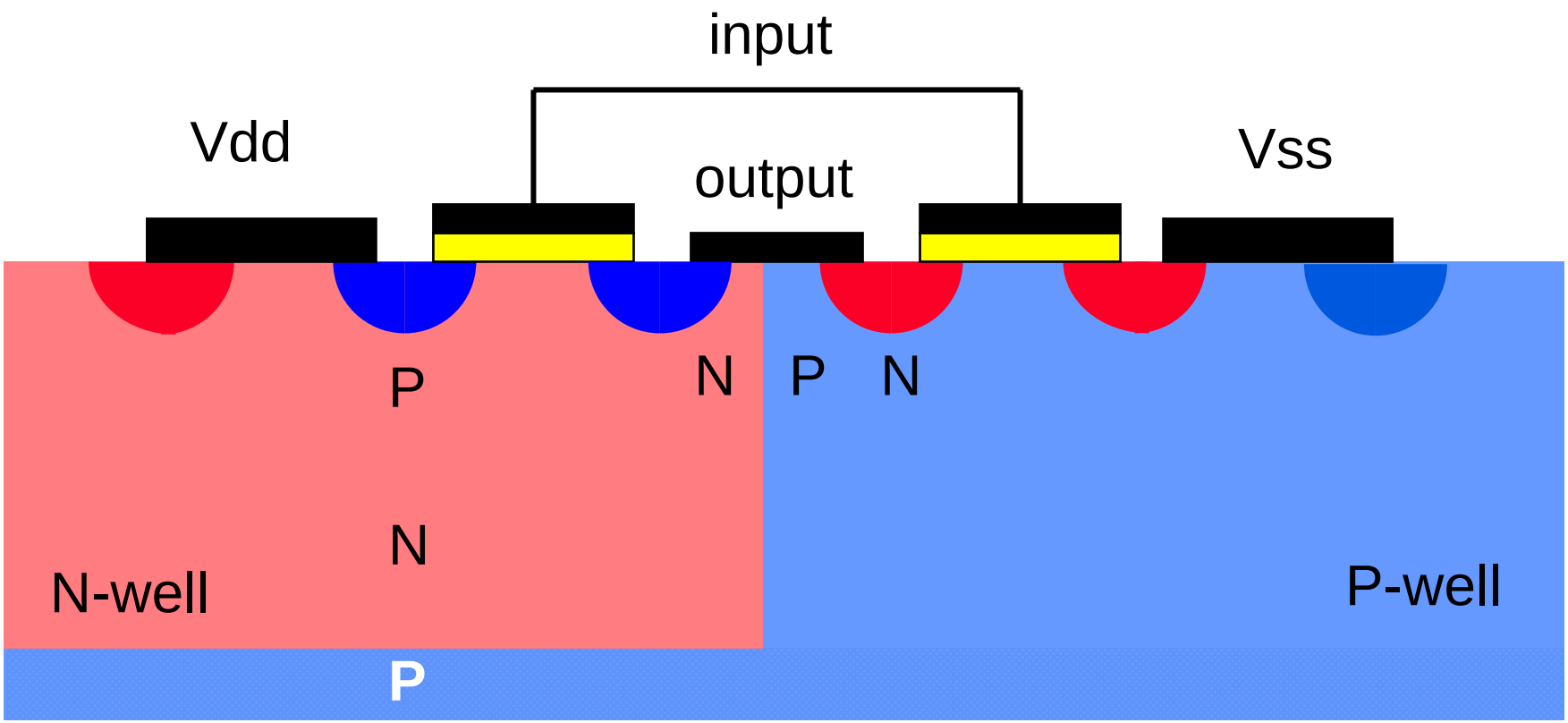
-Reduced S/D junction capacitance (speed/power)

-Low soft-error rate

-No latch-up

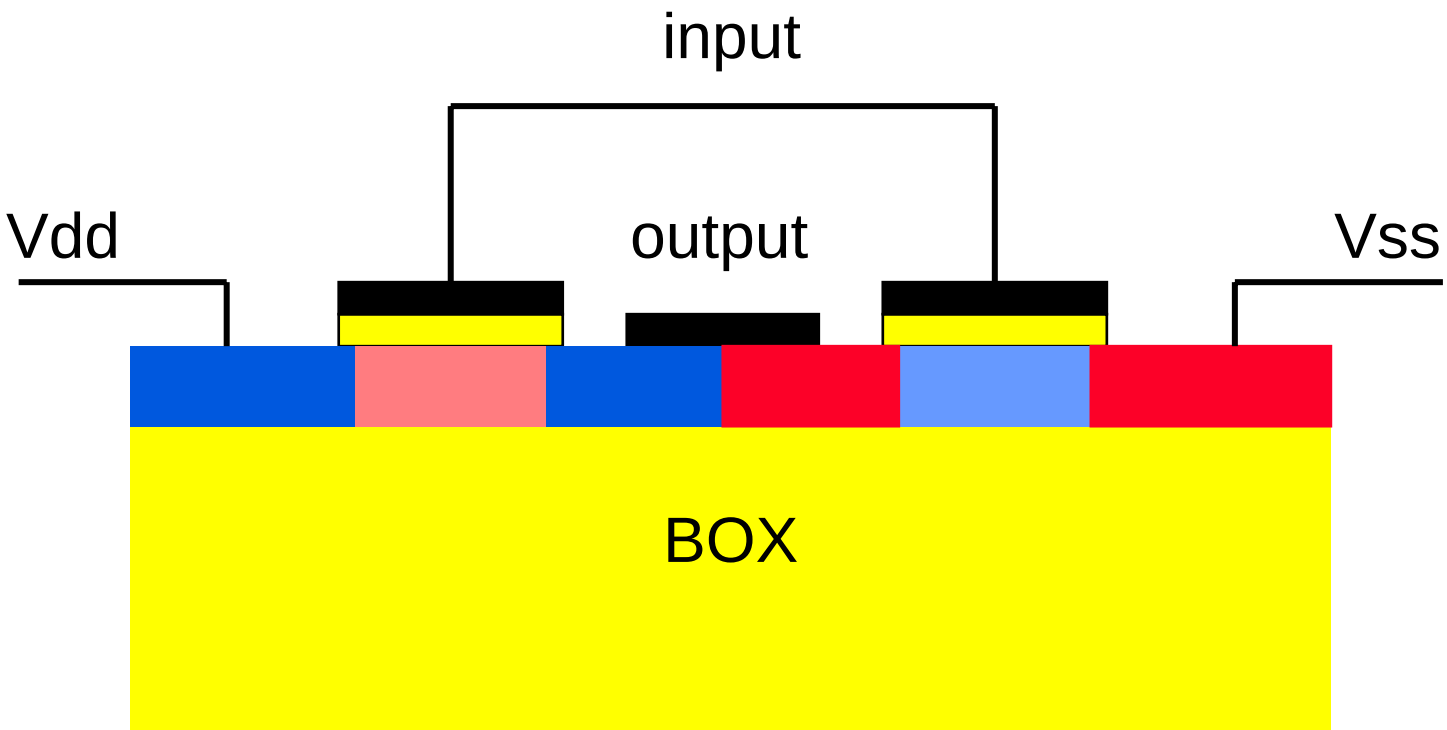
-No (normal) body effect

benefits of SOI



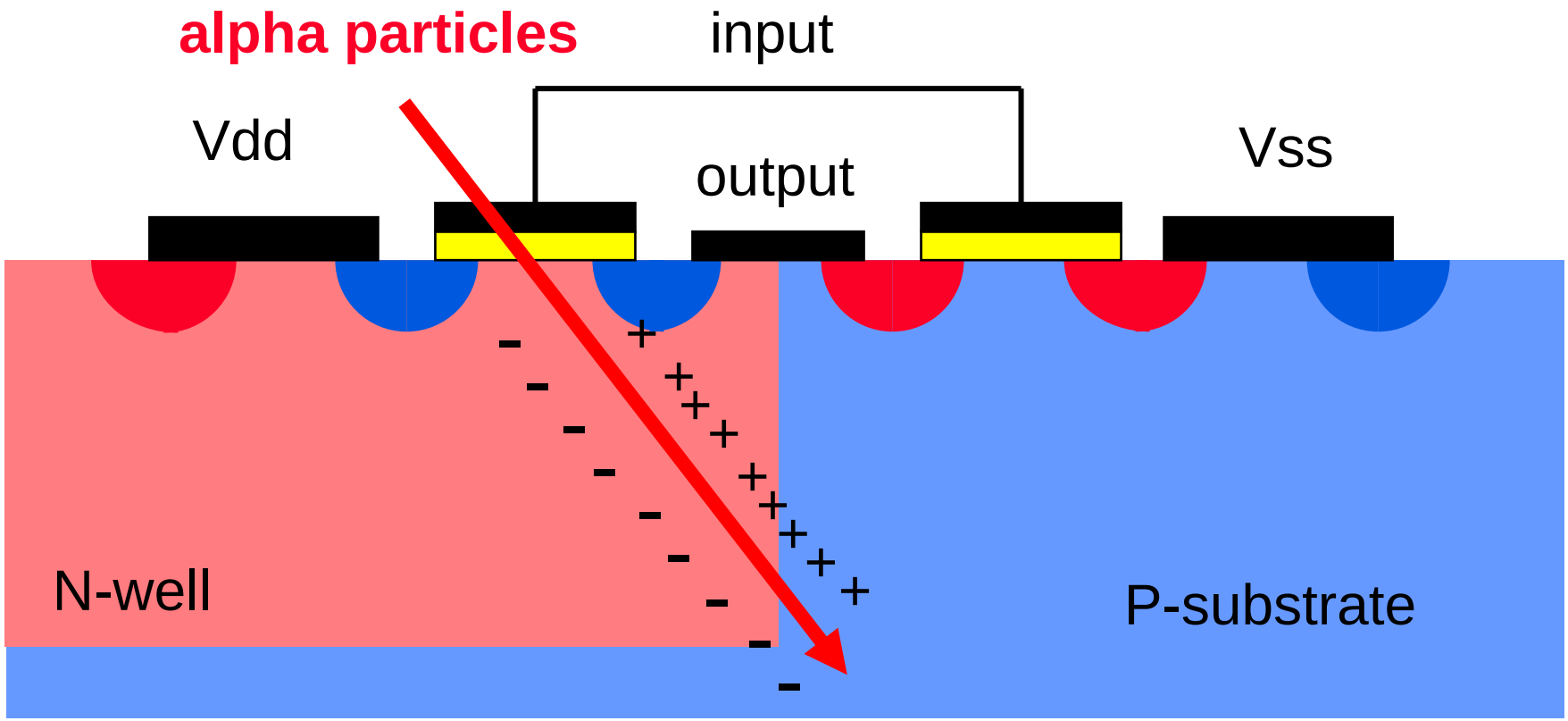
Parasitic bipolar devices ➡ “latchup”

benefits of SOI (ii)



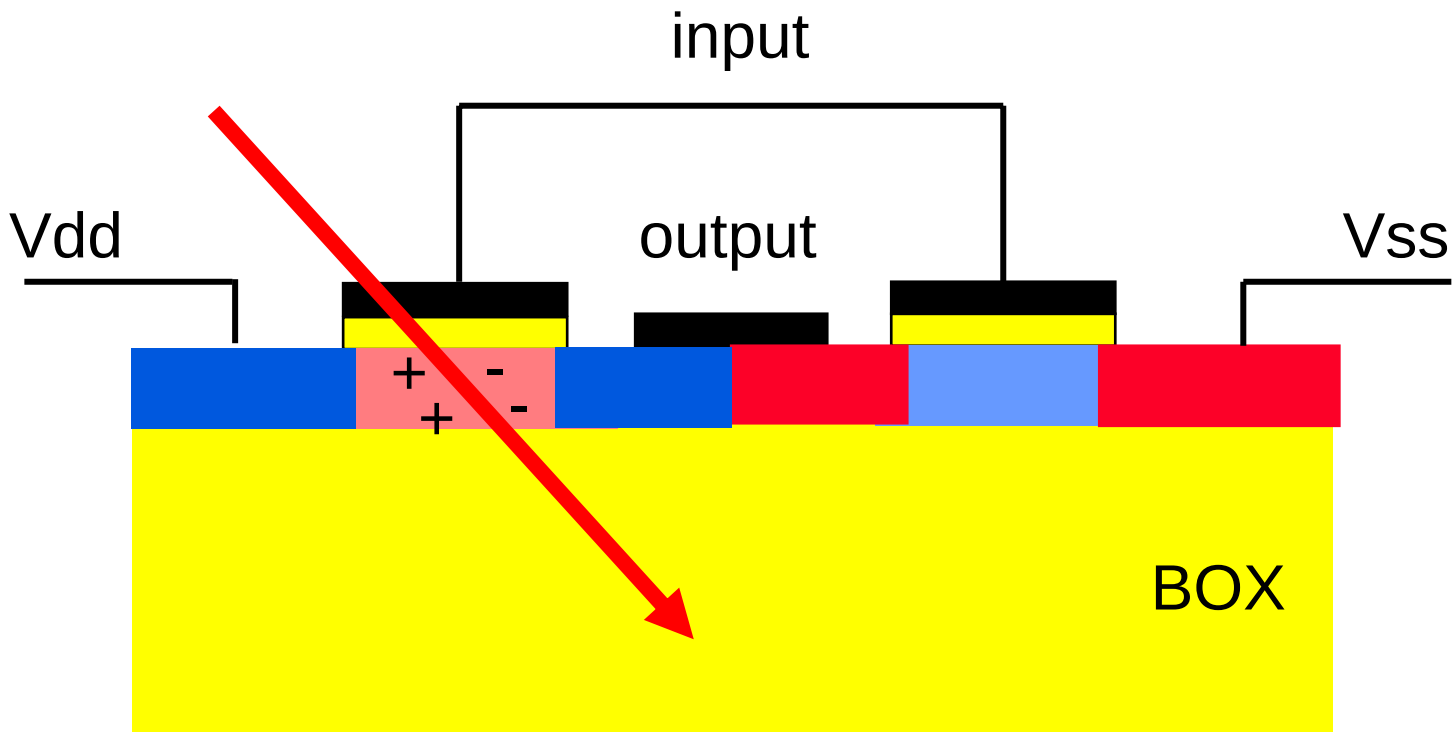
No parasitic bipolar devices ➡ no latchup

soft errors in bulk CMOS



Alpha particles ➡ “soft” errors

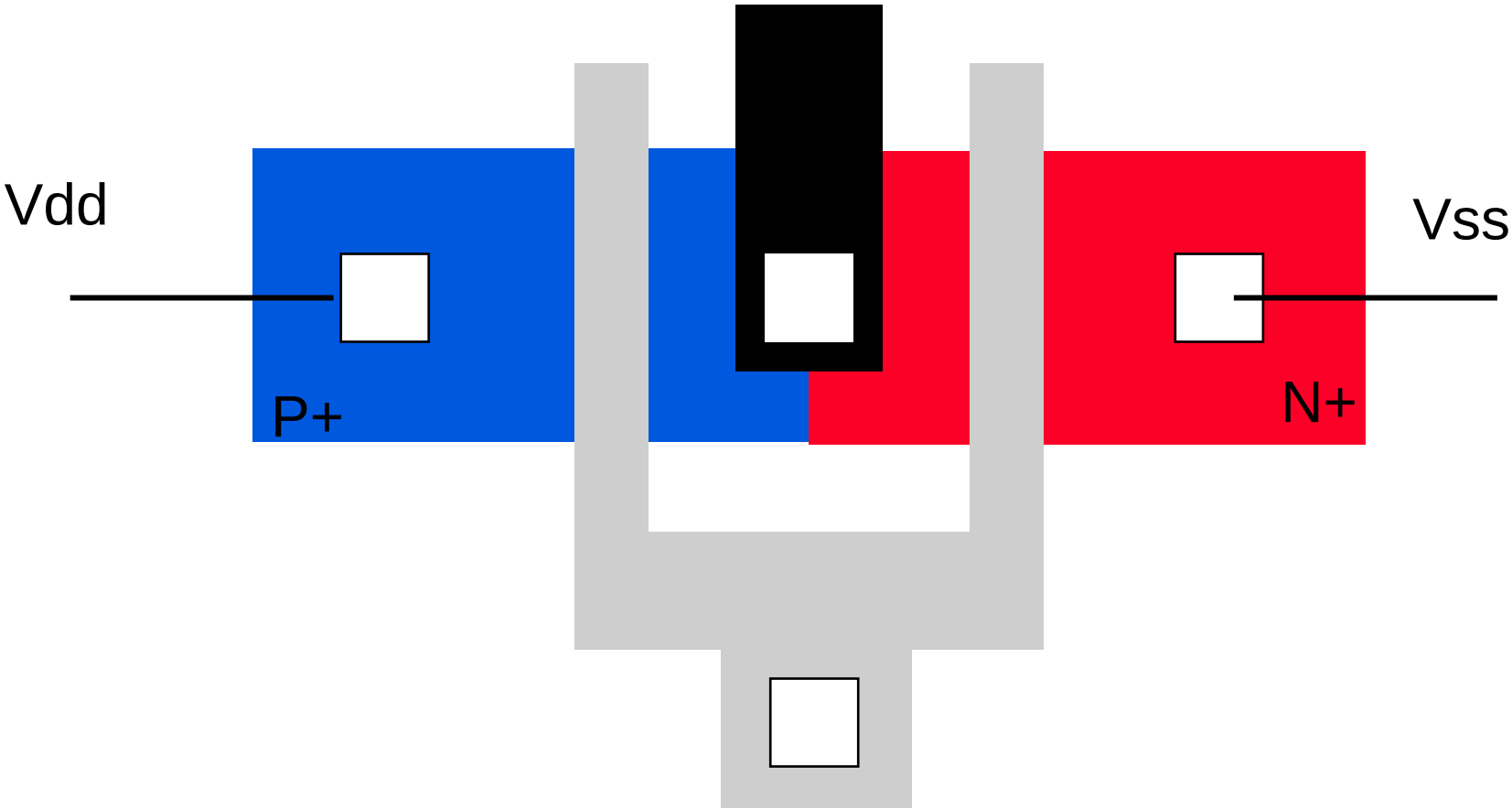
soft errors in SOI



Low soft error rate

layout for bulk CMOS

layout for SOI



Simpler isolation → simpler process → smaller layout

benefits of SOI?

- Simple IC processing (isolation) / but big change
- Higher density
- Reduced S/D junction C / low anyway
- Low soft-error rate
- No latch-up / not a problem now
- No (normal) body effect / FB effects are worse

outline

1) Basic structures and SOI advantages

2) SOI film technologies

3) Partially depleted SOI

4) Fully depleted SOI

5) Advanced SOI devices

SOI film technology

1) SIMOX: Separation by ion Implantation of Oxygen

2) BESOI: Bonded and Etch back

3) ELTRAN: Epitaxial Layer TRANsfer by bonding and etch back of porus Si

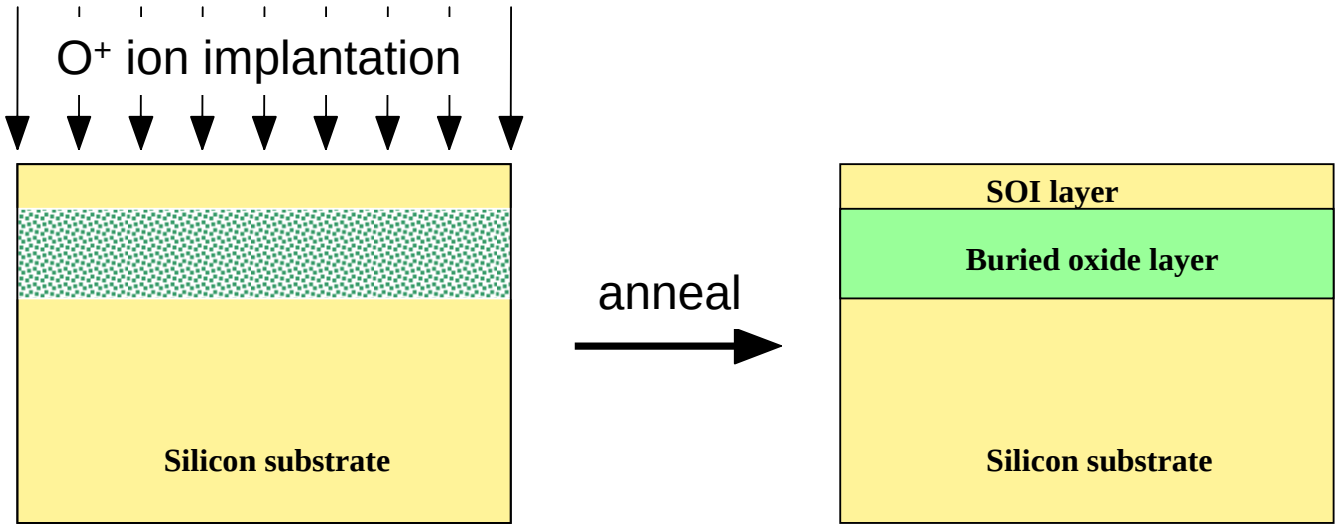
4) Smartcut: (separation by H_2 implantation)

5) ZMR: Zone-melting recrystallization

6) SEG/ELO: Selective epitaxial growth and epitaxial lateral overgrowth

SIMOX

Separation by IMplantation of OXygen



- Deep implantation of oxygen ions into silicon
- Internal oxidation and damage anneal

SIMOX comments

1) demonstrated in 1978 by Izumi et al.

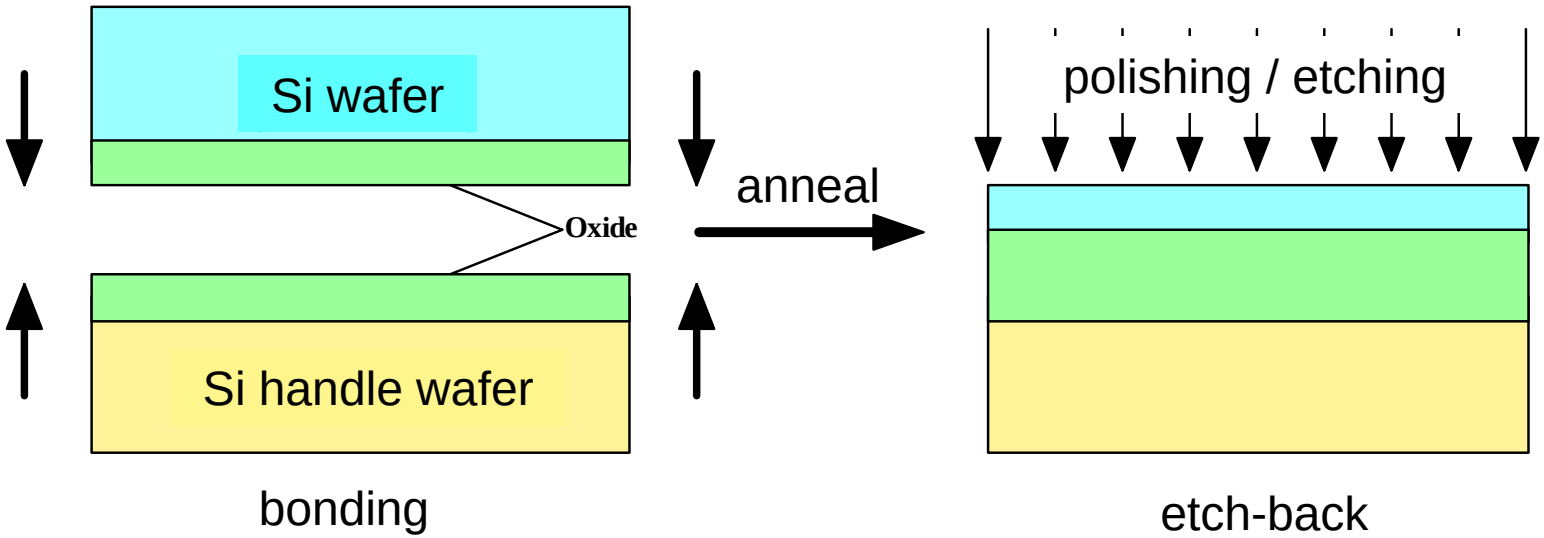
2) dominant SOI technology

3) typical O^+ implant conditions:
   ~2 x 10^{18} cm^{-2} (~1000 times the S/D implant)
   ~150 - 300 KeV
   ~1250-1400C anneal

4) typical numbers:
   BOX ~ 500 nm
   T_{Si} ~ 200 nm

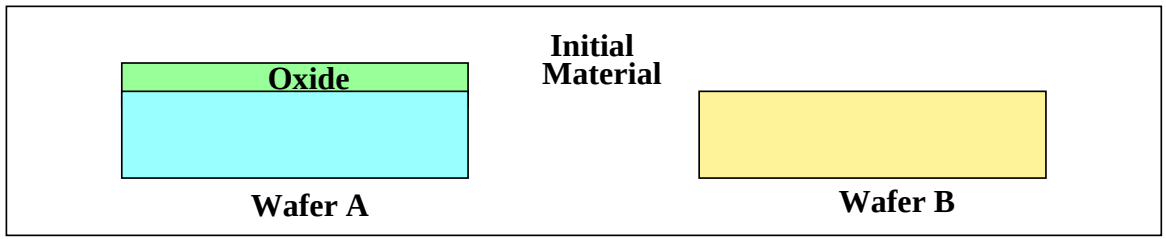
BESOI

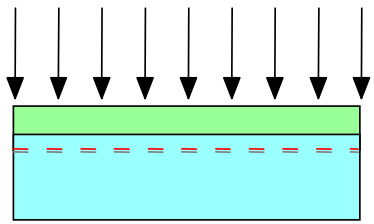
Bonded and Etch-back SOI



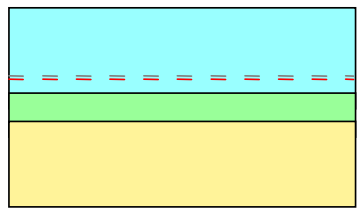
- Two flat oxidized wafers are bonded together and annealed
- The top wafer is thinned down by polishing and etching

“Smart Cut”



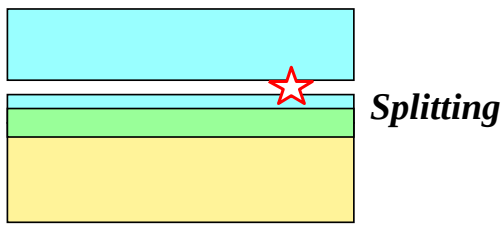


Step 1: Hydrogen implantation into wafer A

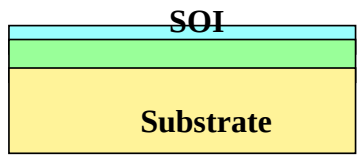


Step 2: Cleaning and bonding of wafer A and B

low temp (400-600C)
high temp (>1000C)

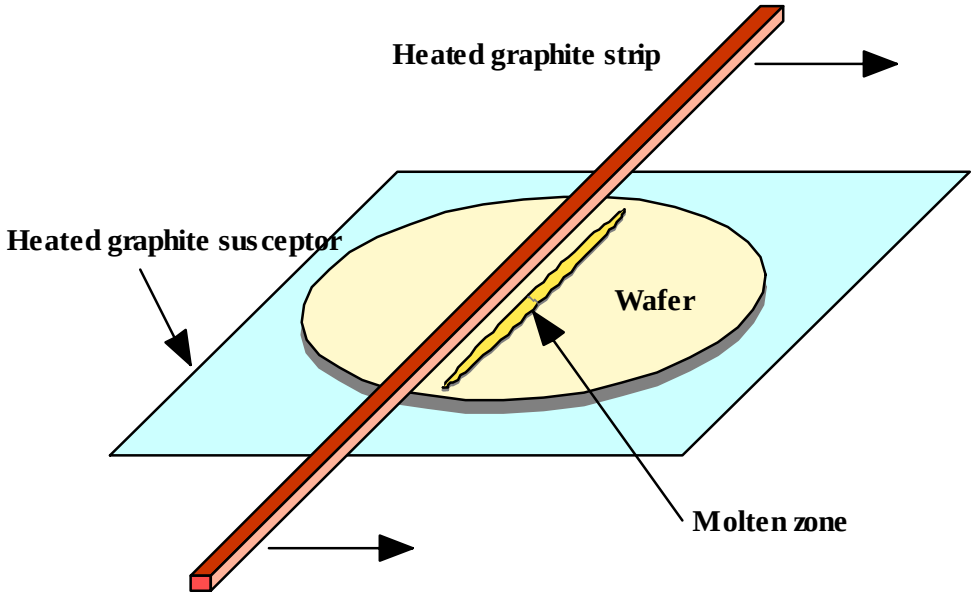


Step 3: Thermal treatment



Step 4: Touch polishing

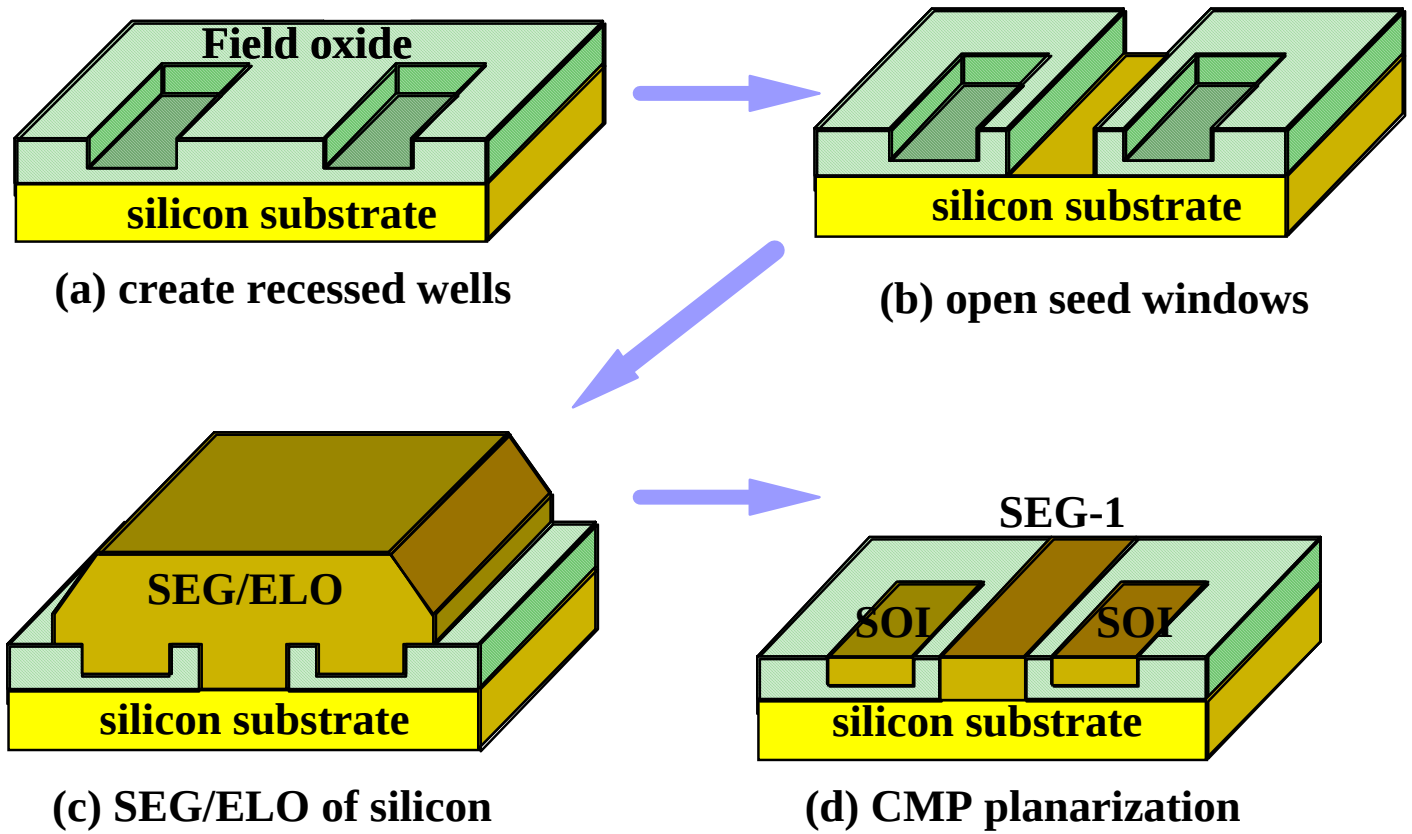
Zone-Melting Recrystallization (ZMR)



- LPCVD amorphous or polysilicon film is deposited on the oxidized silicon wafer

- The film is then recrystallized using e-beam, lasers, or graphite strip heater

SEG/ELO



Prof. G.W. Neudeck, Purdue University

outline

1) Basic structures and SOI advantages

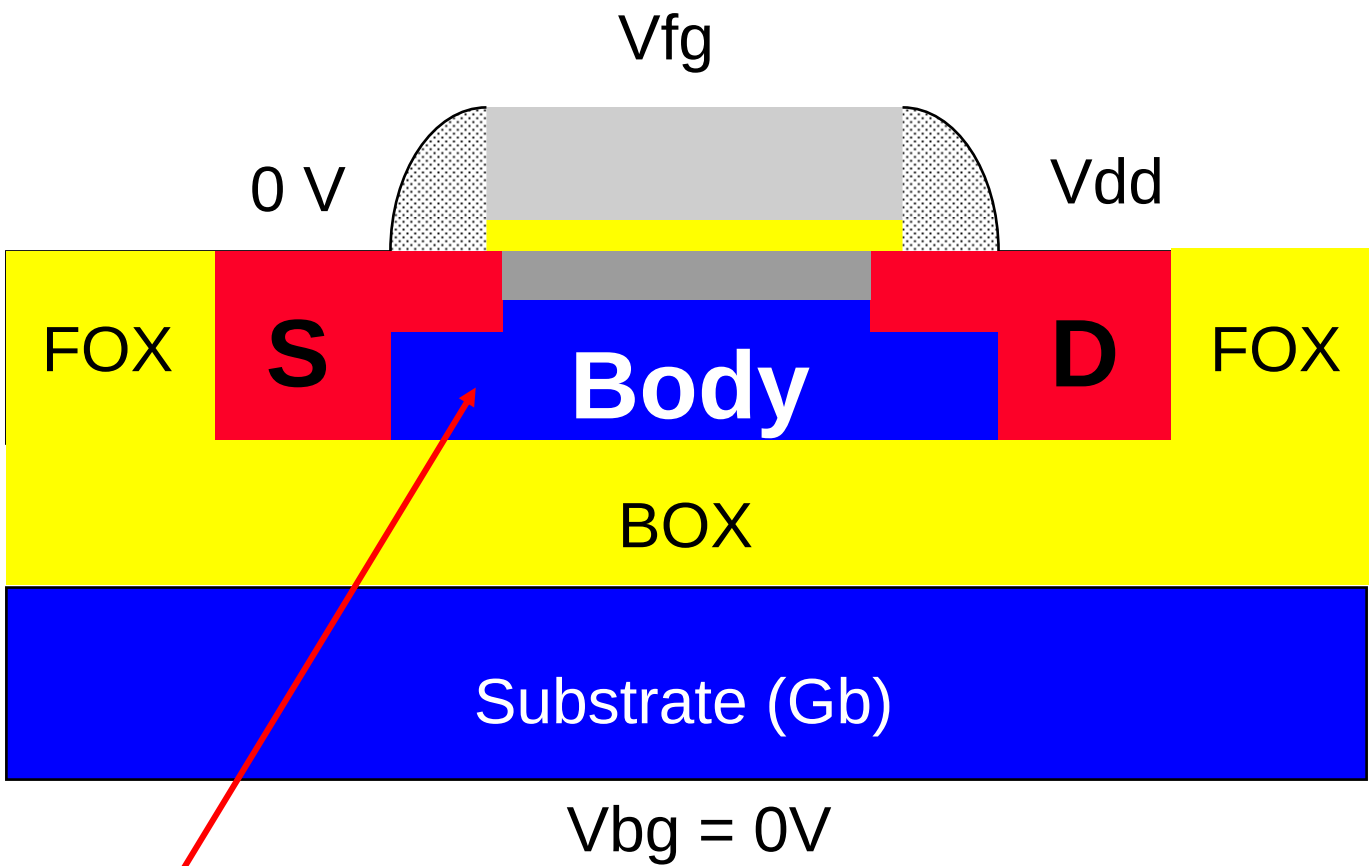
2) SOI film technologies

3) **Partially depleted SOI**

4) Fully depleted SOI

5) Advanced SOI devices

PDSOI



What is V_{bs}?

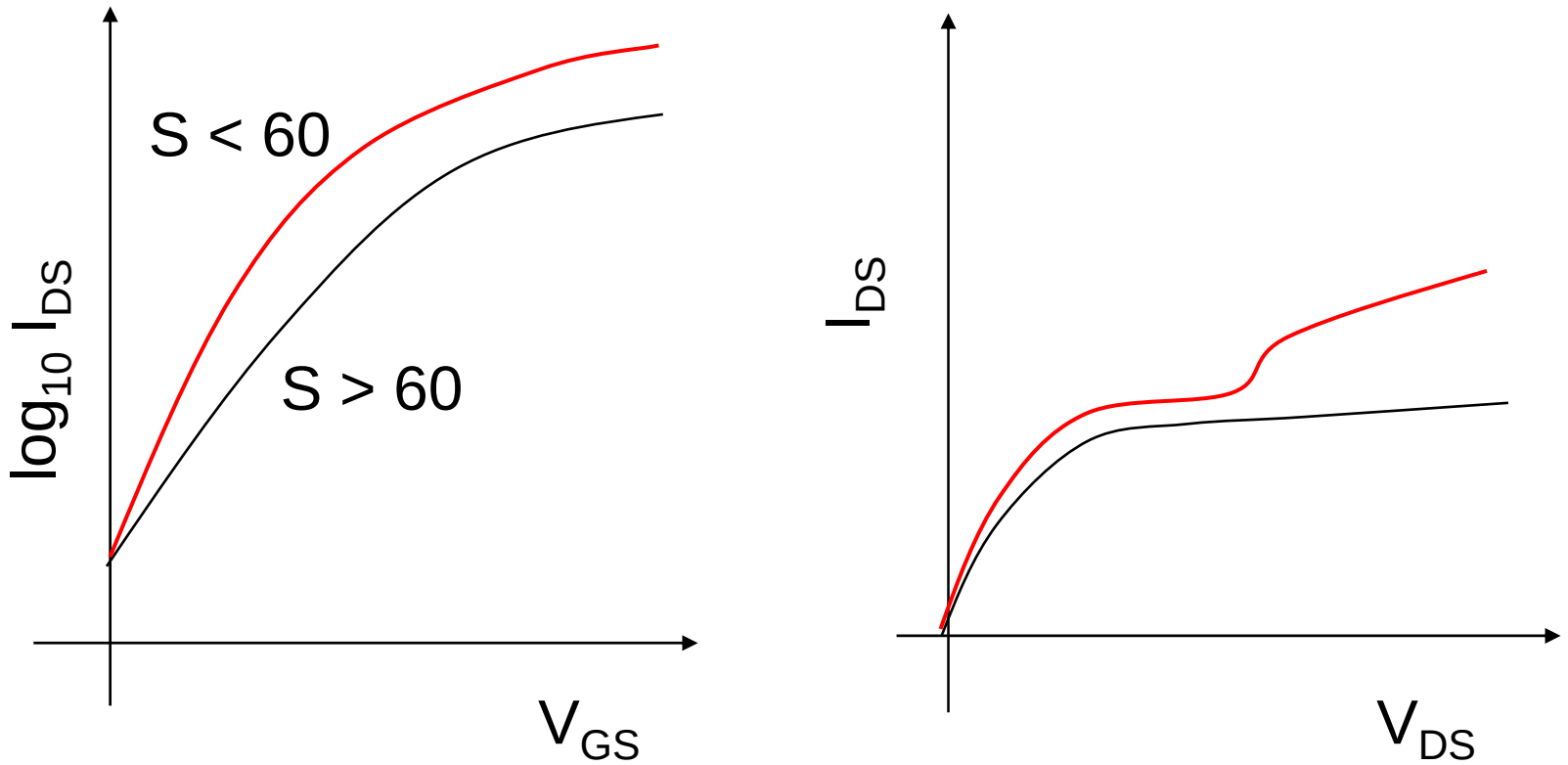
PDSOI: floating body effects

Answer: 0 < Vbs < Vdd

Why does it matter? Because V_T = function(Vbs)

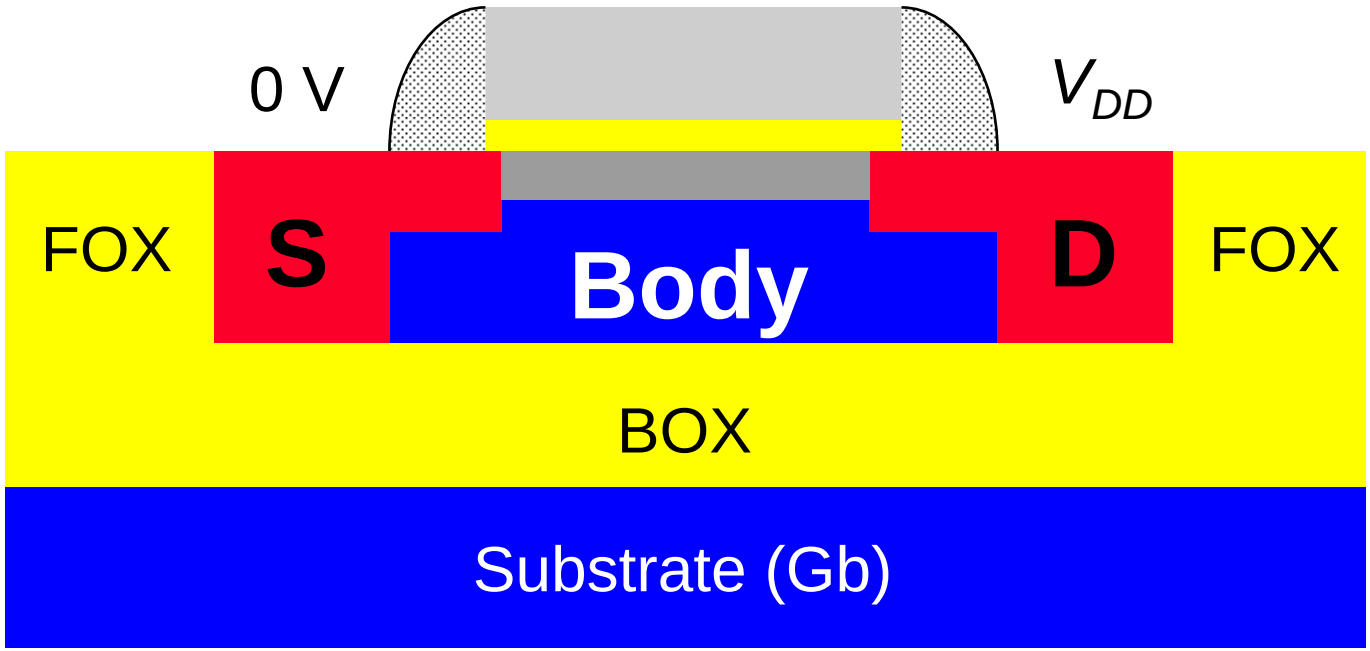
"Kink effect"

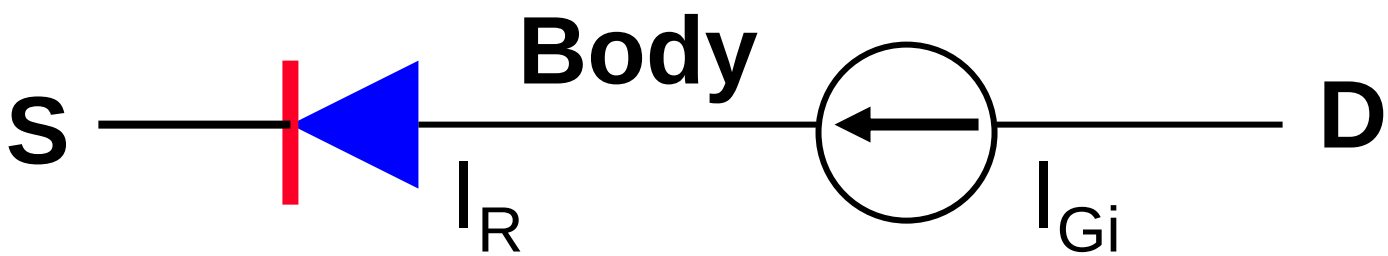
DC Kink effect



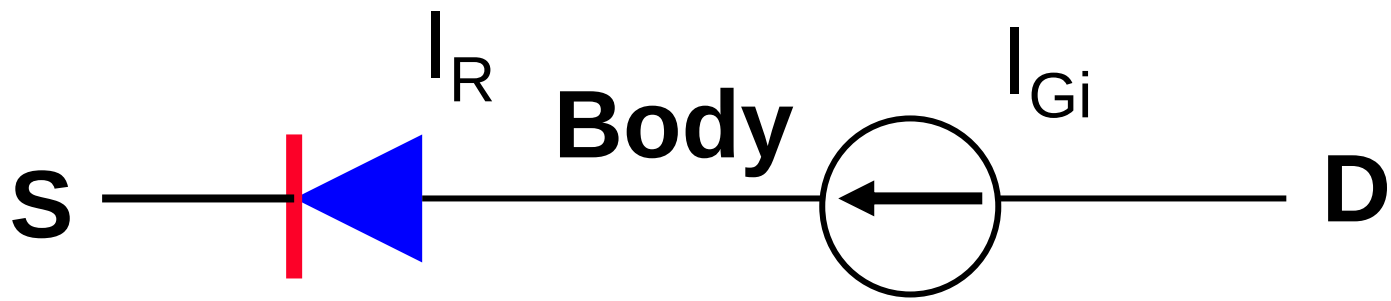
floating body voltage: V_{BS}

What determines the DC body voltage?





floating body voltage (ii)



$$I_R(V_{BS}) = I_{Gi}(V_{DS})$$

$$I_{R0} e^{qV_{bs}/kT} = (M-1) I_{CH}$$

$$(M-1) \sim e^{-B/V_{DS}}$$

- thermal generation
- impact ionization
- junction tunneling
- GIDL

explanation of Kink effect

$$I_{R0} e^{qV_{bs}\,/\,kT} \sim I_{CH}\, e^{-B\,/\,V_{ds}}$$

1) Explains kink in Ids vs. Vds:

Vds ↑ I_{Gi} ↑ Vbs ↑ V_T ↓ Ids ↑

2) Explains kink in Ids vs. Vgs:

Vgs ↑ Ids ↑ I_{Gi} ↑ Vbs ↑ Ids ↑

floating body remedies

1) Raise the temperatures (increases I_R which reduces Vbs)

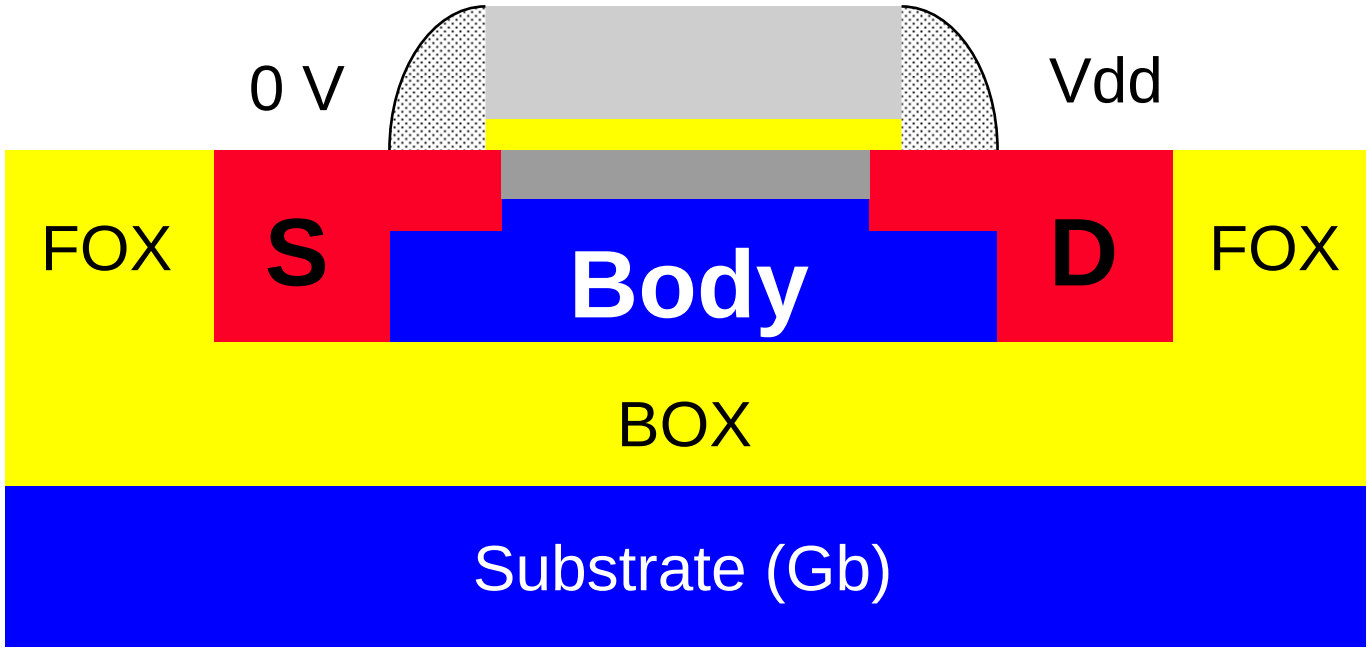
2) Body ties and links

3) Implant damage to reduce lifetime

4) SiGe source to increase diode current

ac floating body effects

What determines the AC or transient body voltage?



Answer: capacitive coupling to the bulk

ac floating body effects voltage

The equivalent circuit of the MOSFET shows capacitive coupling to the body through the:

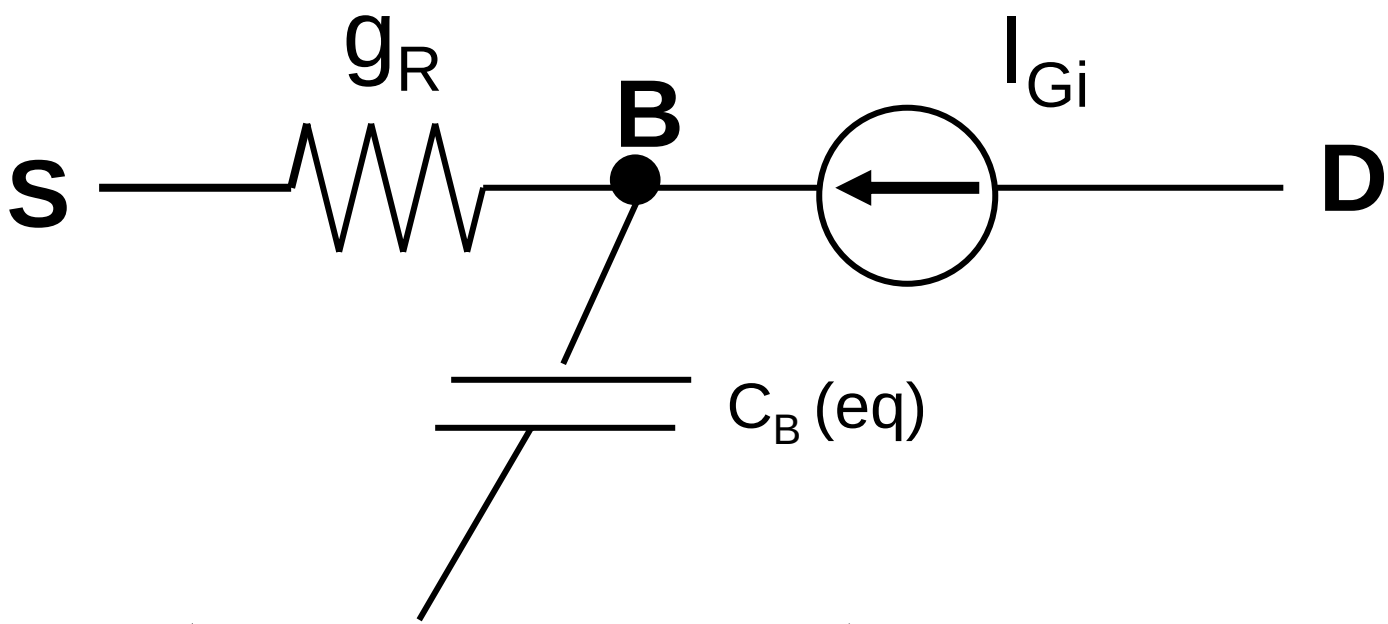
1) gate

2) drain

3) source

ac floating body voltage

Small signal ac conditions:

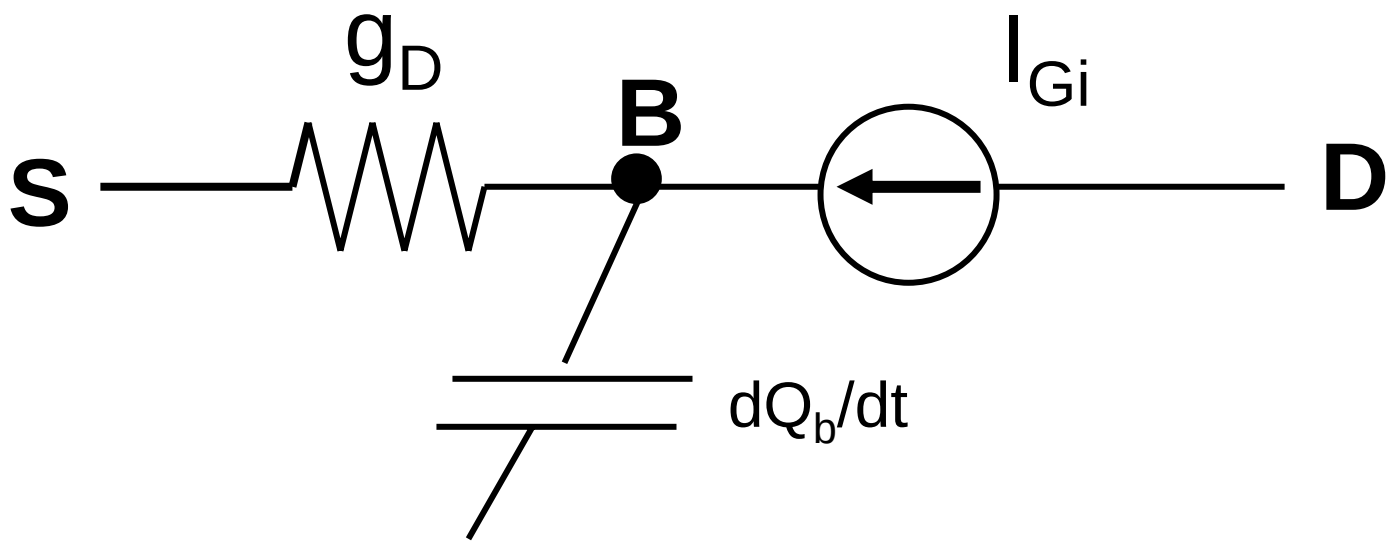


$$V_{bs}\left(g_D + j\omega C_B(eq)\right) = I_{Gi}(V_{DS})$$

s.s. equivalent circuit is frequency dependent!

ac floating body voltage (ii)

transient conditions:



$$\frac{dQ_b}{dt} = C_{BGf}\frac{dV_{Gf}}{dt} + C_{BD}\frac{dV_{DS}}{dt} + C_{BS}\frac{dV_{BS}}{dt}$$

Changing voltage at any terminal affects Vbs!

ac floating body voltasge (iii)

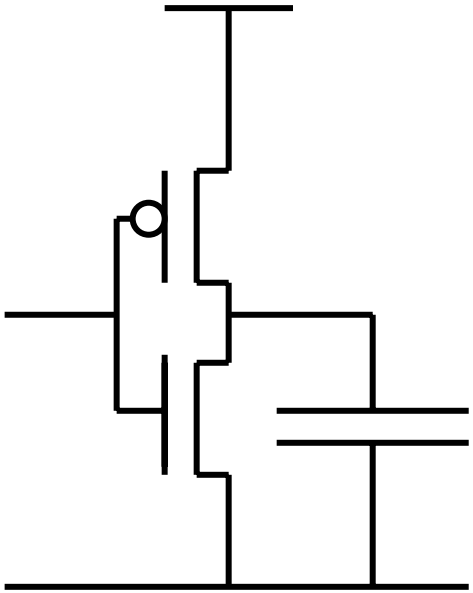
$$V_{bs}(t)$$

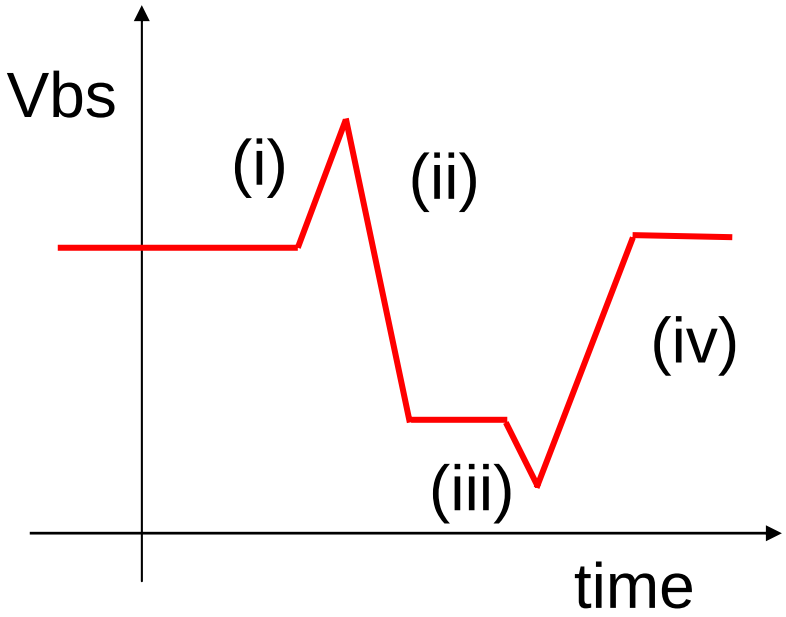
1) fast component due to capacitive coupling

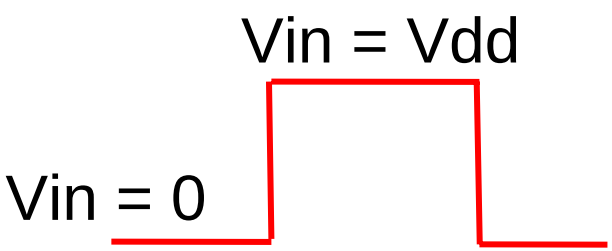
2) slow component due to generation/recombination

3) dynamic floating body effects can benefit circuits

ac floating body example







i) gate pull-up of body
ii) drain pull-down
iii) gate pull-down of body
iv) drain pull-up

ac floating body summary

1) partially depleted SOI MOSFETs are bulk-like except for floating body effects

2) floating body effects can be beneficial but….

3) they need to be modeled and controlled

outline

1) Basic structures and SOI advantages
2) SOI film technologies
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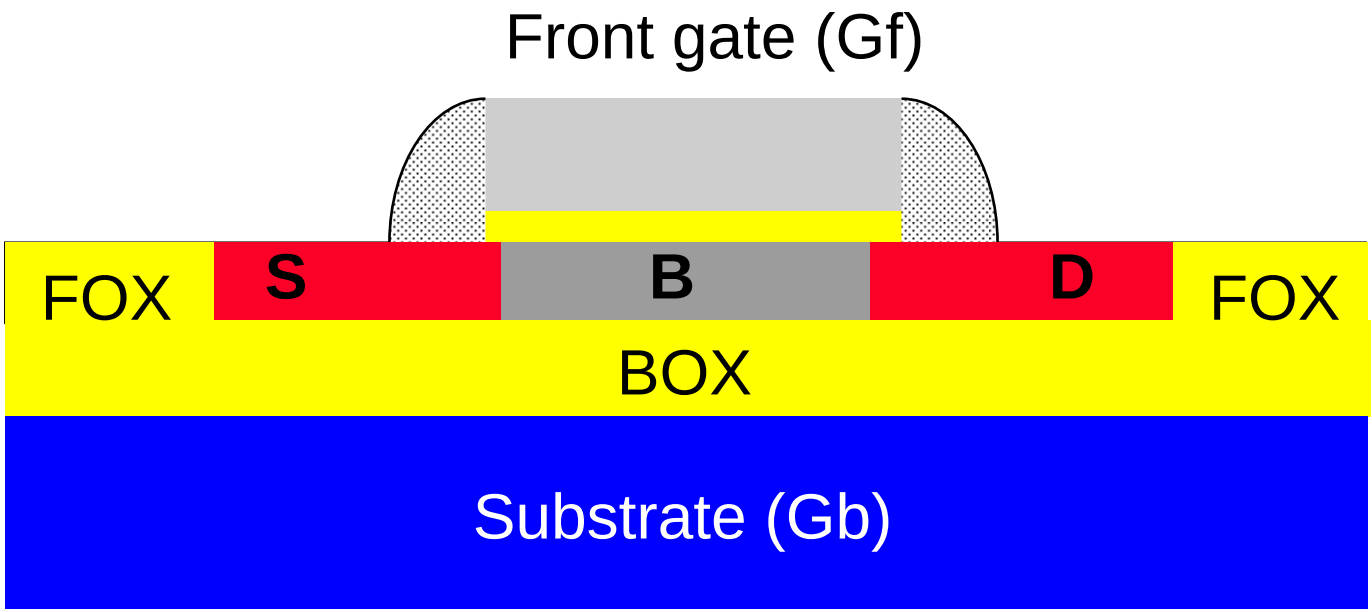
4) **Fully depleted SOI**
5) Advanced SOI devices

fully depleted (FD) SOI



Fully depleted (FD) body

FDSOI characteristics

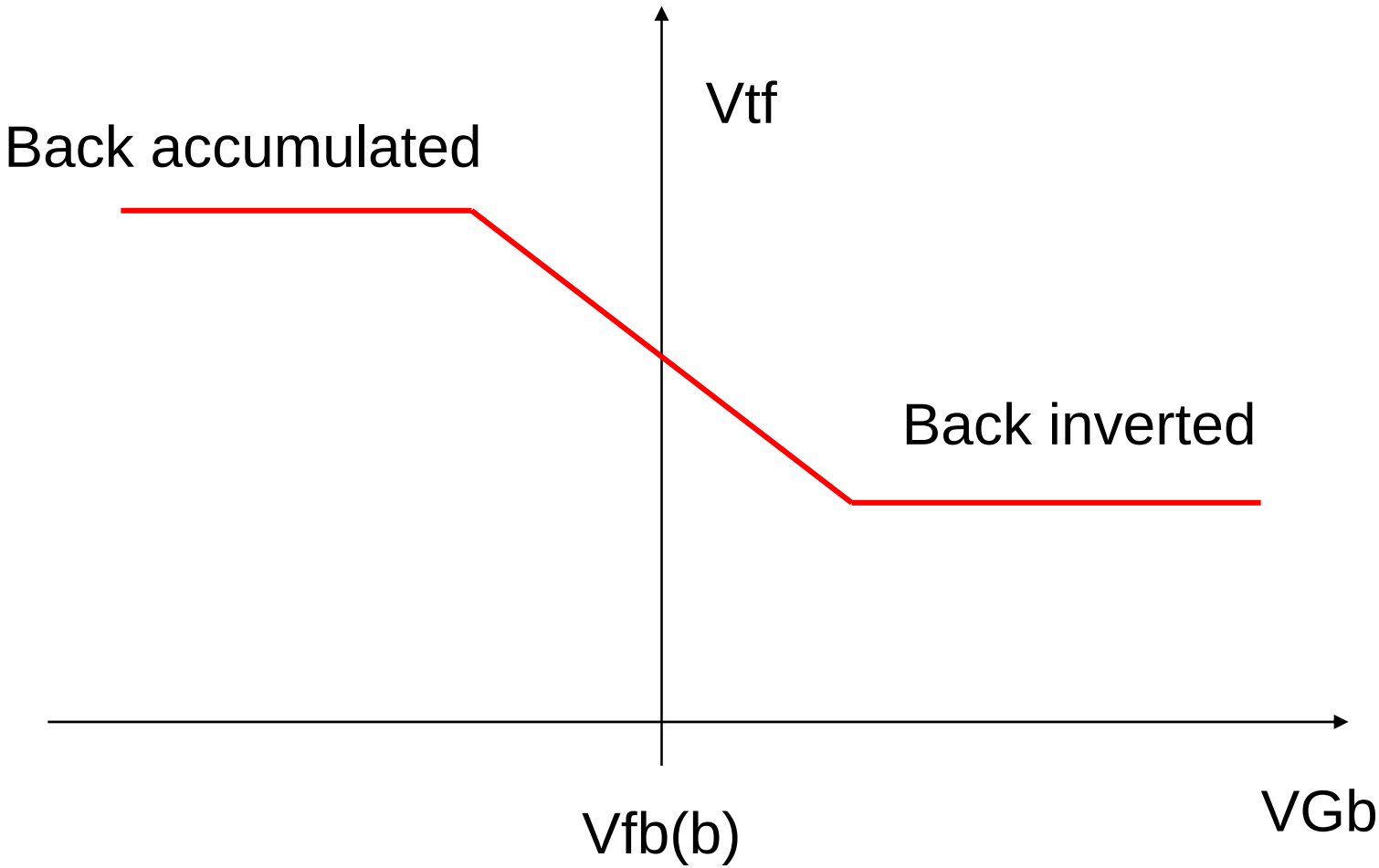
1) FD SOI MOSFETs display small floating body effects

2) But……Vtf = function (VGb)
(front and back gates are coupled)

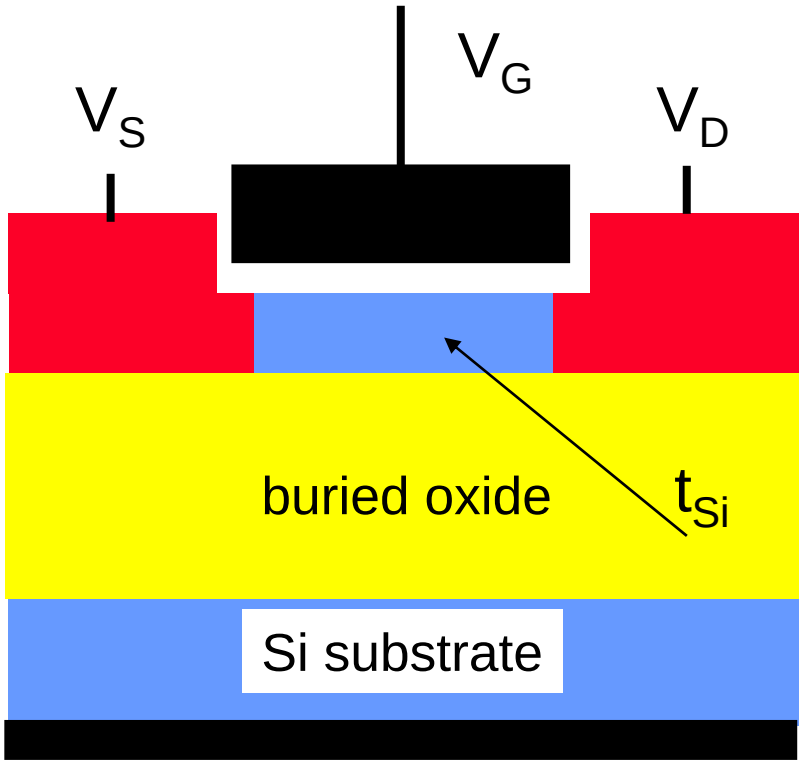
3) FD SOI MOSFETs display ideal subthreshold swing, *S* (60 mV / decade)

as a result, V_T can be lower, speed higher

FDSOI: effect of back gate



FDSOI: subthreshold



Why is *S* ideal?

$$I_{ds} \propto e^{q\varphi_S / kT}$$

$$\varphi_S = \frac{V_G}{m} = \frac{V_G}{\left(1 + \frac{C_2}{C_{ox}}\right)}$$

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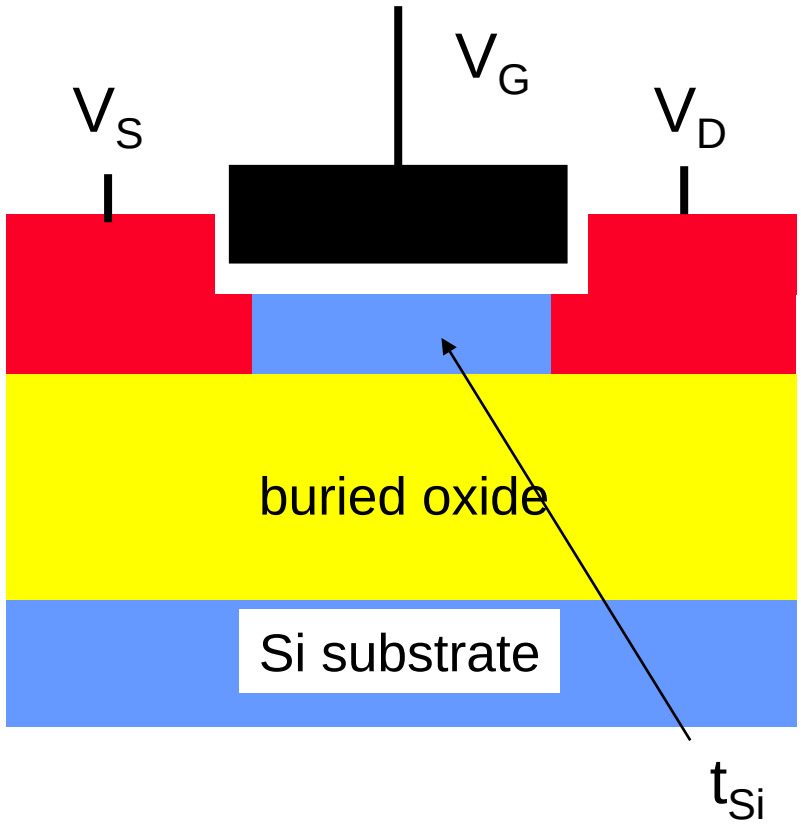
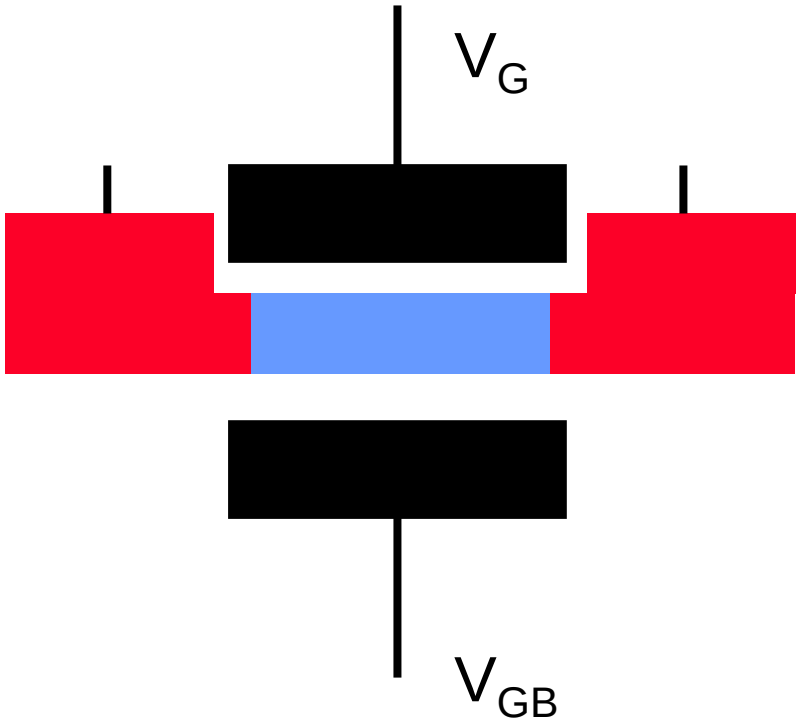
single gate SOI

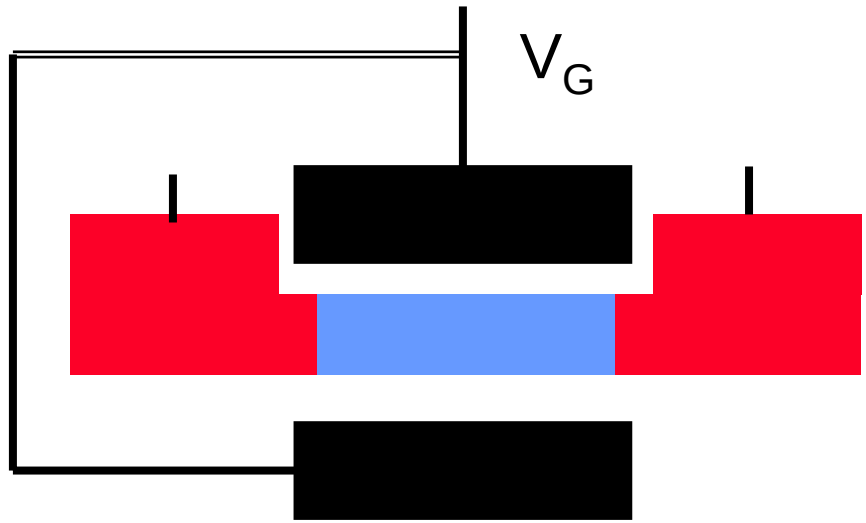


double gate SOI

(b) ground plane



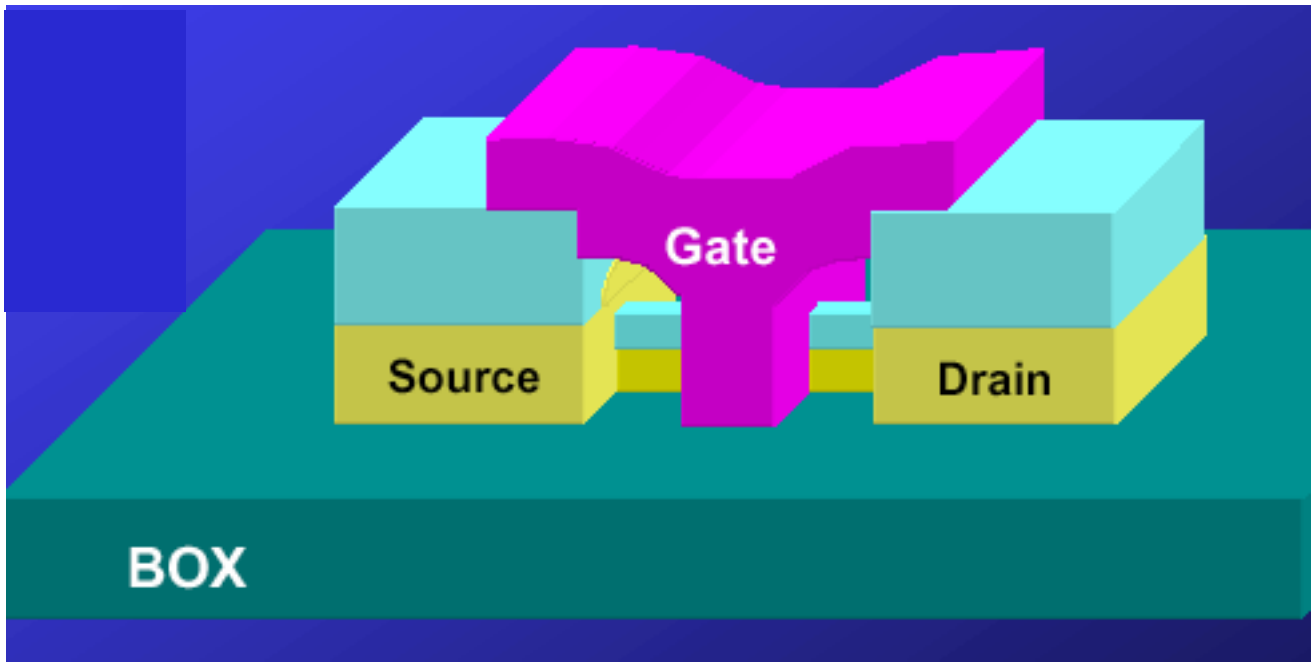
(c) double gate



H-S Philip Wong, et al., IEDM, 1998

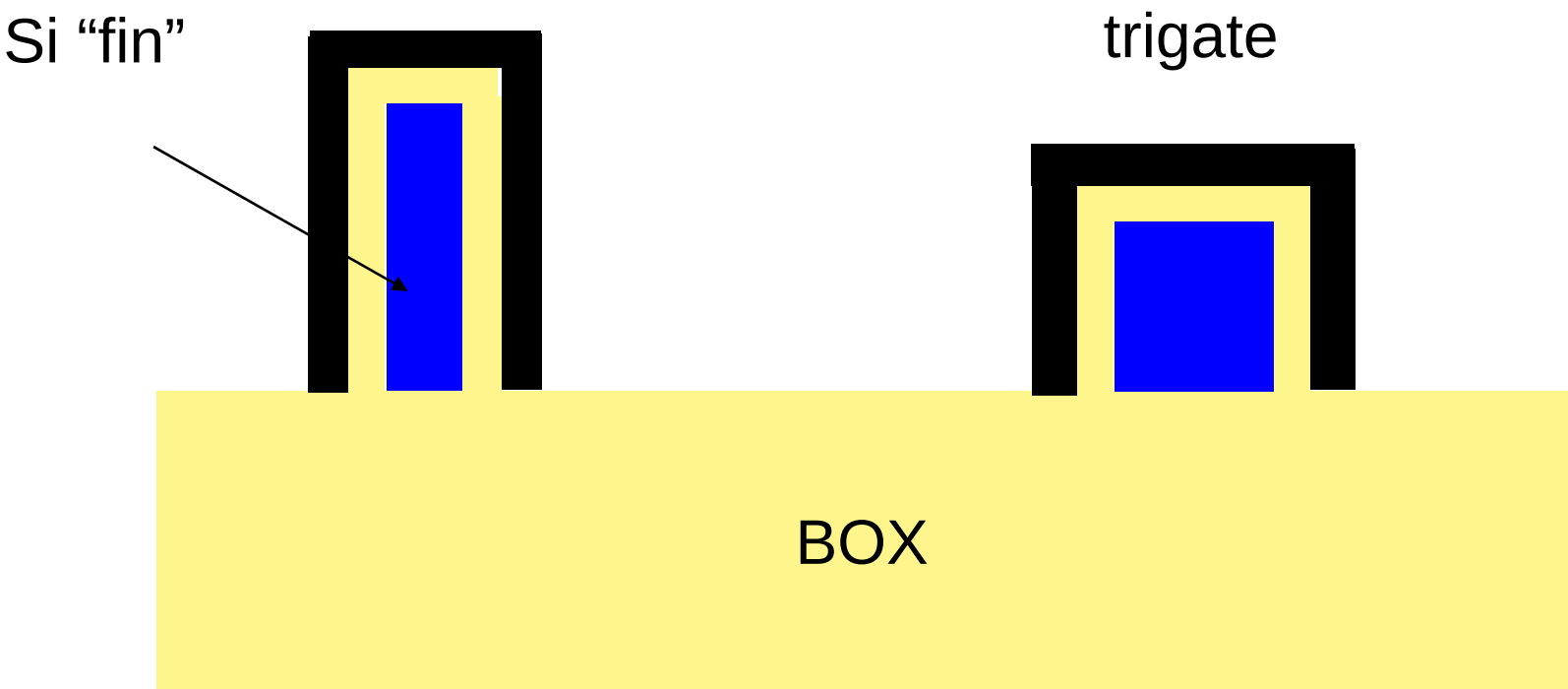
Ultra-thin bodies → good scalability → but high V_t

FinFET



Sub-50 nm FINFET: PMOS, Huang et al, 1999 IEDM

FinFET vs. trigate



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