# Introduction to compact modeling

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# Outline

- What is a compact model
- Why do we need compact models
- Requirements on a compact model
- Building the core long channel compact model
- Adding additional effects: short channel effects, velocity saturation, noise, NQS
- Examples: Finfet, low effective mass material modeling
- Good compact modeling practices
- Summary

# What is a compact model

- Computationally efficient description of the terminal properties of a device as a function of terminal voltages.

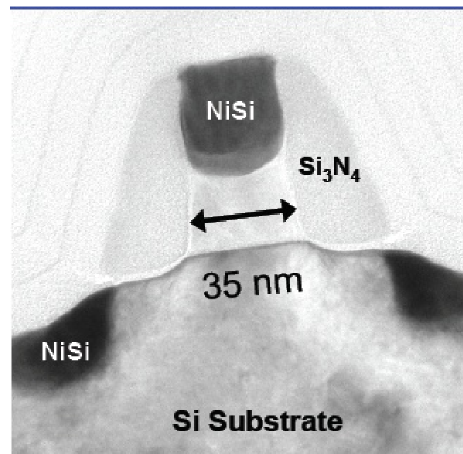
**[{I}, {Q}] = f(Vg, Vd, Vs, Vb)**

- The compact model is implemented inside a circuit simulation engine.

# Two worlds

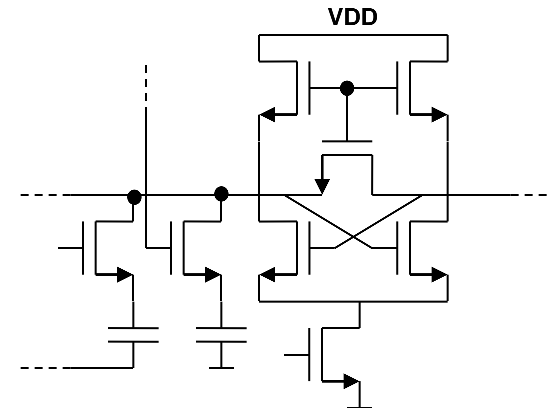
## Technology / process development

- The process of making transistors, resistors, capacitors…etc, through a series of complex lithographical and chemical processes.

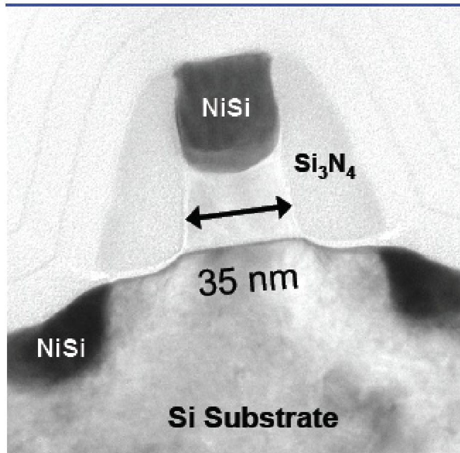


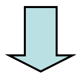

## IC design

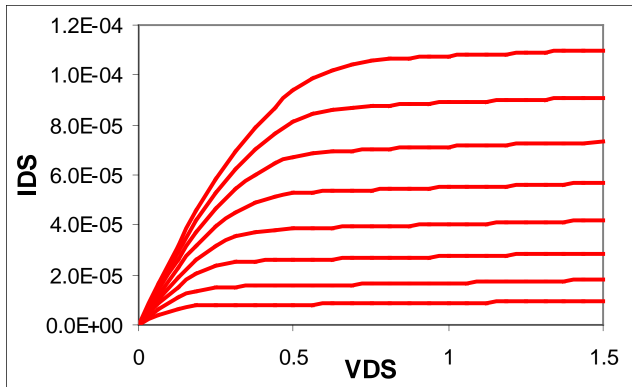
- Design of an electrical network consisting of transistors, resistances, capacitances… etc, to perform a specified task.

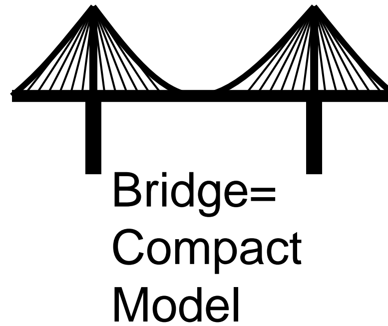


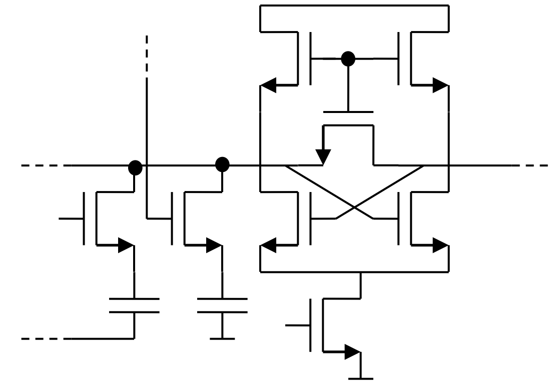
# Connecting the two worlds





Design engineers use those transistors build logic circuits that perform specific functions.

# Toy compact model: Examination

- The technology parameters are μ, Cox, Vth.
  - These are extracted based on experimental data.
  - The technology parameter set is what varies between technologies making the compact model applicable to different technologies.
- The instance parameters L and W, which are used by the designer.
- Applied bias Vgs, Vds, vbs

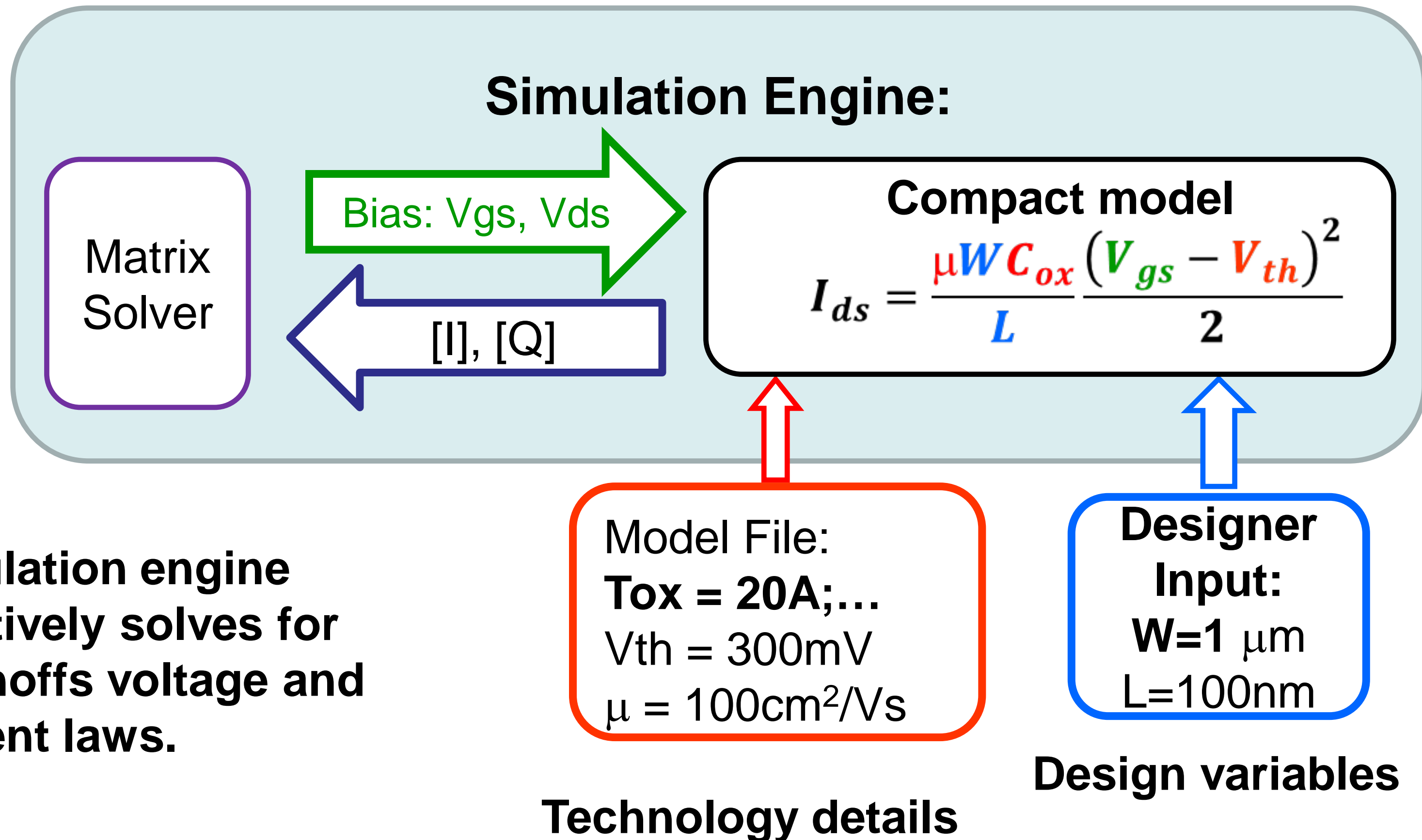
**Linear region**

$$I_{ds} = \frac{\mu W C_{ox}}{L} \frac{\left(V_{gs} - V_{th} - {V_{ds}}/{2}\right) V_{ds}}{2}$$

**Saturation region**

$$I_{ds} = \frac{\mu W C_{ox}}{L} \frac{\left(V_{gs} - V_{th}\right)^2}{2}$$

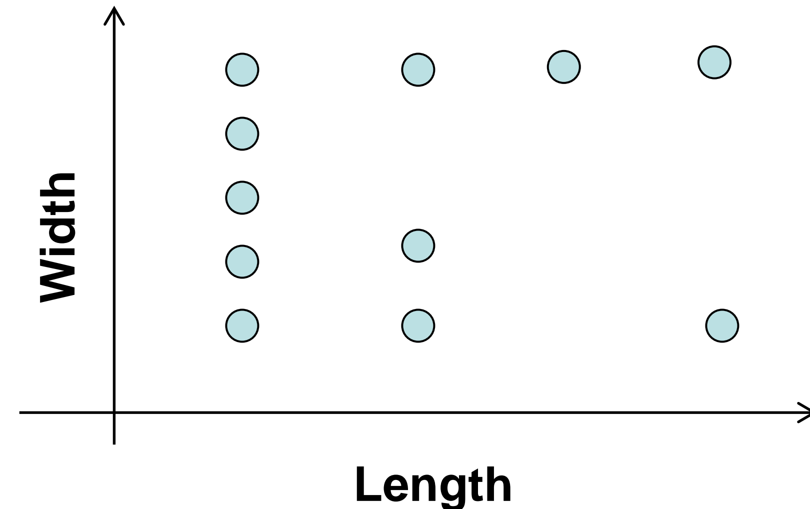
# A simplified view of circuit simulation




- **Simulation engine iteratively solves for Kirchoffs voltage and current laws.**

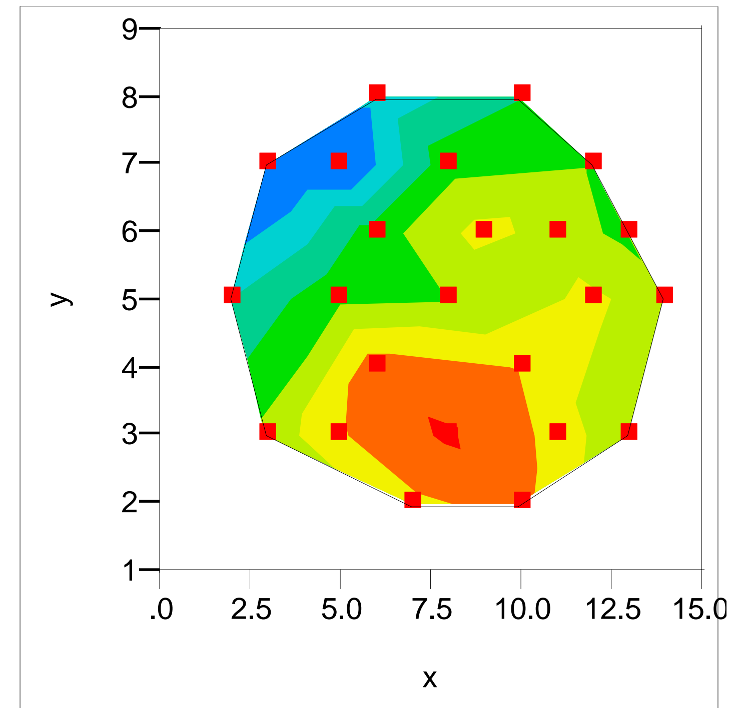
# Model file characterization

- Technology characterization i.e. model files are extracted by using data at multiple widths and lengths based on **median** device data.
- Doping, oxide thickness, mobility, series resistance etc are fixed.
- Usually at two temperatures.



# Compact modeling requirements: I

- Process variations occur within a die, between dies.
- A circuit must be designed so that it “functions” even when there is variation in the transistor characteristics.
  - Example: Gate length variation.
- <u>A compact model must produce accurate result when its parameters are varied i.e. it must be physically based</u>



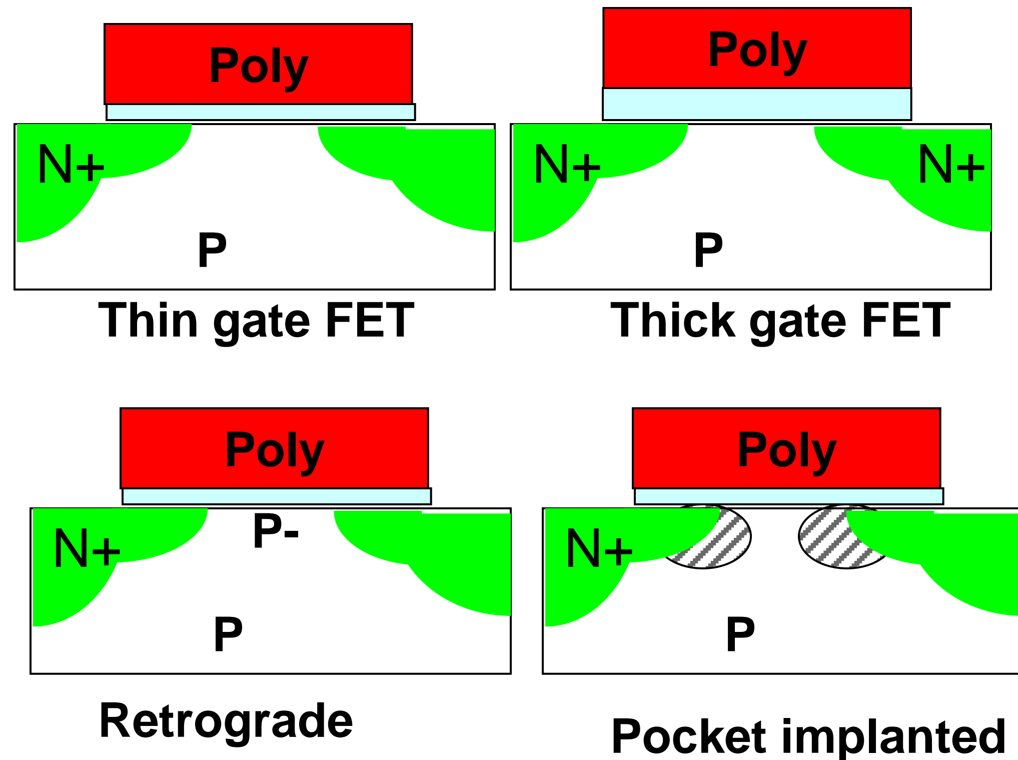

**Drive current variation across a wafer.**

# Problems with unphysical models

- An unphysical model for any of the physical quantities makes the other quantities unphysical also.
  - $I = Q * \mu * E$.
  - If Q is modeled incorrectly w.r.t the bias then mobility has to become unphysical to match the measured current.
- Regional models are other reasons models become unphysical.
  - Need smoothing functions between regions.
- Severe over-design or under-design when predictions due to process variations are incorrect
  - Excessive costs
  - Poor yield

# Compact model requirement:II

- Every foundry / company makes MOSFET transistors that are different.
- Even within a foundry or company there are different types of transistors: thick gate oxide, thin gate oxide process etc.
- <u>A compact model must not be technology dependent.</u>



# Compact model requirement: III

- Speed of evaluation.
  - Circuit simulation speed and accuracy is critical for timely design.
    - Avoid expensive math functions.
    - Avoid Internal nodes, if possible.
      - If internal nodes are used, then let the circuit simulator solve for the quantities on the node
    - Reuse computed quantities and intermediate variables
- Model stability and convergence is important.
  - continuous functions, no singularities
  - Model evaluations that result in 0/0, but have a physical limit need to be carefully dealt with.
  - Consistent derivatives
- Accurate modeling of temperature dependence

# The compact model challenge

POISSON

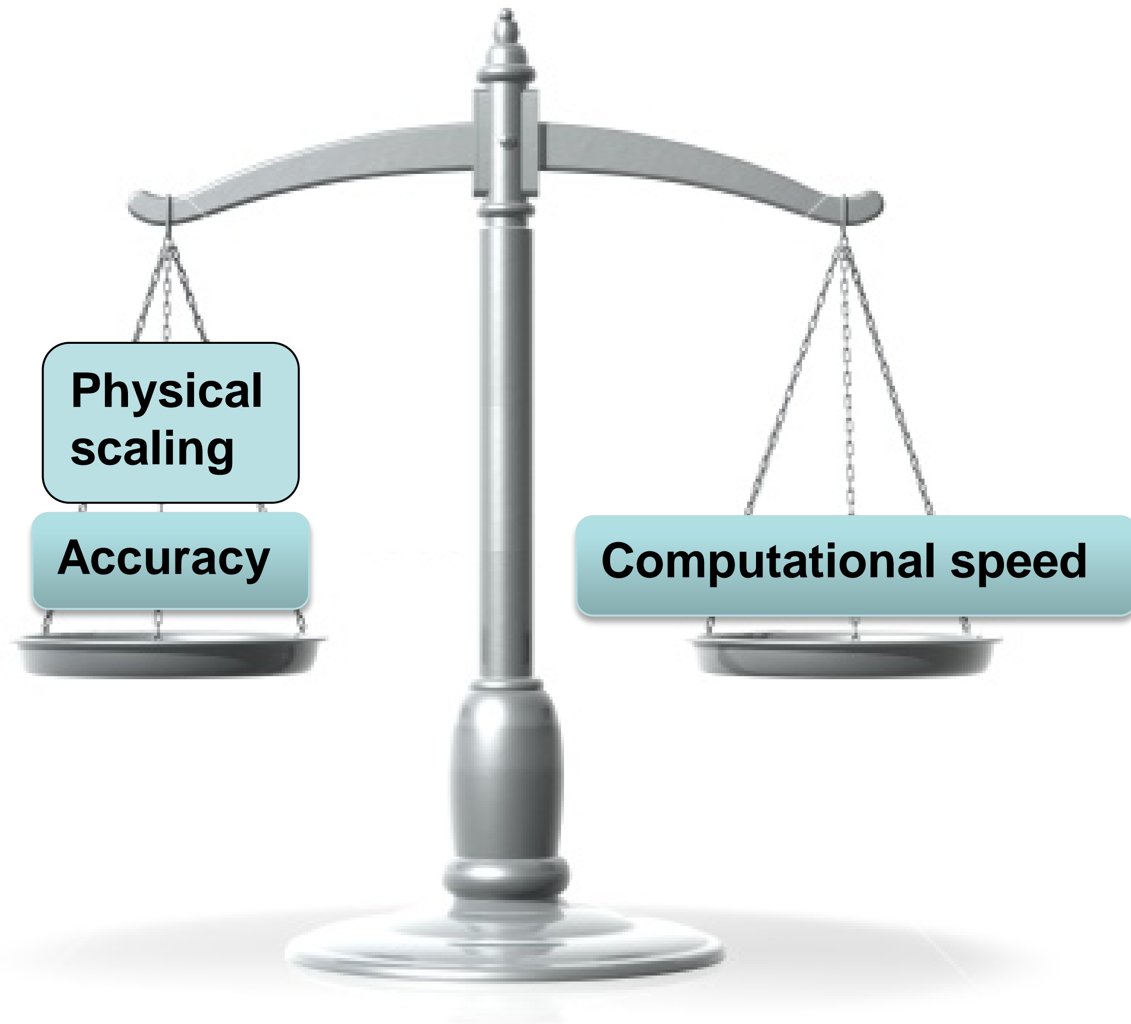
STOCHASTIC LLG

SCHRODINGER

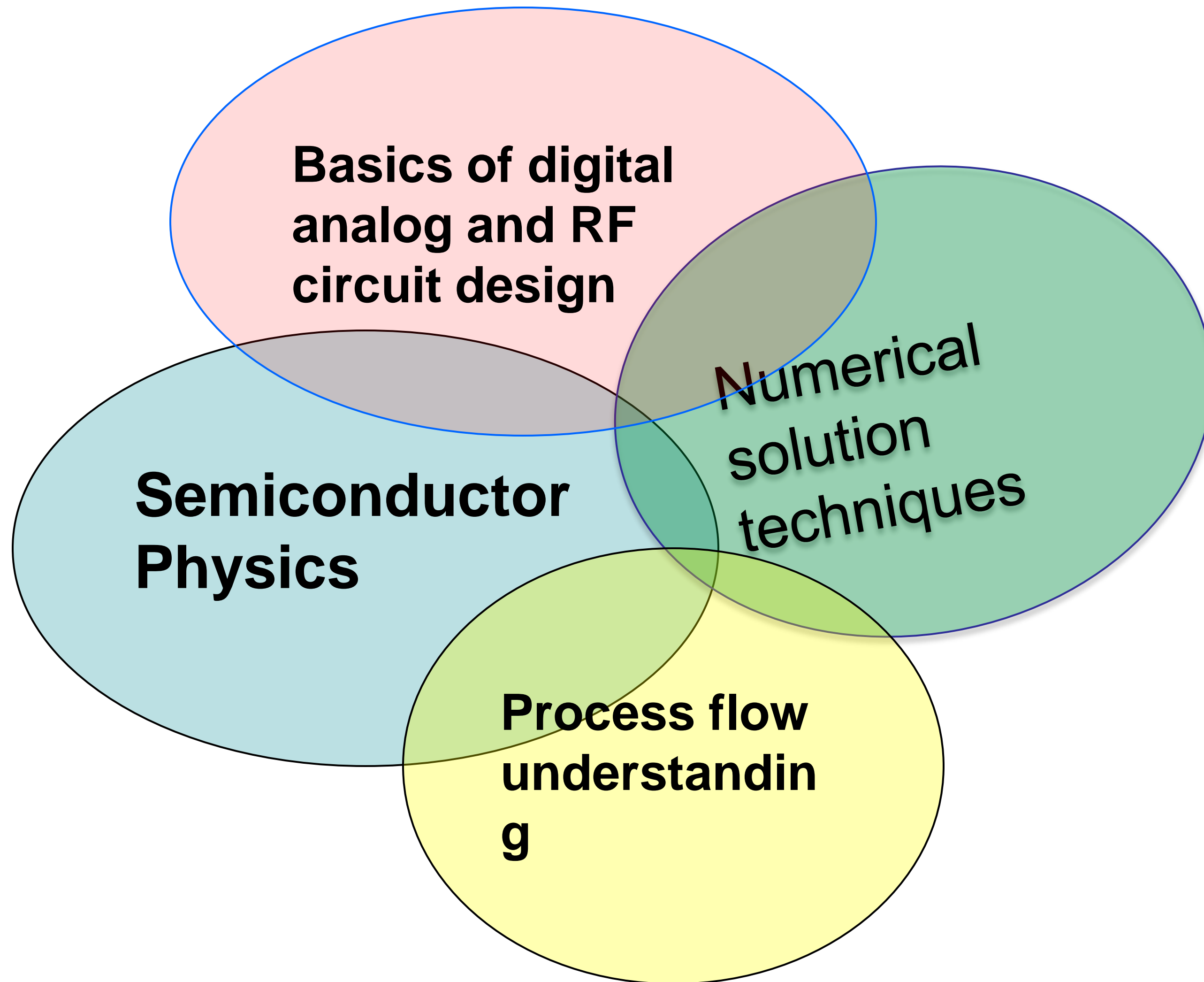
Boltzmann Transport

Compact model

# Striking the right balance



# Developer skill requirements



# Types of compact models

- Macromodels
  - Use of circuits to mimic device behavior.
- Table look up model
  - {I,Q} = F(L, W, T, VD, VG, VD, VB, more)
  - Limited value in early device evaluation.
- Physics based analytical model
  - Computationally efficient
  - Physically based
  - Technology independent

# Building the core compact model: Planar MOSFET

- MOSFETs are 2-D devices, hence need to solve for the potential based on Poisson's equation

$$\frac{\partial^2 \phi}{\partial y^2} + \frac{\partial^2 \phi}{\partial x^2} = -\frac{q}{\varepsilon_{Si}}\left(p - n + N_d^+ - N_a^-\right)$$

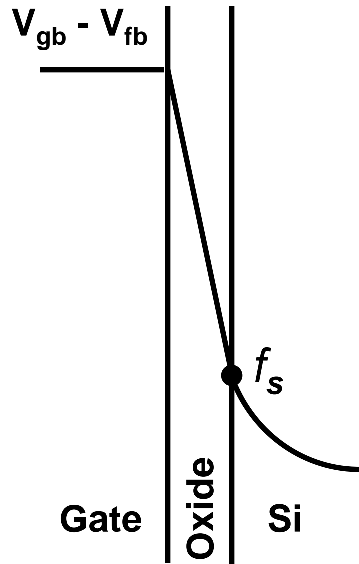
  - Non – trivial to make approximations to formulate a compact model.
- Gradual channel approximation: In a long channel MOSFET the variation of the lateral field (channel direction) is much less than the variation in the perpendicular (to the channel) direction.

$$\frac{d^2 \phi}{dy^2} = -\frac{q}{\varepsilon_{Si}}\left(p - n + N_d^+ - N_a^-\right)$$

  - Even in a long channel this assumption is true only upto the pinch off point.

**Identify ways to reduce PDEs to ODE**

# Solving for $\phi_s$




1-D potential equation
$$\frac{d^2\phi}{dy^2} = -\frac{q}{\varepsilon_{Si}}\left(p - n + N_d^+ - N_a^-\right)$$

**Boundary conditions:**

1. Vgb – Vfb on the gate side
2. Potential goes to zero at some deep in the bulk.

Vfb is the gate voltage needed to restore flat-band condition.

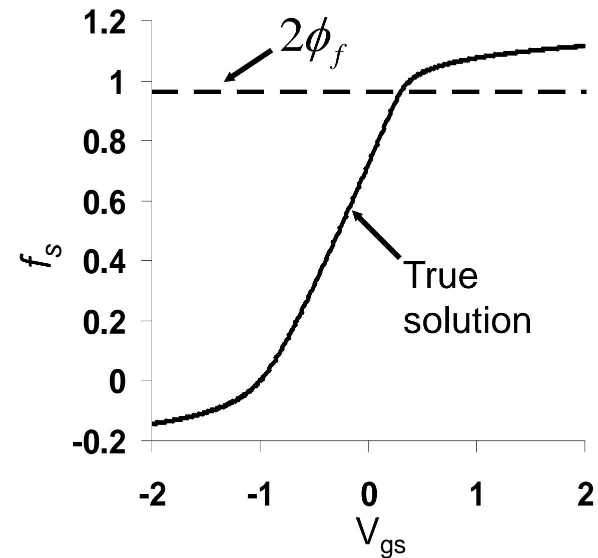
# $\phi_s$ Approaches

- **Pinned (BSIM3/4):**

$$\phi_s = 2\phi_f - V_{bs}$$

$$\phi_f = \frac{KT}{q}\ln\left(\frac{N_{dop}}{ni}\right)$$

Simple, but valid only at onset of inversion




- **Non-pinned**

$$\frac{(V_{gb} - V_{fb} - \phi_s)^2}{\gamma^2} = V_t \exp\left(\frac{V_{bd} - 2\phi_f}{V_t}\right)\left[\exp\left(\frac{\phi_s}{V_t}\right) - 1\right] + V_t\left[\exp\left(\frac{-\phi_s}{V_t}\right) - 1\right] + \phi_s$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{ox}}$$

Implicit equation, but valid from accumulation to depletion to inversion.

**Solving implicit equation yields continuous solution valid over all regions → no need for regional solution**

# Analytical modeling approaches

- Threshold voltage approach: BSIM3/4[1]
  - Surface potential is constant or pinned above Vgs = “Vth”.
  - Below Vth, the current is exponentially related to Vgs.
- Qi, inversion charge approach: EKV[2], BSIM6[1]
  - The inversion charge in the channel is solved as the state variable.
- Surface potential based: PSP[3], MOS11[4], HiSim[5]
  - Surface potential is the state variable.

# Basic MOSFET Model Equations

Drift

Diffusion

(1) Continuity: $$I_{channel} = -\frac{W}{L}\int_{\phi_{ss}}^{\phi_{sd}} \mu\left(Q_{inv}\frac{d\phi_s}{dx} - v_t\frac{dQ_{inv}}{dx}\right)\mathrm{dx}$$

(2) Gauss' law $$Q_{gate} = C_{ox}\left(V_{gb} - V_{fb} - \phi_s\right)$$

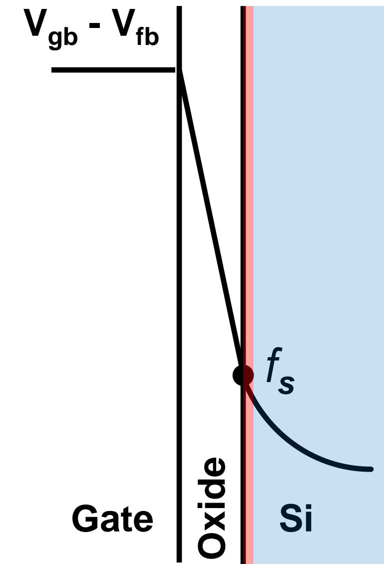
(3) Charge cons: $$Q_{inv} = Q_{gate} - Q_{body}$$

- $Q_{inv}$ is the integrated electron concentration along the depth
- $Q_{body}$ is the integrated depletion and hole concentration along the depth.
- Neither $Q_{inv}$ nor $Q_{body}$ are simple analytic expressions.

# Compact modeling of $Q_{inv}$ and $Q_{body}$

- Charge sheet model approximation [6]:
  - Inversion charge is contained in a negligibly thin sheet at the surface.
  - Since the thickness is negligibly small, the drop across that layer is also negligibly small.
  - Hence, $Q_{body}$ can be modeled similar to depletion region in a diode

$$Q_{body} = \sqrt{2q\varepsilon_{Si}N_A}\sqrt{\phi_s}$$




**Look at "equivalent" systems for inspiration.**

# Basic MOSFET Model Equations

Drift | Diffusion

(1) Continuity: $$I_{channel} = -\frac{W}{L}\int_{\phi_{ss}}^{\phi_{sd}} \mu\left(Q_{inv}\frac{d\phi_s}{dx} - v_t\frac{dQ_{inv}}{dx}\right)\mathbf{dx}$$

(2) Gauss' law: $$Q_{gate} = C_{ox}(V_{gb} - V_{fb} - \phi_s)$$

(3) Depletion approx.: $$Q_{body} = \sqrt{2q\varepsilon_{Si}N_A}\sqrt{\phi_s} = C_{ox}\gamma\sqrt{\phi_s}$$ *

(4) Charge cons: $$Q_{inv} = Q_{gate} - Q_{body}$$

* **Not accurate near flatband and accumulation**

# Channel current

- Assuming mobility is a constant…

$$I_{drift} = \frac{\mu W C_{ox}}{L}\left((V_{gb} - V_{fb})(\phi_{sd} - \phi_{ss}) - \frac{({\phi^2}_{sd} - {\phi^2}_{ss})}{2} - \frac{2}{3}\gamma\left({\phi^{\frac{3}{2}}}_{sd} - {\phi^{\frac{3}{2}}}_{ss}\right)\right)$$

$$I_{diff} = \frac{\mu W C_{ox}}{L}\left(v_t(\phi_{sd} - \phi_{ss}) + v_t\gamma\left(\sqrt{\phi_{sd}} - \sqrt{\phi_{ss}}\right)\right)$$

$$I_{channel} = I_{drift} + I_{diff}$$

Analytical model for the channel current, but circuit simulators also need compact analytical expressions for charge on all the terminals to compute all the capacitances.

# Charge modeling

**Gate node charge:** $$Q_G = W\int_0^L Q_{gate}\,dx = W\int_{\phi_{ss}}^{\phi_{sd}} Q_{gate}\frac{dx}{d\phi}\,d\phi$$

**Bulk node charge:** $$Q_B = W\int_{\phi_{ss}}^{\phi_{sd}} Q_{bulk}\frac{dx}{d\phi}\,d\phi$$

- The charge associated with the drain and source node is calculated by partitioning the total inversion charge.
  - Trivial at vds = 0
  - At non-zero drain bias the partitioning is achieved by the use of Ward-Dutton partition scheme [7]

# Charge modeling

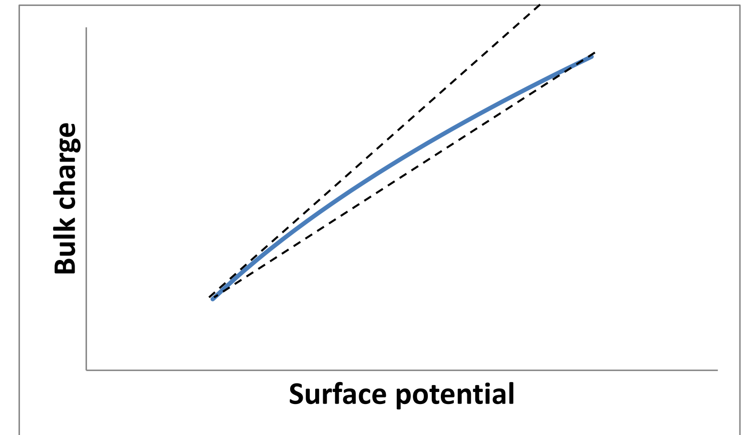
**Drain node charge:** $Q_D = W \int_{\phi_{ss}}^{\phi_{sd}} \frac{x}{L} Q_{inv} \frac{dx}{d\phi} d\phi$ **Ward-Dutton partition scheme [7]**

- For calculating these charges, we need $dx/d\phi$ and $x = f(\phi)$.
- These are derived from the continuity equation and the channel current expression.
- ***However, they become very cumbersome very quickly, because of the powers of 3/2 and ½ in the current expressions…*** [8]

**Ward-Dutton partition scheme is valid only for uniform doping and invalid for drain field dependent mobility[9].**

# Compact modeling of bulk charge

- The terms with powers of 3/2 and ½ come from the bulk charge expression
- This is overcome by linearizing the body charge about some point in the channel




$$\sqrt{\phi_s} = \sqrt{\phi_{ss}} + \frac{1}{2\sqrt{\phi_{ss}}}(\phi_s - \phi_{ss})$$

$$Q_{inv} = C_{ox}\left(V_{gb} - V_{fb} - \phi_s - \gamma\sqrt{\phi_{ss}} - \frac{\gamma}{2\sqrt{\phi_{ss}}}(\phi_s - \phi_{ss})\right)$$

# Linearized inversion charge and current

- $Q_{inv}$ can be rewritten as

$$Q_{inv} = C_{ox}\left(V_{gb} - \delta - \alpha(\phi_s - \phi_{ss})\right)$$

**Where** $\alpha = 1 + \frac{\gamma}{2\sqrt{\phi_{ss}}}$ **and** $\delta = V_{fb} + \phi_{ss} + \gamma\sqrt{\phi_{ss}}$

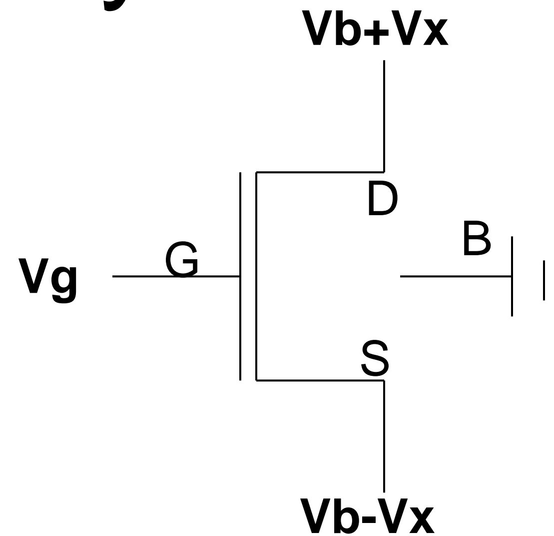
- $\delta$ is the classic long channel threshold voltage when $\phi_{SS} = 2\phi_B$
- The final current now has a simpler form

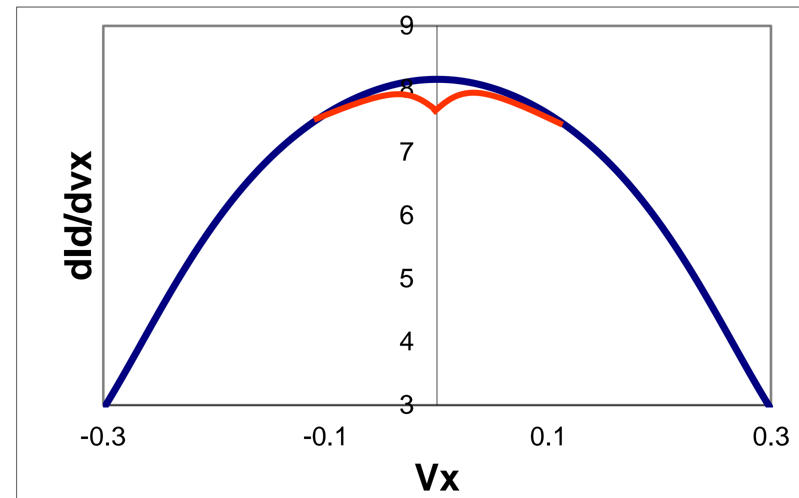
$$I_{Channel} = \frac{\mu W C_{ox}}{L}\left((V_{gb} - \delta + \alpha v_t)(\phi_{sd} - \phi_{ss}) - \frac{\alpha}{2}(\phi_{sd} - \phi_{ss})^2\right)$$

**The base framework needs to be amenable to both Current and Charge formulations.**

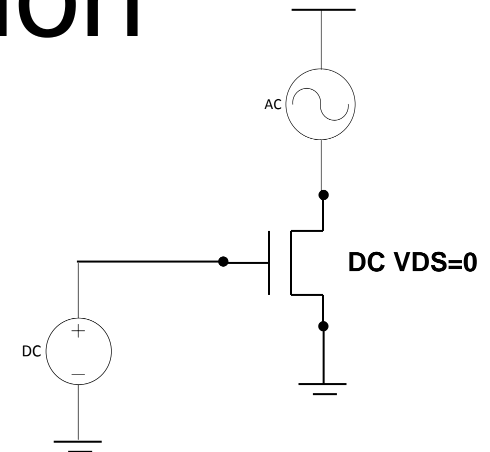
# Gummel symmetry

- Transistors are designed to be symmetric w.r.t to source and drain interchange.
- Models, however, need to be *intentionally* formulated to preserve this symmetry.
- MOSFET model implementations in circuit simulators use this symmetry assumption and flip the source and drain when VDS < 0.
- If the model is not symmetric then there will be singularities in the higher order derivatives at VDS = 0.



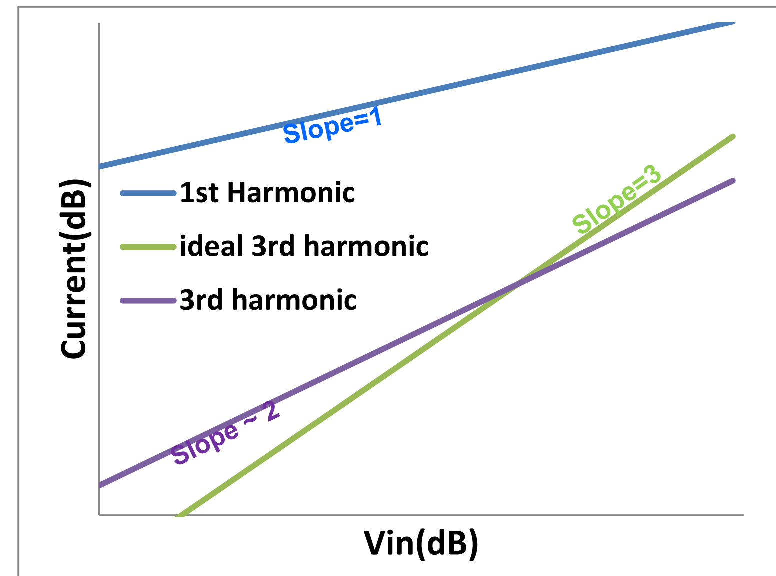



# Distortion prediction

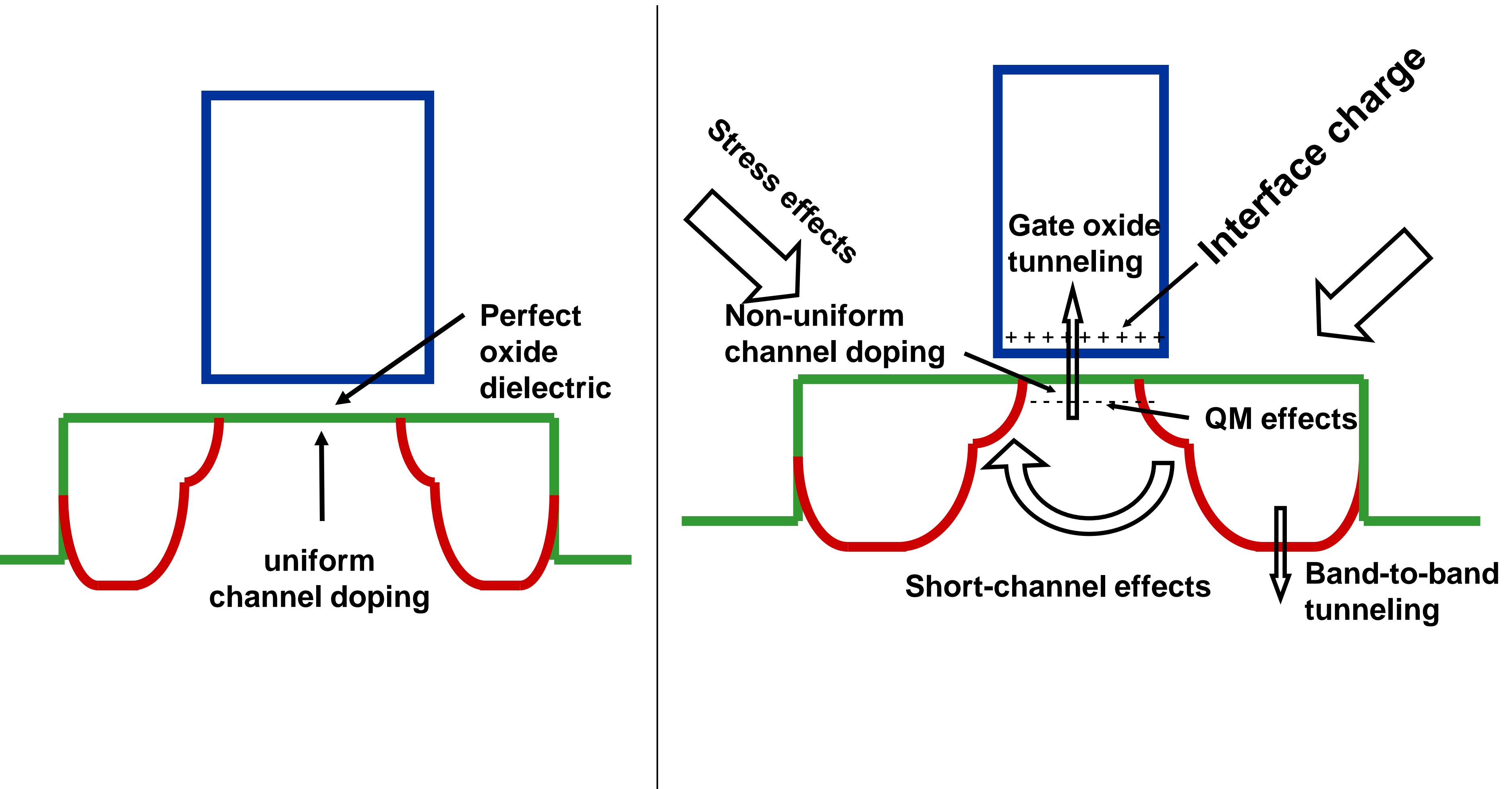



- Distortion prediction from simulations is critical for passive mixers and other RF circuits[10].
- Need higher order derivatives to be continuous at VDS=0
- Core long channel transistor model needs to be symmetric by construction.
- Linearizing bulk charge about $\frac{\phi_{sd}+\phi_{ss}}{2}$ [11][12], results in a symmetric long channel model.
- Additional tests [13].

**Understand the usage and requirements of your designers.**

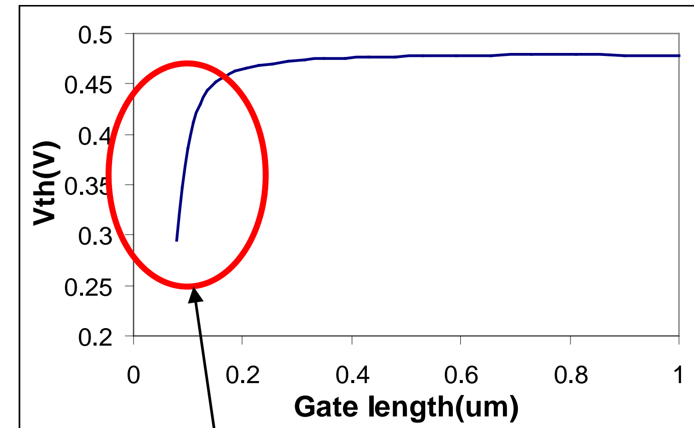


# Other effects



# Compact modeling of SCE

- Long channel assumption breaks down.
  - Changes in vertical and lateral fields are comparable.
- Observations:
  - Change in VT with length
  - VT changes with drain bias, output impedance decreases.
- Approach: Quasi-2d analysis [14]
  - Ignore the mobile charge contribution
  - Solve for the potentials distribution
  - Evaluate the change in barrier height in going from long channel to short channel




**Long channel approximation is not valid.**

# Modeling velocity saturation

- Traditionally a challenging component of a compact model.
- Most commonly used expression was formulated by Caughey-Thomas[18]
- N=2 makes the current and charge derivations iterative [19].
  – Most compact models use N=1

$$v = \frac{\mu_{eff} E}{\left[ 1 + \left( \frac{\mu_{eff} E}{V_{sat}} \right)^n \right]^{1/n}}$$

$$Electrons : n = 2$$

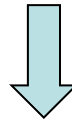
$$Holes : n = 1$$

$$I_{ch} = \frac{\mu}{1 + \kappa \frac{\varphi_{ds}}{L}} f\left(\phi_{ss}, \phi_{sd}\right) \varphi_{ds}$$

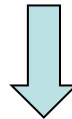
# Modeling velocity saturation

**Solve for drain side surface potential $\phi_{sd}^{sat}$ at the onset of velocity saturation:**

$$I_{ch} = \frac{\mu}{1+\kappa \frac{\varphi_{ds}^{sat}}{L}} f\left(\phi_{ss}, \phi_{sd}^{sat}\right)\varphi_{ds}^{sat} = WQ_{sat} v_{sat}$$



**Solve for $V_{DS}^{sat}$ = $V_{DS}$ at which $\phi_{sd}$ = $\phi_{sd}^{sat}$**



**Limit $V_{DS}$ to $V_{DS}^{sat}$**

# Gain compression and distortion

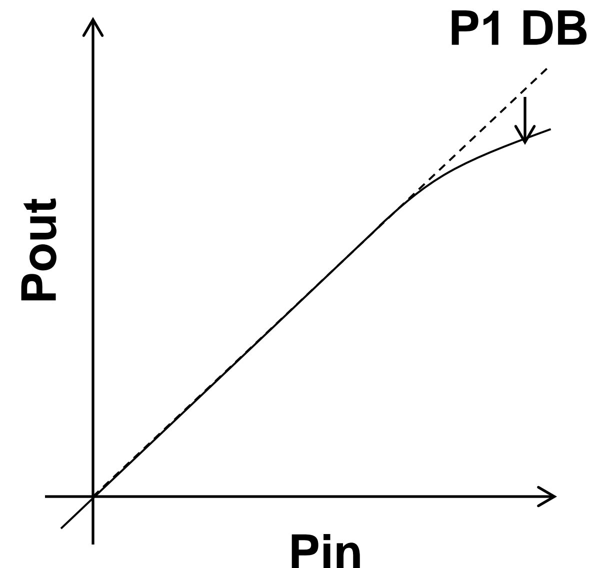
For a sinusoidal excitation at the gate

$$I_{Drain} = A_1 v Sin(\omega t) + A_2 v^2 Sin^2(\omega t) + A_3 v^3 Sin^3(\omega t) + \ldots$$

- Gain is linear only for a small signal amplitude.

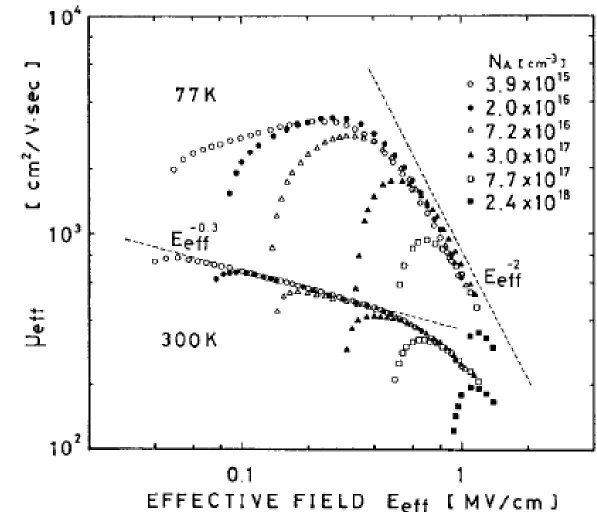
$$G_1 = A_1 + \frac{3}{4} A_3 v^2$$

$$A_n \propto \frac{\partial^n I_{drain}}{\partial V_{gs}^n}$$



# Mobility Modeling: field dependence

- Higher order derivatives are determined by the right modeling of gate field dependent mobility [17]
- Mobility is not included in the integral when the long channel current is derived.
- Hence typically an effective field [15,16] is used to account for the gate bias dependence.
  - Can't be empirical
  - important for analog and RF.




Source: [12]Takagi et al, pp 398-401, IEDM 1988

**Higher order derivatives are important for analog and RF applications. The compact model is required to reproduce this without having to explicitly fit to data.**

# Mobility Modeling: gate field dependence

**Matthiessen's Rule:**

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{Cou}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{SR}}$$

$$Eeff = \frac{Q_B + \eta Q_i}{\varepsilon_{Si}}$$

Scattering due to dopant atoms

$$\mu_{Cou} = F\left(\frac{Q_i}{N_{dop}}\right)$$

Scattering lattice vibrations

$$\mu_{Ph} = K_{Ph} E_{eff}^{-m}$$

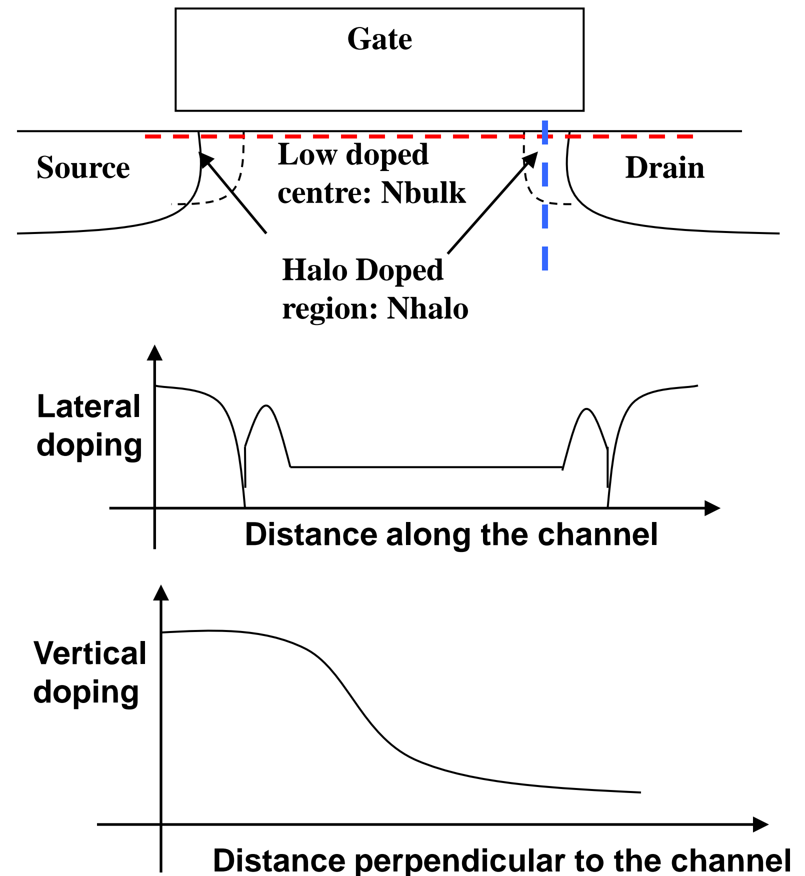
Scattering due to surface roughness of the $Si\text{-}SiO_2$ interface.

$$\mu_{SR} = K_{SR} E_{eff}^{-n}$$

**The exact equations vary depending on the compact model.**

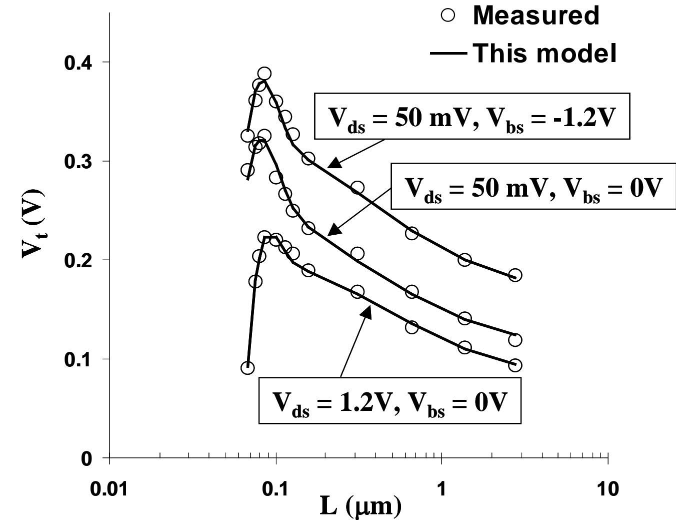
# Non-uniform doping

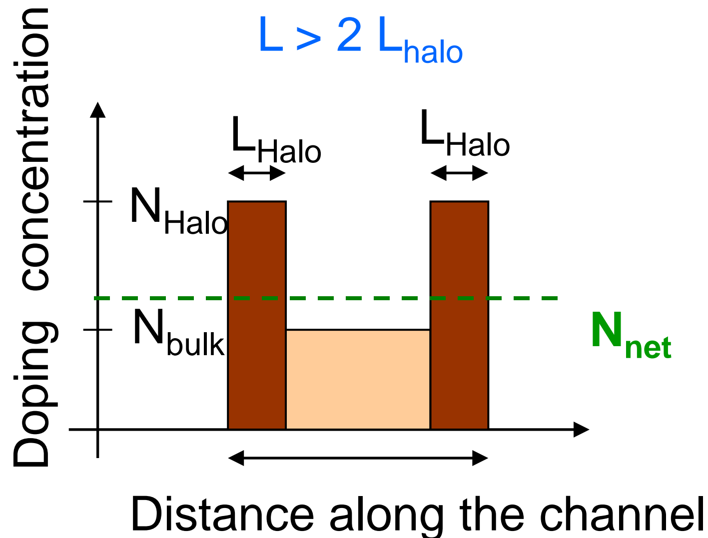
- Scaling requires the use of Halo implants for control of short channel devices
- Lateral non uniform doping
  - Reverse short channel effect
  - Long channel DIBL [20]
  - Degradation of output resistance at longer lengths [21]
- Vertical non-uniform doping
  - Back bias dependent doping concentration.

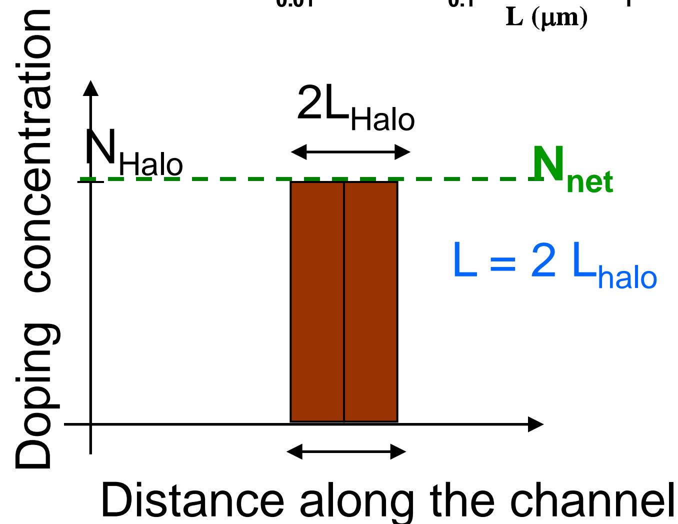


# Reverse short channel effect

- Effective / net doping increases as the channel length is reduced.
- Resulting in an increase in threshold voltage as the gate length reduced.

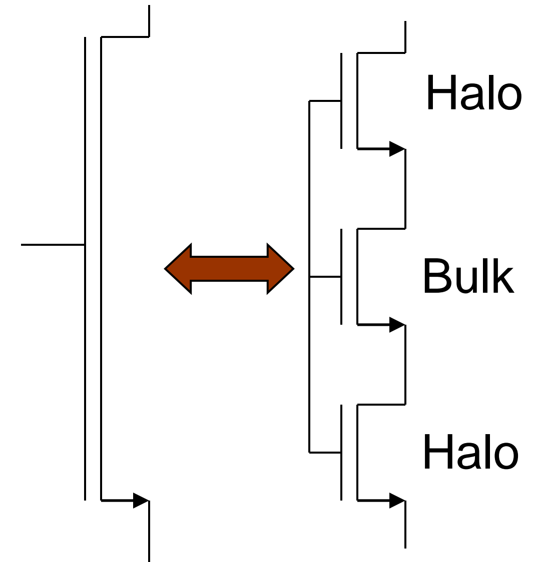


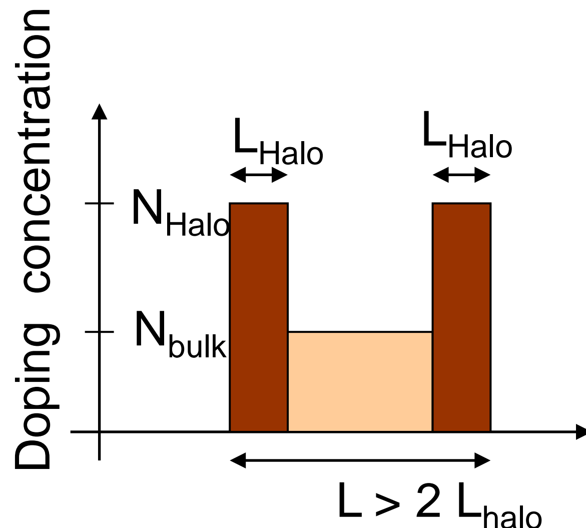



# Reverse short channel effect

- In compact models RSCE is modeled by using a length dependent doping concentration.
  - Match the subthreshold current across the 3 transistors to extract an equivalent doping [22].
- The core quantities in a compact model are calculated assuming a uniform doping.
  - Charge and current need different doping!.

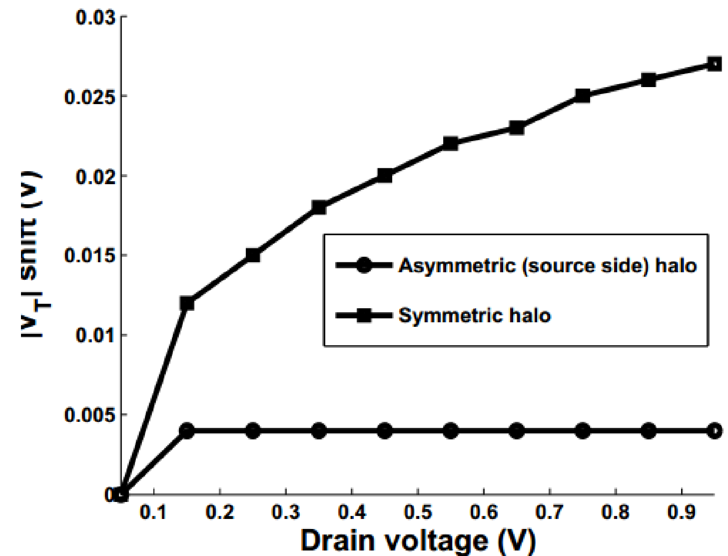


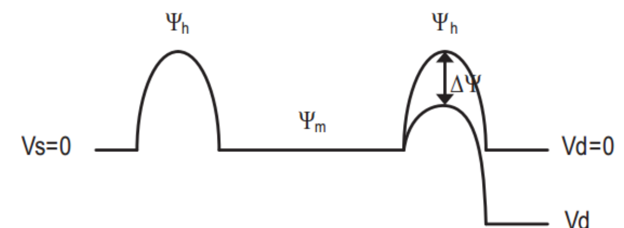




**Electrical engineering based concepts are also used to solve problems**

# Long channel DIBL modeling

- Even for long channel devices, sub-threshold current increases with increased drain bias.
- In subthreshold, current is controlled by the conductance of the region around the potential peaks corresponding to the halos.
  - Applying the drain bias can effecting eliminate one of these peaks by increasing the current by a maximum of 2X! [20].

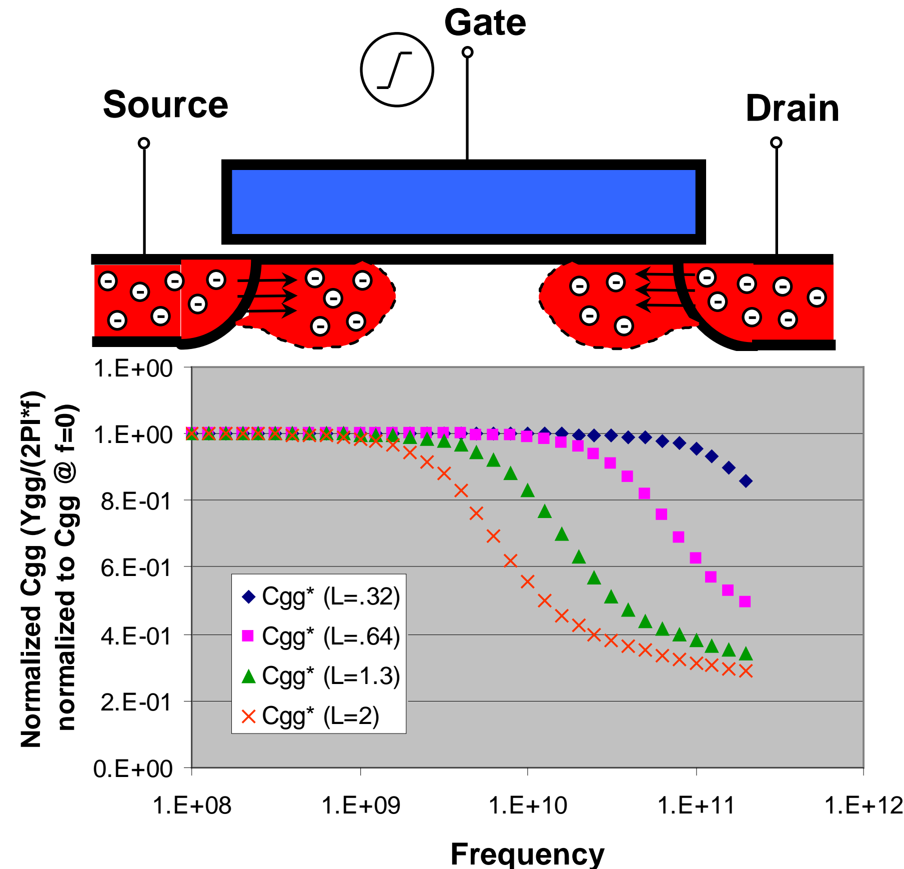



**Use numerical simulations to thoroughly understand the problem before compact model development.**

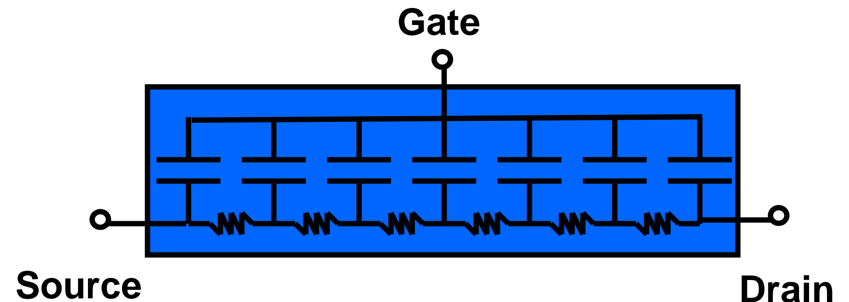
# Non Quasi-Static Effects

- Quasi-static approaches assume that capacitors charge instantaneously in response to a change in voltage.
- Quasi-static approximations only work when the applied signal has a long rise or fall time so that a steady-state condition can be achieved with the applied signal.
- Non-quasi-static effects (NQS) become important when the transient signal is comparable or changes faster than the carrier transit time [23].



# Small-Signal NQS Compact Model

- NQS effect can be reproduced by segmenting the channel.
- Application of weighted residuals method [24] is computationally efficient.

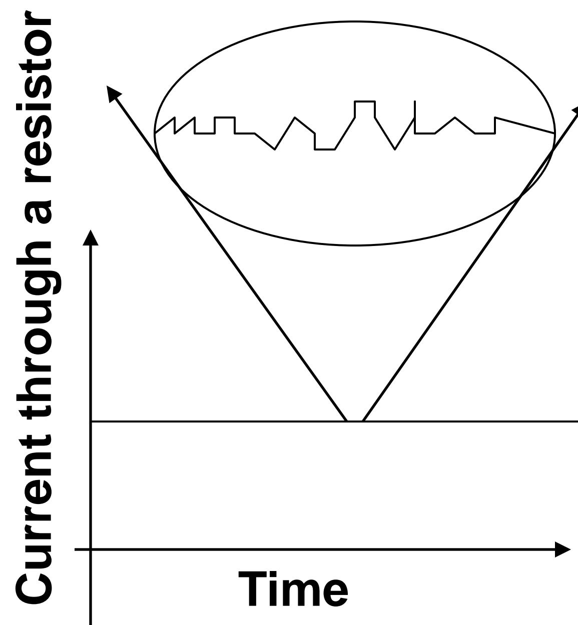



$$\frac{\partial q_i}{\partial t} + \mu \frac{\partial}{\partial x}\left[\left(\frac{q_i}{dq_i / d\phi_s} - v_t\right)\frac{\partial q_i}{\partial x}\right] = 0$$

**Compact models are derived under quasi-static assumption. However, some applications don't meet this condition**

# Noise Characteristics

- Different types of noise are important at different frequencies [25]
- Thermal noise and 1/f noise models are common.
- Noise modeling and characterization is critical for analog and RF designs (LNA)
  - Digital designs suffer from phase noise in PLLs leading to jitter.



# Noise sources and modeling

- Thermal Noise in a Resistor
  - Origin: Thermal agitation of carriers.
  - Frequency independent, white noise.
- Modeling

$$\overline{v_n^2} = 4KTR\Delta f \text{ or } \overline{i_n^2} = \frac{4KT\Delta f}{R}$$

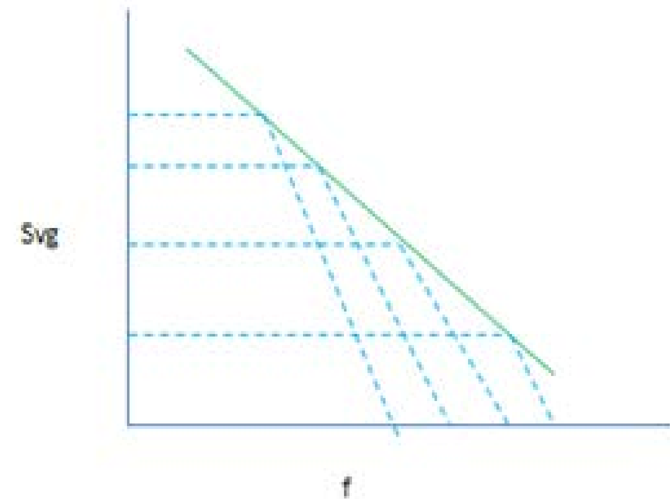
- Shot Noise, example: Gate current noise
  - Origin: Granular nature of charge, randomness of charge transport across a barrier.
  - Associated with the flow of current.
  - White noise

$$\overline{i_n^2} = 2qI_G\Delta f$$

# Noise sources and modeling

- Flicker Noise
  - Origin: Charge trapping and de-trapping
  - Random Telegraph Signals (RTS)
    - Observable in small devices
    - Example: Drain current fluctuations as a function of time.
  - 1/f noise
    - Superposition of several RTS events, leading to a 1/f distribution
    - Modeled as fluctuations in number of carriers and mobility fluctuations [26]

$$\overline{i_n^2} = \frac{K}{f}\Delta f$$

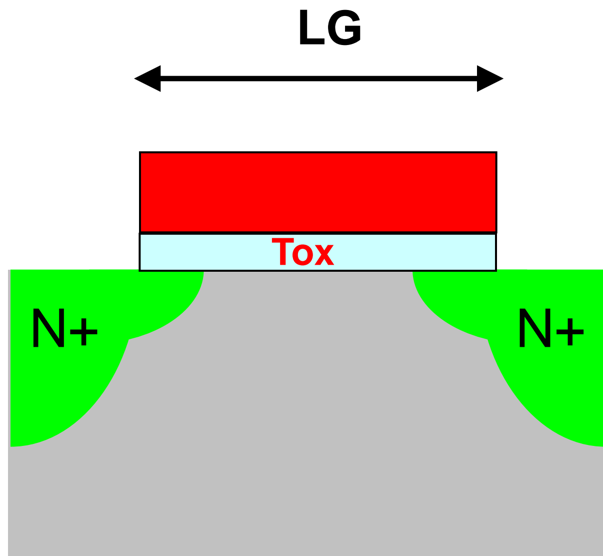


# Other models… Important nonetheless

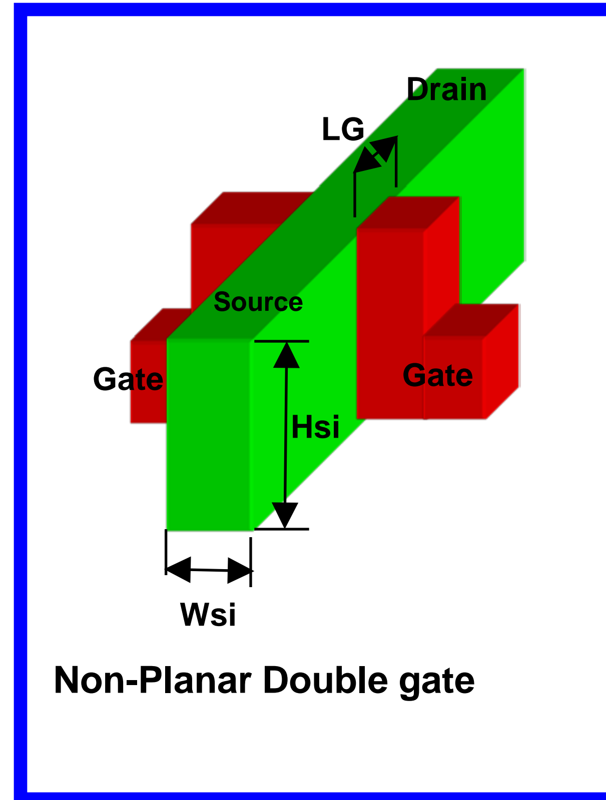
- Narrow width models
  - The change in device characteristic with reducing width.
  - The narrow width characteristics are a strong function of the fabrication process and sequence.
  - These models are typically more empirical in nature to accommodate the application of the model to several processes.
- Stress effect: modeling based on layout

# Core compact models for recent devices

# Double gate FET



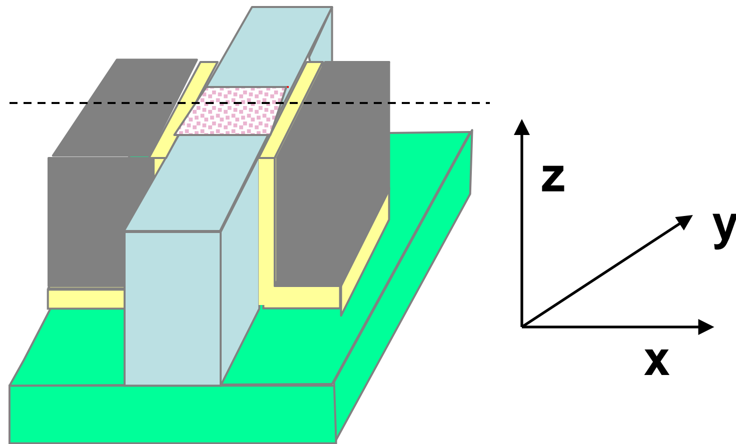
Planar



Non-Planar Double gate

**Improved SCE, reduced variability.**

# Poisson equation for a Double gate MOSFET



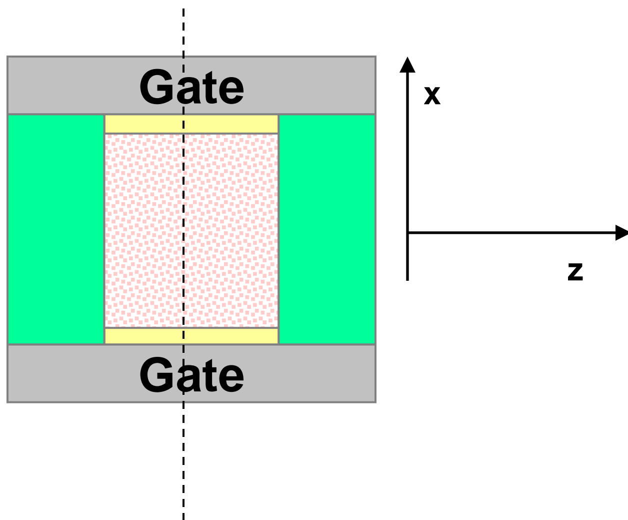

$$\frac{\partial^2\phi}{\partial x^2}+\frac{\partial^2\phi}{\partial y^2}+\frac{\partial^2\phi}{\partial z^2}=-\frac{q}{\varepsilon_{Si}}\left(p-n+N_d^+-N_a^-\right)$$

**Gradual channel approximation**

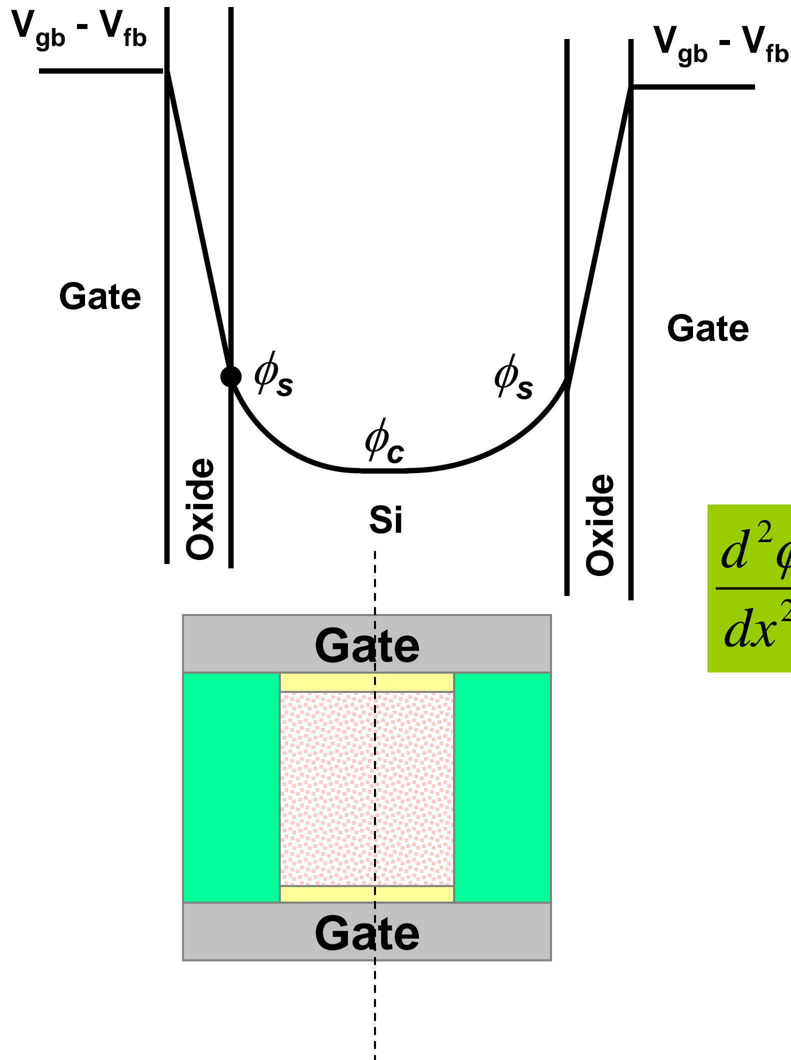
$$\frac{\partial^2\phi}{\partial x^2}+\frac{\partial^2\phi}{\partial y^2}=-\frac{q}{\varepsilon_{Si}}\left(p-n+N_d^+-N_a^-\right)$$

**Variation in potential along the Z direction is negligible.**

$$\frac{d^2\phi}{dx^2}=-\frac{q}{\varepsilon_{Si}}\left(p-n+N_d^+-N_a^-\right)$$



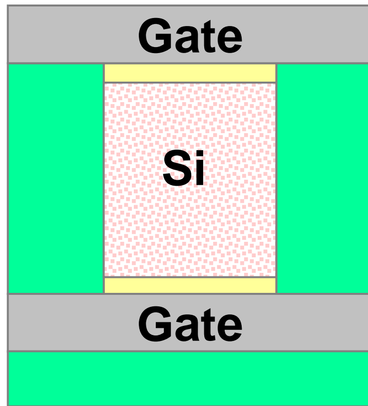
# Modeling Double gate transistors



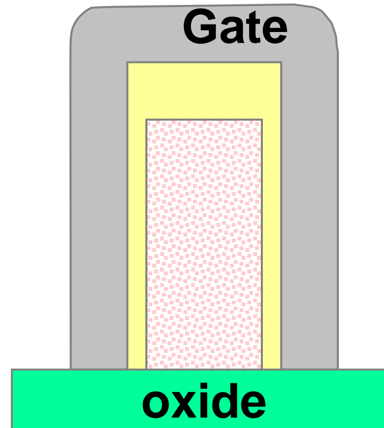

$$\frac{d^2\phi}{dx^2} = \frac{q}{\varepsilon_{Si}} n$$

- Symmetric double gate mosfet
  - Need the solution for $\phi_s$ and $\phi_c$(implicitly) to evaluate the device characteristics.
  - In deriving the surface potential for a planar MOSFET $\phi_c$ is set to zero.
  - Typically these devices are doped low enough that the Poisson's equation can be solved only for the electron contribution (for an Ntype fet)[28]
  - Compact modeling is more involved for DG MOSFETs especially if doping also needs to be taken into account.

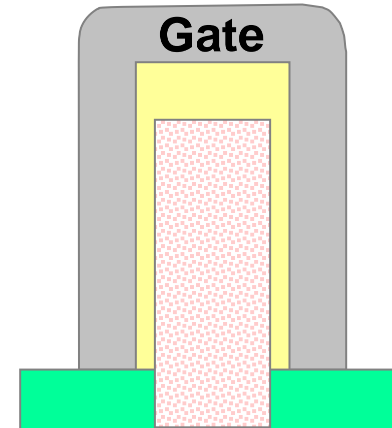
# Multi gate model



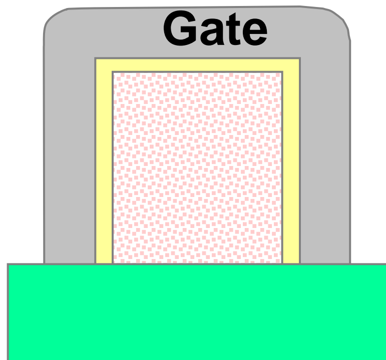

double gate




finfet




bulk finfet

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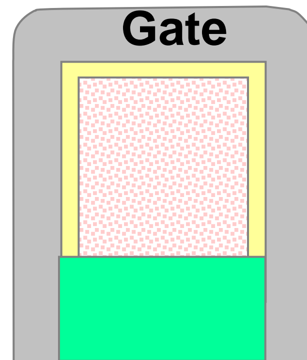
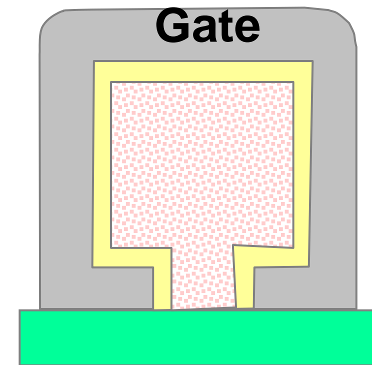



pi-gate

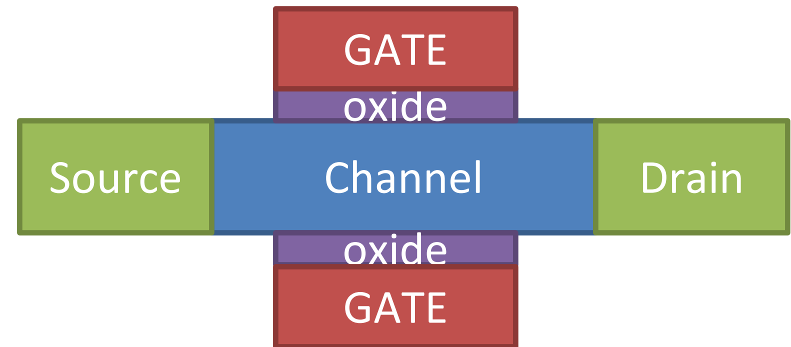


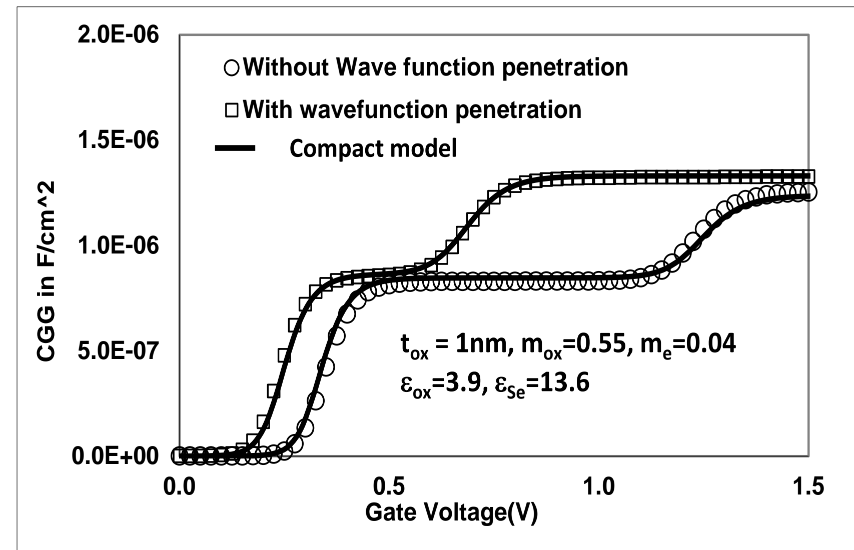

omega gate

**A Universal Core Model for Multiple-Gate Field-Effect Transistors, [29]**

# Low effective mass device modeling

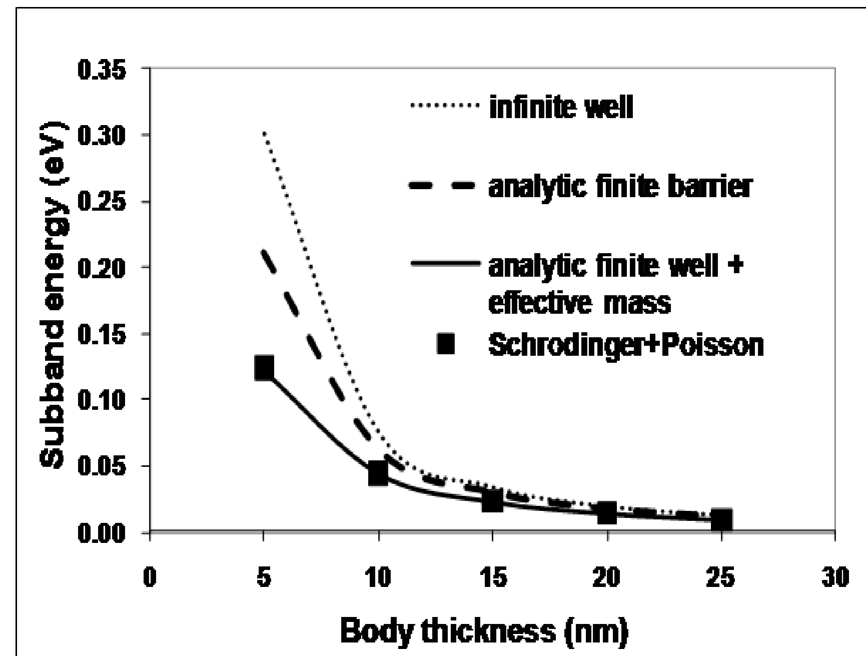
- Motivation:
  - Need higher drive currents without higher caps.
  - Higher mobility
  - Low DOS means lower charge, but also low cap
- For target supply voltages upto two subbands were occupied.
- Need physical model that correctly predicts the cap with changes in oxide and semiconductor properties like effective mass, barrier height etc.



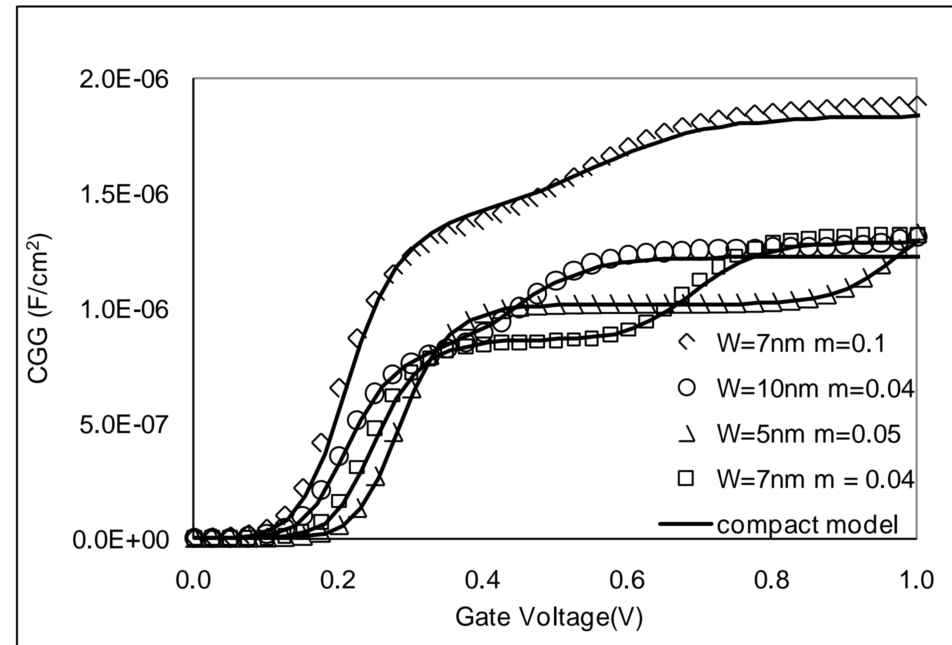
# Low effective mass device modeling -I

- Solve for subband energies assuming wave function penetration into the oxide and finite well height.
  - Iterative solve, but gives physical result with changes in barrier height and oxide thickness
- Use Fermi-Dirac(FD) statistics to capture the DOS effect.
  - Will produce physical scaling with changes in effective mass



# Low effective mass device modeling -II

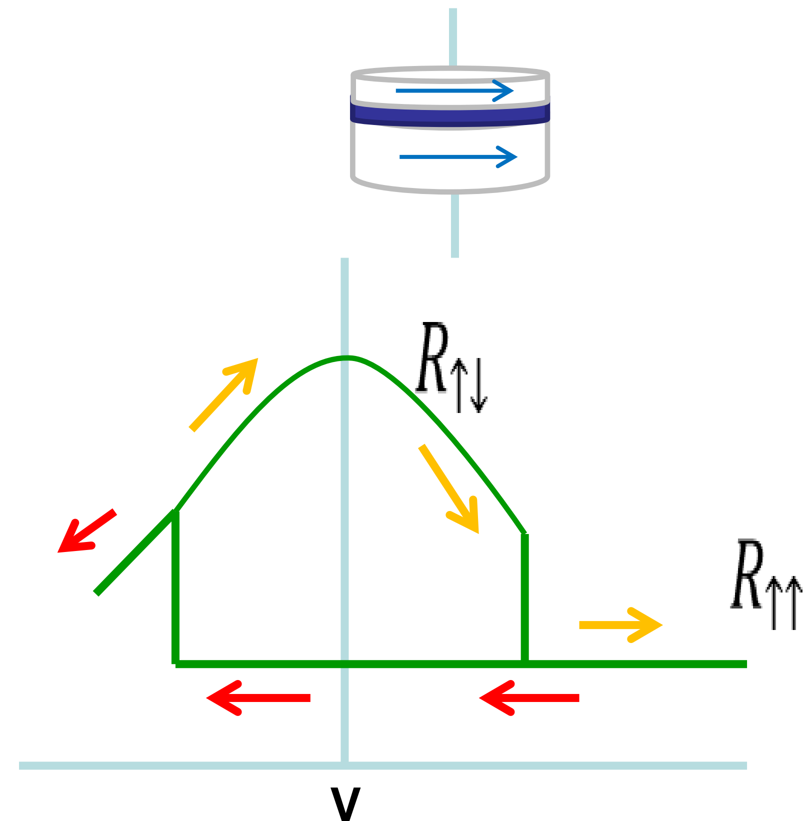
- Integration of Poisson is non-trivial with FD.
  - Treat the variation in $\phi$ as negligible in semiconductor
- Account for charge centroid effects by assuming ideal wavefunction forms (sinusoids), then make engineering approximations, [30], [31].




$$t_{ox}^{eff} = t_{ox} + 0.7 \frac{t_{se}}{4} \frac{\varepsilon_{ox}}{\varepsilon_{se}}$$

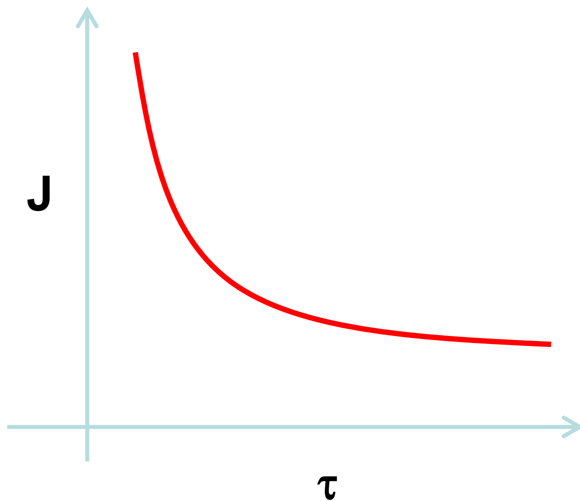
# Modeling MRAM devices

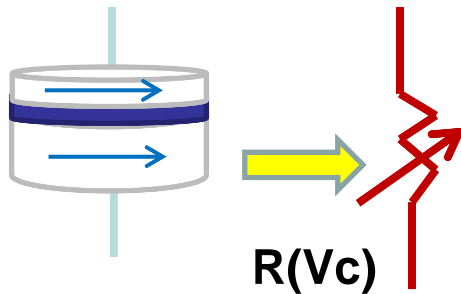
- Most modeling is done using MATLAB…
- Designers need a model inside standard circuit simulation engines.
- 0th order model:
  - DC model with bias dependent resistance with a “state” variable.
  - Sufficient for biasing evaluation.
  - Insufficient for timing read and write




**Hysteresis cannot be handled by table lookup model**

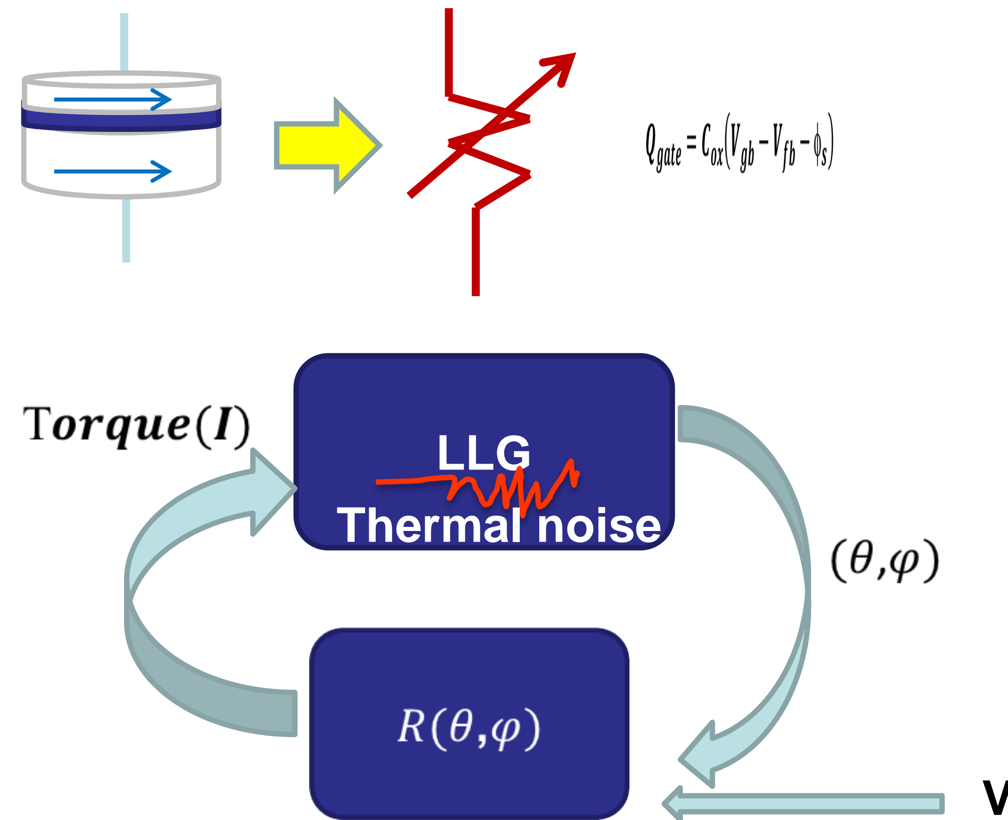
# Option 1: equivalent circuit models




- MRAM does not switch its state instantly.
- Vc is modeled using ideal circuit elements such as Resitances, capacitances, Schmidt trigger etc [32]
- For use in memory block design
  - For timing simulations
  - Need to know the delay in switching for a given current level.

# Option 2: Physical model




- MTJs exhibit additional source of variation due to thermal agitation.
- Solve stochastic LLG to account for thermal agitation [33].
  - $\theta,\varphi$ solved as additional nodes by the circuit simulator.
- Needed for designing memory circuits.

# Good compact modeling practices - I

- Use numerical simulations to fully understand the physics of the problem.
  - Should be able to explain the mechanism to a design engineer.
- Model needs to be true for asymptotic behaviors.
  - Strong inversion limit, short channel limit, weak inversion limit.
- Let physics dictate the bias dependence (never let the data dictate the bias dependence of a phenomenon).
  - Helps to make sure that the model naturally transitions when the effect is not significant
  - No artificial smoothing needed to splice regions together.

# Good compact modeling practices -II

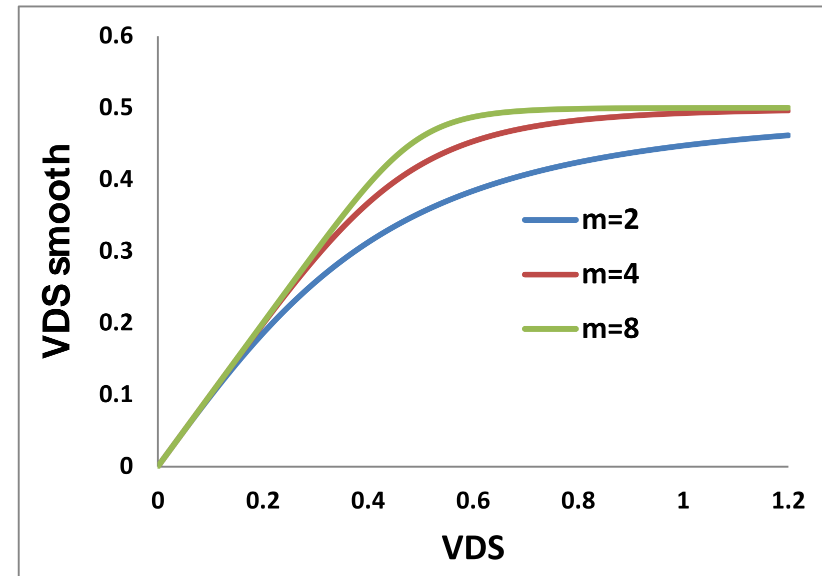
- Circuit simulators can ask for compact model evaluations at unreasonable bias conditions or operating conditions.
  - Numerical underflow and overflow.
  - Example: Low temperature conditions

$$\frac{\left(V_{gb} - V_{fb} - \phi_s\right)^2}{\gamma^2} = V_t \exp\left(\frac{V_{bd} - 2\phi_f}{V_t}\right)\left[\exp\left(\frac{\phi_s}{V_t}\right) - 1\right]$$

- $exp\left(\frac{V_{bd}-2\phi_f}{V_t}\right)$ becomes too small (underflow)
- $exp\left(\frac{\phi_s}{V_t}\right)$ becomes too large (overflow)
- However, the product is still reasonable, so the developer could rewrite as $exp\left(\frac{\phi_s+V_{bd}-2\phi_f}{V_t}\right)$, improving the stability of the model over a wider temperature range.

# Good compact modeling practices -III

- Beware of the model's numerical limitations.
  - Examples :
    - $\sqrt{2\phi_B + V_{BS}}$, $\log\left(a + f(V)\right)$, $\frac{1}{b+g(V)}$
  - All limiting must be done smoothly.
    - No if (VDS >= VDSAT) then vds=vdsat
    - Use $\left(\frac{vds^m * vdsat^m}{vds^m + vdsat^m}\right)^{1/m}$ instead
  - Limiting functions can sometimes contribute strongly to derivatives relevant to a designer
    - In the vdsat example for example Rout is strongly affected for smaller values of 'm'



# Good compact modeling practices -IV

- Validate, validate, validate
  - Over all available data
  - well beyond the range of application
  - On as many circuits as available

# Summary

- Compact models act as bridge of information between the manufacturing/Process team and the design teams
- Compact models are developed with very stringent requirements of (1) accuracy, (2) speed and (3) predictability based on true physics.
- The core model is developed based on a long channel assumption. All the additional complex behaviors due to short channel behavior are added as corrections to the core model.
- Understanding the usage of the compact model in actual design is important.
- NQS, Noise, higher order derivatives are all important irrespective of the device

# Acknowledgements

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- Mark Stettler
- Rios Rafael
- Mark Lundstrom

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