

## The deployment and evolution of the first NEEDS-certified model MIT virtual source compact model for silicon nanotransistors

Shaloo Rakheja

Email: shaloo.rakheja@nyu.edu

Electrical and Computer Engineering, New York University

Thanks: Prof. Dimitri Antoniadis, MIT



NEW YORK UNIVERSITY





DS NANO-ENGINEERED ELECTRONIC DEVICE SIMULATION NODE

#### Nano-Engineered Electronic Device Simulation Node

NEEDS has a vision for a new era of electronics that couples the power of billiontransistor CMOS technology with the new capabilities of emerging nano-devices and a charter to create high-quality models and a complete development environment that enables a community of compact model developers.

NEEDS Team: Purdue, MIT, U.C. Berkeley, and Stanford.

REGISTER NOW for the May 11-12 NEEDS annual meeting and workshop.

NEWEST COMPACT MODEL RELEASE: UCSB 2D Transition-Metal-Dichalcogenide (TMD) FET model 1.0.0. See Compact Models Page

NEEDS announces the public release of Berkeley MAPP, a MATLABbased platform for prototyping compact models and simulation algorithms.

GET STARTED ON COMPACT MODELING: Take Colin McAndrew's online workshop.

For presentations on these device technologies by experts in the field, see the NEEDS Seminar Series on "Emerging Transistor Technologies." SEMINARS, COURSES, ETC. NEEDS Seminar Series, nanoHUB-U and more



NEEDS is a resource for nanoelectronics supported by the National Science Foundation and by the Semiconductor Research Corporation. needs.nanohub.org

### **NEEDS compact model development**

## **Compact models**

NEEDS is charged to develop compact models for a very wide variety of novel nanodevices. A set of carefully chosen compact models that encompass a wide variet of nanodevice physics is being developed to provide concrete guidelines for how compact models can be grounded in fundamental physics and detailed simulations at then carefully validated by experiments. Developing these models also provides a "laboratory" for addressing formulational, numerical, and convergence issues that aris for compact models. The models developed will provide the community with a library high-quality and tested models, provide NEEDS with a set of case studies and examp and drive the development of the NEEDS compact model development platform.

NEEDS models are licensed with the Compact Model Council (CMC) Standard licens as described in the following document – CMC\_Standard\_license.pdf (155 KB) and follow the CMC recommendations for versioning.

#### **NEEDS** model releases will include:

- Matlab version for downloading
- Verilog-A version for downloading
- Manual (with a complete list of equations used and procedures to calibrate the

- A list of compact models for nanoscale devices available to download.
- Total number of models till date: 20
- Models from NEEDS member universities: 12/20 (60%)

### **NEEDS model release history**



## NEEDS compact models: top user downloads



### This presentation focuses on



#### I. MVS model

- Nanotransistor basics
- Model formulation
- Experimental verification
- Mathematical issues





## II. Model deployment on nanoHUB

- Process and requirements
- Current status
- Future goals



## PART I MIT Virtual Source Model For Nanotransistors

#### **Textbook MOSFET** *I-V* **theory**





#### What is MVS model?



 $\frac{Currents}{Id = f(Vg, Vd, Vs, Vb)}$ Ig = Ib = 0

MIT Virtual Source (MVS) nanotransistor model gives *currents* and *charges* as functions of terminal voltages.

#### <u>Charges</u>

Qs = f1(Vg,Vd,Vs,Vb)Qd = f2(Vg,Vd,Vs,Vb)Qb = f3(Vg,Vd,Vs,Vb)Qg = -(Qs+Qd+Qb)

### **MVS model: I-V characteristics**



#### **MVS 1.0.0 model formulation**

$$\begin{array}{l} \textbf{1} \quad I_{DS} = WQ_{x0} \left( V_{GS}, V_{DS} \right) F_{SAT} \left( V_{DS} \right) \upsilon_{x0} \\ \textbf{2} \quad Q_{x0} \left( V_{GS} \right) = -C_{inv} m \left( k_B T/q \right) \ln \left( 1 + e^{q \left( V_{GS} - V_T + \alpha \left( k_B T_L/q \right) F_f \right) / m k_B T} \right) \\ V_T = V_{T0} - \delta V_{DS} \\ \textbf{3} \quad F_{SAT} \left( V_{DS} \right) = \frac{V_{DS} / V_{DSAT}}{\left[ 1 + \left( V_{DS} / V_{DSAT} \right)^{\beta} \right]^{1/\beta}} \\ \textbf{4} \quad V_{DSAT} = \frac{\upsilon_{x0} L}{\mu_{app}} \end{array}$$
 Only 10 parameters in this model:  
 
$$C_{inv}, V_T, \delta, m, \upsilon_{x0}, \mu_{app}, L, \\ R_{SD0} = R_{S0} + R_{D0}, \\ \alpha, \beta \end{array}$$



## **Charge partitioning/ Dynamic model**

- Charge partitioning tells us the charge associated with the various terminals in the transistor.
- Transient analysis needs charges and inter-nodal capacitances.
- In MVS, dynamic model is obtained self-consistently with the static transport model → no additional fitting parameters.





## **References for MVS model equations**

- A. Khakifirooz et al., "A simple semi-empirical short-channel MOSFET current-voltage model continuous across all regions of operation and employing only physical parameters," IEEE Trans. Electron Devices, vol. 56, no. 8, <u>July 2009</u>.
- L. Wei et al., "Virtual-source-based self-consistent current and charge FET models: from ballistic to drift-diffusion velocitysaturation operation," IEEE Trans. Electron Devices, vol. 59, no. 5, <u>May 2012</u>.
- 3. S. Rakheja and D. Antoniadis, "MVS 1.0.1 Nanotransistor Model (Silicon)," <u>https://nanohub.org/resources/19684</u> (<u>Nov. 2013</u>)

# MVS model verification with experiments







#### III-V HEMT (Intel & MIT)



(MIT) Test chip fabricated using CVD grown  $MoS_2$ 

#### Si ETSOI (IBM)

#### Graphene (IBM, Columbia, MIT)





# Extremely thin silicon-on-insulator (SOI) (IBM, 2014)

**Output characteristics** 



**Transfer characteristics** 



$$L_{eff} = 30 \ nm$$

Symbols  $\rightarrow$  experiment Solid lines  $\rightarrow$  model

Page 15

### FinFET CMOS technology (Intel, 2014)



$$L_{eff} = 20 \ nm$$

Symbols  $\rightarrow$  experiment Solid lines  $\rightarrow$  model

### **Ambipolar graphene RF FETs**



Epitaxial GFETs fabricated at IBM, 2013.

Symbols  $\rightarrow$  experiment Solid lines  $\rightarrow$  model

Page 17

# Mathematical issues in writing compact models: "smoothness" is key



"A quick circuit simulation primer" https://nanohub.org/resources/20610

#### **Example of non-smooth functions**



#### **Problem areas in MVS model**



## PART II MVS model deployment on nanoHUB

## MVS 1.0.1 package release snapshot



# MVS 1.0.1 release package contents on nanoHUB: 1/2

#### **1. MATLAB-related**

- i. Model implementation
- ii. Model exerciser
- iii. Numerical parameter extractor

#### 2. Verilog-related

- i. Model implementation
- ii. Test-benches for simple circuits
- **3.** Experimental data for model calibration
- 4. Model manual

# MVS 1.0.0 release package contents on nanoHUB: 2/2

- **5.** Update log (when a new version is released)
- 6. License agreement

*Link to the model on nanohub:* <u>https://nanohub.org/publications/15</u>

*Wiki for model-release checklist:* <u>NEEDS  $\rightarrow$  For Developers  $\rightarrow$  First item on Resources</u>

### **Quick checklist for model release**

Component	Associated files and/or requirements		
MATLAB	<ul> <li>Model file Model exerciser</li> <li>Parameter extraction (analytical/non-linear)</li> <li>Readme file</li> </ul>	+	CMC license agreement Update log (if needed)
Verilog-A	<ul> <li>Model file</li> <li>SPECTRE/HSPICE netlists for simple circuits Readme file</li> </ul>		
Experimental data	• Readme file for data format and references		
Model manual	<ul> <li>Explaining all of the model equations</li> <li>Simulation results</li> <li>Extraction methodology</li> <li>Proper references</li> </ul>		

### **MVS-related seminars on nanoHUB**

NEEDS Compact Model Release –
 Lessons Learned from MVS 1.0.0

https://nanohub.org/resources/20139

Steps to follow when releasing your own compact model

The MVS Nanotransistor Model:A Case Study in Compact Modeling

https://nanohub.org/resources/21712

Dealing with mathematical issues in compact models

#### **MVS model evolution**



#### **MVS model evolution**



### **MVS 1.0.0 model evolution**



#### **Issues:**

- o Unused variables
- Hidden states
- o Parameter range
- o Indentation

MVS 1.0.1 Nov. 2013

#### **Issues:**

- Capacitance discontinuity
- Better ways needed to fix some other numerical issues in VA



 While we fixed some existing bugs in MVS 1.0.1, the mathematical issues still exist.

#### **MVS model evolution**



![](_page_30_Picture_0.jpeg)

#### **MVS 2.0.0 provides two implementations:**

- For **III-V HEMTs** which have degeneracy and gm-reduction under high drain current
- For <u>Si ETSOI</u> devices which operate under non degeneracy and do not have any gm-reduction.

MVS 2.0.0 provides only static transport model.

https://nanohub.org/publications/74

Contains links to all other versions of MVS

#### **MVS Nanotransistor Model 2.0.0**

By Shaloo Rakheja<sup>1</sup>, Dimitri Antoniadis<sup>1</sup>

#### Massachusetts Institute of Technology (MIT)

The MIT Virtual Source (MVS) model is a semi-empirical compact model for nanoscale transistors that accurately describes the physics of quasi-ballistic transistors with only a few physical parameters.

Listed in Compact Models | publication by group NEEDS: Nano-Engineered Electronic Device Simulation Node

![](_page_31_Picture_6.jpeg)

Supporting Docs Versions Reviews Wishlist Questions

#### Abstract

MVS 2.0.0 is an improved physics-based virtual source (VS) model to describe transport in quasi- ballistic transistors. The model is based on Landauer scattering (i) degeneracy on thermal velocity and mean free path of carriers in the channel, (ii) drain-bias dependence of gate capacitance and VS charge including the effects non-linear resistance of the extrinsic device region on gm-degradation at high drain currents in the channel.

Citations

Other MIT Virtual Source Models:

#### • MVS 1.2 HEMT

## Links to all MVS versions available on the same page

This version of the MVS model is specifically targeted toward III-V HEMT devices that show a reduction in the transconductance at high drain currents. The mechanical correction to the gate-channel capacitance.

Finally, the static transport model is supplemented with a charge partioning model. As in the previous MVS model versions, we provide the drift-diffusion no NVSAT) and blended quasi-ballistic charge model.

#### MVS 1.1 Silicon

This version of the MVS model is specifically targeted toward silicon devices. It contains slightly more empiricism than the more detailed MVS 2.0, and it is models.

#### InGaAs HEMTs with MVS 2.0.0

![](_page_32_Figure_1.jpeg)

## **Key references for MVS 2.0.0**

 S. Rakheja, M. Lundstrom, D. Antoniadis, "An Improved Virtual-Source-Based Transport Model for Quasi-Ballistic Transistors – Part I: Capturing Effects of Carrier Degeneracy, Drain-Bias Dependence of Gate Capacitance, and Non-linear Channel-Access Resistance," <u>IEEE Transactions on Electron Devices,</u> vol. 62, no. 9, pp. 2786-2793, Sep. 2015.

 S. Rakheja, M. Lundstrom, D. Antoniadis, "An Improved Virtual-Source-Based Transport Model for Quasi-Ballistic Transistors – Part II: Experimental Verification," <u>IEEE Transactions on</u> <u>Electron Devices, vol. 62, no. 9, pp. 2794-2801, Sep. 2015.</u>

# Summary- MVS nanotransistor models

- Two VS Models (MVS-1 and 2) provide a progression of approximation accuracy to the Transmission Model suitable for any FET structure.
- Despite its simplicity MVS-1 provides a suitable tool for FET carrier transport benchmarking for technology assessment.
- MVS-2 is based on physically sound charge-control and transport models to allow quantitative analysis of band-structure characteristics.

#### **MVS future plans**

![](_page_35_Figure_1.jpeg)