

EE-612: Lecture 27: RF CMOS

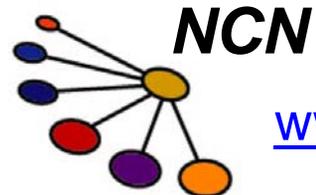
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www.nanohub.org

why analog / RF CMOS?

many applications involve analog / rf signals:

- 1) many natural signals are analog (sensors)
- 2) disk drive electronics
- 3) wireless receivers
- 4) optical receivers
- 5) microprocessors / memories

CMOS:

- 1) many systems are both analog and digital
- 2) CMOS is the dominate technology for digital electronics
- 3) CMOS performance has recently become suitable for analog

Reference: B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.

CMOS device metrics (digital)

1) on-current: $I_D(\text{ON})$

2) off-current: $I_D(\text{OFF})$

3) subthreshold swing: $S = \partial(\log_{10} I_D) / \partial V_{GS} \big|_{V_{DS}}$

4) device delay: $\tau = C_G V_{DD} / I_D(\text{ON})$

5) DIBL, etc.

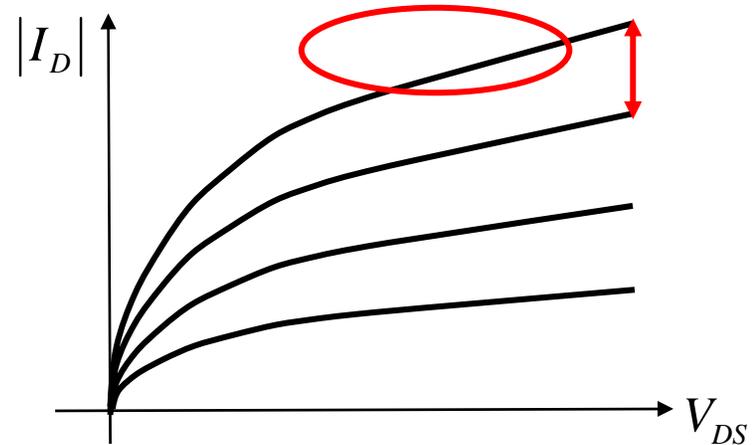
CMOS device metrics (analog)

1) transconductance: $g_m = \partial I_D / \partial V_{GS} |_{V_{DS}}$

2) output resistance: $r_o = \partial V_{DS} / \partial I_D |_{V_{GS}}$

3) f_T and f_{max} : $f_T = 1/2\pi\tau$

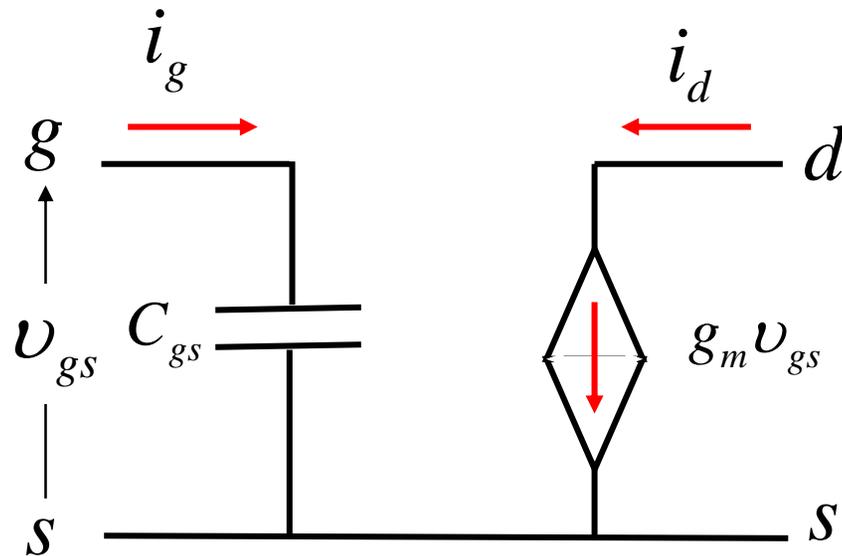
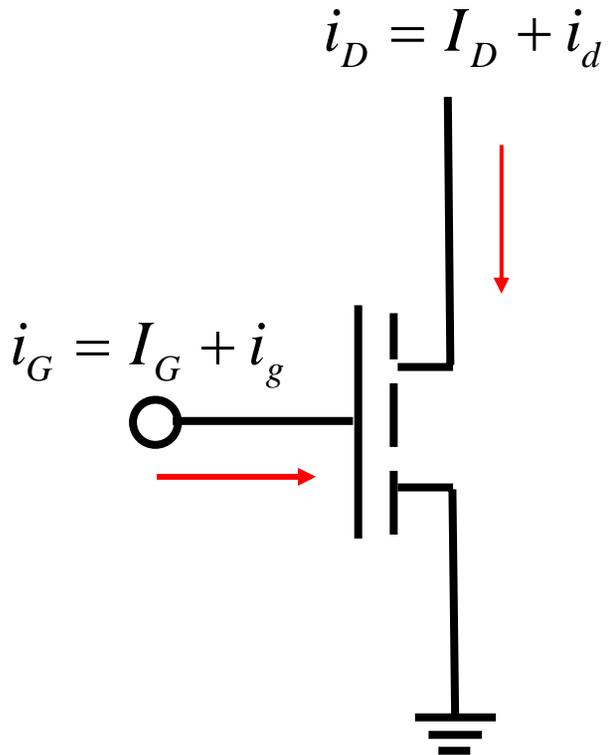
4) noise, mismatch, linearity, etc.



outline

- 1) Introduction
- 2) Small signal model**
- 3) Transconductance
- 4) Self-gain
- 5) Gain bandwidth product
- 6) Unity power gain
- 7) Noise, mismatch, linearity...

small signal model

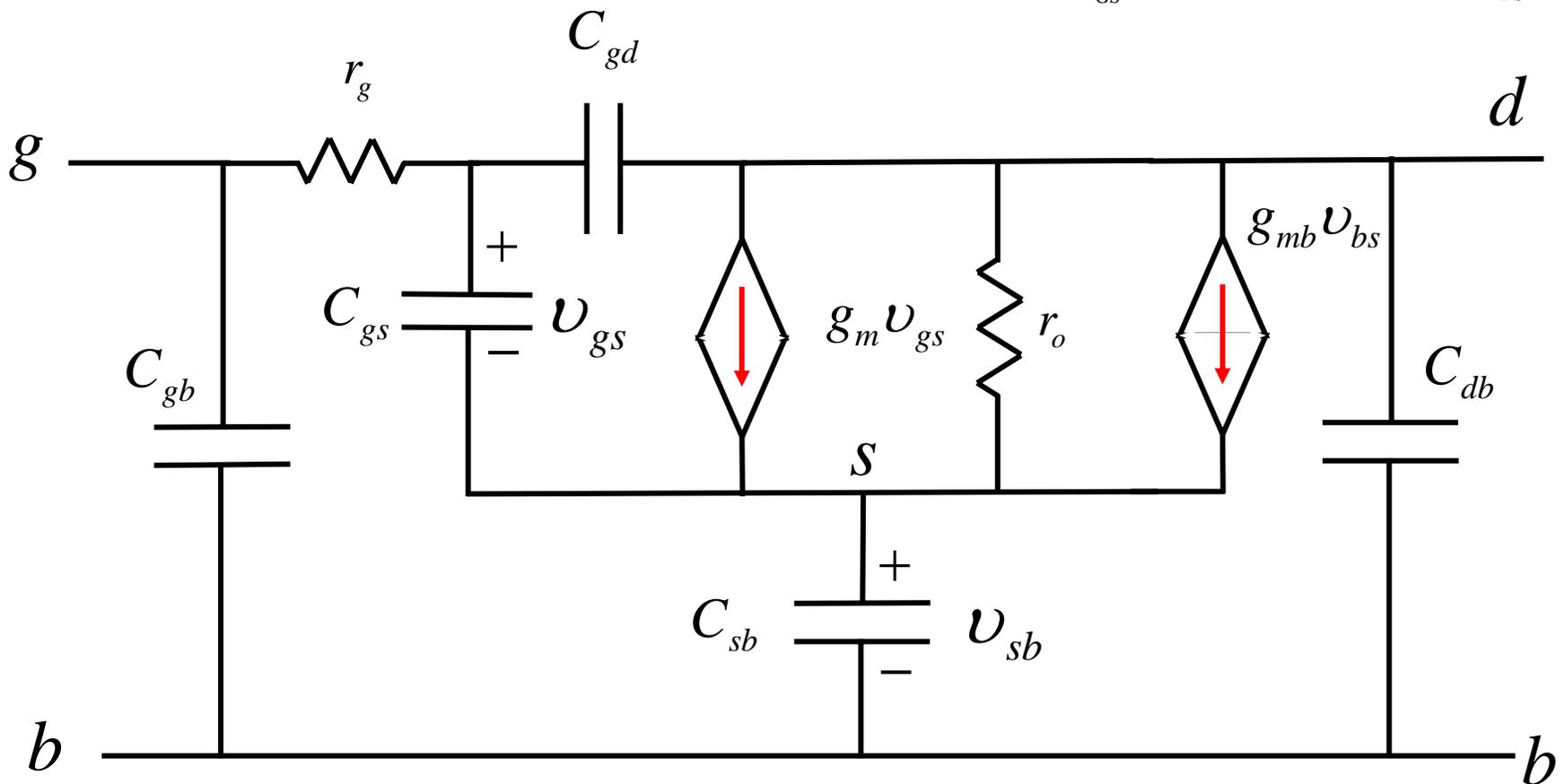


$$i_d = g_m v_{gs} \quad g_m = \frac{i_d}{v_{gs}} \approx \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}}$$

(quasi-static assumption)

small signal model (ii)

$$r_o = \left. \frac{\partial V_{DS}}{\partial I_D} \right|_{V_{GS}} \quad g_{mb} = \left. \frac{\partial I_D}{\partial V_{BS}} \right|_{V_{DS}}$$



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transconductance

MOS (above V_T , saturated)

$$g_m = \partial I_D / \partial V_{GS} \big|_{V_{DS}}$$

$$I_D = WC_{OX} \nu_{sat} (V_{GS} - V_T)$$

$$g_m = WC_{OX} \nu_{sat}$$

$$g_m / I_D = 1 / (V_{GS} - V_T)$$

$$g_m / I_D = 1 / (1.1 - 0.17) \approx 1 \text{ V}^{-1}$$

(65 nm HP)

bipolar

$$g_m = \partial I_C / \partial V_{BE} \big|_{V_{CE}}$$

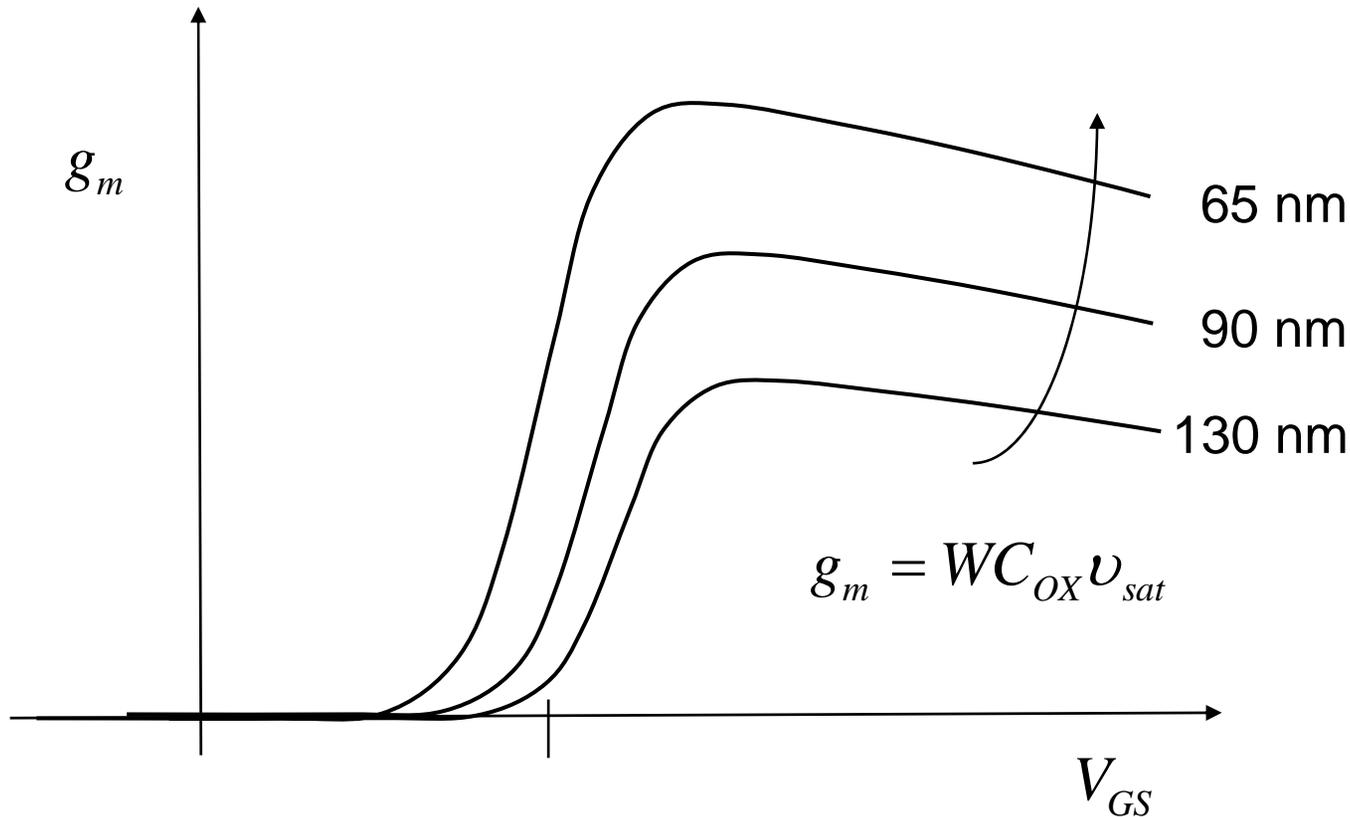
$$I_C = I_{C0} e^{qV_{BE} / k_B T}$$

$$g_m = I_C / (k_B T / q)$$

$$g_m / I_C = 1 / (k_B T / q)$$

$$g_m / I_C = 1 / (0.026) \approx 40 \text{ V}^{-1}$$

MOSFET transconductance



T_{OX} scaling, high-k, mobility improvements (e.g. strain) increase g_m .

transconductance (subthreshold)

MOS (below V_T , saturated)

$$g_m = \partial I_D / \partial V_{GS} \Big|_{V_{DS}}$$

$$I_D = I_{OFF} e^{qV_{GS} / mk_B T}$$

$$g_m = I_D / (mk_B T / q)$$

$$g_m / I_D = 1 / (mk_B T / q)$$

$$g_m / I_D = 1 / 1.3(0.026) \approx 30 \text{ V}^{-1}$$

bipolar

$$g_m = \partial I_C / \partial V_{BE} \Big|_{V_{CE}}$$

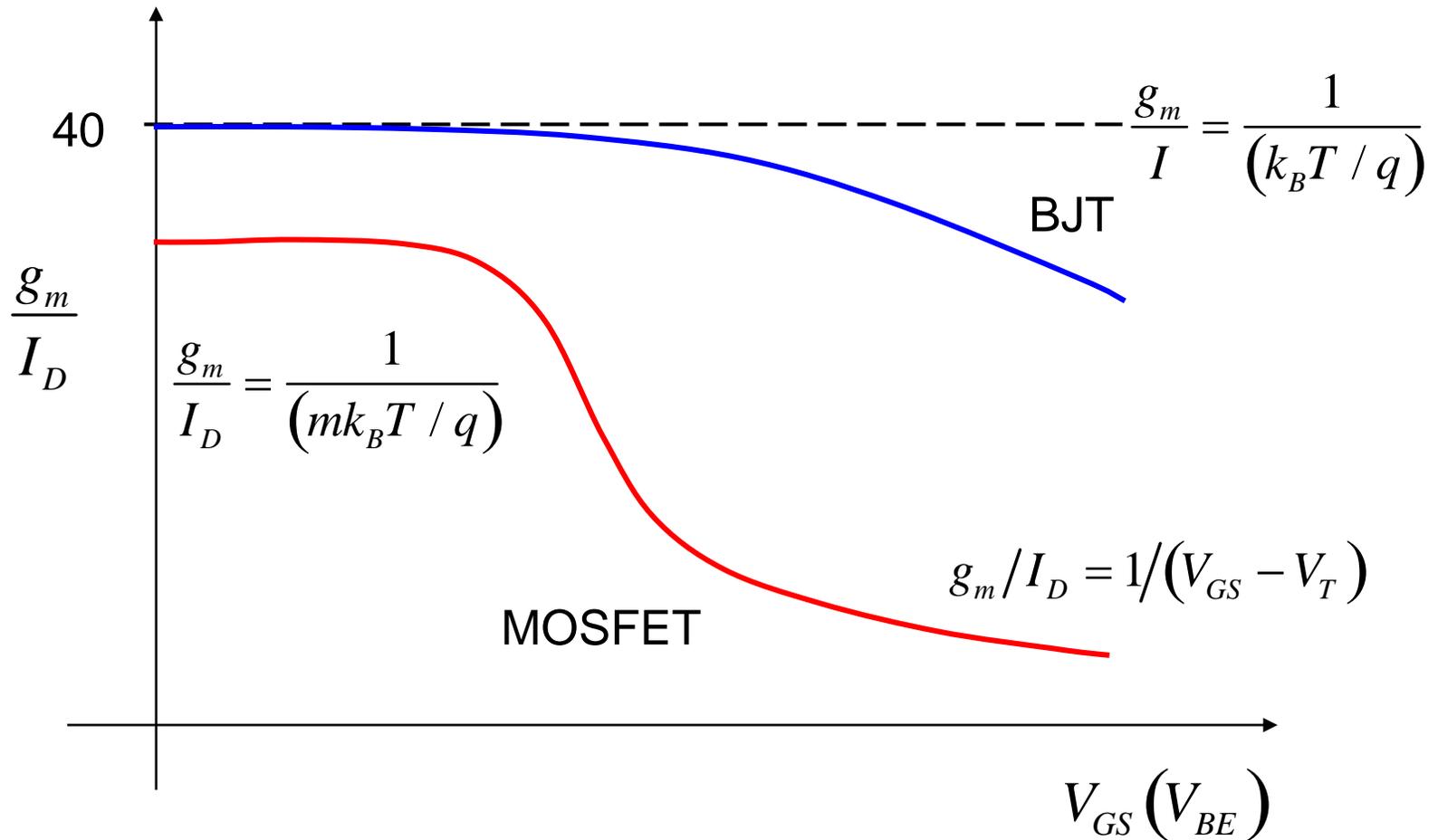
$$I_C = I_{C0} e^{qV_{BE} / k_B T}$$

$$g_m = I_C / (k_B T / q)$$

$$g_m / I_C = 1 / (k_B T / q)$$

$$g_m / I_C = 1 / (0.026) \approx 40 \text{ V}^{-1}$$

g_m / I_D figure of merit

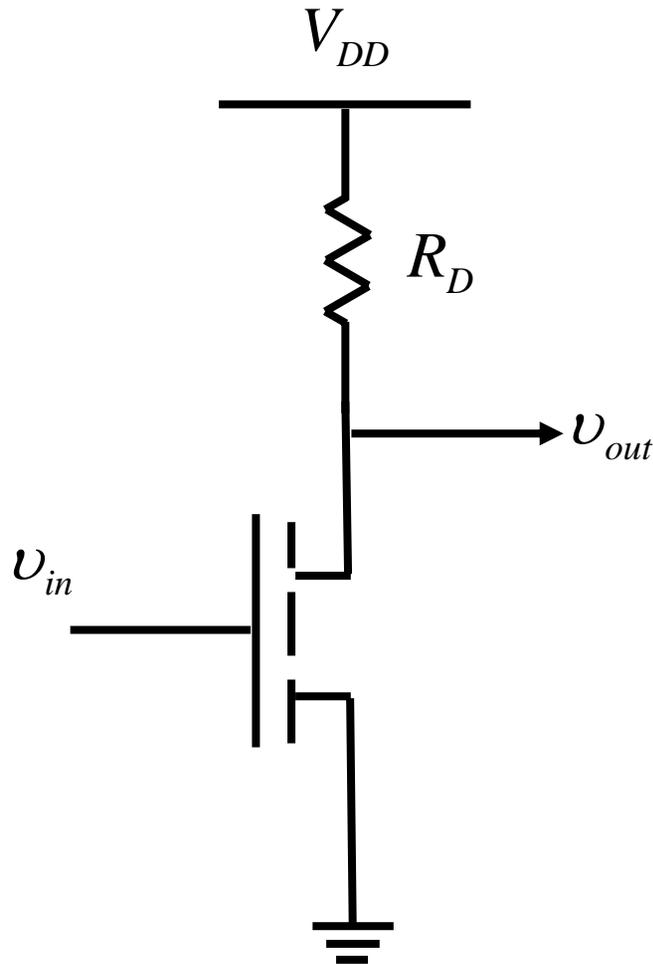


B. Murmann, P. Nikaeen, D.J. Connelly, and R. W. Dutton, "Impact of Scaling in Analog Performance and Associated Modeling Needs, *IEEE Trans. Electron Dev.*, 2006.

Outline

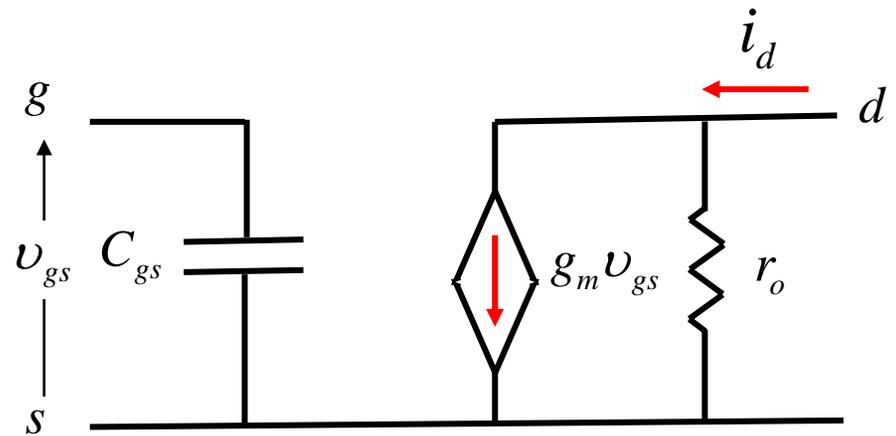
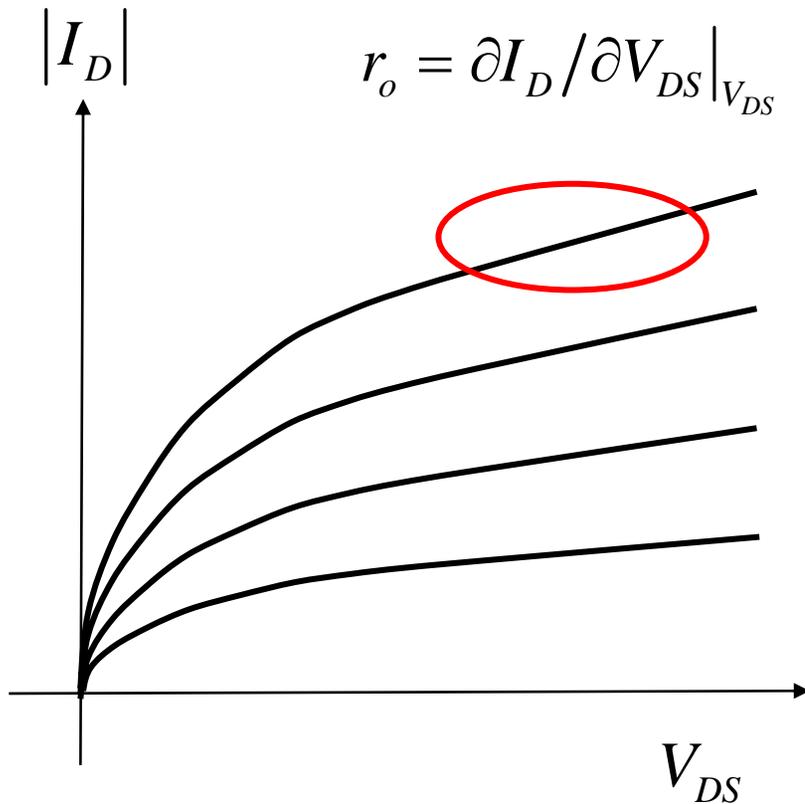
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- 5) Gain bandwidth product
- 6) Maximum power gain
- 7) Noise, mismatch, linearity

small signal gain

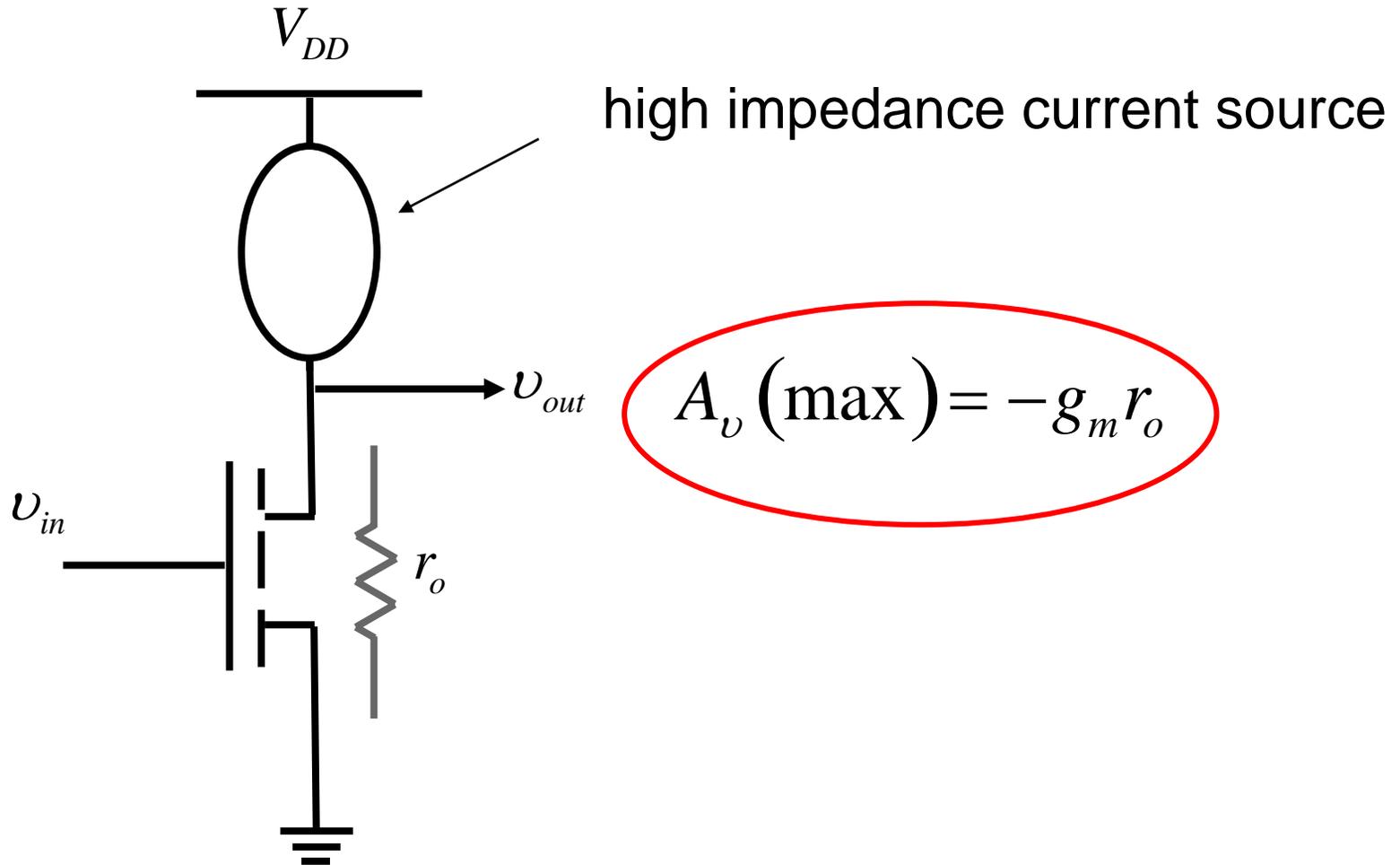


$$\frac{v_{out}}{v_{in}} = A_v = -g_m R_D$$

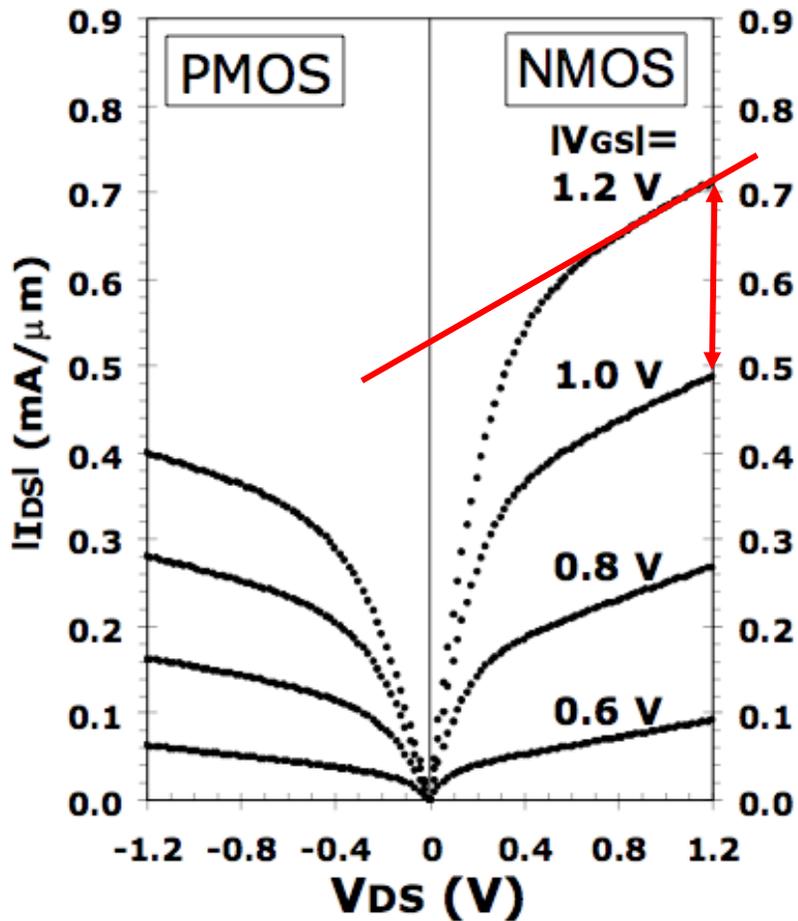
effect of output resistance



self-gain



self-gain for 65 nm digital CMOS



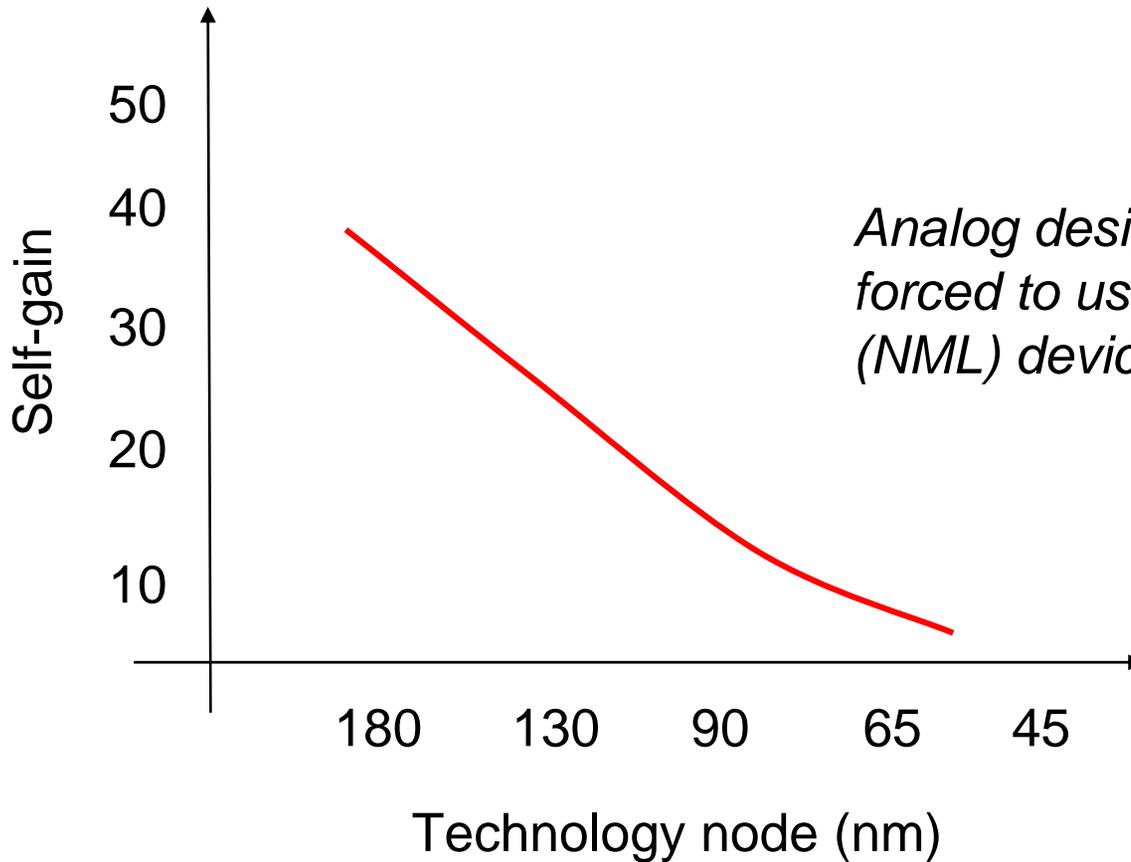
$$g_m \approx \frac{0.2 \text{ mA}/\mu\text{m}}{0.2 \text{ V}} = 1 \text{ mS}/\mu\text{m}$$

$$r_o \approx \frac{1.2 \text{ V}}{0.18 \text{ mA}/\mu\text{m}} \approx 7 \text{ K}\check{\Omega} - \mu\text{m}$$

$$|A_v(\text{max})| = g_m r_o \approx 7$$

C.-H. Jan. et al., 2005 IEDM

self-gain vs. scaling

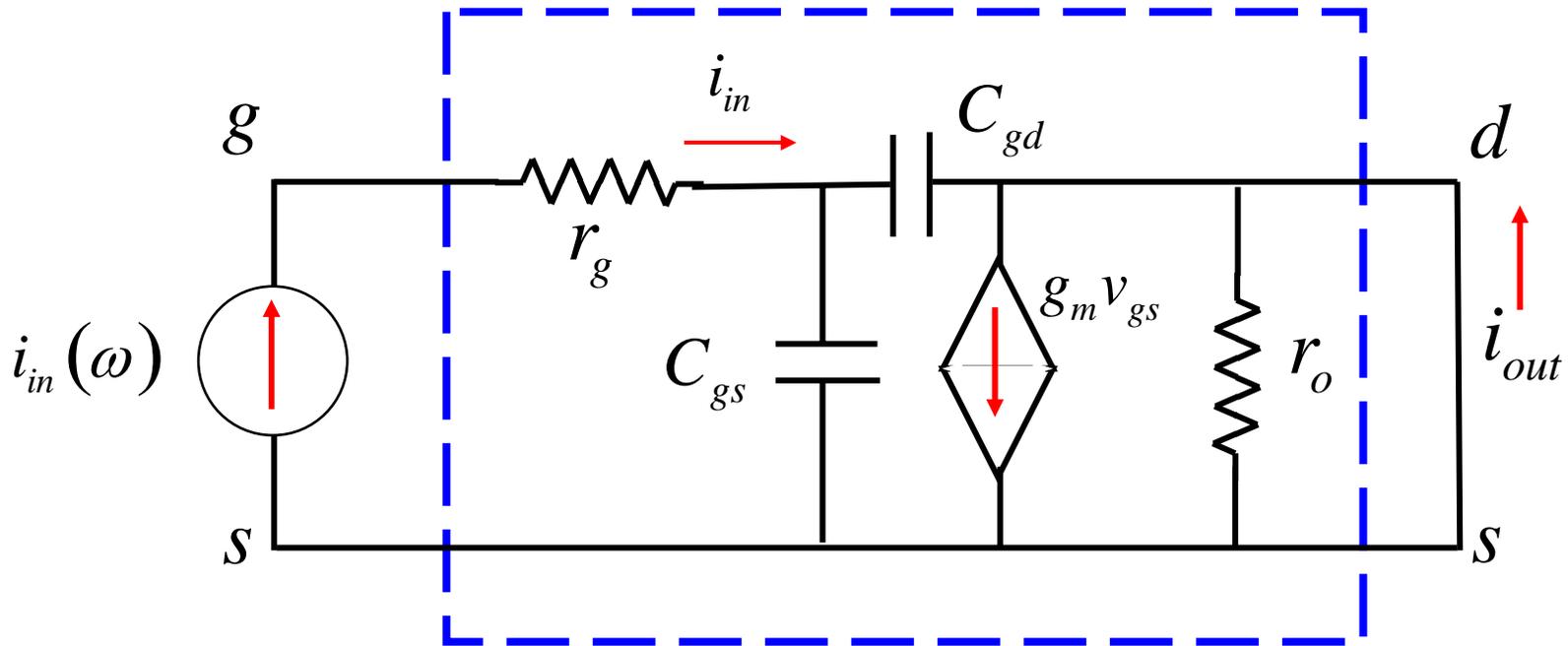


Analog designers are frequently forced to use non-minimum length (NML) devices.

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short-current current gain

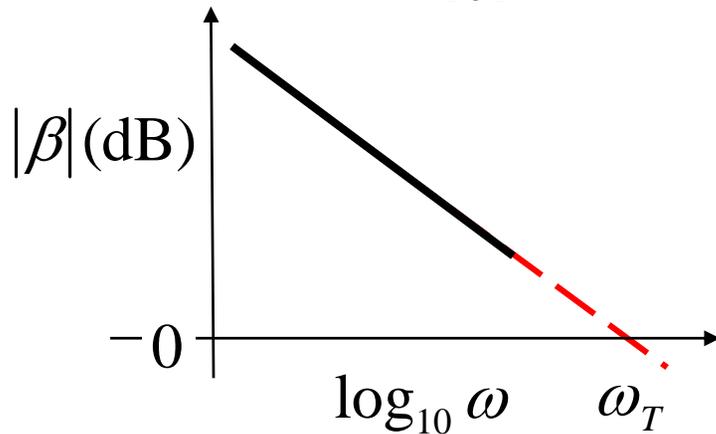


$$\left. \begin{aligned} i_{out} &\approx g_m v_{gs} \\ v_{gs} &= i_{in} \frac{1}{j\omega (C_{gs} + C_{gd})} \end{aligned} \right\} i_{out} \approx \frac{g_m}{j\omega C_{TOT}} i_{in}$$

gain-bandwidth product

$$i_{out} \approx \frac{g_m}{j\omega C_{TOT}} i_{in}$$

$$|\beta(\omega)| \approx \frac{g_m}{\omega C_{TOT}}$$



$$|\beta(\omega_T)| = 1 = \frac{g_m}{\omega_T C_{TOT}}$$

$$f_T = \frac{g_m}{2\pi C_{TOT}}$$

65 nm CMOS

$$g_m \approx 1 \text{ mS}/\mu\text{m}$$

$$C_{TOT} \approx 0.7 \text{ fF}/\mu\text{m} \quad (\text{ITRS})$$

$$f_T \approx 230 \text{ GHz}$$

gain-bandwidth product (ii)

$$\omega_T = \frac{g_m}{C_{TOT}}$$

$$g_m \approx WC_{OX}v_{SAT}$$

$$C_{TOT} \approx WLC_{OX}$$

$$\omega_T \approx \frac{v_{SAT}}{L} = \frac{1}{t_t}$$

device delay metric

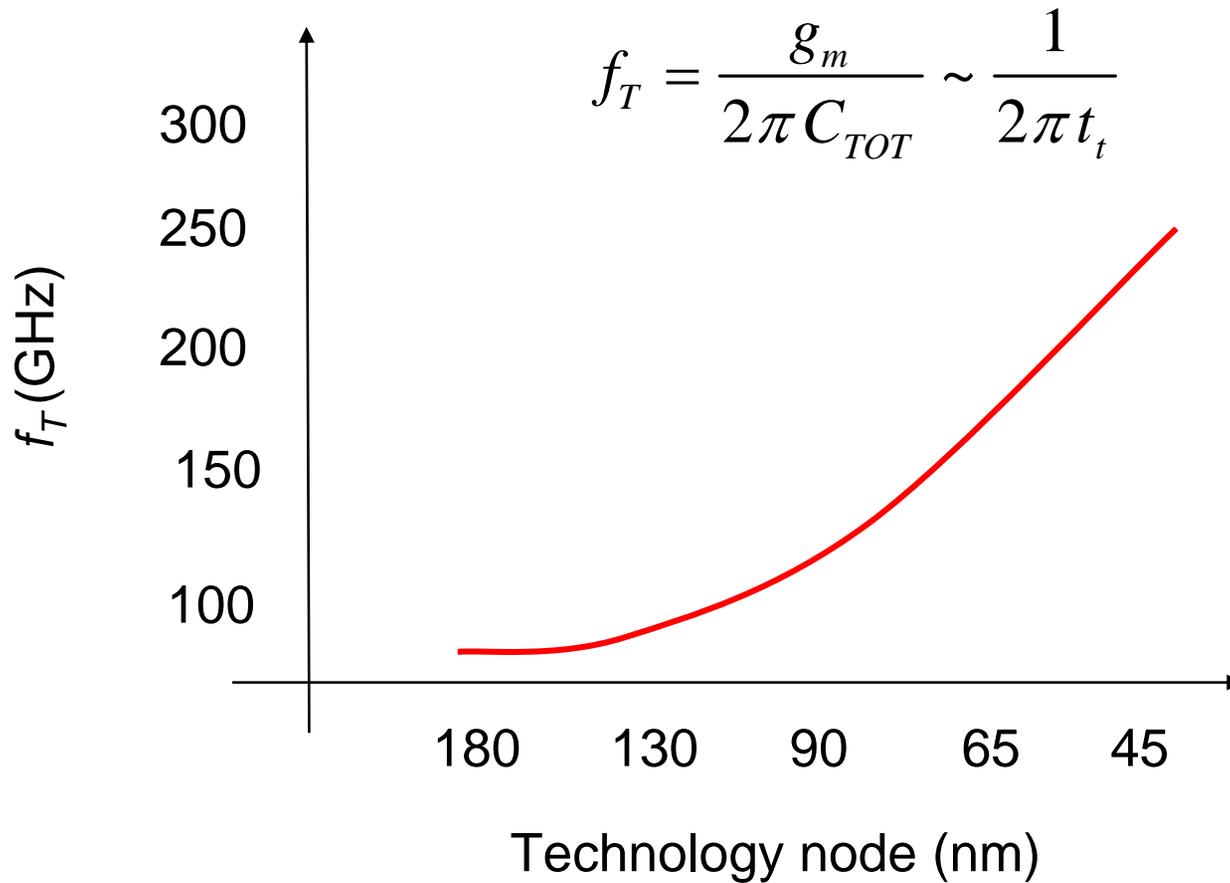
$$\tau = \frac{C_G V_{DD}}{I_{ON}}$$

65 nm NMOS:

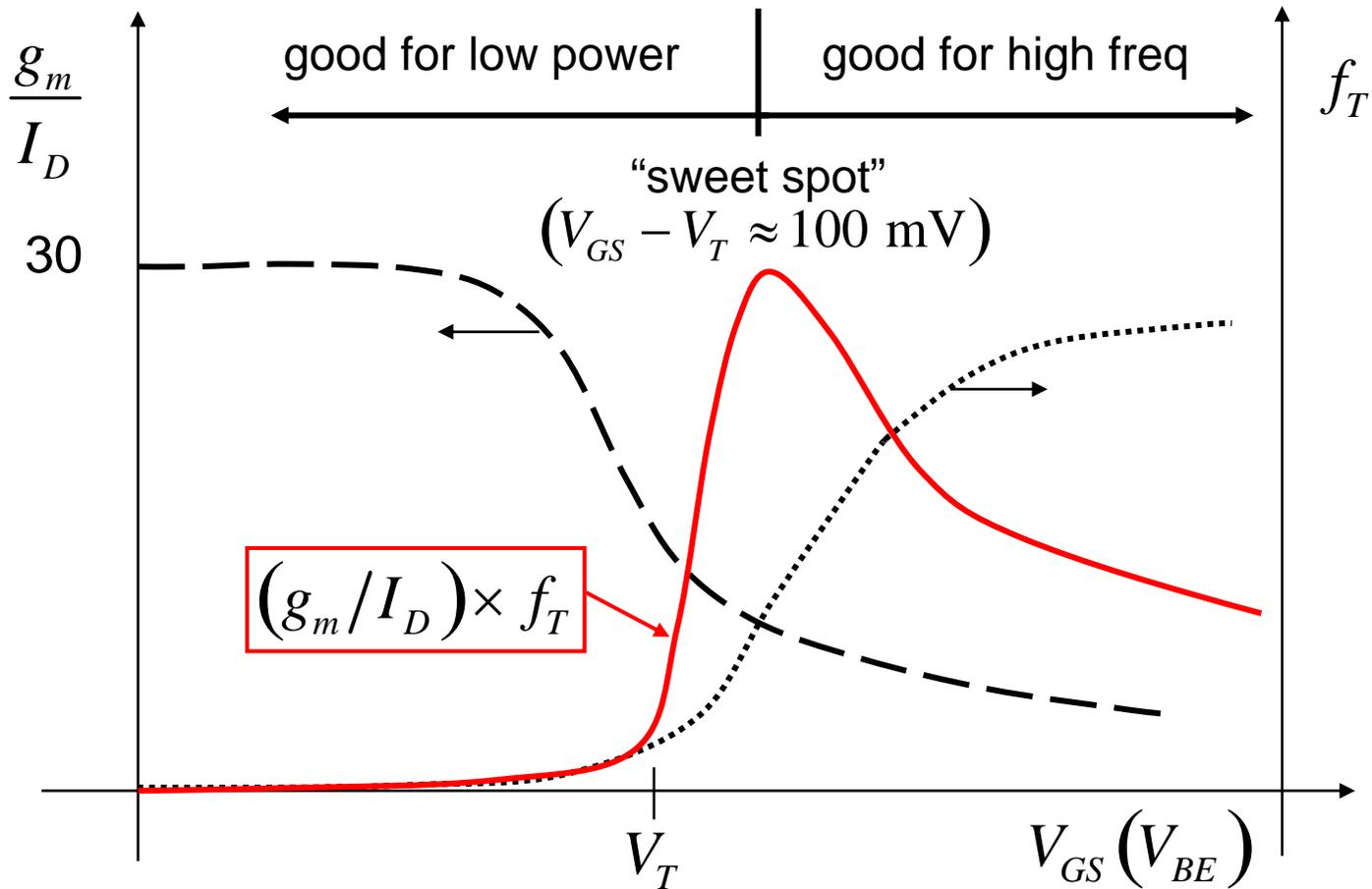
$$\tau \approx 1 \text{ ps}$$

$$\frac{1}{2\pi\tau} \approx 160 \text{ GHz}$$

f_T vs. scaling



$$g_m / I_D \times f_T$$



B. Murmann, P. Nikaeen, D.J. Connelly, and R. W. Dutton, "Impact of Scaling in Analog Performance and Associated Modeling Needs, *IEEE Trans. Electron Dev.*, 2006.

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f_{max}

$$f_T = \frac{g_m}{2\pi C_{TOT}}$$

insensitive to r_g and r_o

independent of W

channel length scaling
increases g_m and lowers C_{TOT}

$$f_{MAX} \approx \frac{\omega_T}{\sqrt{4r_g \left(\frac{1}{r_o} + \omega_T C_{gd} \right)}}$$

sensitive to
parasitics

$$\begin{aligned} -r_g &\sim W \\ -r_o &\sim 1/W \\ -C_{gd} &\sim W \end{aligned}$$

need small W

channel length scaling
increases r_g and lowers r_o

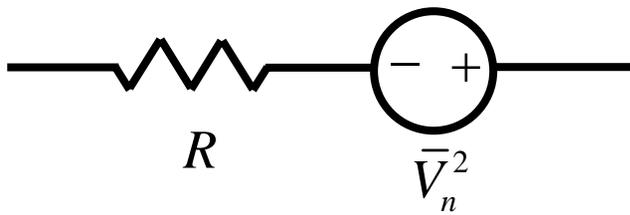
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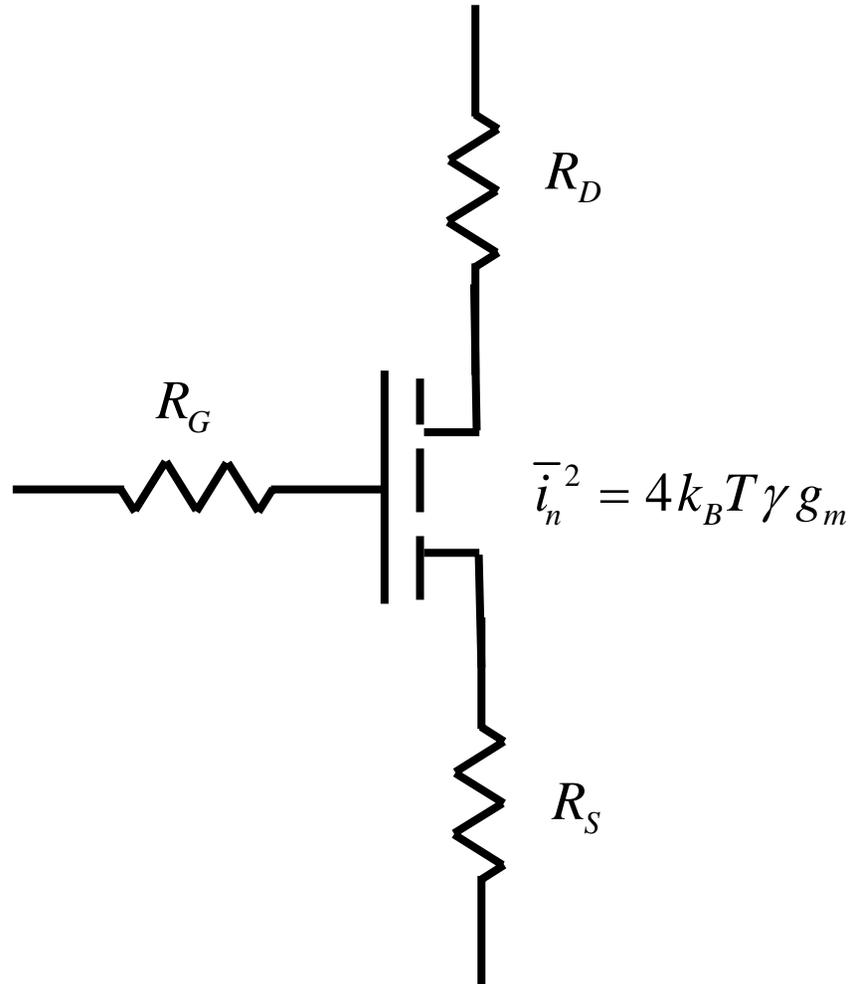
thermal noise

thermal noise

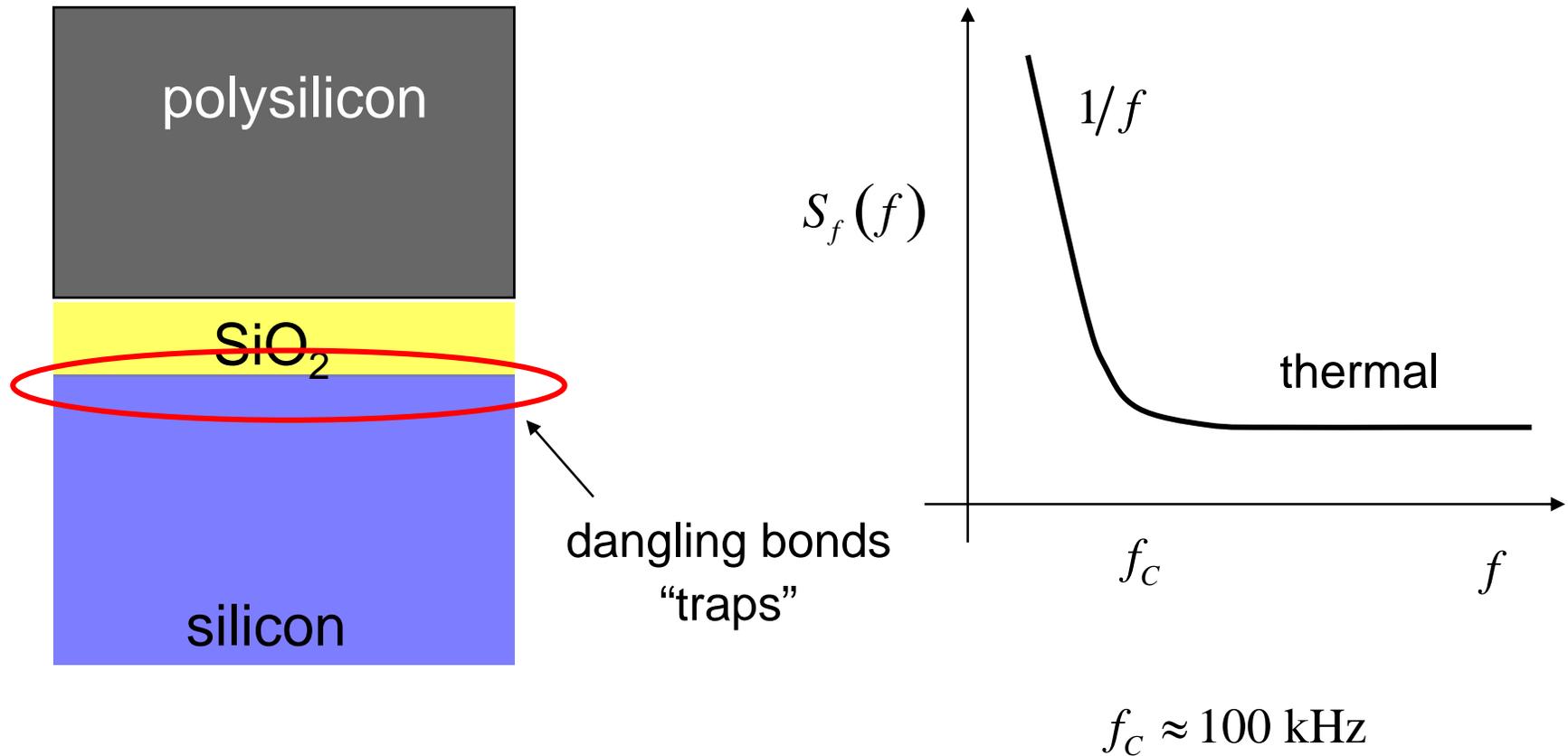
Johnson noise



$$\bar{V}_n^2 = S_f(f)\Delta f = 4k_B T R \Delta f$$

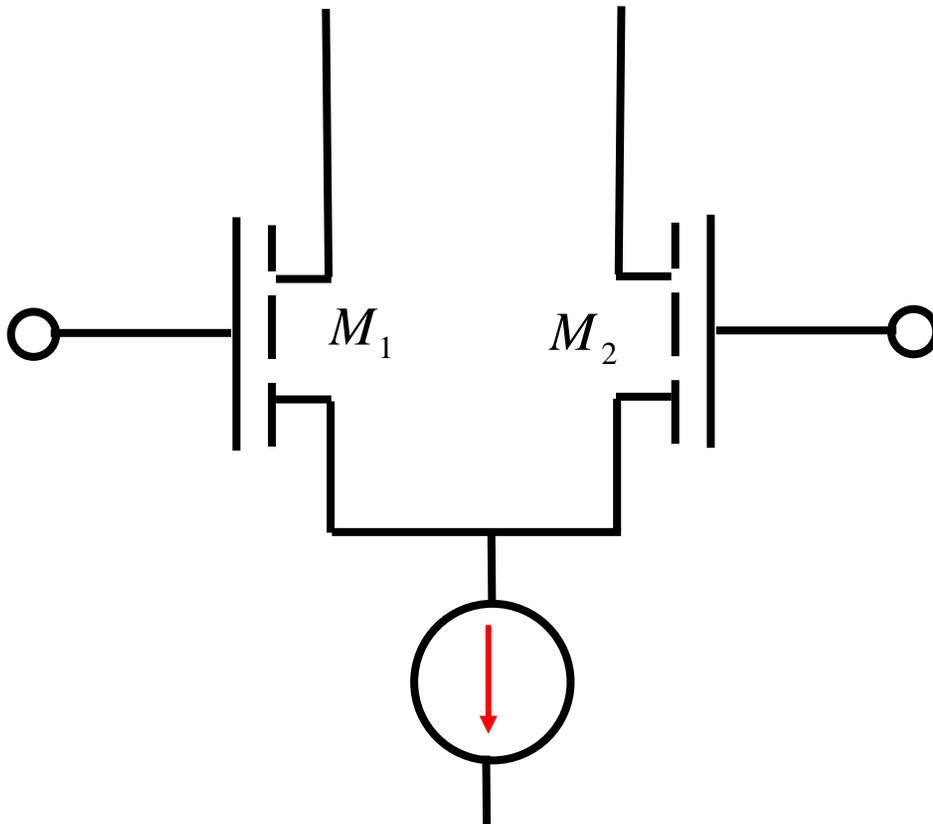


1/f “flicker” noise



mismatch

differential pair



analog circuits make use of matched transistors

sources of mismatch:

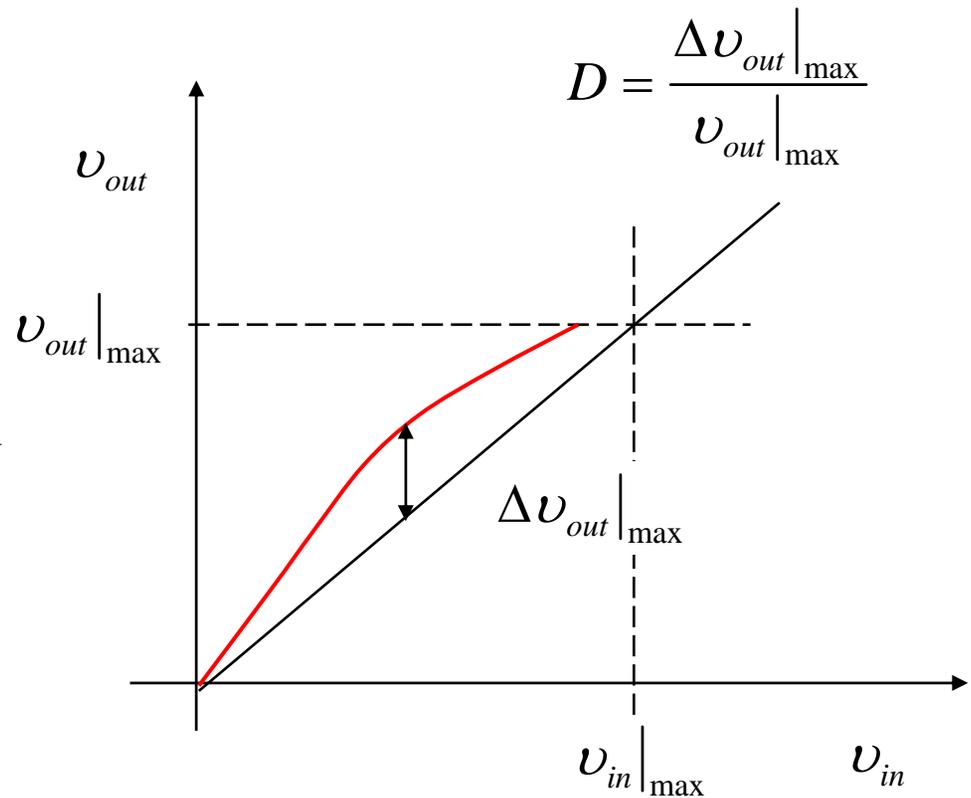
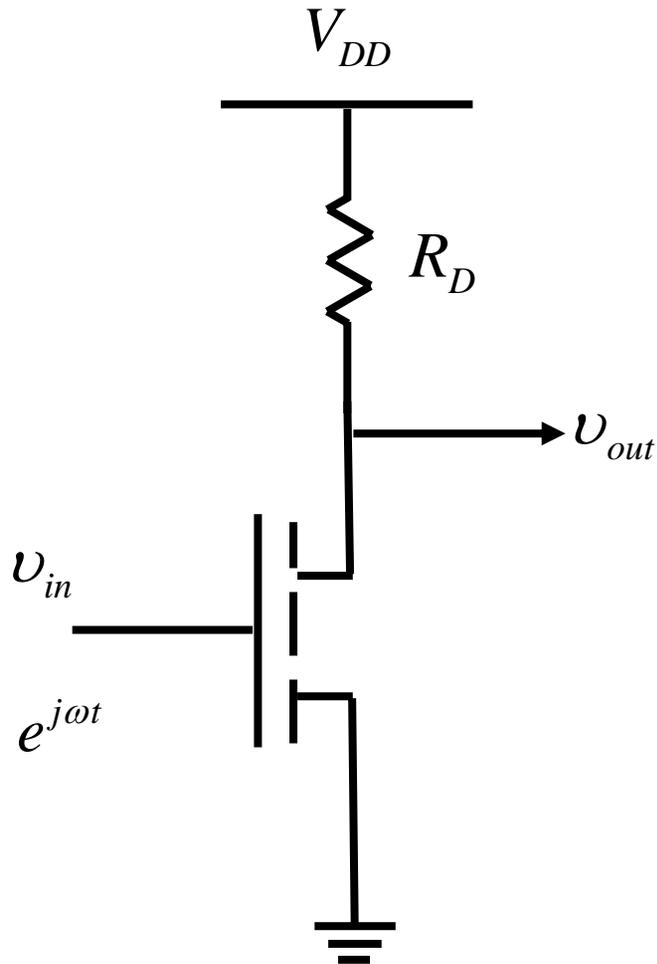
- variations in geometry
- ΔV_T , $\Delta T_{ox}, \dots$
- thermal effects, etc.

$$\Delta A = \frac{K}{\sqrt{WL}}$$

dealing with mismatch:

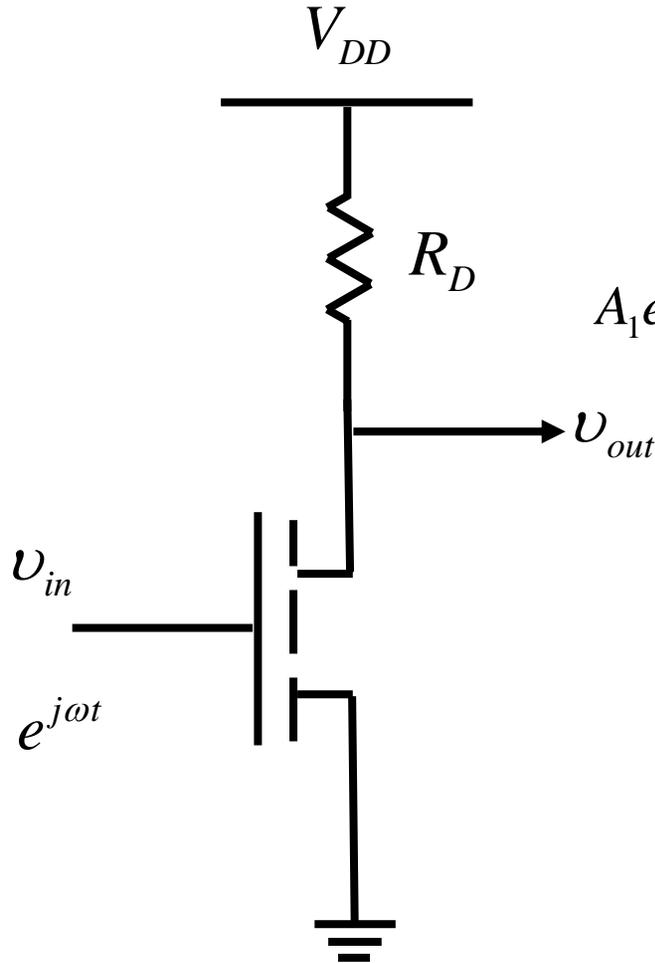
- circuit design
- careful layout

linearity



(below threshold)

harmonic distortion



$$A_1 e^{j\omega t} + A_2 e^{j2\omega t} + A_3 e^{j3\omega t} + \dots$$

$$i_d = \frac{\partial I_D}{\partial V_{gs}} v_{gs} + \frac{1}{2!} \frac{\partial^2 I_D}{\partial V_{gs}^2} v_{gs}^2 + \frac{1}{3!} \frac{\partial^3 I_D}{\partial V_{gs}^3} v_{gs}^3 + \dots$$

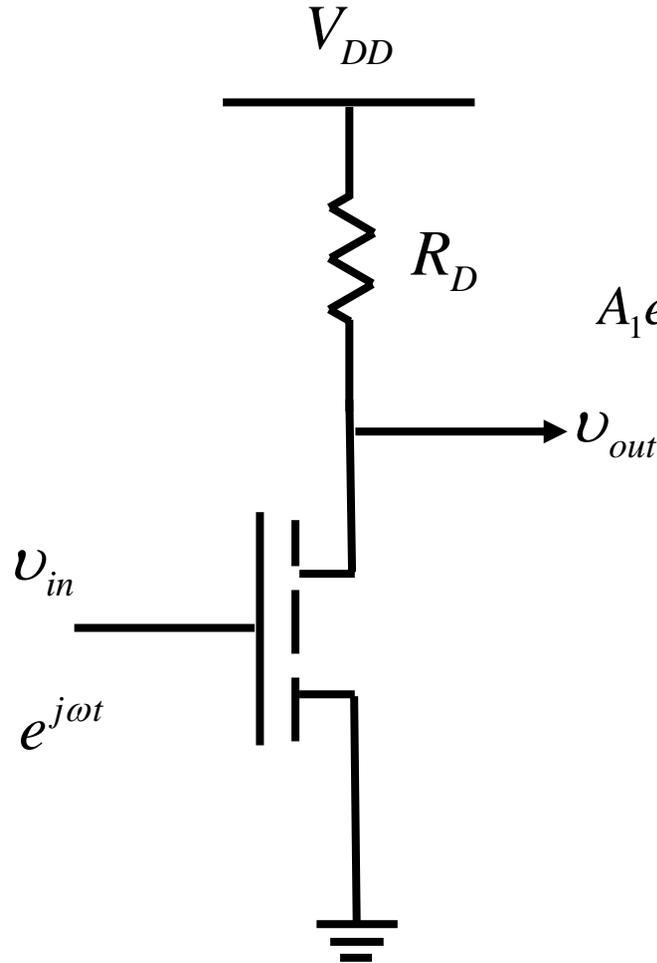
$$i_d = g_{m1} v_{gs} + g_{m2} v_{gs}^2 + g_{m3} v_{gs}^3 + \dots$$

$$VIP_2 \quad VIP_3$$

extrapolated gate voltage amplitude at which
the amplitude of the harmonic = amplitude of
fundamental

Audio Missing

harmonic distortion



$$A_1 e^{j\omega t} + A_2 e^{j2\omega t} + A_3 e^{j3\omega t} + \dots$$

$$i_d = \frac{\partial I_D}{\partial V_{gs}} v_{gs} + \frac{1}{2!} \frac{\partial^2 I_D}{\partial V_{gs}^2} v_{gs}^2 + \frac{1}{3!} \frac{\partial^3 I_D}{\partial V_{gs}^3} v_{gs}^3 + \dots$$

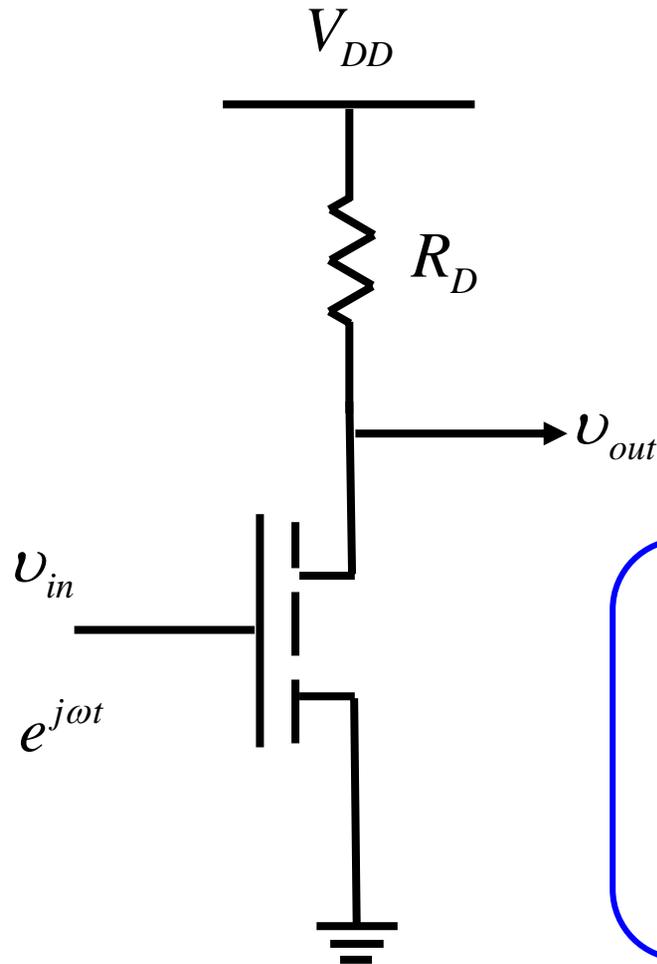
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extrapolated gate voltage amplitude at which
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Audio Missing

distortion and the devices



$$A_1 e^{j\omega t} + A_2 e^{j2\omega t} + A_3 e^{j3\omega t} + \dots$$

$$i_d = \frac{\partial I_D}{\partial V_{gs}} v_{gs} + \frac{1}{2!} \frac{\partial^2 I_D}{\partial V_{gs}^2} v_{gs}^2 + \frac{1}{3!} \frac{\partial^3 I_D}{\partial V_{gs}^3} v_{gs}^3 + \dots$$

$$I_D \sim (V_{GS} - V_T)^\alpha \quad (\text{above threshold})$$

DIBL

$$I_D \sim e^{qV_{GS}/k_B T} \quad (\text{below threshold})$$

Audio Missing

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