Inter-band Tunnel Transistors: Opportunities and Challenges

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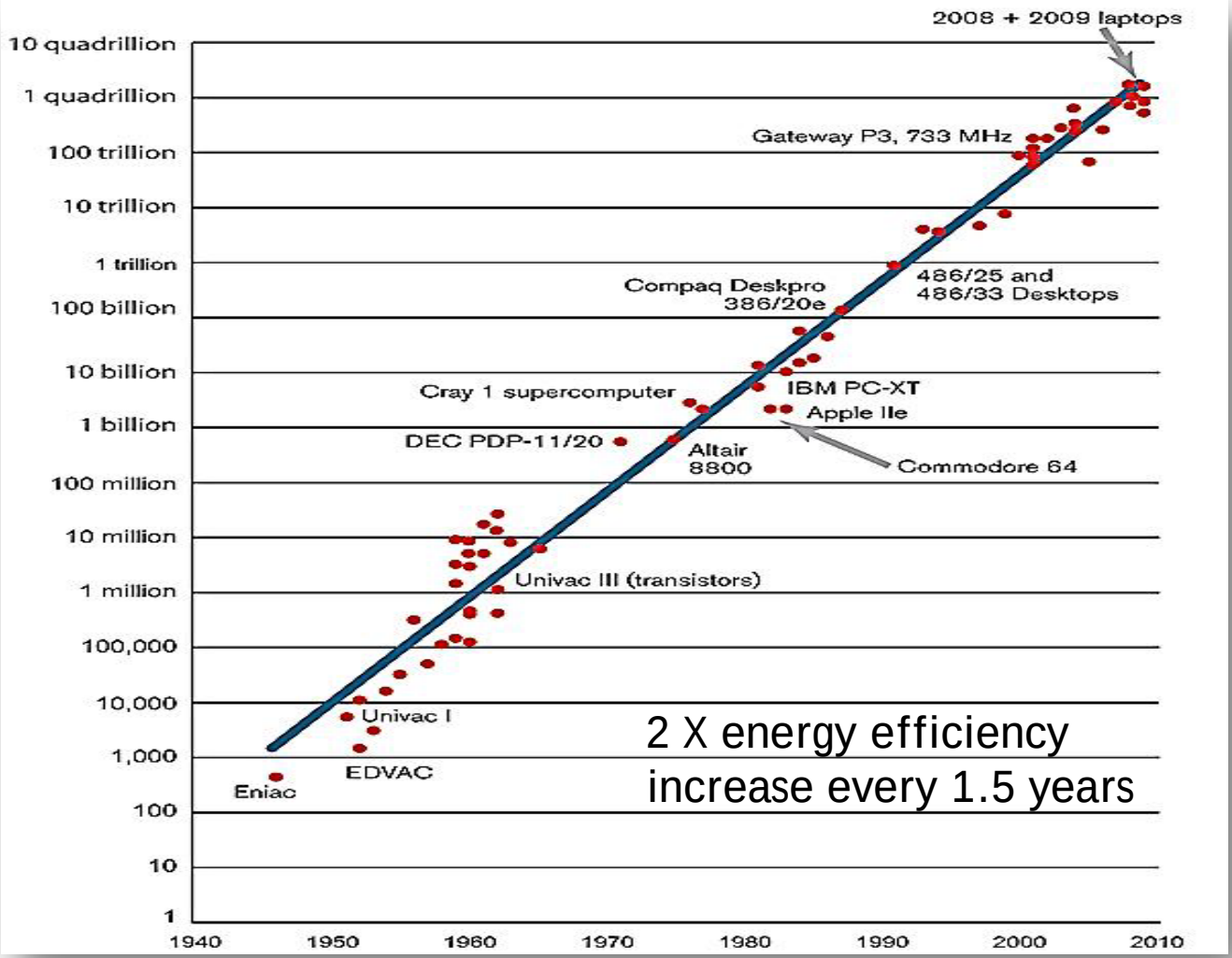
Outline

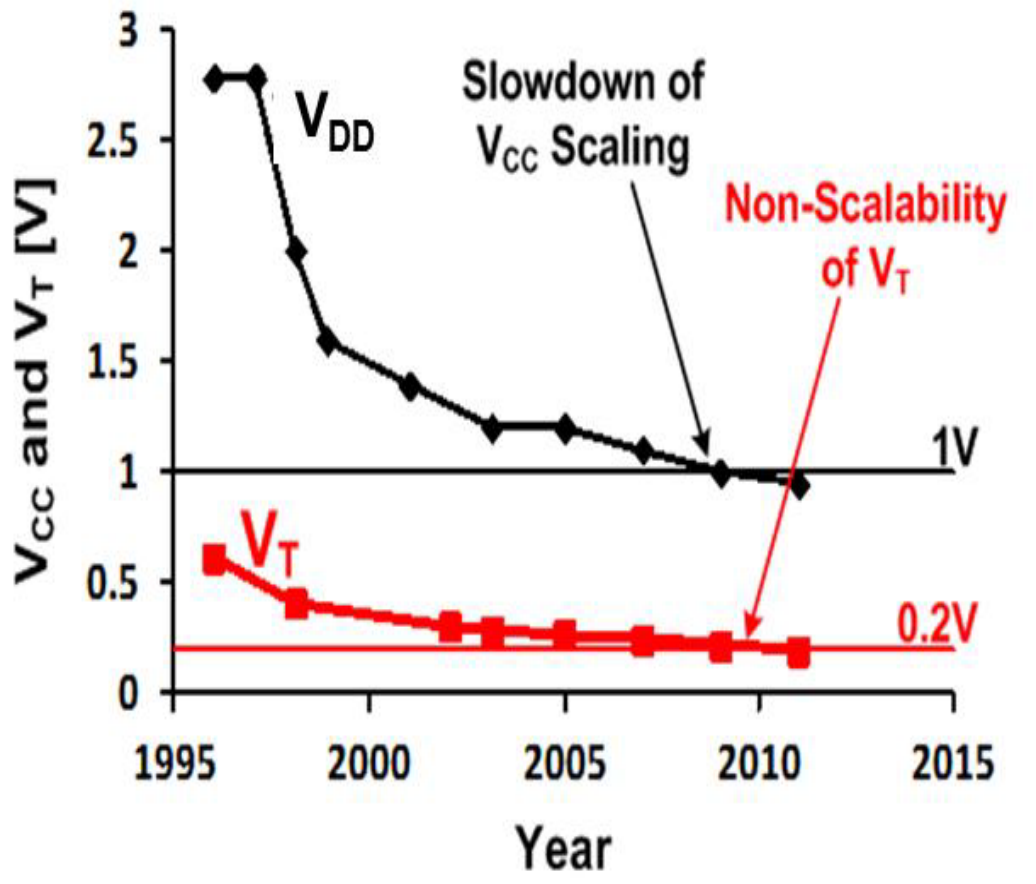
- FinFETs and GAA NW FETs
- Promise of Inter-band Tunnel FETs
- Experiments
- Benchmarking
- Much remain to be done

Computation per kW-hr



Computing gets cheaper and energy efficient

Voltage Scaling



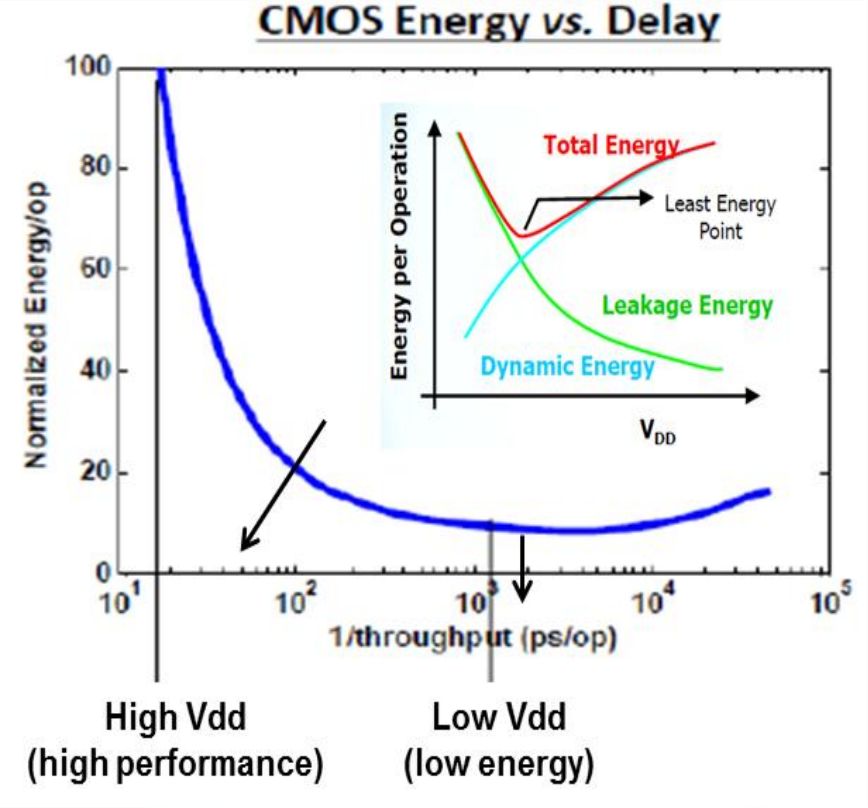
$$I_{on} = C_{gate} v_{eff} (V_{dd} - V_{th})$$

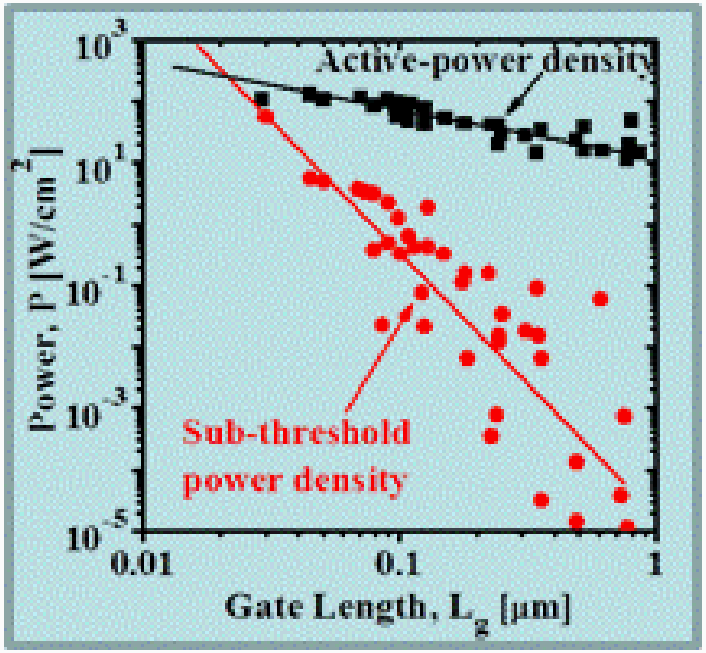
$$I_{off} = I_o 10^{-V_{th}/SS}$$

Constant field scaling worked before

Recent years, voltage scaling has slowed down

Challenges





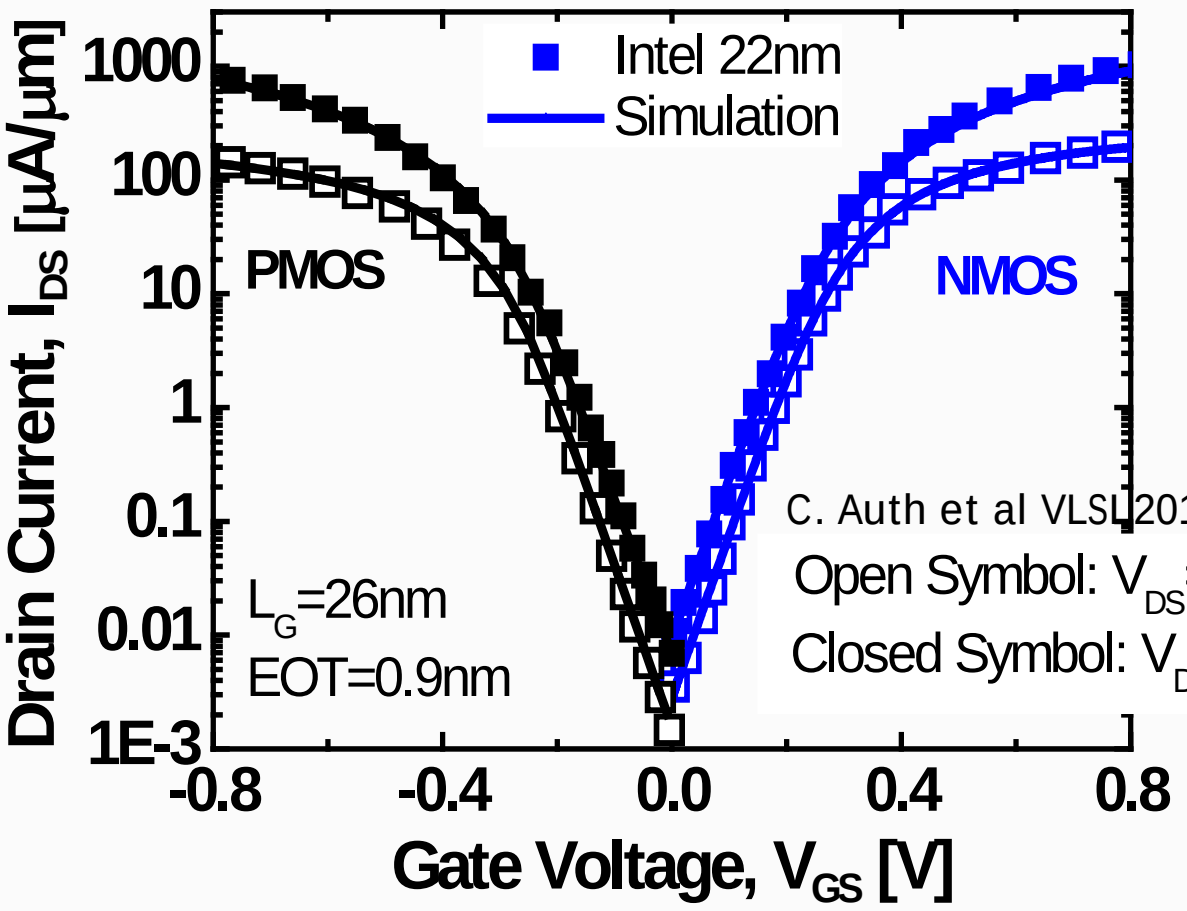
$$E = \tfrac{1}{2} C_{gate} V_{DD}^2 \alpha + I_{leak} V_{DD} \tau$$

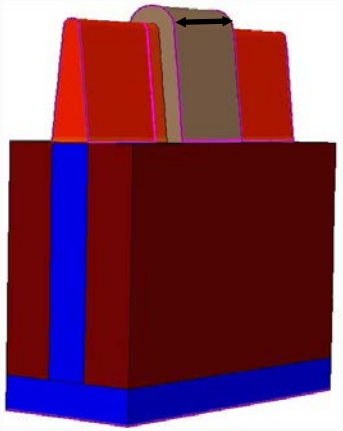
$$I_{on} = C_{gate} v_{eff} (V_{dd} - V_{th})$$

$$I_{off} = I_o 10^{-V_{th}/SS}$$

- increase veff
- reduce SS

Si CMOS

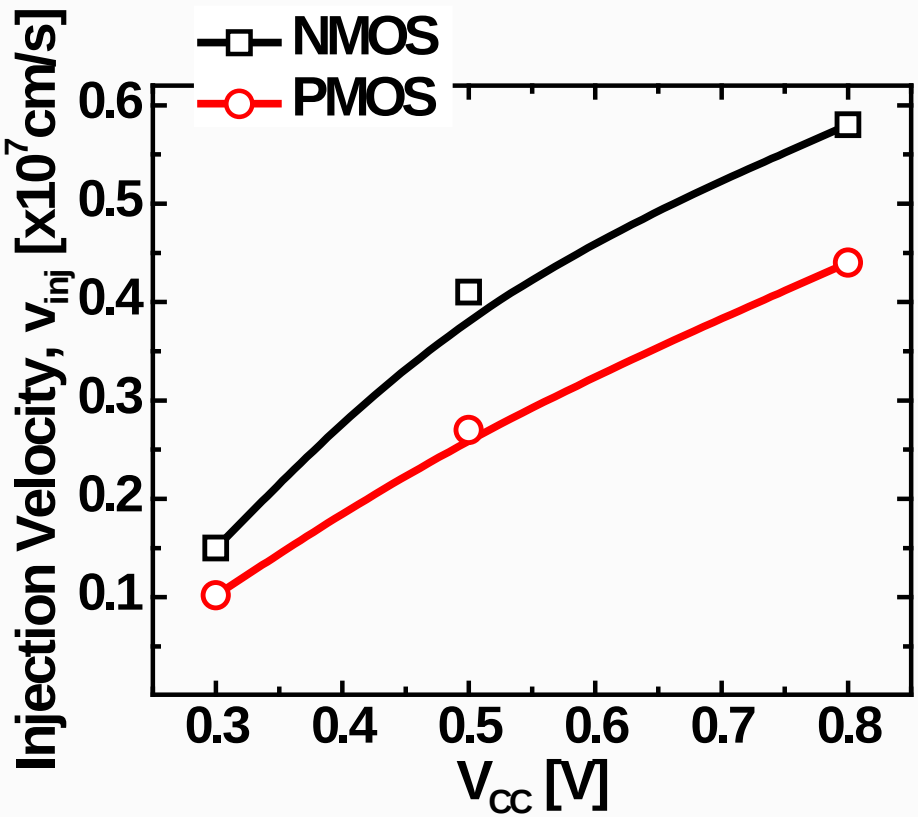


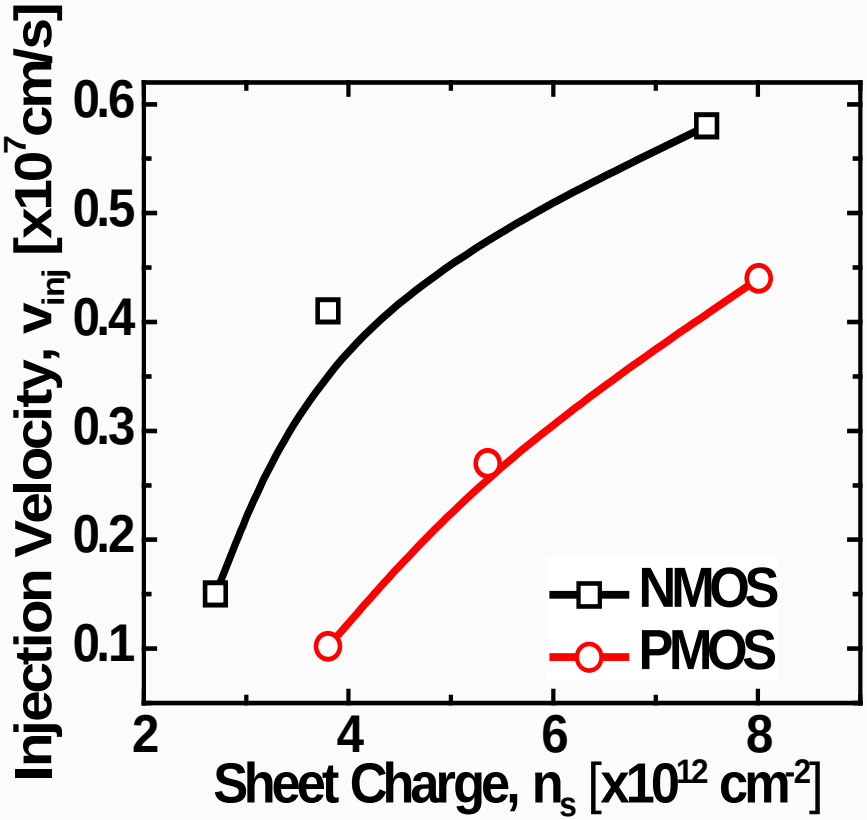


Chipworks

3D Continuum model (modified drift-diffusion and quantum corrected density gradient approximation) captures Id-Vg

Injection Velocity: 22nm Si CMOS

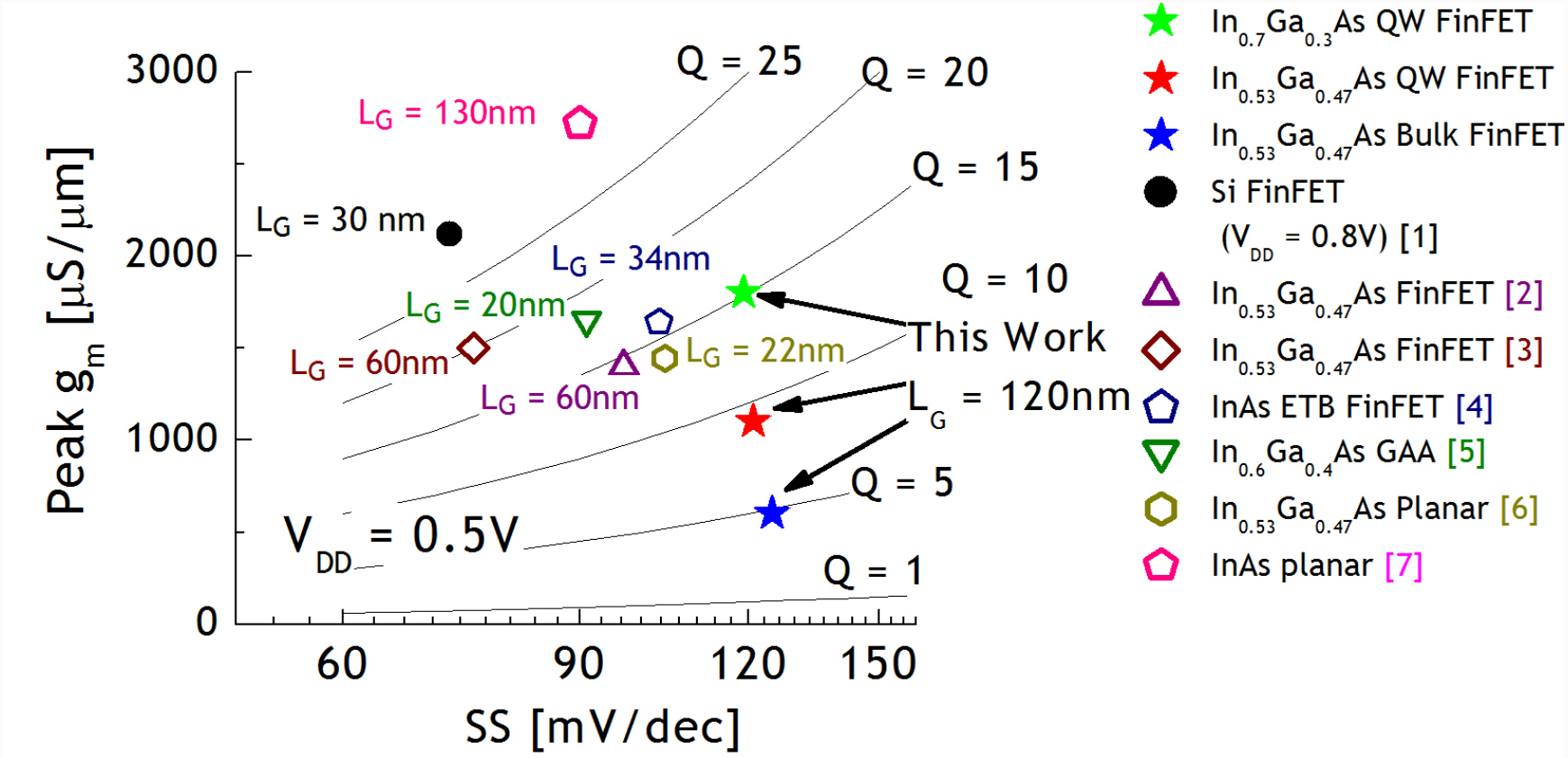




Injection velocity in the range of 4 to 6 x10^6 cm/s

Carrier density in the range of 6 to 8 x10^{12} /cm^2

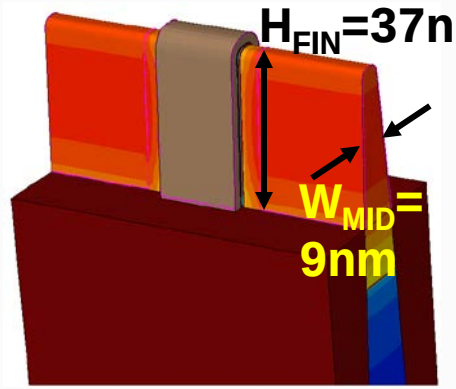
g_m vs. SS benchmarking



- Q factor improves with higher In % and quantum confinement
- Q = 15 measured for $In_{0.7}Ga_{0.3}As$ QW FinFET

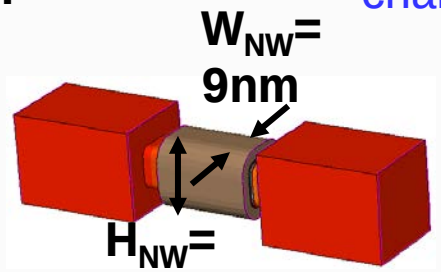
[1] C Auth *et al*, VLSI 2012 (Intel) [2] M Radosavljevic *et al*, IEDM 2011 (Intel) [3] T W kim *et al*, IEDM 2013 (sematech) [4] S H Kim *et al*, IEDM 2013 [5] JJ Gu *et al*, IEDM 2012 [6] J Lin *et al*, IEDM 2012 [7] S W Chang *et al*, IEDM 2013 (TSMC)

Multi-Nanowire GAA: Architectures



14nm Si Bulk FF

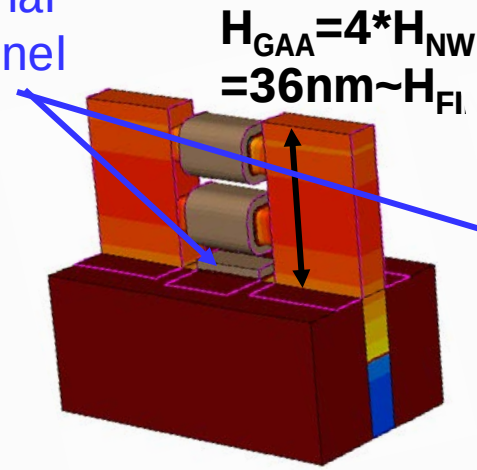
- ✓ L_G=20nm, W_{MID}=9nm, H_{FIN}=37nm



14nm Si GAA (1NW)

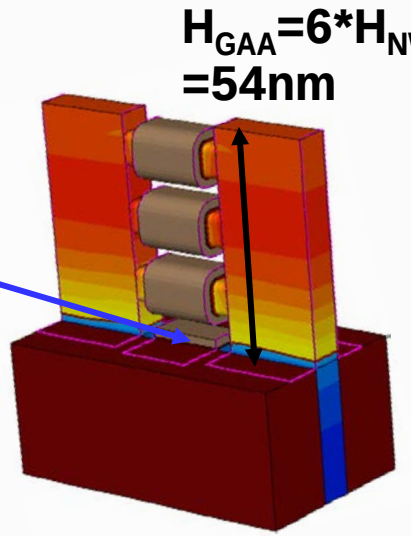
- ✓ L_G=20nm, W_{NW}=9nm, H_{NW}=9nm

Additional "planar" channel



14nm Si GAA (2NW)

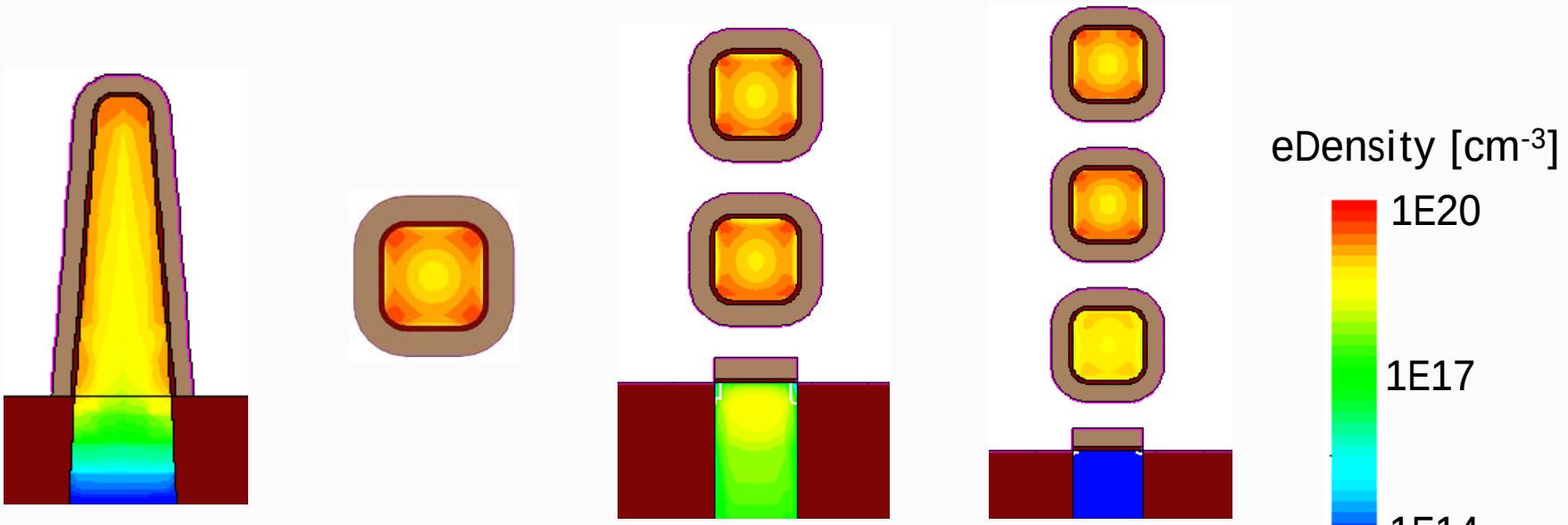
- ✓ L_G=20nm, W_{NW}=9nm, H_{NW}=9nm
- ✓ H_{GAA}=4*H_{NW}=36nm~H_{FIN}
- ✓ Additional "planar" channel at the lowest SiGe layer removal



14nm Si GAA (3NW)

- ✓ L_G=20nm, W_{NW}=9nm, H_{NW}=9nm
- ✓ H_{GAA}=6*H_{NW}=54nm
- ✓ Additional "planar" channel at the lowest SiGe layer removal

Electron Density Comparison

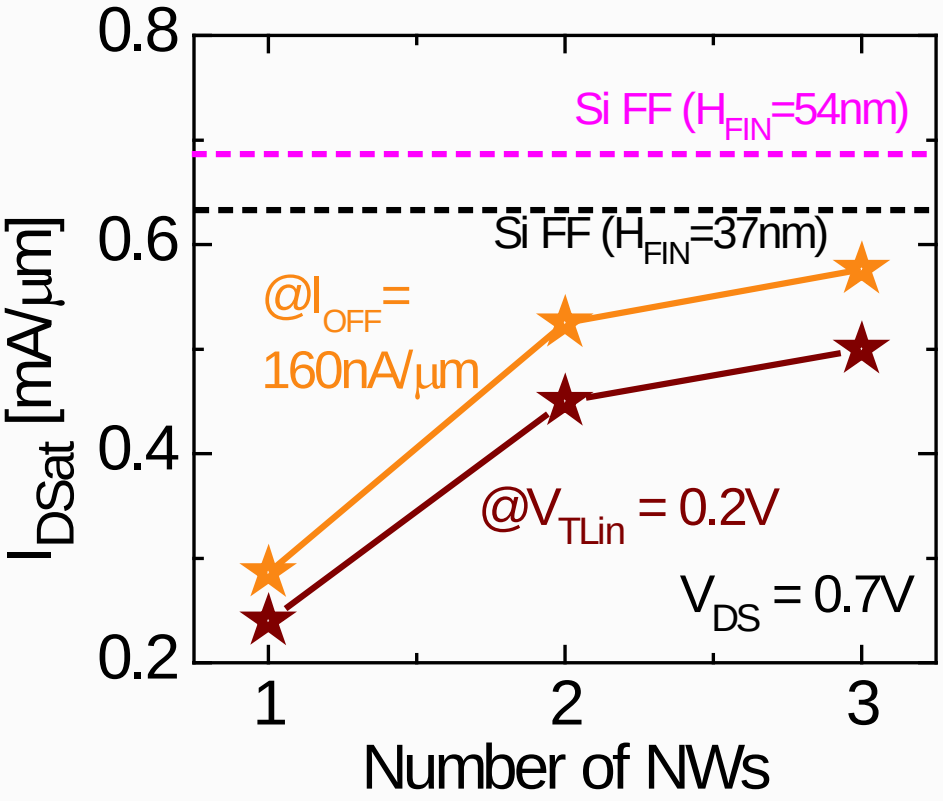


(a) Si FinFET (b) 1-NW GAA (c) 2-NW GAA (d) 3-NW GAA

- Less electrostatic control at the wider bottom of FinFET
  - Better DIBL and SS in GAA than FinFET
- High electron density along the entire height of the FinFET
  - Higher ON current in FinFET than GAA
- Bottommost NW of 3-NW GAA contributes very less electrons due to the increased access resistance (SD doping profile slide 5)

FinFETs vs GAA NWFETs

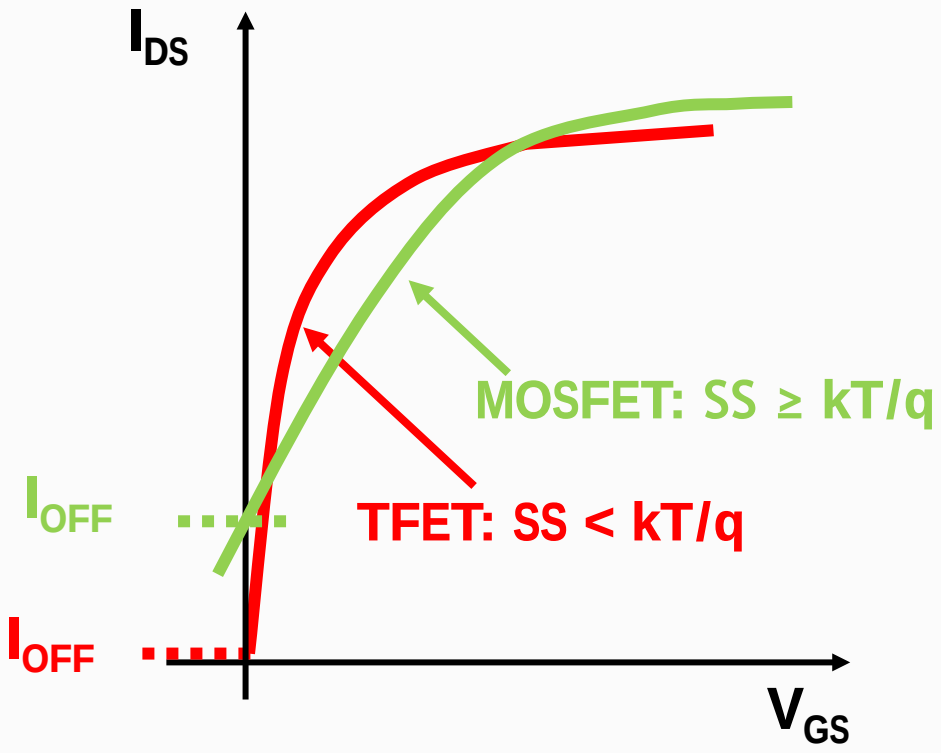
Normalization Scheme: $1\mu m_{layout}$ = 10 fins or Pillars



Parameters	I_{ON} (mA/μm) @V_{GS}=V_{DS}=0.7 V	$\Delta I_{ON}/I_{ON\_FF}$
Si FinFET	0.630	0
1 NW GAA	0.286	-0.55
2 NW GAA	0.525	-0.17
3 NW GAA	0.576	-0.09
Si FF (H_{FIN}=54nm)	0.690	+0.095

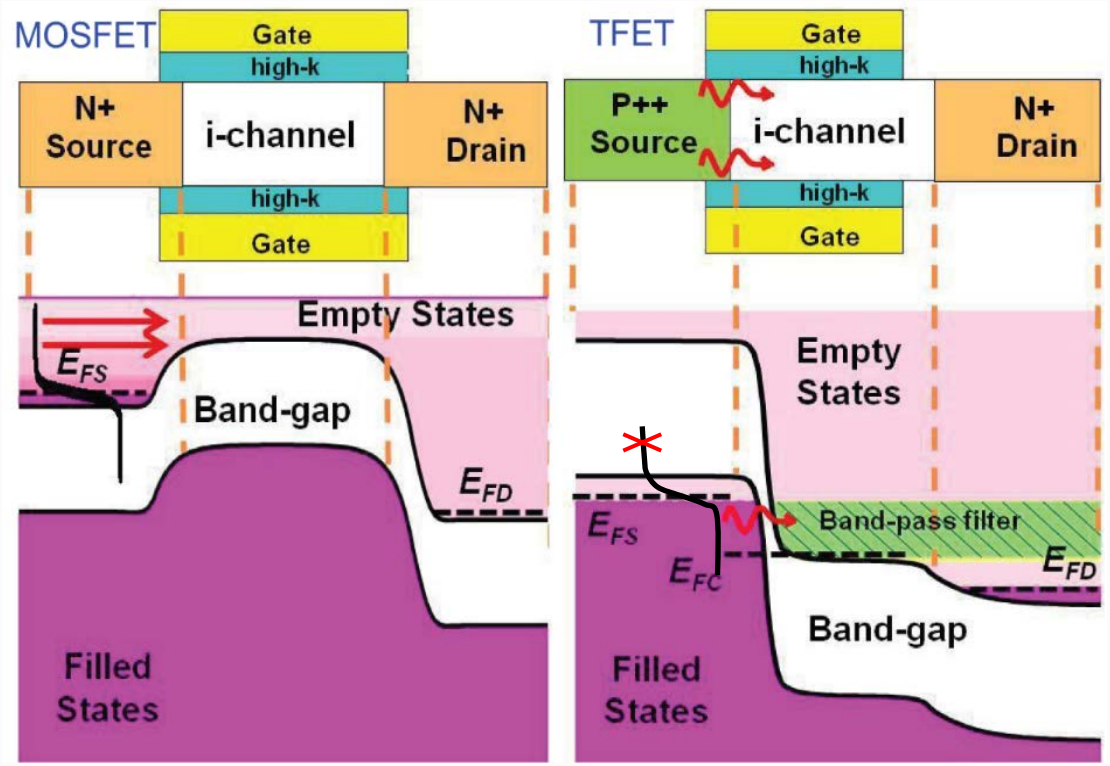
The Si FF with H_{FIN}=54nm shows about 17% higher I_{ON} than the equivalent 3 NW GAA device

Inter-band Tunnel FET: steep switching FET



✓ **Promise of Tunnel FETs is based on sub-kT/q operation**

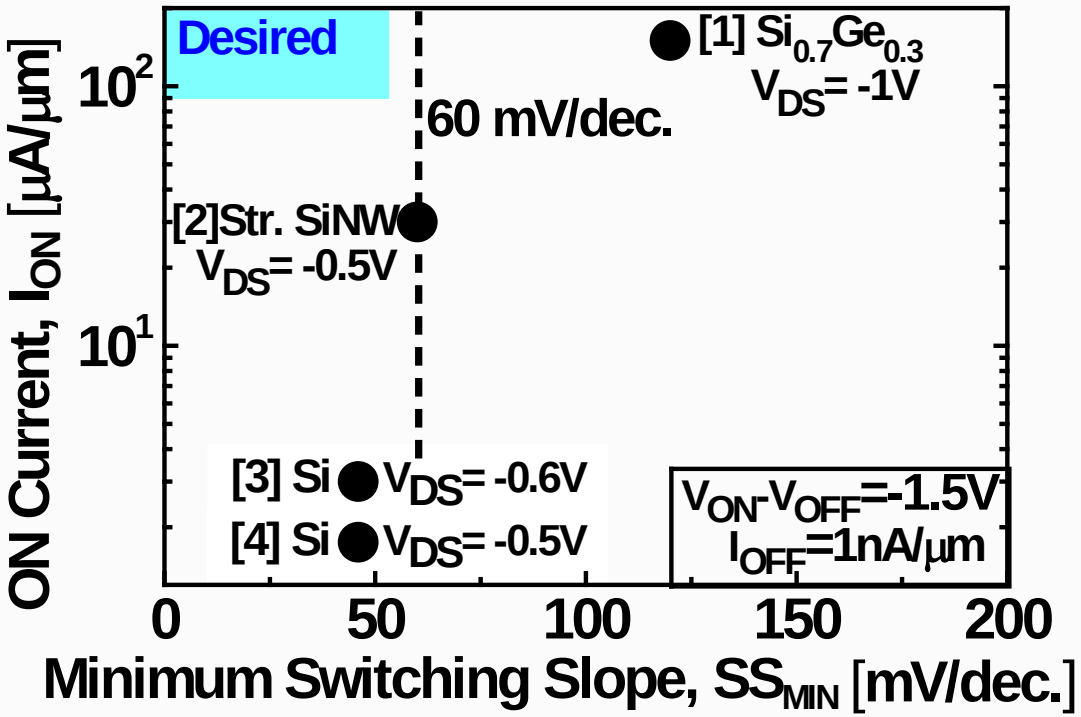
Tunnel FET: steep switching MOSFET alternative

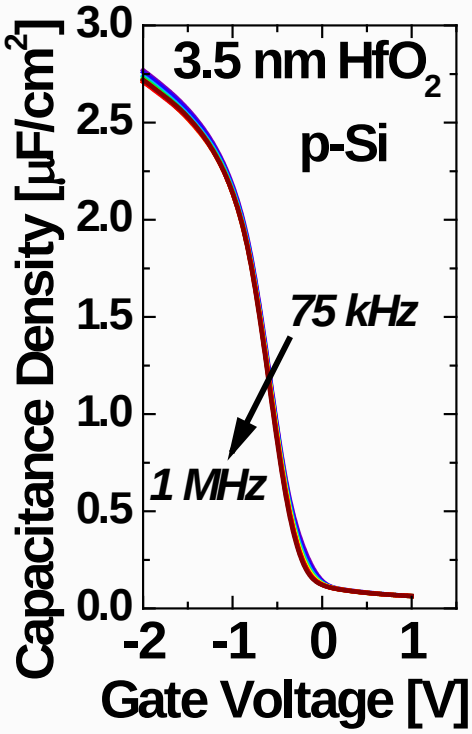


Thermionic emission **Interband-tunneling**

- ✓ **High energy tail carrier distribution filtered during source to channel tunneling leading to Sub kT/q switching**

P-channel TFET: State of Art

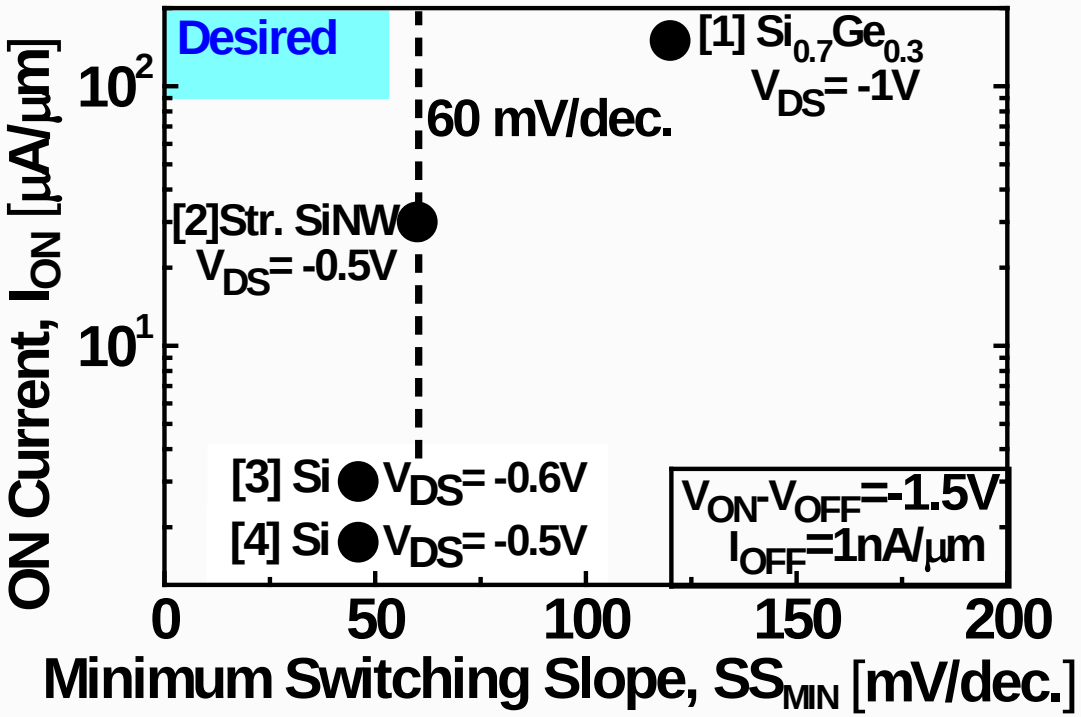


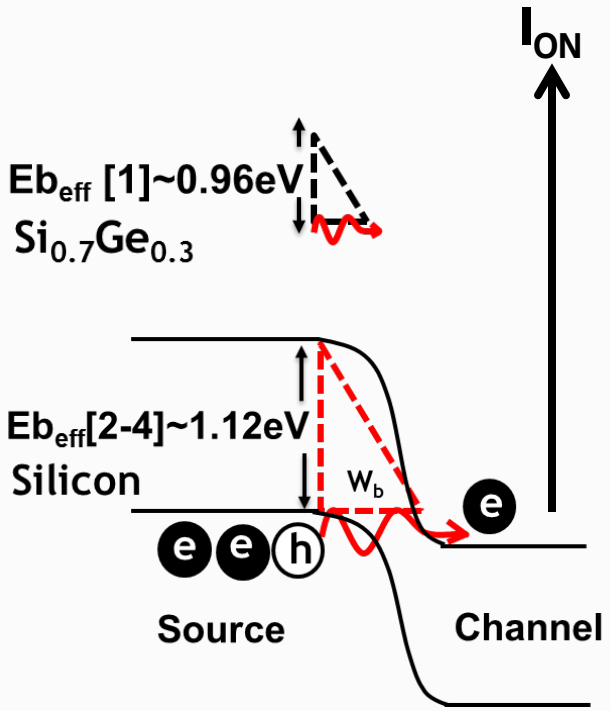


- ✓ SS_{MIN} limited by High-K/channel interface trap density [D_{it}]
- ✓ Si-channel based TFET have excellent interfaces [D_{it}<$10^{12}cm^{-2}eV^{-1}$]

[1] A. Villalon et al., TED, Dec. 2013
[2] L. Knoll et al., IEDM, 2013
[3] D. Leonelli et al., JJAP, 2010
[4] K. Jeon et al., VLSI, 2010

P-channel TFET: State of Art

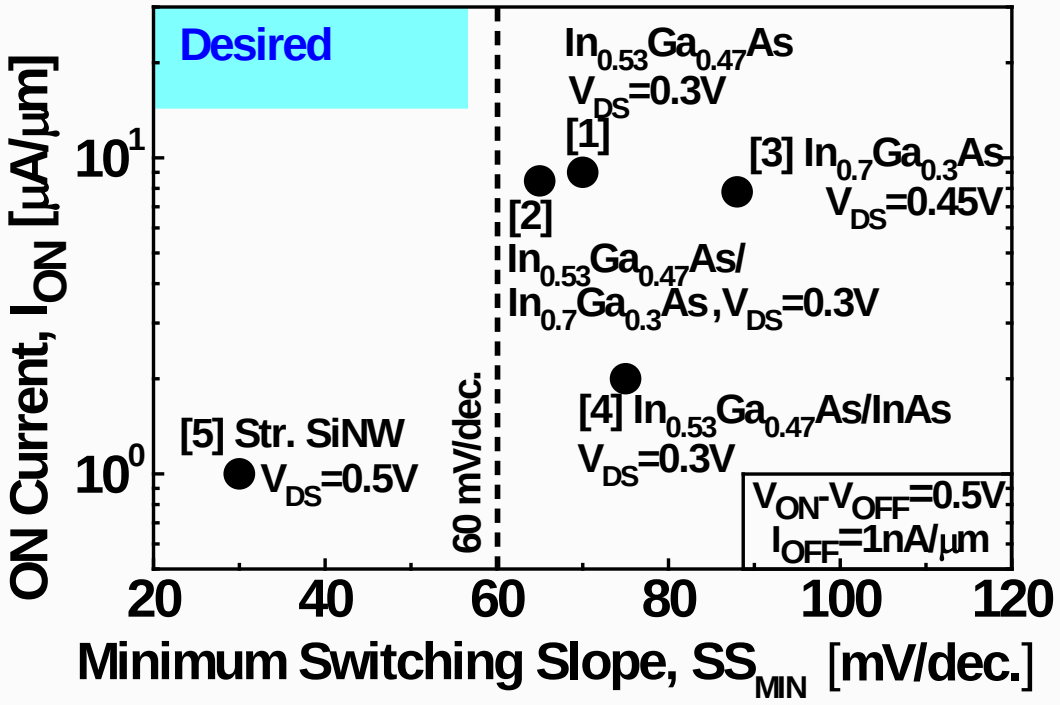


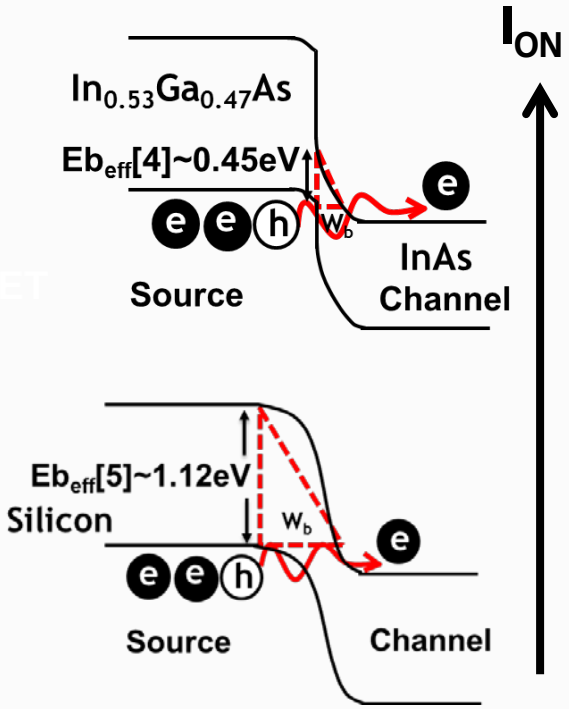


- ✓ I_{ON} limited by tunnel barrier height [Eb_{eff}]
- ✓ Si based TFET have high Eb_{eff}

[1] A. Villalon et al., TED, Dec. 2013
[2] L. Knoll et al., IEDM, 2013
[3] D. Leonelli et al., JJAP, 2010
[4] K. Jeon et al., VLSI, 2010

N-channel TFET: State of Art





	Ebeff [eV]
[1]	0.74
[2]	0.59
[3]	0.59

✓ **III-V staggered Hetero-junction TFET**

- Eb_{eff} can be engineered to provide high I_{ON}

[1] Noguchi et al., IEDM, 2013

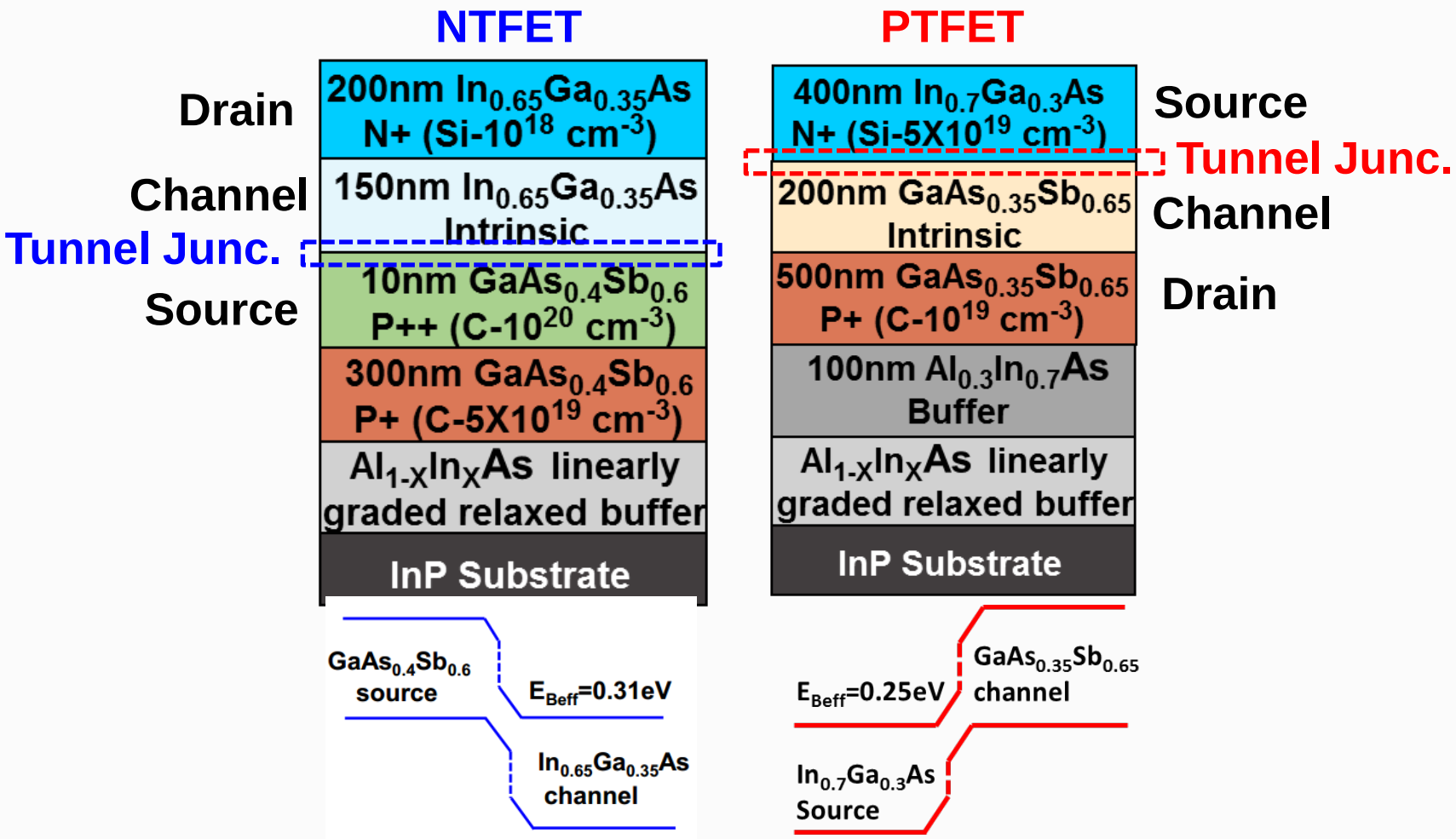
[2] G. Dewey et al., IEDM, 2011

[3] H. Zhao et al., EDL, Dec. 2010

[4] X. Zhao et al., IEDM, 2014

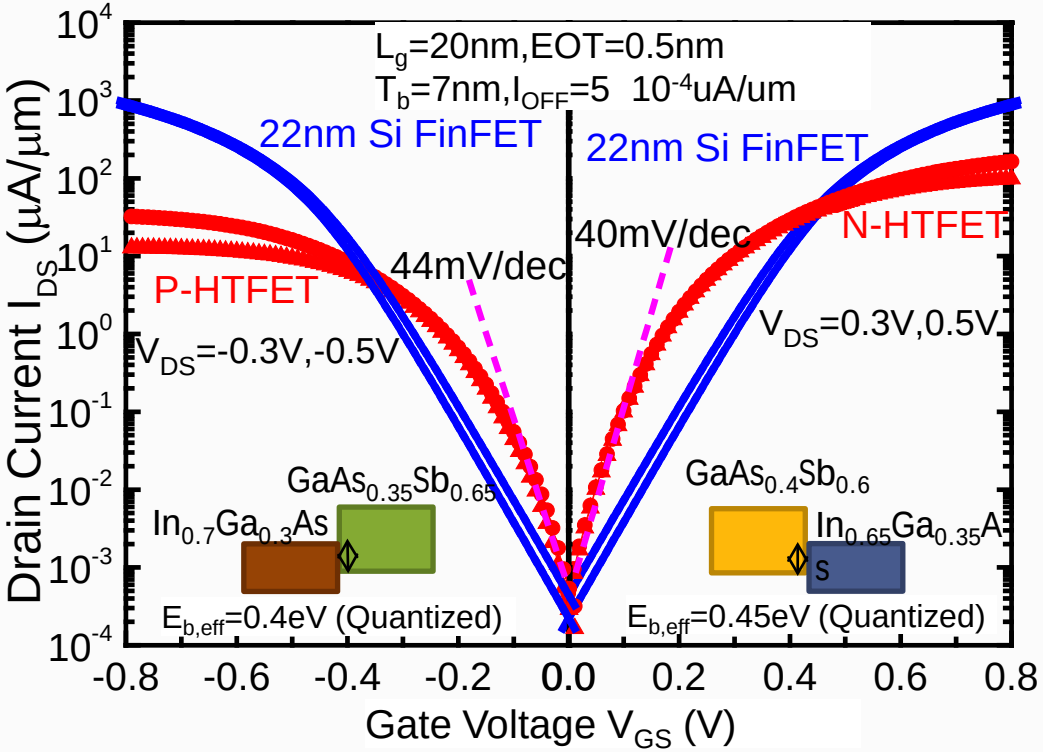
[5] L. Knoll et al., IEDM, 2013

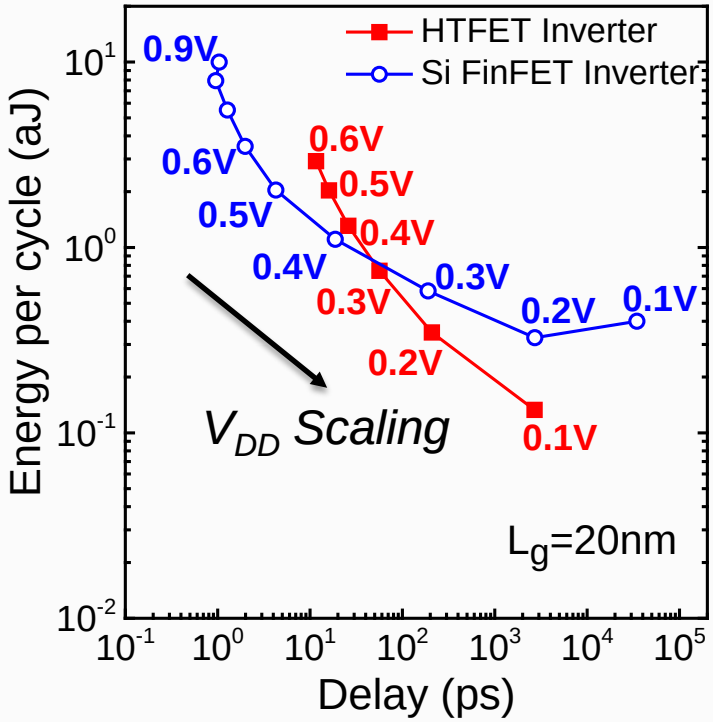
N and P-channel HTFET



✓ **High quality abrupt hetero-junctions to maximize I_{ON} and I_{ON}/I_{OFF}**

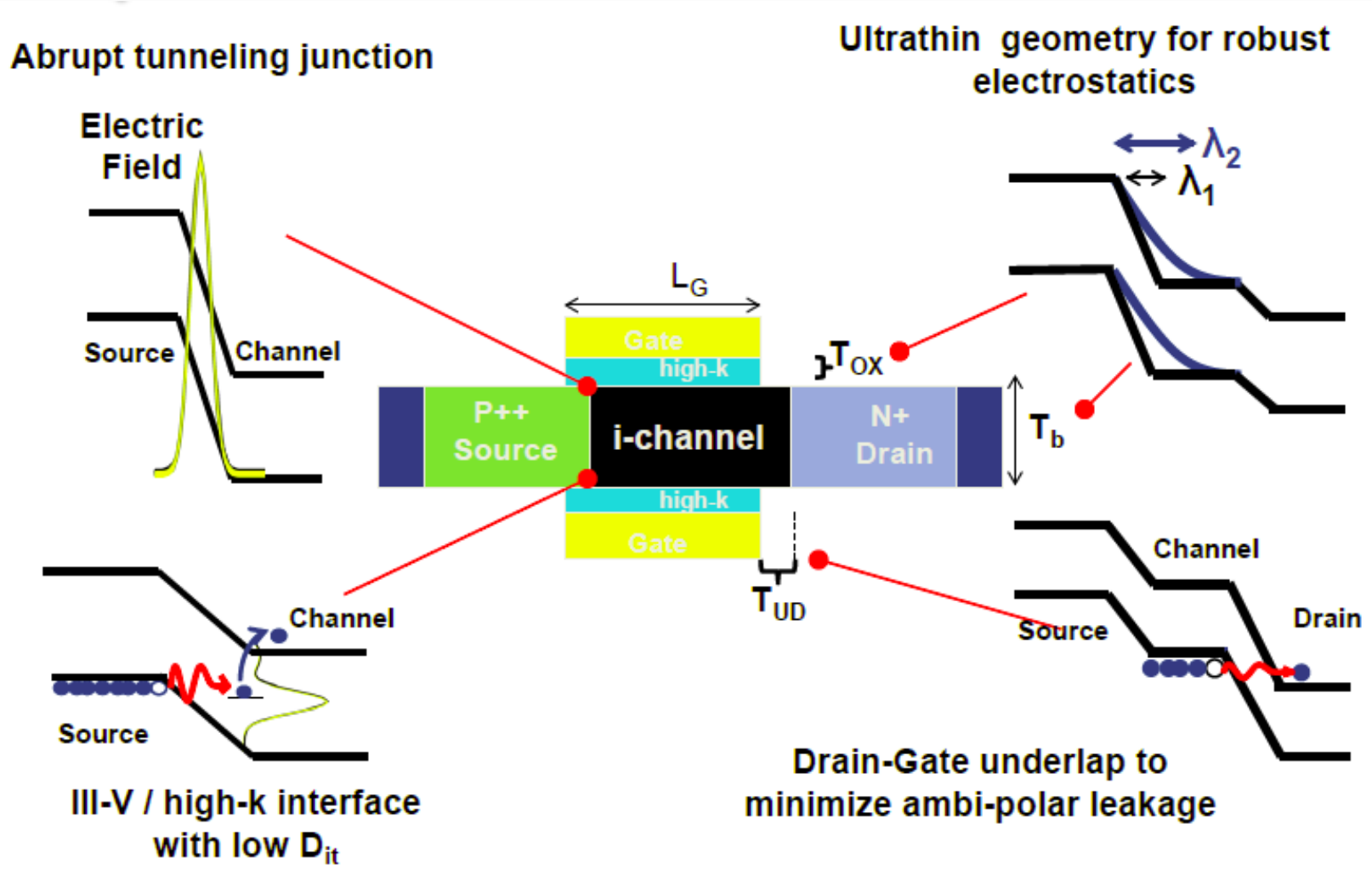
HTFET inverter: Energy Delay Promise





✓**HTFET inverter shows energy efficient operation over CMOS at ultra low V_{DD} application (in theory)**

TFET Demonstration Challenges

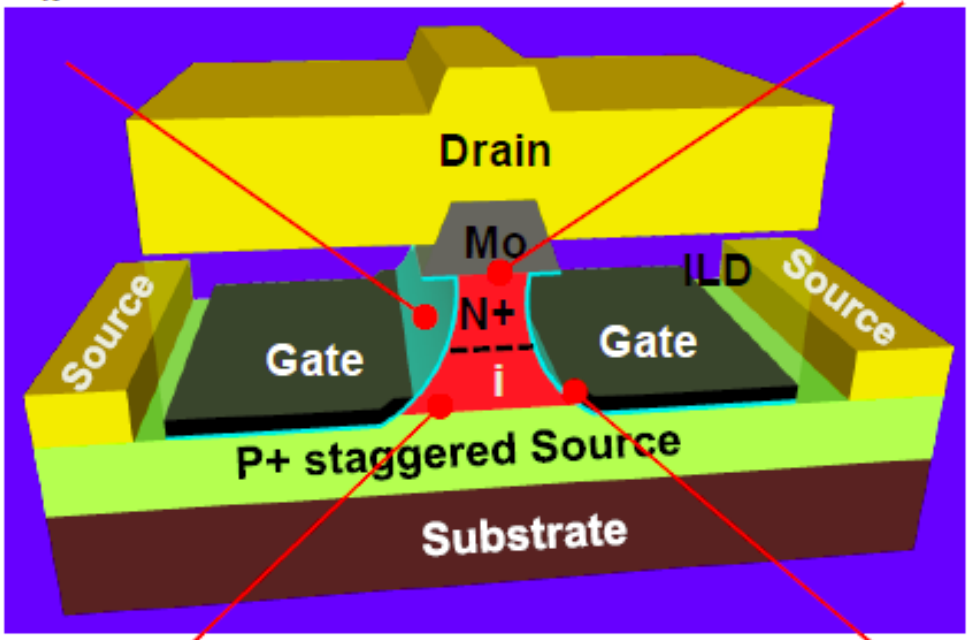


Tunnel FET requirements more stringent than MOSFETs

Vertical Tunnel FET

III-V / high-k interface with low D_{it}

Pillar based ultrathin T_b

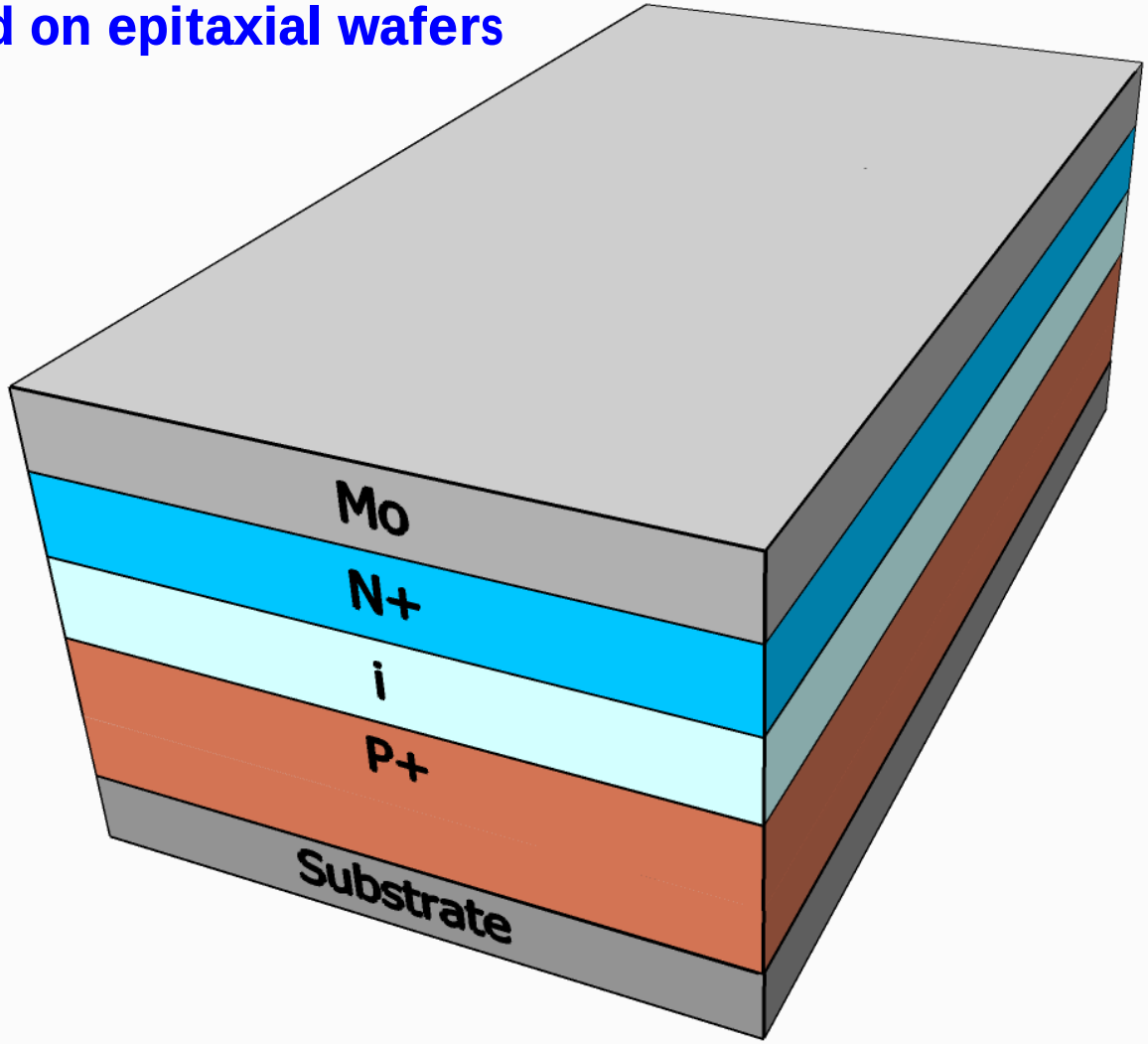


In situ doped Molecular Beam Epitaxially grown junctions

Drain-Gate underlap structure

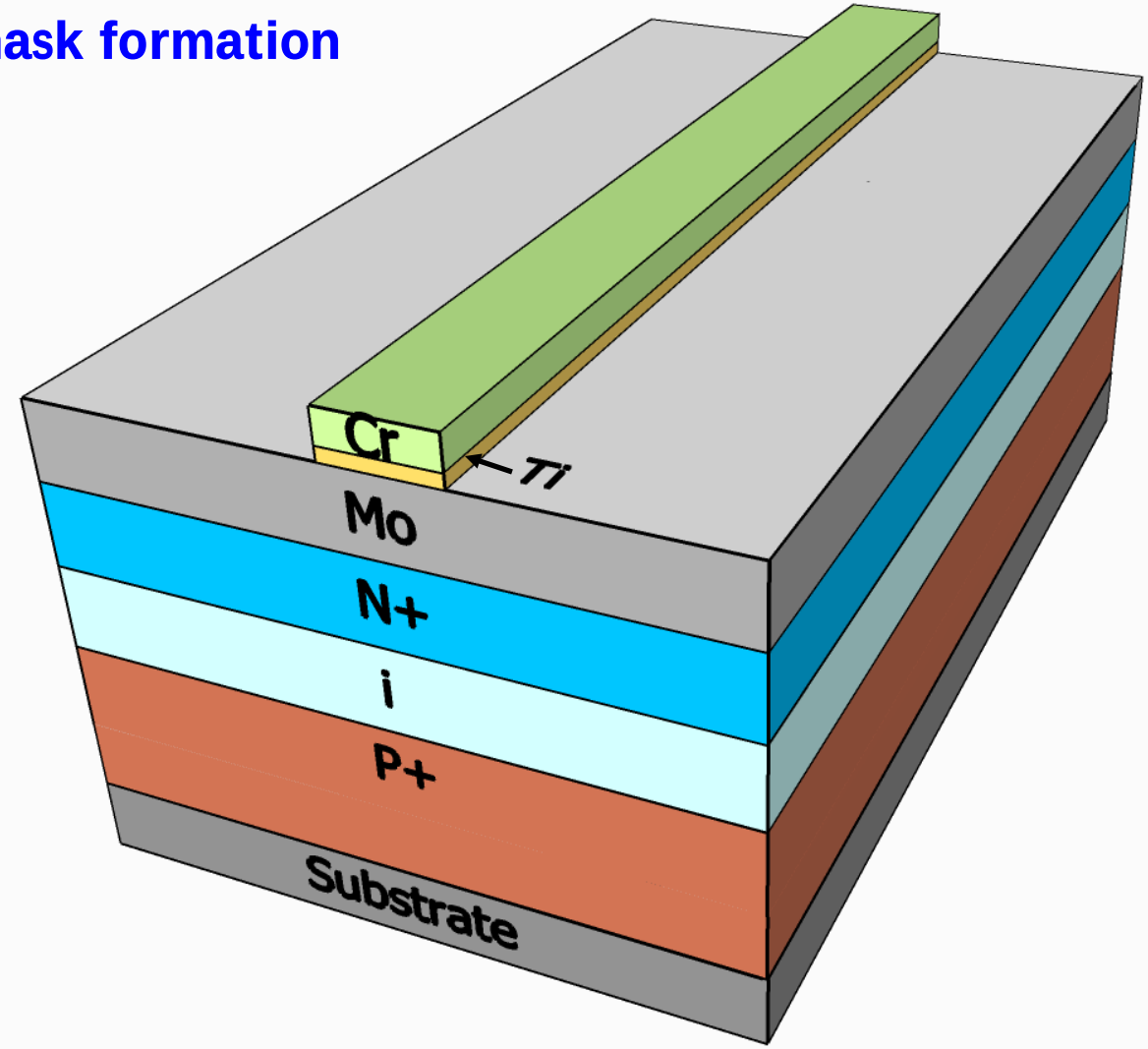
HTFET Process Flow

Mo Deposited on epitaxial wafers



HTFET Process Flow

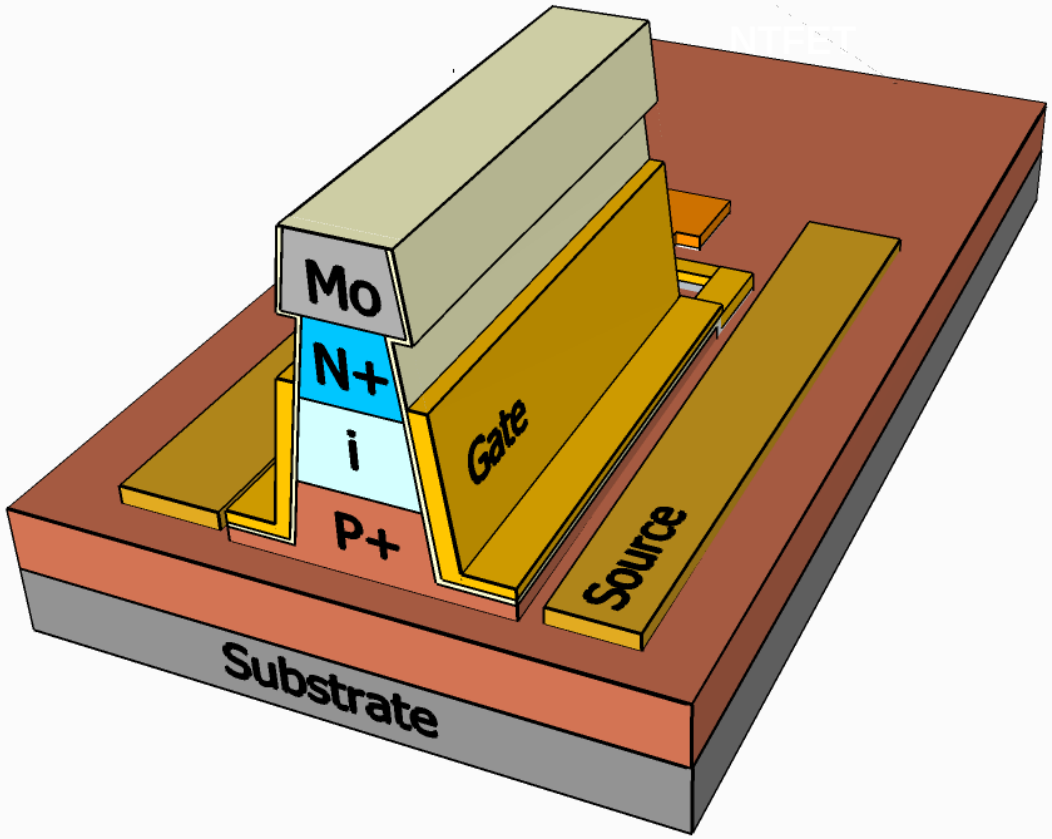
Ti/Cr etch mask formation



HTFET Process Flow

Etch to create MESA pillar

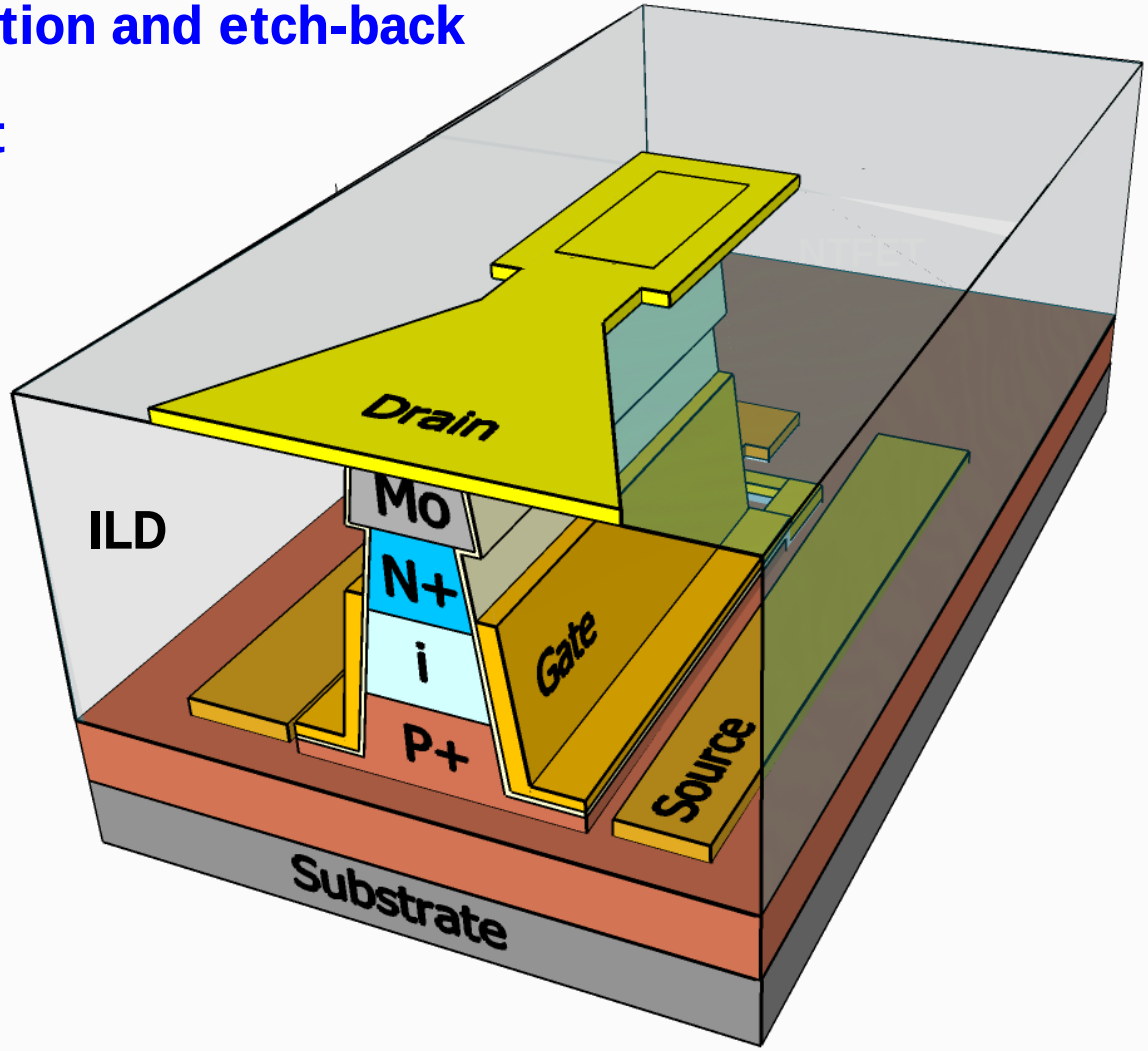
High-K/metal gate deposition



HTFET Process Flow

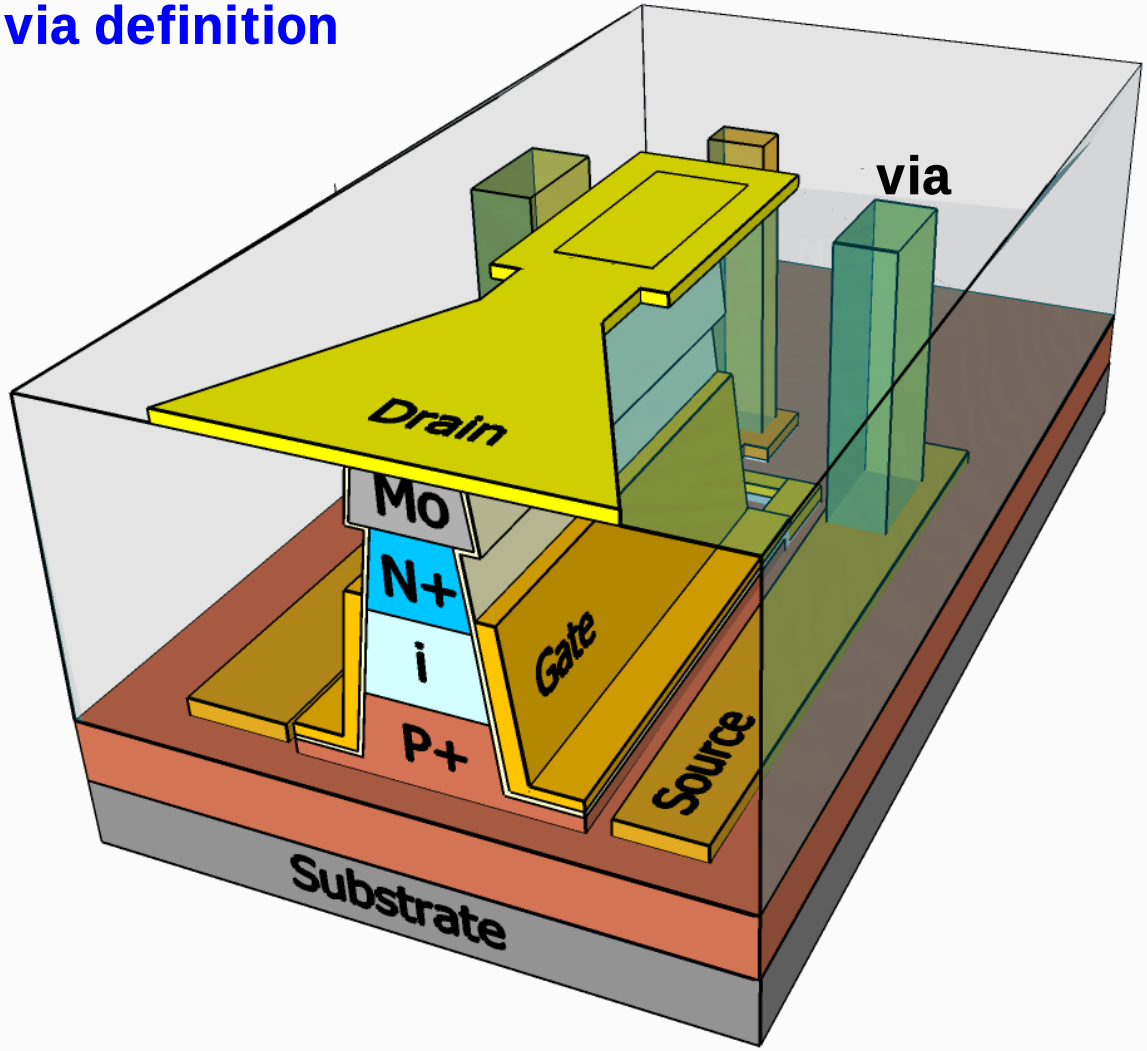
ILD planarization and etch-back

Drain contact



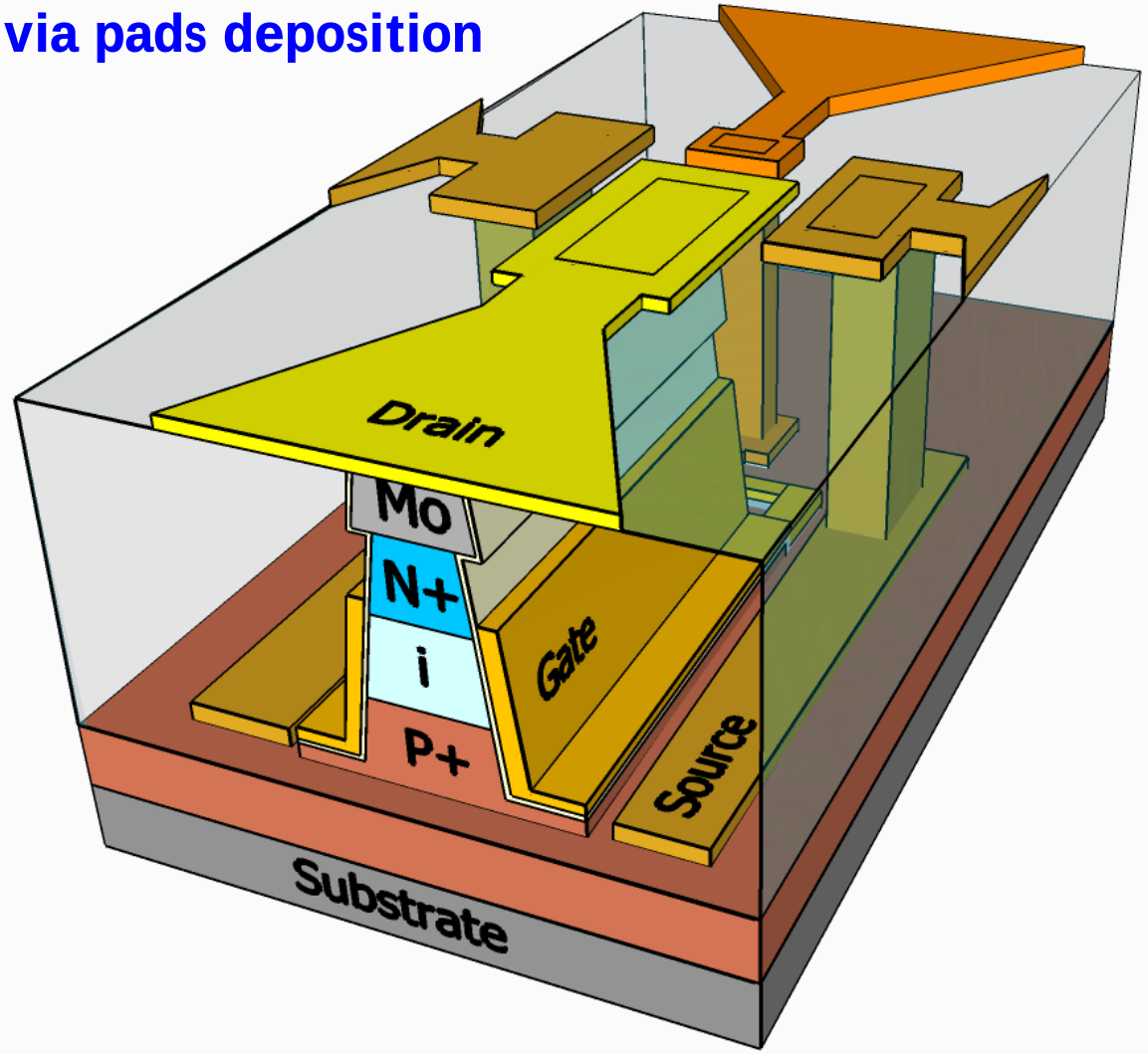
HTFET Process Flow

Gate, source via definition

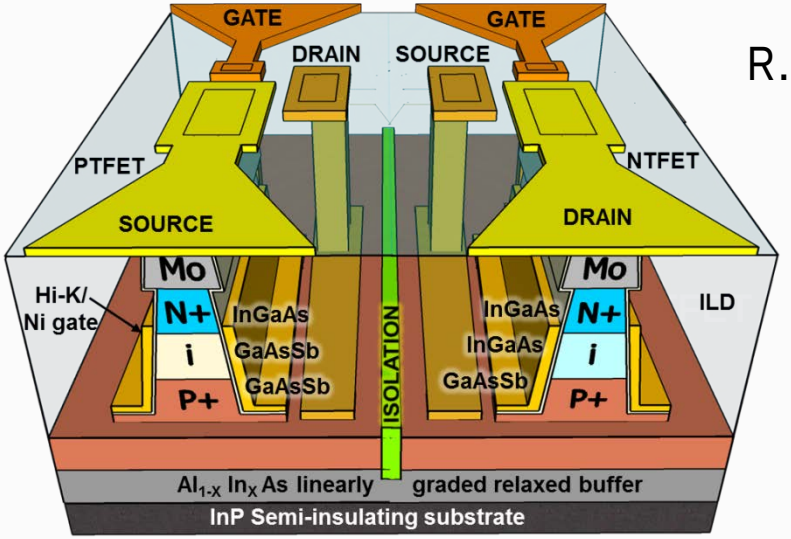


HTFET Process Flow

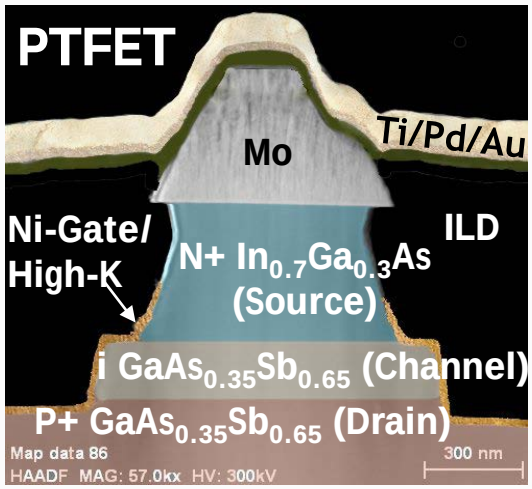
Gate, Source via pads deposition

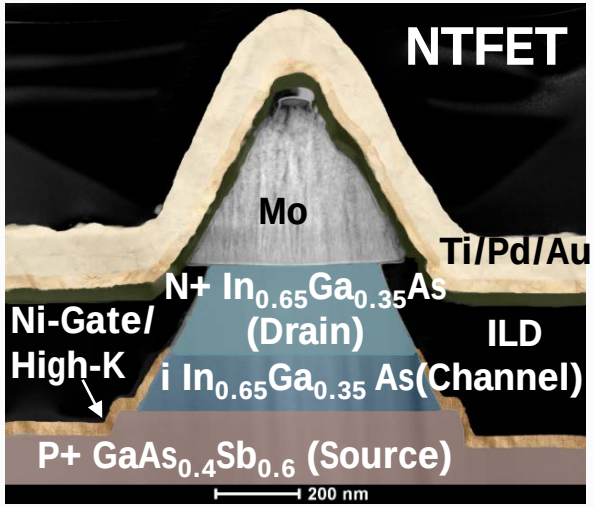


HTFET: Cross-section TEM



R. Pandey, VLSI 2015



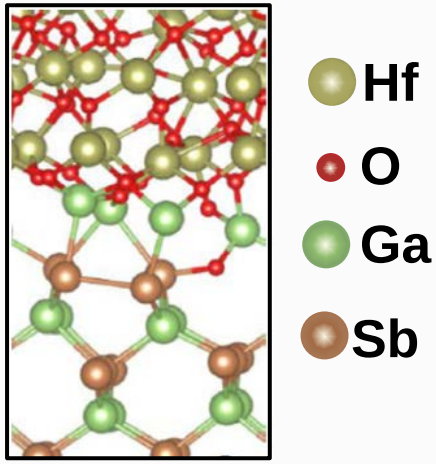


✓ **Complimentary HTFET on common metamorphic buffer**

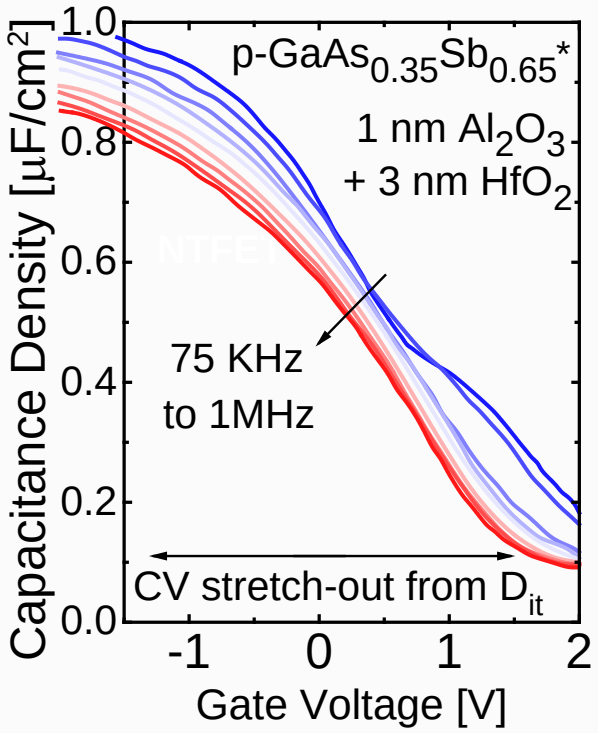
PTFET: Gate Stack Optimization

PTFET

HfO_2 / Ga(As)Sb



K. Xiong et al., APL 2013
[Robertson Group, Camb. U.]



✓ **Highly reactive interface:**

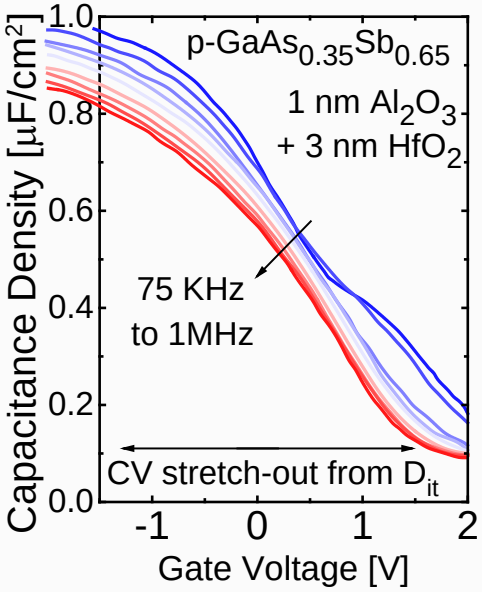
-Ga dangling bonds, Sb-Sb bonds

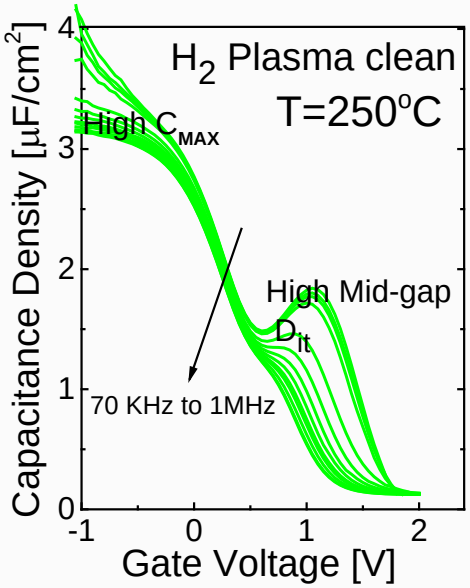
-Sb oxides and anti-site defects

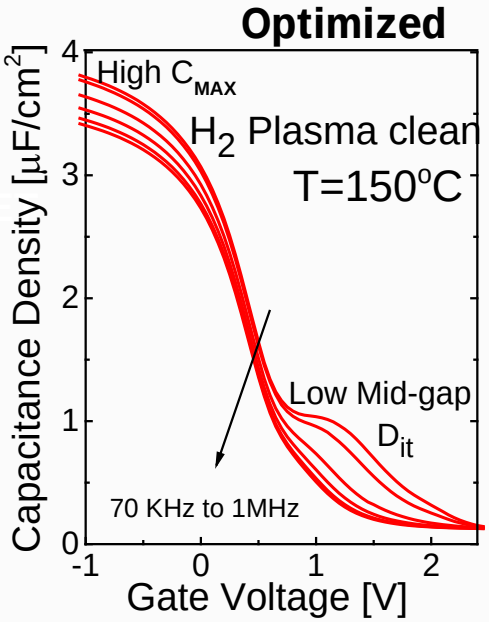
* Bijesh et al., Apex, 2013

PTFET: Gate Stack Optimization

$HfO_2/GaAs_{0.35}Sb_{0.65}$ Interface

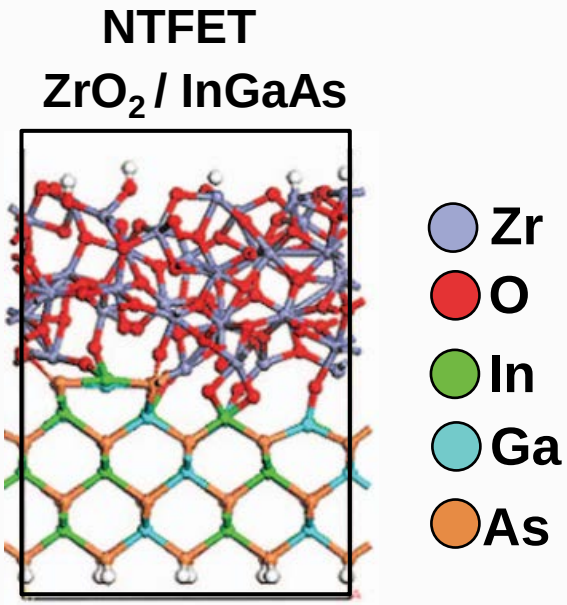




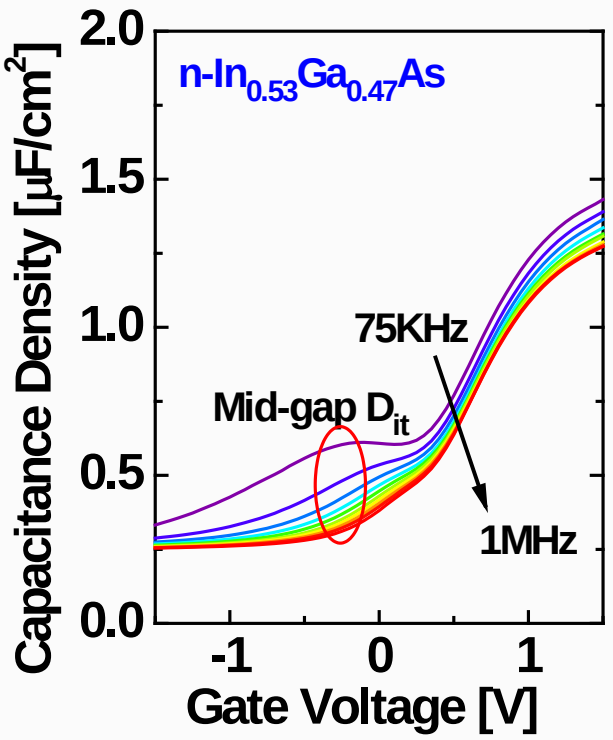


- ✓ **In-Situ H_2 plasma treatment**
  - **Removes Sb-oxides and passivates defect states**
- ✓ **Efficient native oxide removal at 150°C [CET=1.2 nm]**
  - **T<200°C suppresses Sb formation which degrades D_{it}**

NTFET: Gate Stack Optimization



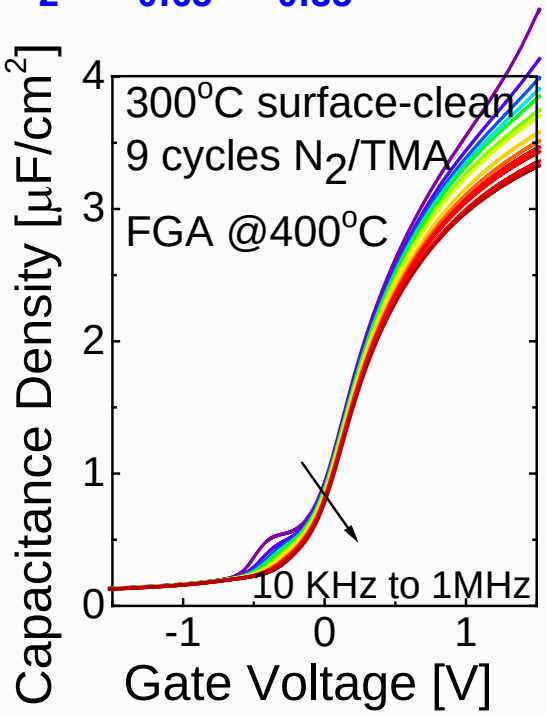
Chagarov et al., JCP 2011
[Kummel Group, UCSD]



- ✓ **Highly reactive interface:**
  - **-Ga Dangling bonds, As-As bonds**
  - **-As oxides and anti-site defects**

NTFET: Gate Stack Optimization

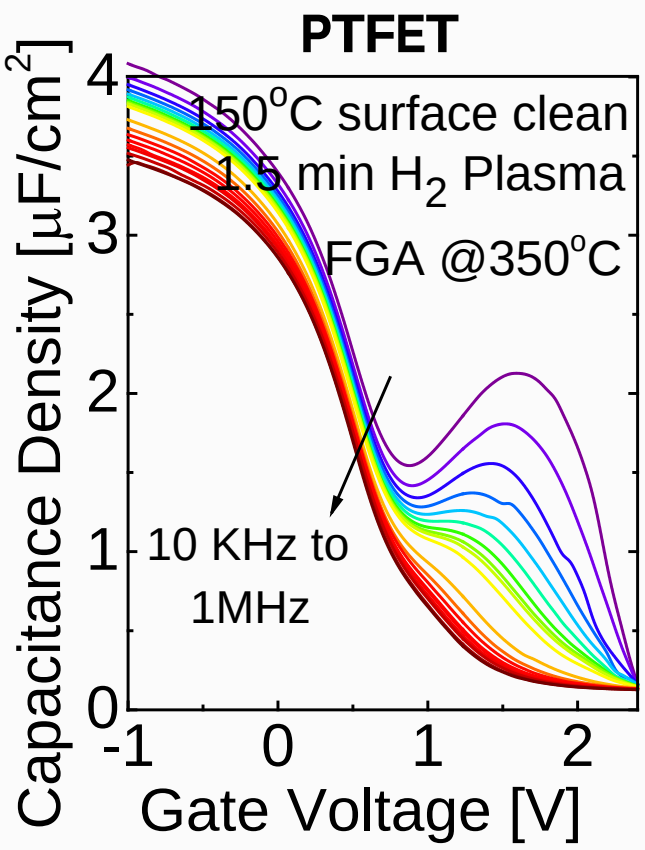
ZrO_2 /$In_{0.65}Ga_{0.35}As$ Interface

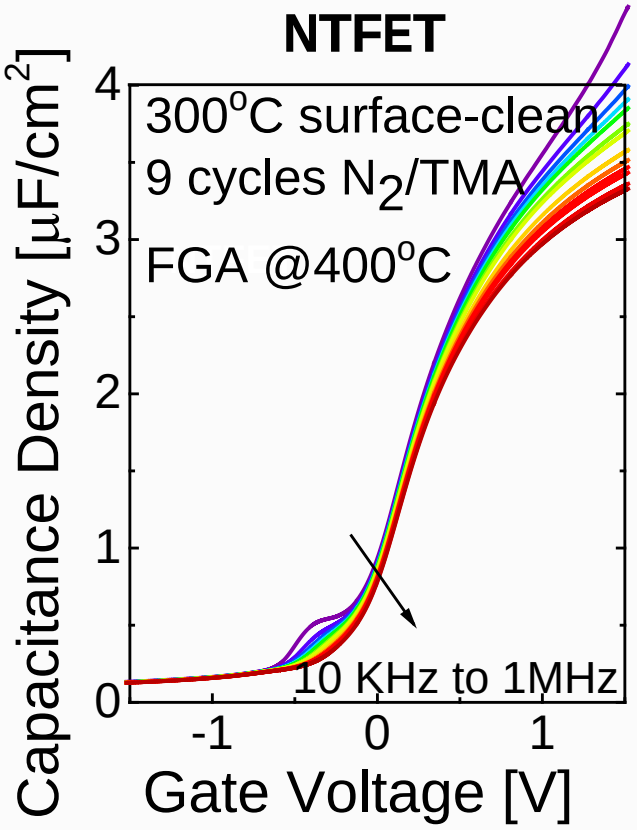


- ✓ **Ex-situ BOE clean and In-Situ N_2 plasma/TMA cyclic treatment***
  - **Removes As-oxides and passivates defect states**
- ✓ **CET=1.1 nm with 9 plasma cycles**
  - **Plasma over-exposure can damage the surface**

** V. Chobpattana et al., APL, May 2014; Collaboration with UCSB*

Optimized Gate Stacks



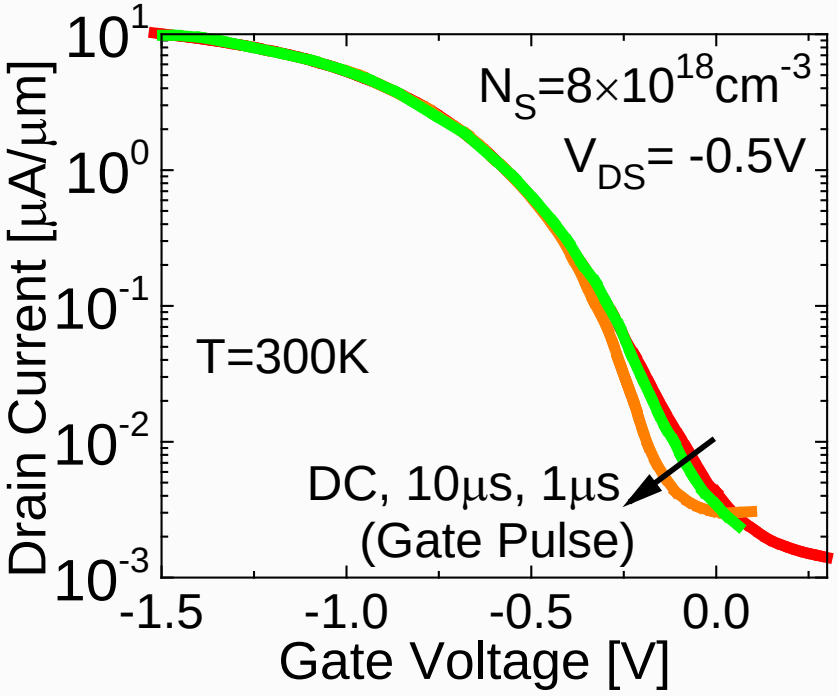


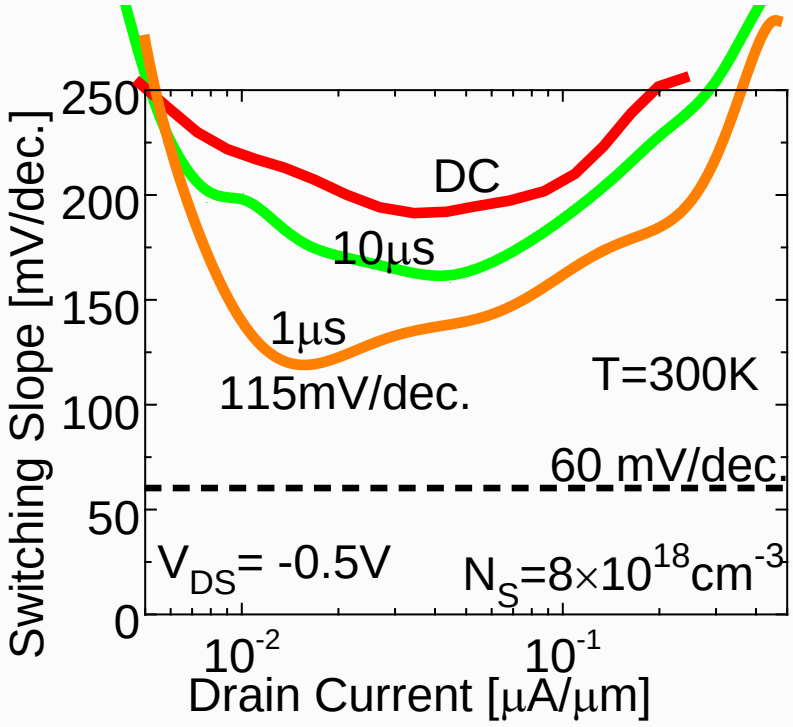
$HfO_2/GaAs_{0.35}Sb_{0.65}$ Interface

ZrO_2 /$In_{0.65}Ga_{0.35}As$ Interface*

** V. Chobpattana et al., APL, May 2014; Collaboration with UCSB*

P-channel HTFET

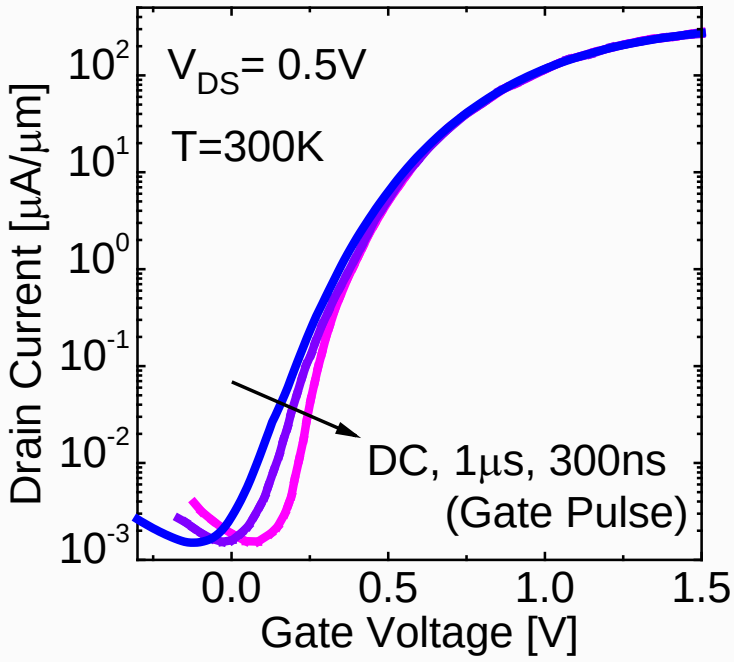


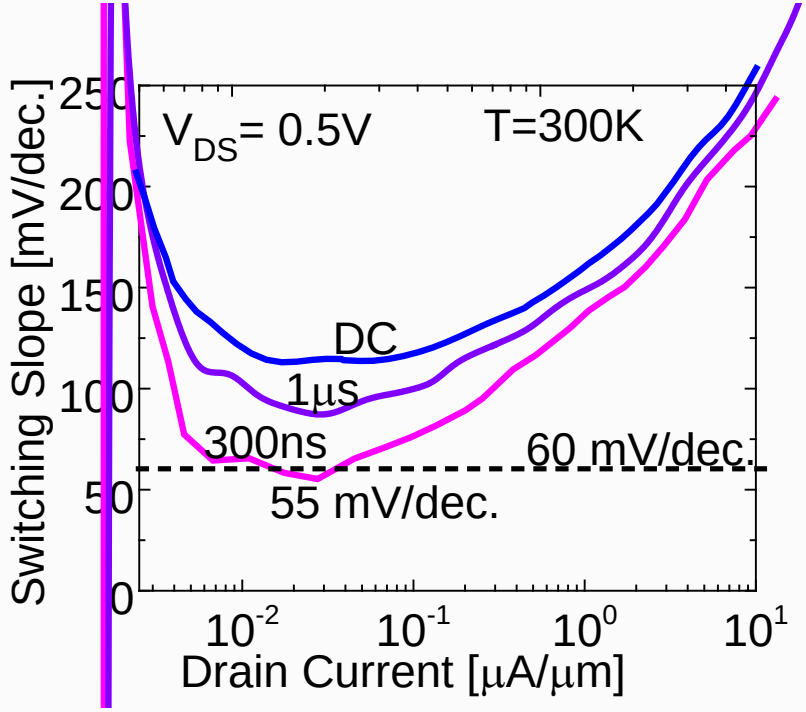


✓**Minimum switching slope =115mV/decade at room temp.**

Fast IV measurements performed at NIST, MD

N-channel HTFET

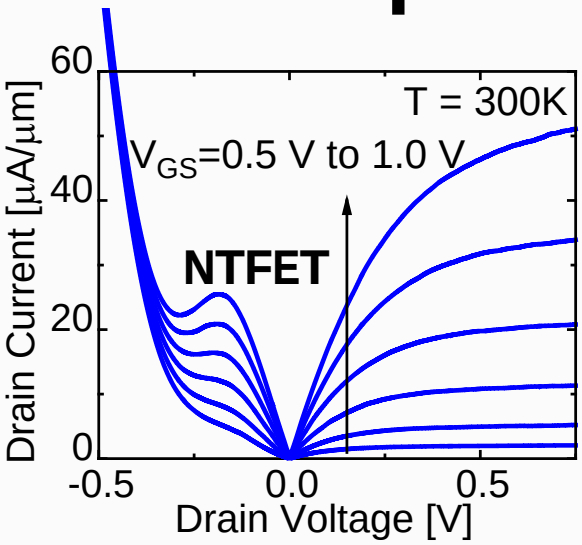


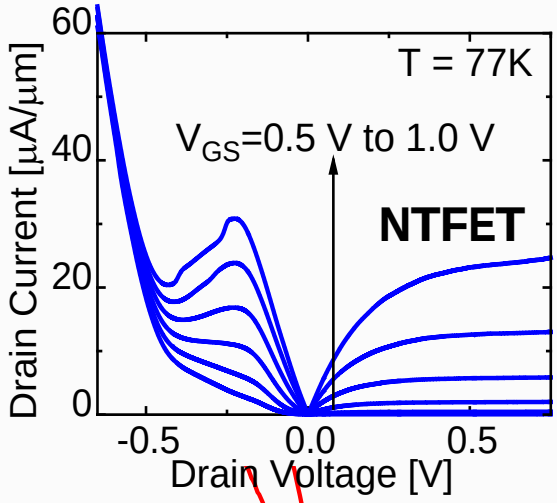


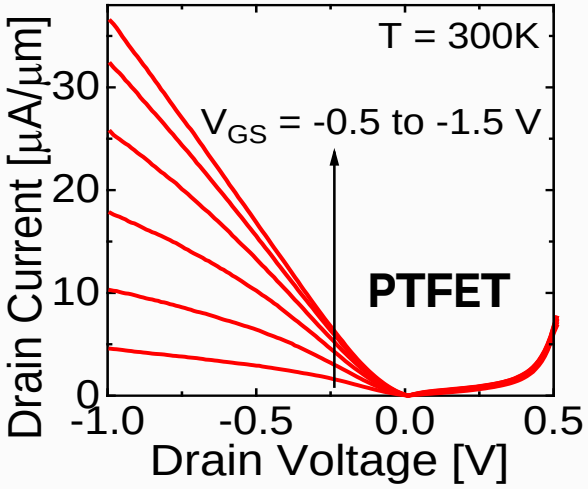
✓**Minimum switching slope = 55mV/decade at room temp.**

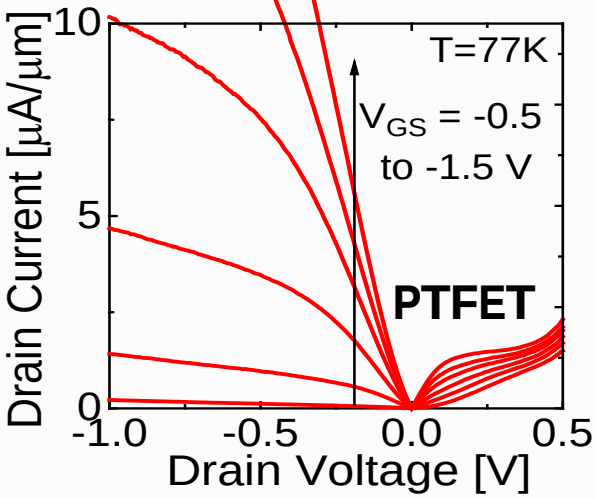
Fast IV measurements performed at NIST, MD

Output Characteristics



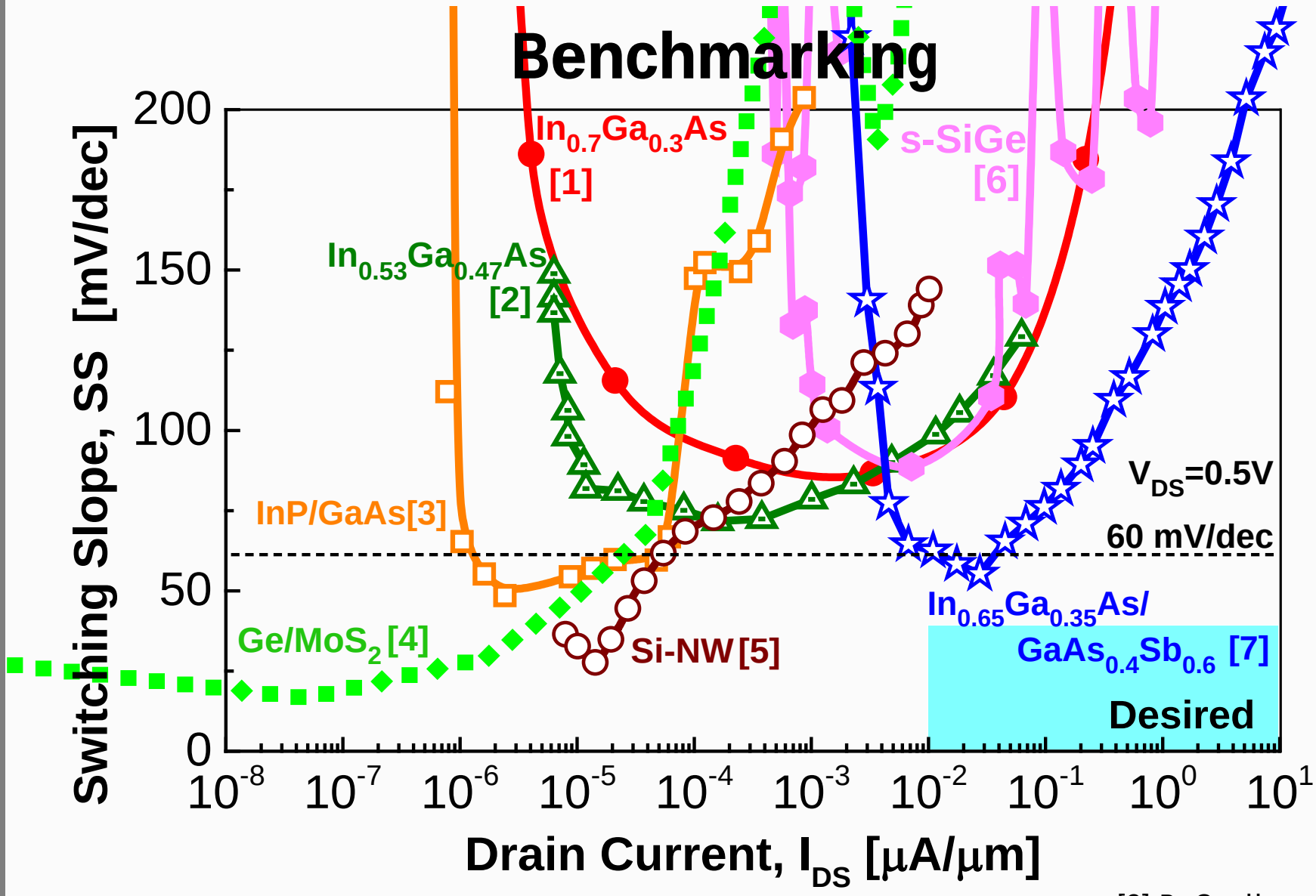






✓**NDR present in all devices**

-Tunneling as fundamental switching mechanism



[1] H. Zhao et al, IEEE EDL, Dec. 2010

[2] M. Noguchi et al., IEDM 2013

[3] B. Ganjipour et al., ACS Nano, Apr. 2012

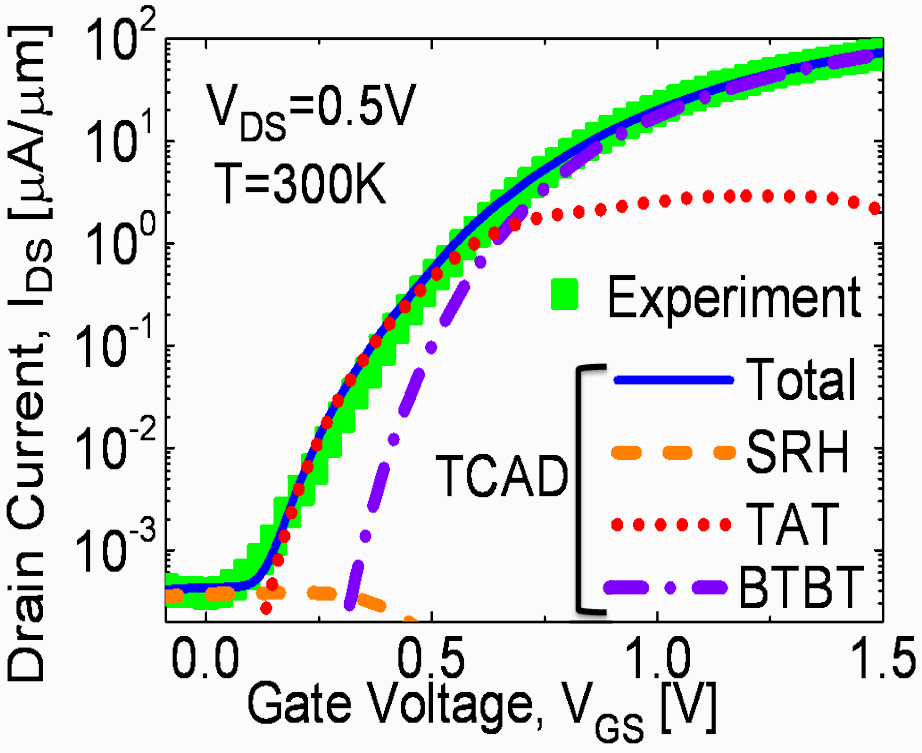
[4] D. Sarkar. et al., Nature Vol. 526, Oct. 2015

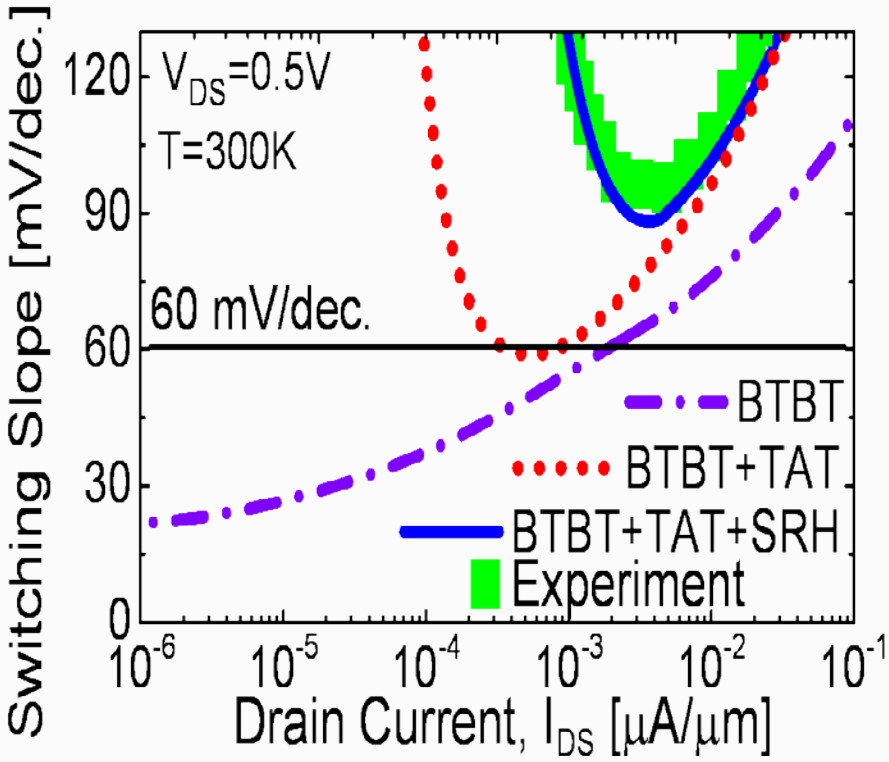
[5] L. Knoll et al., IEEE EDL, June 2013

[6] A. Villalon et al., VLSI 2012

[7] R. Pandey et al., VLSI 2015

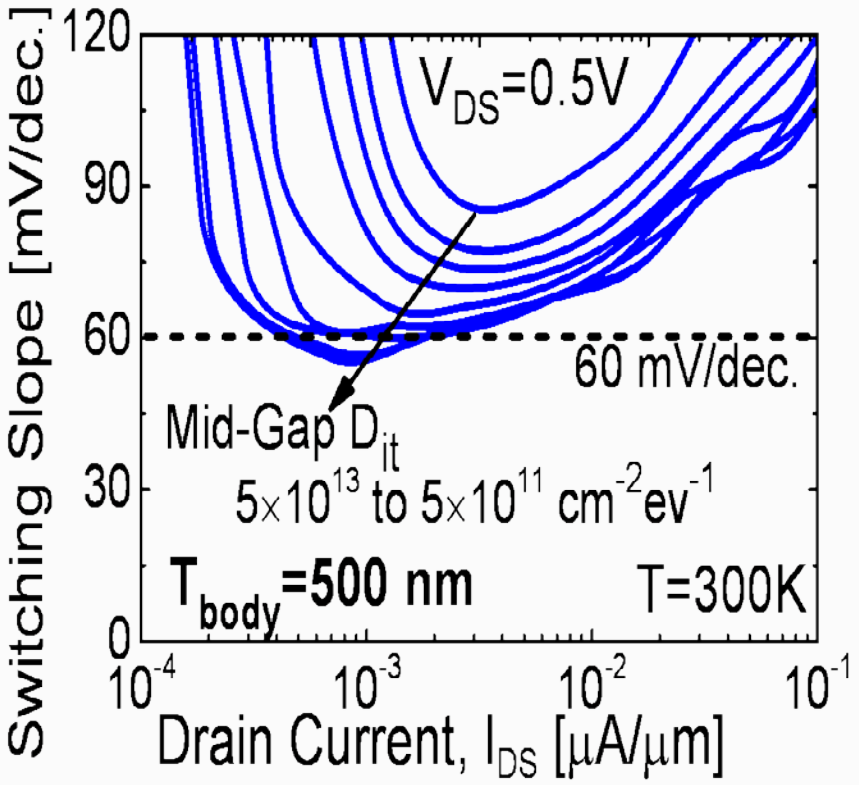
Components of Transport in TFET

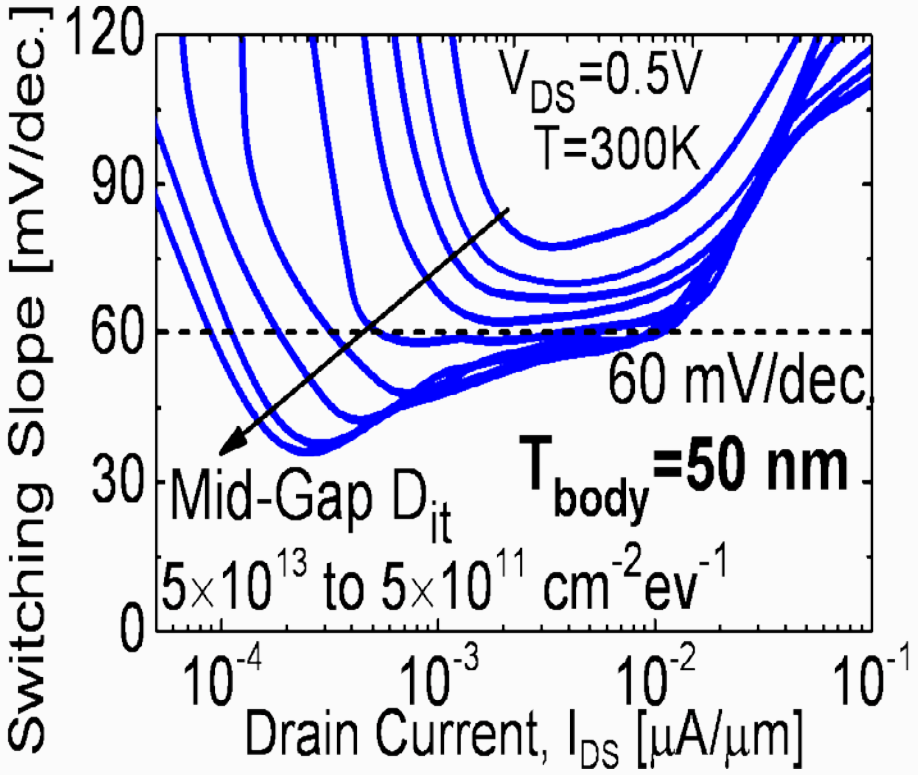




Reduced Dit (TAT), reduced body thickness (SRH) are necessary for demonstrating steep slope TFETs

Dit, Tbody (simulation)

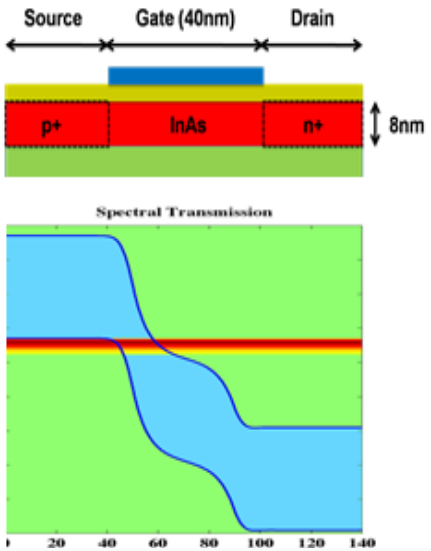




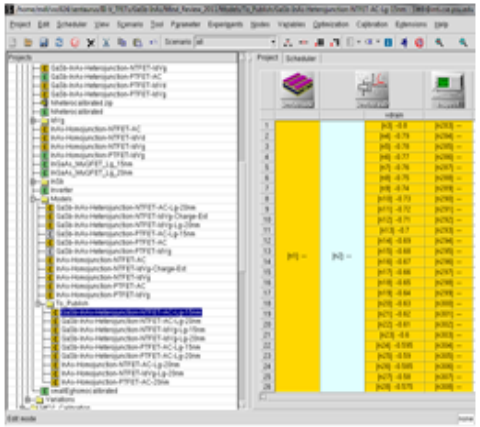
Our current focus is to Dit and Tbody reduction for vertical Heterojunction TFETs

Devices to Circuits

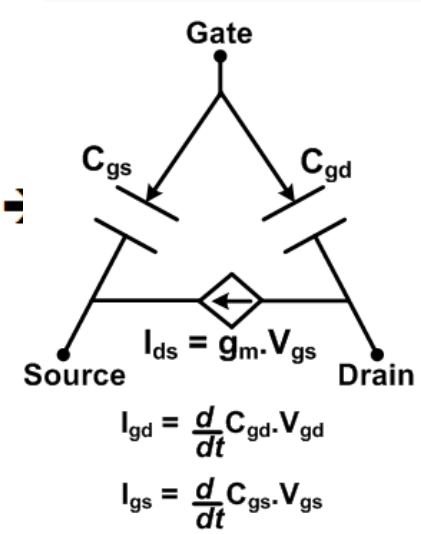
Full band Atomistic simulation (Purdue Nanohub)

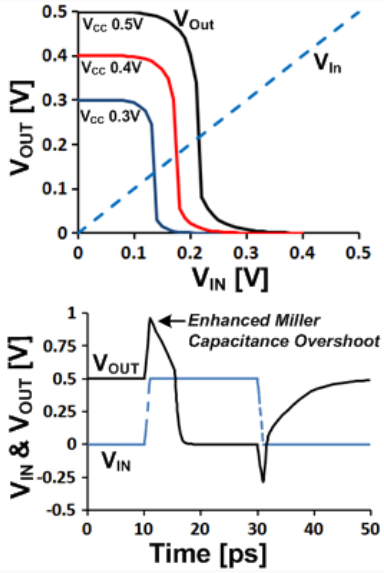


I-V/C-V sweep (experimentally verified)



Look-up Table Based Verilog-A Modeling

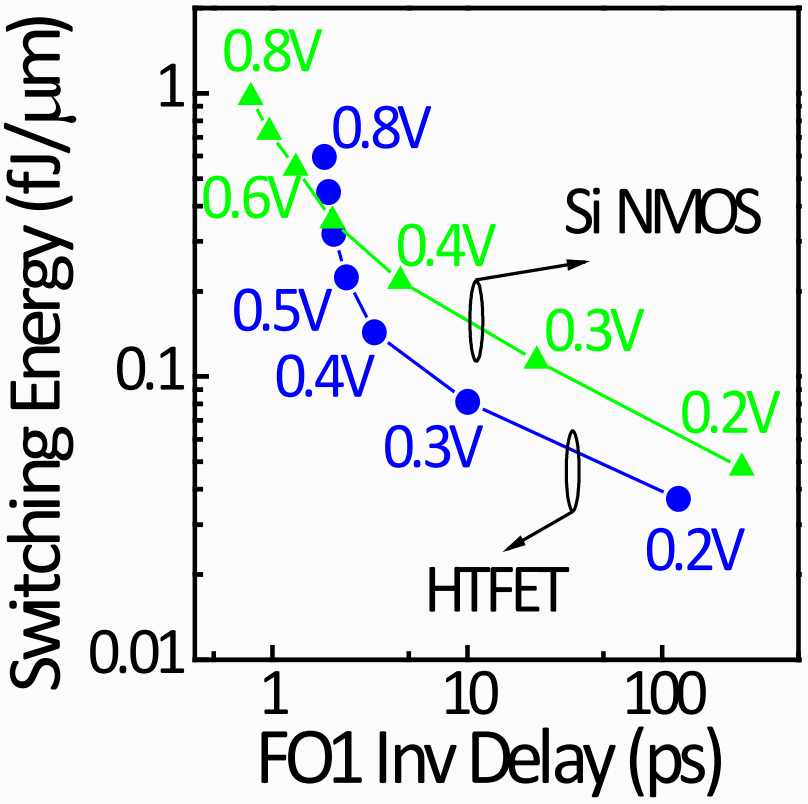


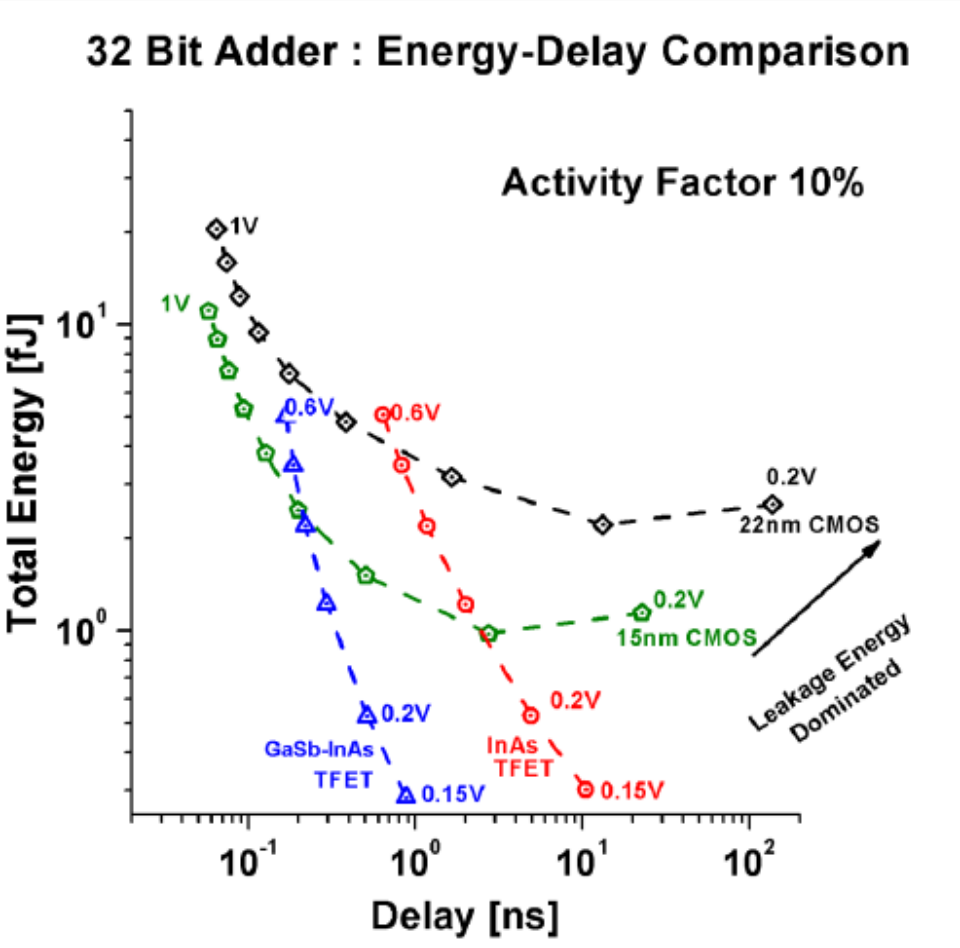


V. Saripalli, V. Narayanan, S. Datta *IEEE/ACM Nanoarch* 2011.

- ✓ Lookup Table based Verilog-A model of Heterojunction Tunnel FET;
- ✓ Collaborate with NSF funded NEEDS (Nano-Engineered Electronic Device Simulation Node)

Energy-Delay Comparison

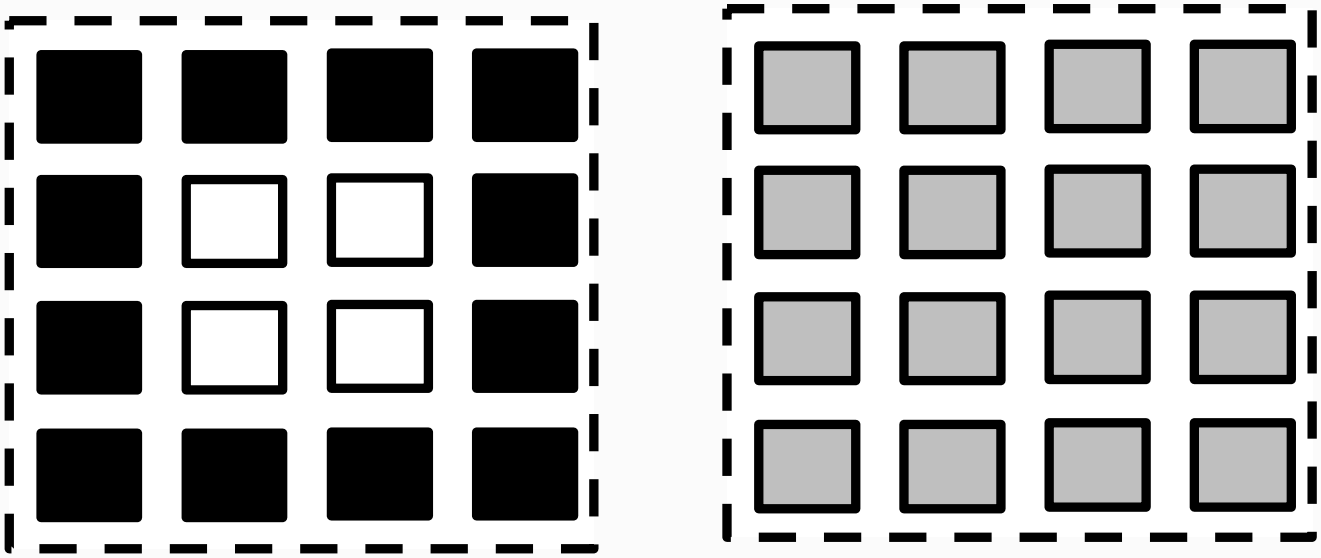




Tunnel FETs show better energy delay performance below 0.5V

Hybrid Core Processor

Evaluated multi-core configurations



Dark silicon

Dim silicon

Run serial applications on CMOS cores in dark silicon setting
Run parallel applications on TFET cores in dim silicon setting

Tunnel FETs for beyond 5nm ?

MOSFETs

ITRS Year	2018	2020	2022
M1 Half-Pitch	15	11.9	9.5
Gate Length	13.1	10.8	8.9
EOT	0.78	0.70	0.63
$t_{Multi\text{-}gate}$	8.7	7.1	5.7

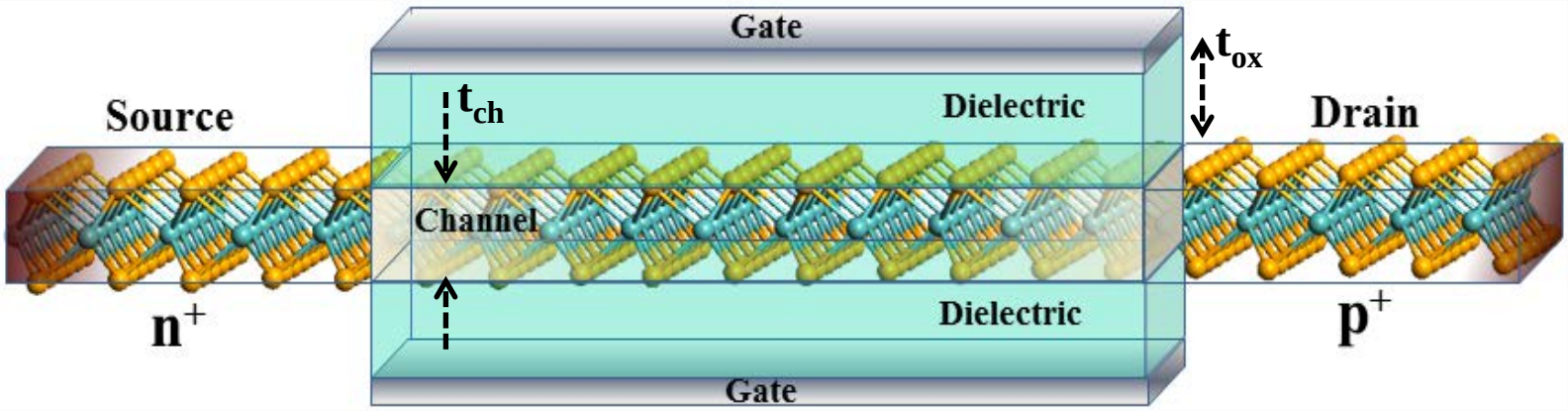
TFETs

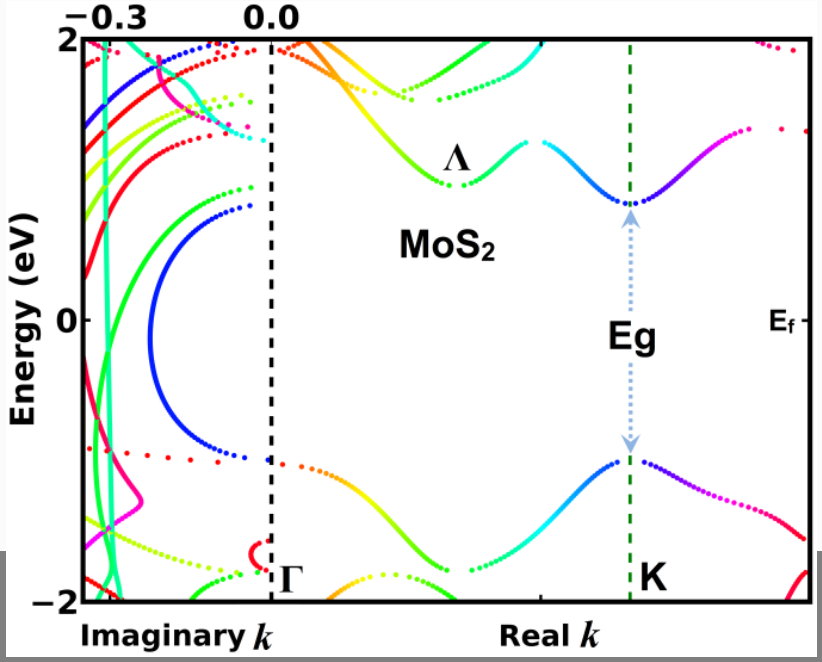
ITRS Year	2018	2020	2022
M1 Half-Pitch	15	11.9	9.5
Gate Length	13.1	10.8	8.9
EOT	0.78	0.78	0.78
$t_{Multi\text{-}gate}$	3.0	2.4	1.9
$t_{Nanowire}$	4.7	3.8	3.0

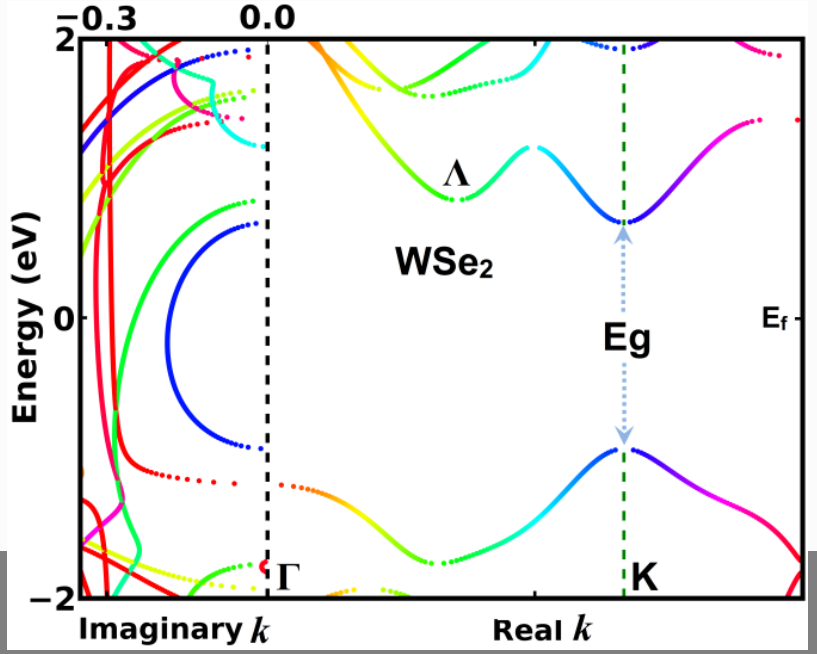
- Body thickness requirement more stringent for Tunnel FETs at highly scaled technology nodes

2D TMD Tunnel FETs

Atomically thin channels for scaled TFET operation

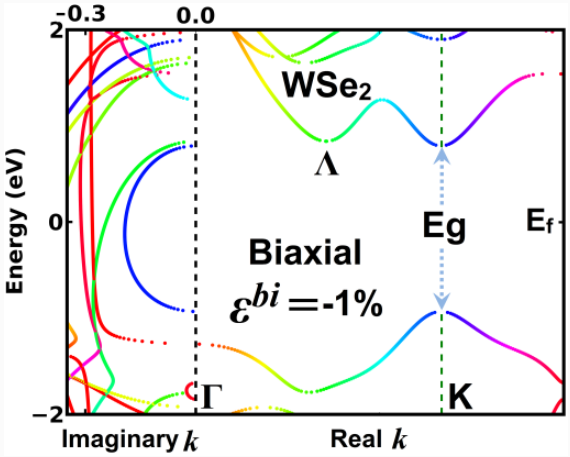




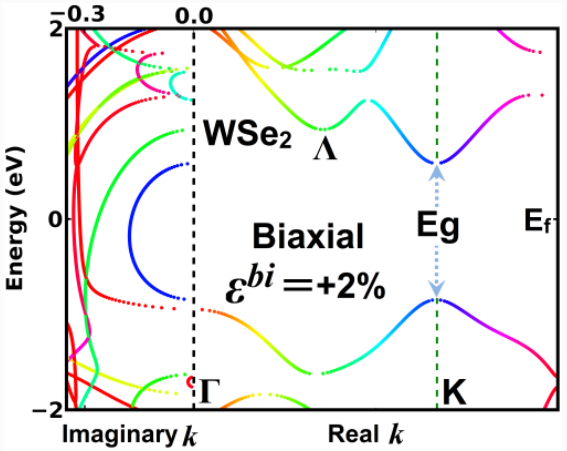


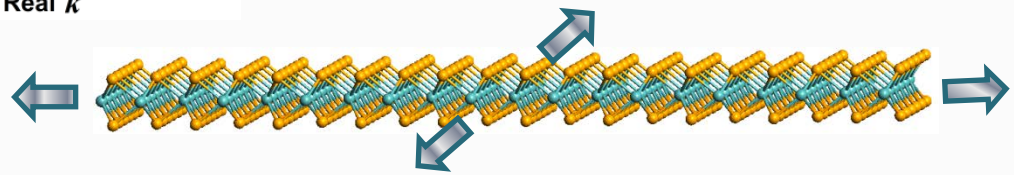
Elastic strain effect on monolayer TMD

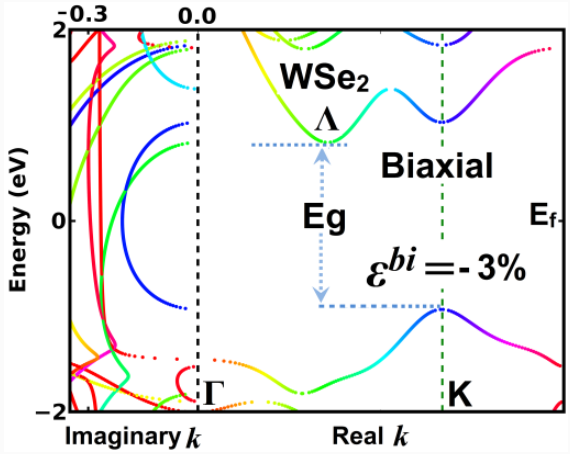
Compressive

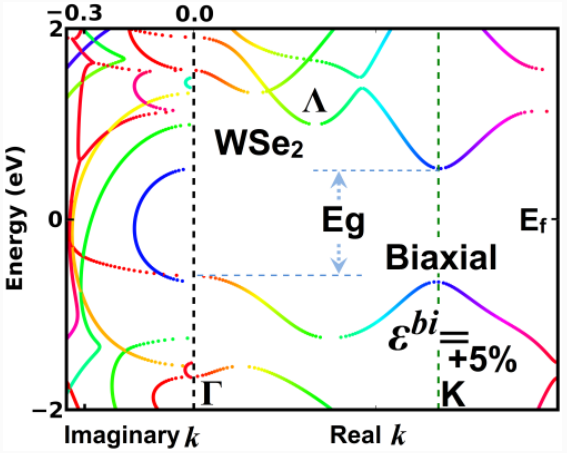


Tensile



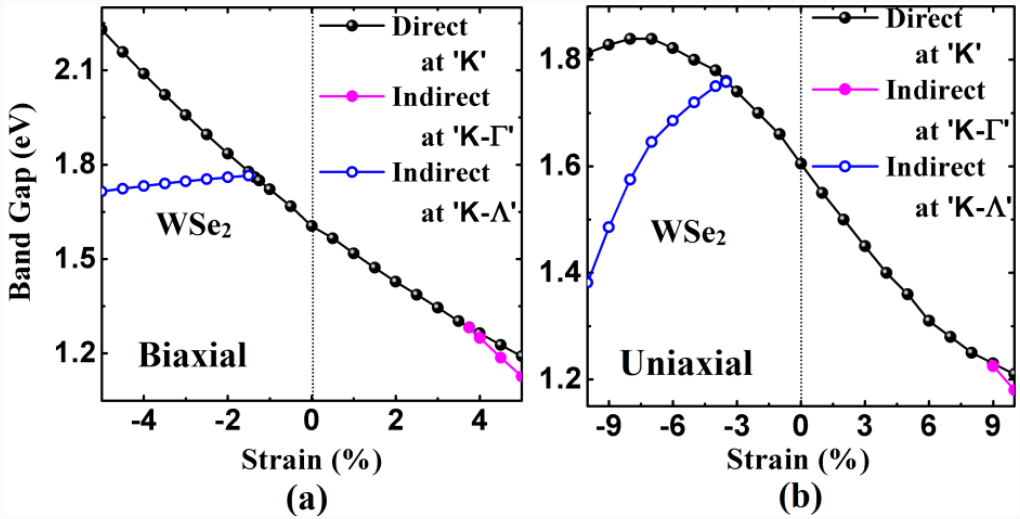




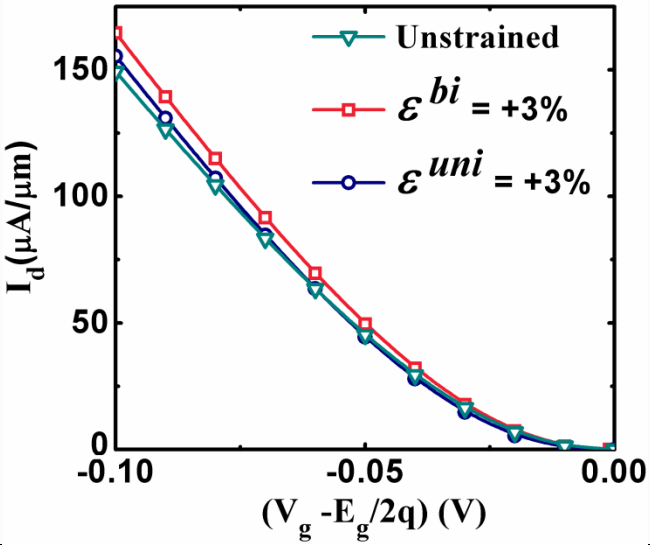


R. K. Ghosh *et al.*, IEEE J. Elec. Dev. Society 99 (2013)

(contd…)



Tensile strain improves the tunneling probability by reducing bandgap

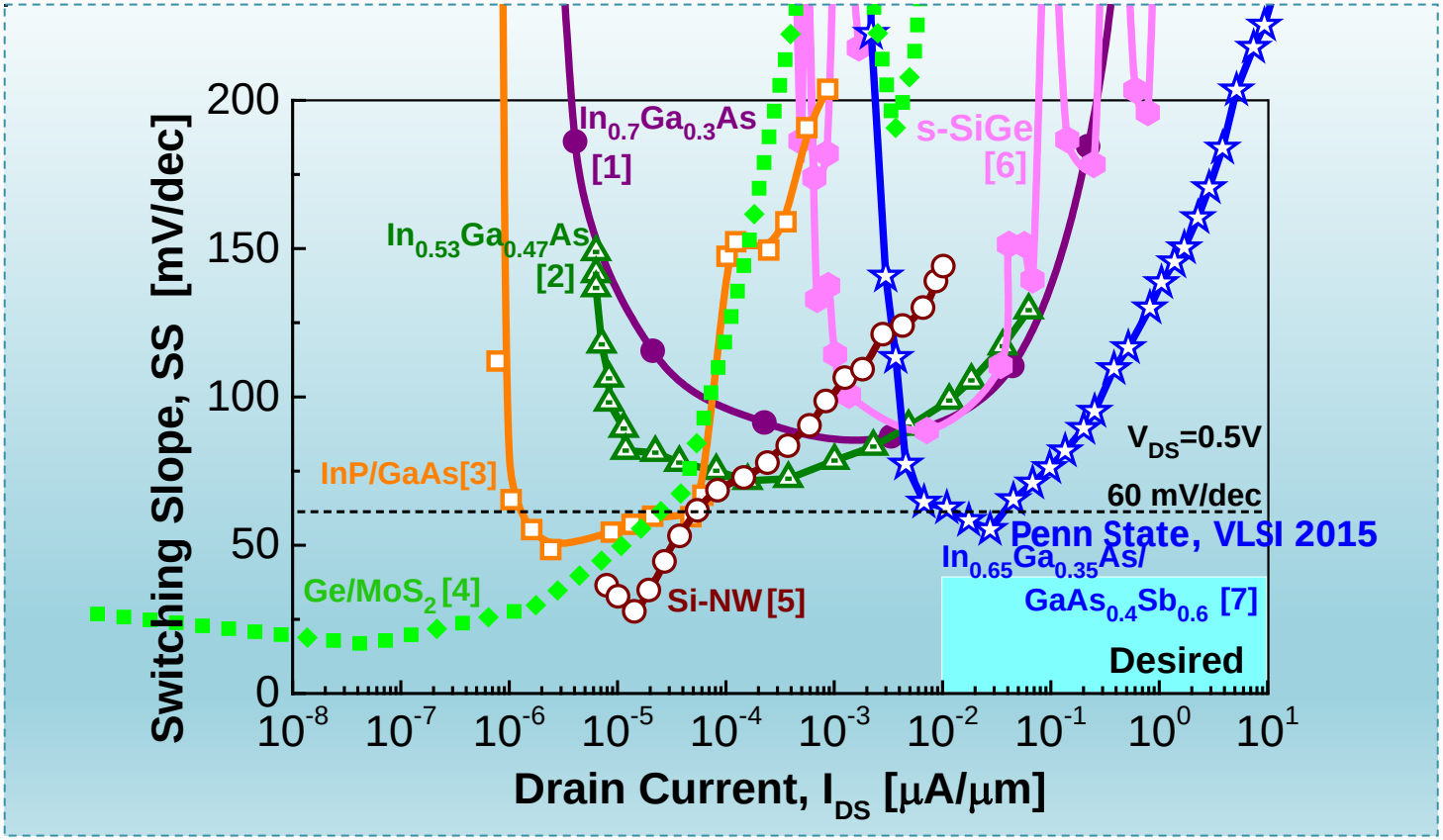


Different MX_2: different Strains to attain direct to indirect

ON-current increases ~ 13% (or ~ 9%) with the application of ε^{bi} = +3% (or ε^{uni} = +3%)

R. K. Ghosh *et al.*, IEEE J. Elec. Dev. Society 99 (2013)

TFET State of the ART



[1] H. Zhao et al, IEEE EDL, Dec. 2010

[2] M. Noguchi et al., IEDM 2013

[3] B. Ganjipour et al., ACS Nano, Apr. 2012

[4] D. Sarkar. et al., Nature Vol. 526, Oct. 2015

[5] L. Knoll et al., IEEE EDL, June 2013

[6] A. Villalon et al., VLSI 2012

[7] R. Pandey et al., VLSI 2015

Take Home Message

- Promise of Tunnel FETs
  - Circuit level benefit for Vcc < 0.3V
- Experiments
  - Heterojunction key to improving Ion
  - Sidewall passivation key to lowering Dit
- Benchmarking
  - Steep slope with respectable Ion still elusive till date
- Much remain to be done
  - Gate stack
  - Scaling of body thickness in vertical configuration