Emerging CMOS Technology at 5 nm and Beyond:

Device Options and Trade-offs

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CMOS today

14 nm **10 nm** **7 nm** **5 nm**

$L_{eff} \approx 20$ nm

$L_{eff} \approx 10\text{-}12$ nm

CTO to senior device engineer:

"As we begin work on the 5 nm node. Is their a new device technology we should be seriously looking at?"

Challenges at the 5 nm node

1) Electrostatics
2) Parasitics
3) Leakage
4) Low-voltage operation

Question: What performance at V_{DD} = 0.5 V do various emerging device options promise at the 5 nm node?

-how does it work?
-why is it promising?
-what are the trade-offs?
-where do things stand?

10 min / option

Acknowledgements

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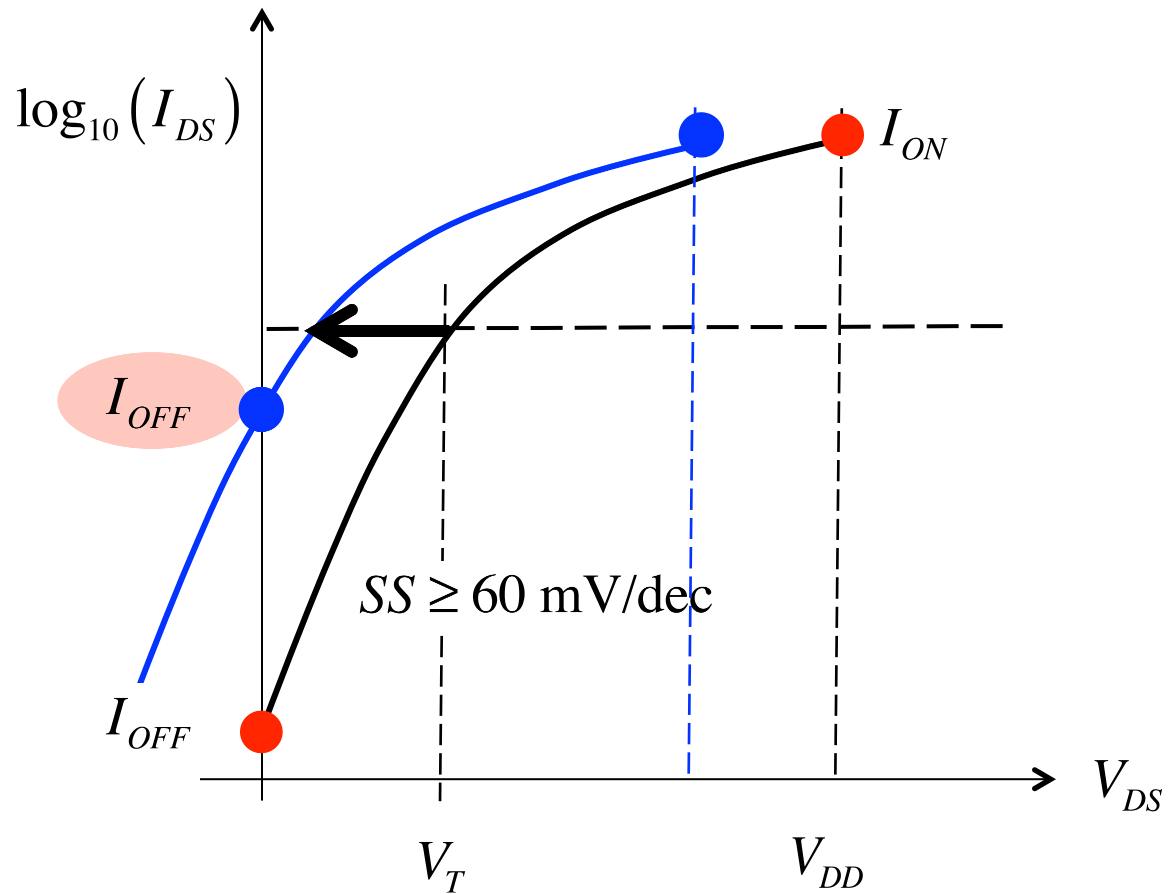
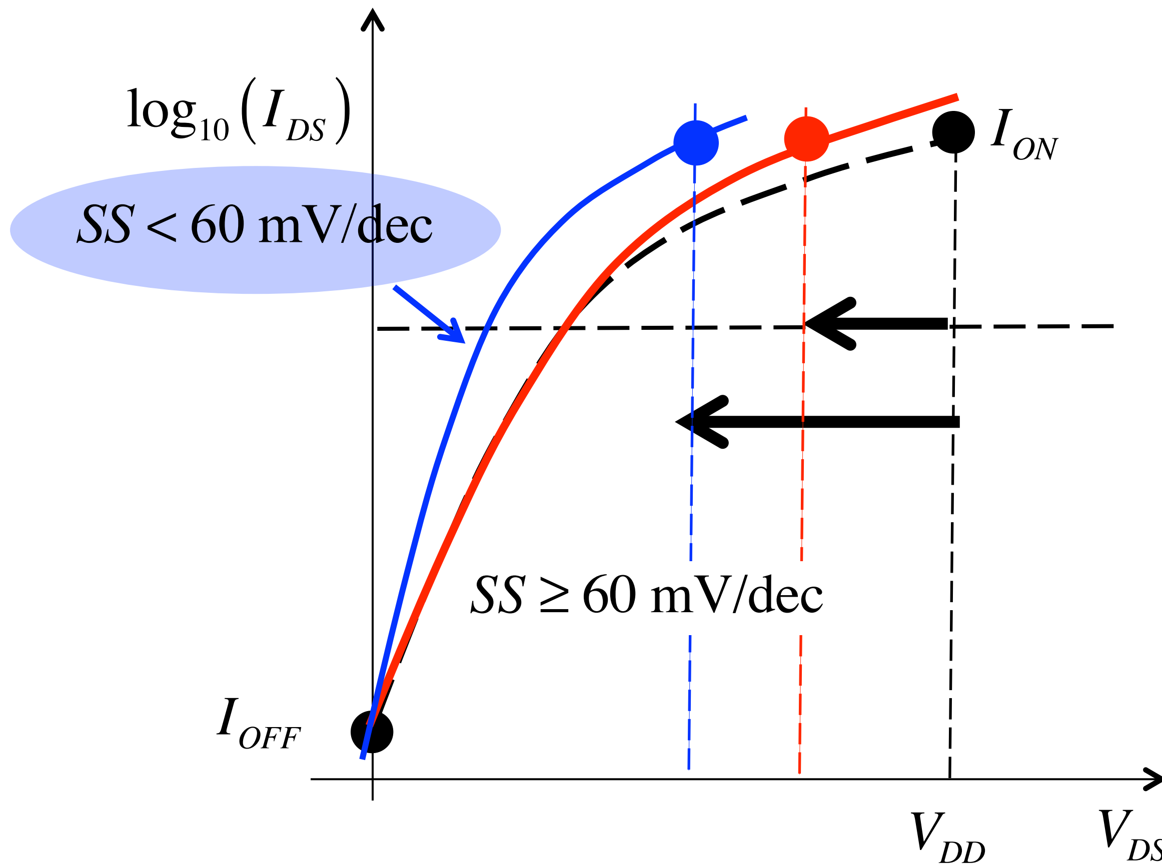
Low-voltage: challenges



Lundstrom, et al. IEDM 2015

Low-voltage: approaches



1) Red option:

-ON-currernt (III-V FETs, NW FETs, even BJTs)

2) Blue option:

-SS (internal gain FETs, TFETs)

Lundstrom, et al. IEDM 2015

MIT VS (MVS) Model

1674 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 56, NO. 8, AUGUST 2009

A Simple Semiempirical Short-Channel MOSFET Current–Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters

$$\frac{1}{\mu_n} \rightarrow \frac{1}{\mu_{app}}$$ "apparent mobility"

$$\upsilon_{sat} \rightarrow \upsilon_{inj}$$ "injection velocity"

M. S. Lundstrom and D. A. Antoniadis, "Compact Models and the Physics of Nanoscale FETs," *IEEE Trans. Electron Dev.*, **61**, pp. 225-233, 2014.

MVS-2 Model

- Includes FD statistics and nonparabolicity
- Improved capacitance model (i.e. quantum effects)
- Semi-empirical electrostatics
- **Predicts** injection velocity and complete IV characteristics from m*, mobility, L_{eff}, and degeneracy.

(See invited paper 28.6 by Rakheja and Antoniadis.)

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1) Introduction

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3) High channel mobility MOSFETs
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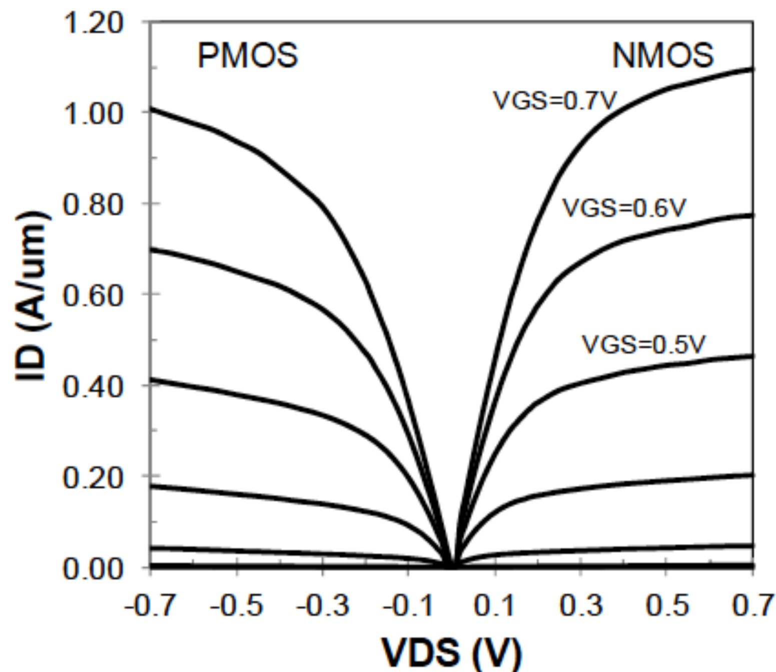
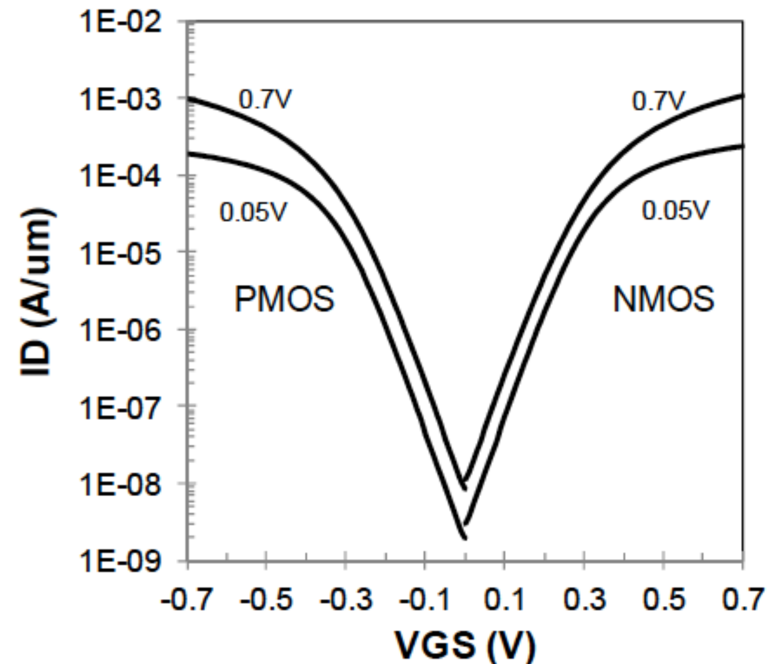
14 nm CMOS FinFET technology





S. Natarajan, *et al.*, "A 14 nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 μm^2 SRAM cell size." IEDM 2014.

Benchmark Low Voltage Si Device

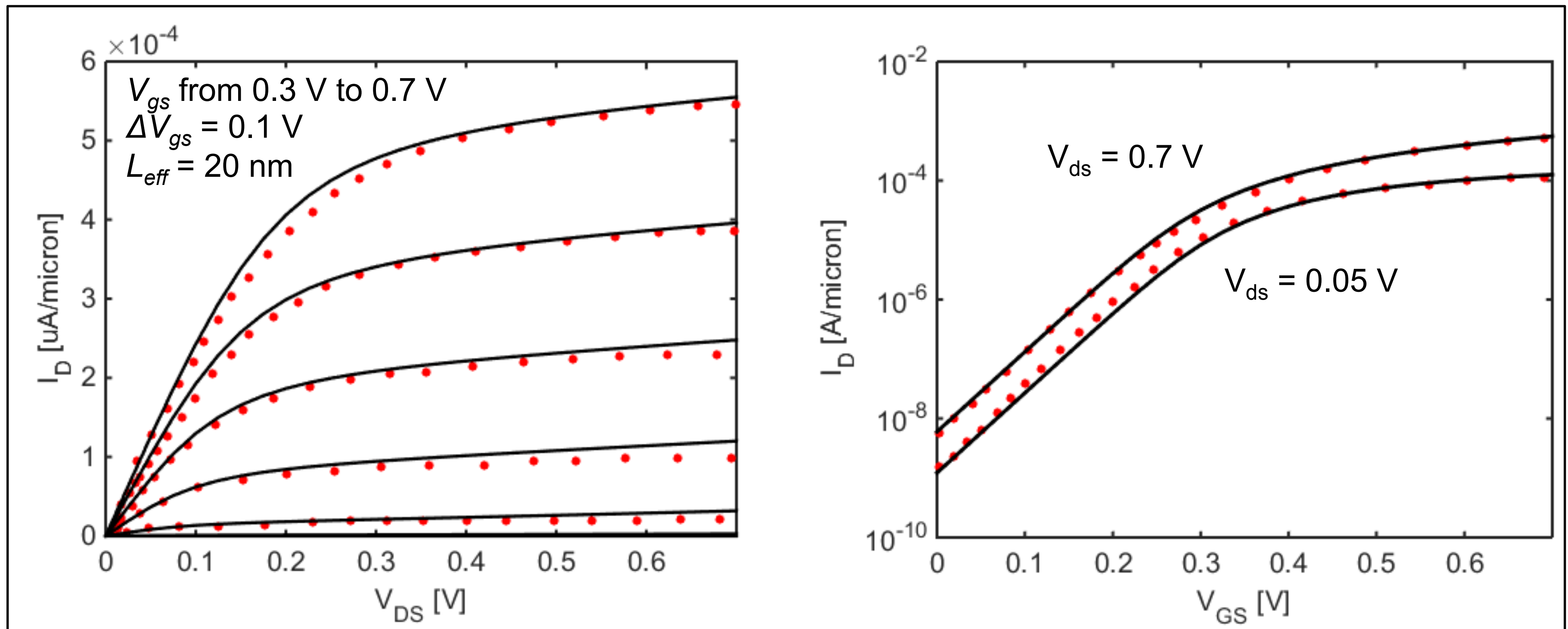
1) Map the FinFET to an "equivalent" planar structure. (Divide measured current per micron by 2)

2) Fit the 14 nm Intel data with a planar MVS-2 model.

3) Then, assume EOT = 0.6 nm and T_{Si} = 8 nm and the same MVS fitting parameters for *SS*, *DIBL*, mobility, R_S and R_D, etc., to produce two benchmark low voltage devices:

Low Power: V_{DD} = 0.5 V, I_{OFF} = 100 pA/um
High Performance: V_{DD} = 0.5 V, I_{OFF} = 100 nA/um

MVS-2 fit to 14 nm FinFET data

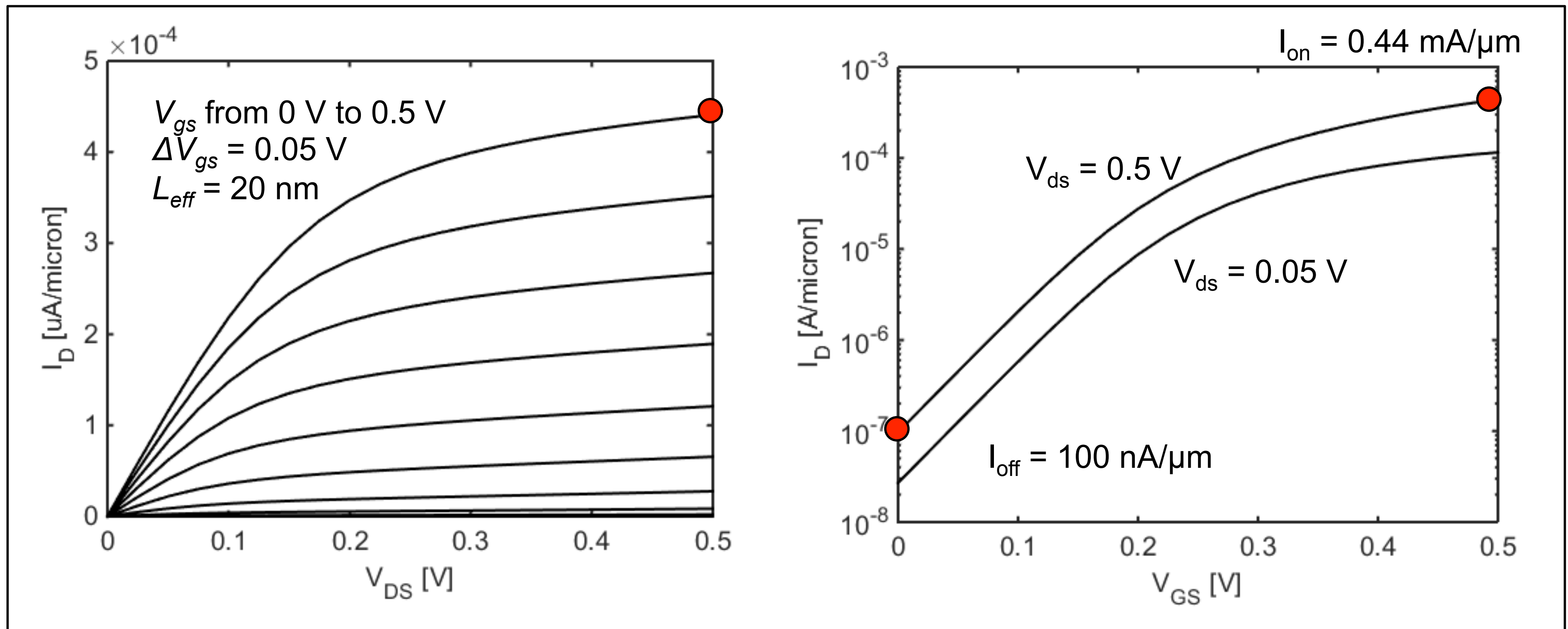


<u>Key parameters</u>

EOT= 0.9 nm / L_{eff} = 20 nm
Subthreshold Swing = 75 mV/decade
DIBL = 50 mV/V
R_S, R_D = 100 ohm.µm

Effective mobility= 200 cm^2/V.s
$m_t^* = 0.19m_0$; $m_l^* = 0.89m_0$
$v_T = 1.13\text{x}10^7$ cm/s (non-degenerate):
assumed constant v_{inj}

Benchmark LV / High Performance Si N-MOSFET



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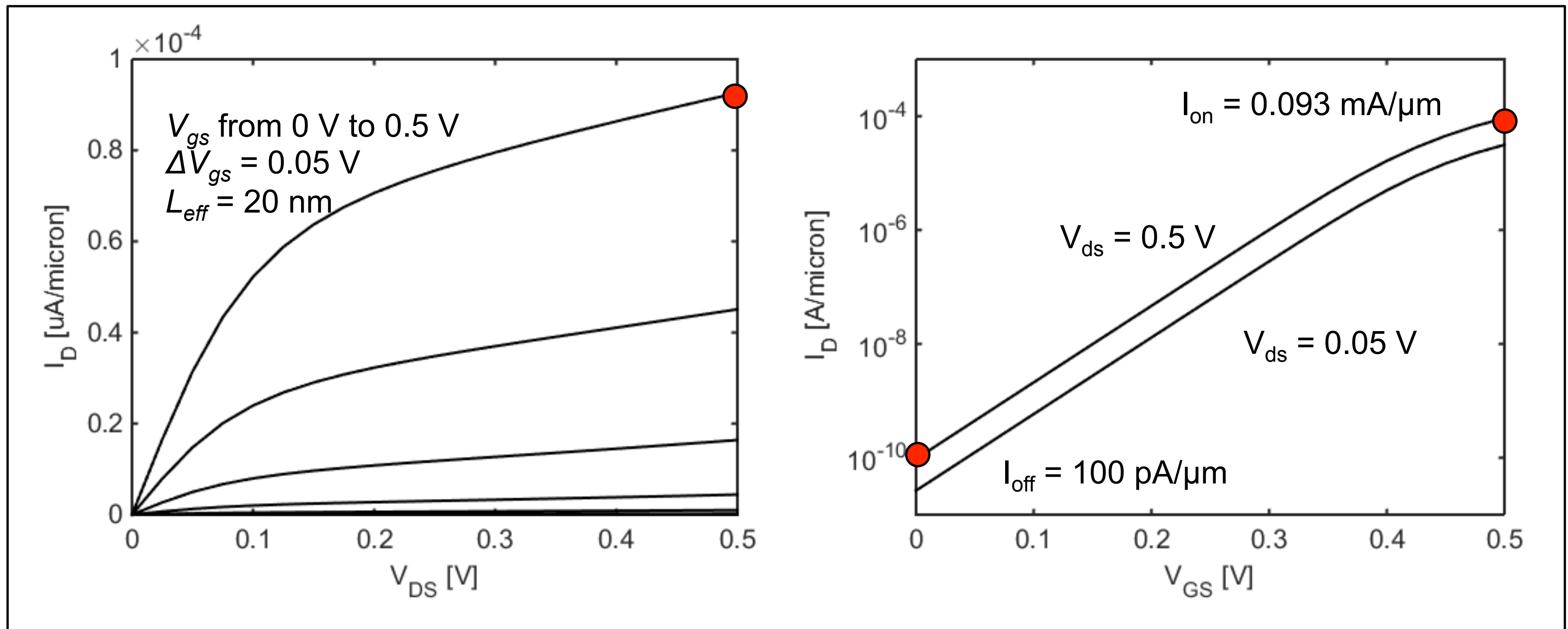
Effective mobility= 200 cm^2/V.s
m_t^* = 0.19m_0; m_l^* = 0.89m_0 ->
v_T = 1.13x10^7 cm/s (non-degenerate):
assumed constant $v_{inj} \approx$ 0.9 x10^7 cm/s

Benchmark LV / Low Power Si N-MOSFET



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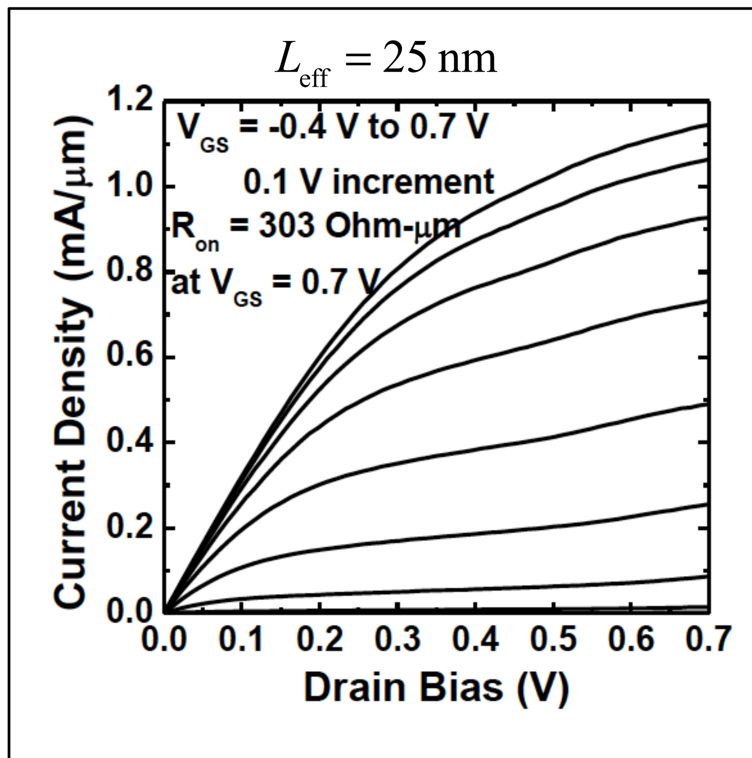
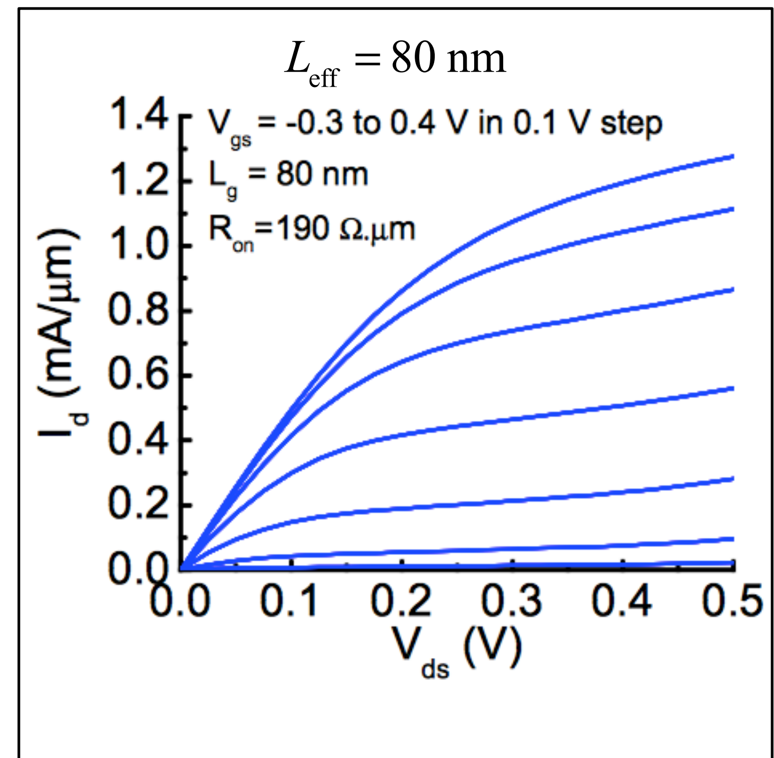
III-V MOSFETs; recent results

Rodwell Group



S. Lee, et al., VLSI Tech. Symp. 2014.

del Alamo Group



J. Lee, et al., IEDM, 2014.

III-V MOSFETs

Potential advantages:

- ✓ High mobility
- ✓ High injection velocity (small m^*)
- ✓ Near-ballistic performance

Trade-offs and Concerns:

- o Low DOS and gate cap (small m^*)
- o Tunneling (small m^*)
- o Source starvation

Lundstrom, et al. IEDM 2015

Mobility and injection velocity

Silicon:

$$\mu_n \approx 200 \text{ cm}^2/\text{V-s} = \frac{\upsilon_T \lambda}{2\left(k_B T/q\right)}$$

$$\upsilon_T = 1.13 \times 10^7 \text{ cm/s}$$

$$\lambda_0 \approx 9 \text{ nm}$$

InAs:

$$\mu_n \approx 12{,}500 \text{ cm}^2/\text{V-s}$$

$$\upsilon_T = 2.9 \times 10^7 \text{ cm/s} \quad \left(m^* = 0.035 m_0\right)$$

$$\lambda_0 \approx 200 \text{ nm}$$

***L* = 20 nm**

Si: $L \approx 2$ mfps

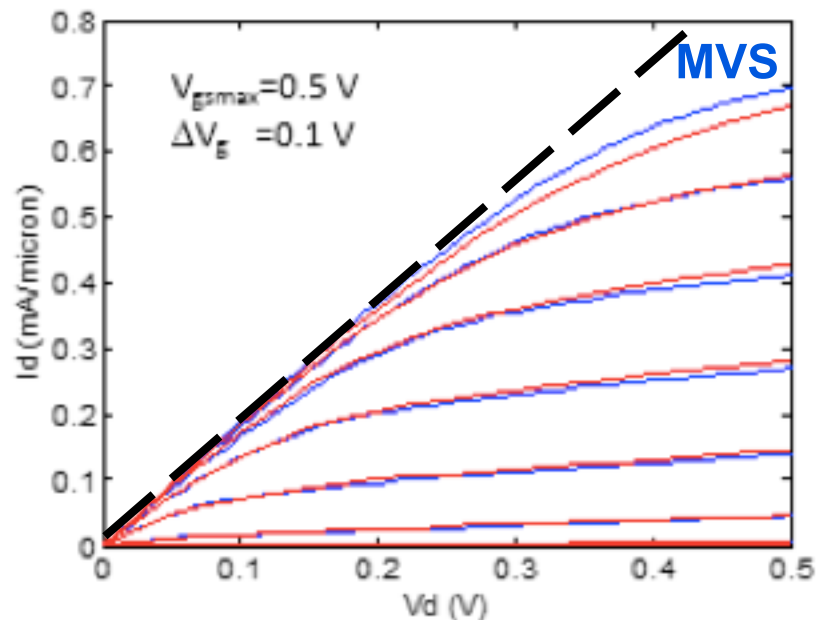
InAs: $L \approx 0.1$ mfp

Expect near-ballistic operation.

Lundstrom, et al. IEDM 2015

Increasing importance of ballistic mobility

InGaAs 30-nm gate length HEMT
(D.H. Kim and J. del Alamo, EDL 08)



$$\mu_{app} \approx 1300 \text{ cm}^2/\text{V-s}$$

$$\mu_n \approx 12{,}500 \text{ cm}^2/\text{V-s}$$

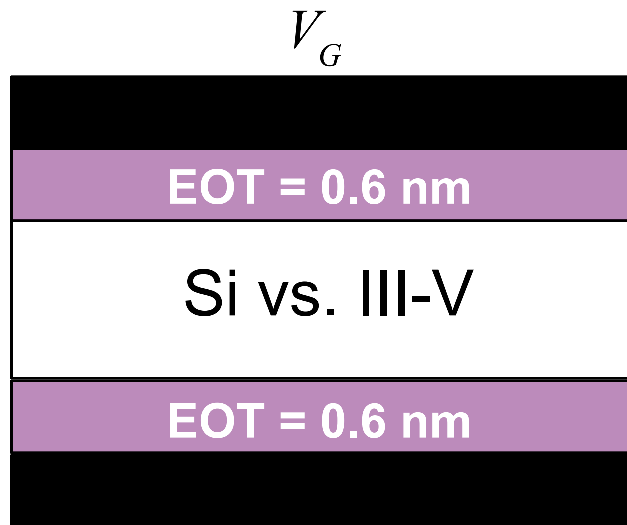
$$\frac{1}{\mu_{app}} = \frac{1}{\mu_n} + \frac{1}{\mu_B}$$

$$\mu_n = \frac{\upsilon_T \lambda}{2\left(k_B T/q\right)} \qquad \mu_B = \frac{\upsilon_T L_{eff}}{2\left(k_B T/q\right)}$$

Lundstrom, et al. IEDM 2015

“DOS bottleneck”

nextNano SP simulations



V_G

$$\frac{1}{C_G} = \frac{1}{2C_{ox}} + \frac{1}{C_S}$$

$$C_S < C_Q = q^2 D_{2D}\left(E_F\right)$$

Silicon:

EOT = 0.6 nm
T_{Si} = 8 nm

$$C_G = 0.6 \times 2C_{ox}$$

InAs:

EOT = 0.6 nm
T_{InAs} = 8 nm

$$C_G = 0.2 \times 2C_{ox}$$

Lundstrom, et al. IEDM 2015

InAs MOSFET vs. Si CMOS

Approach:

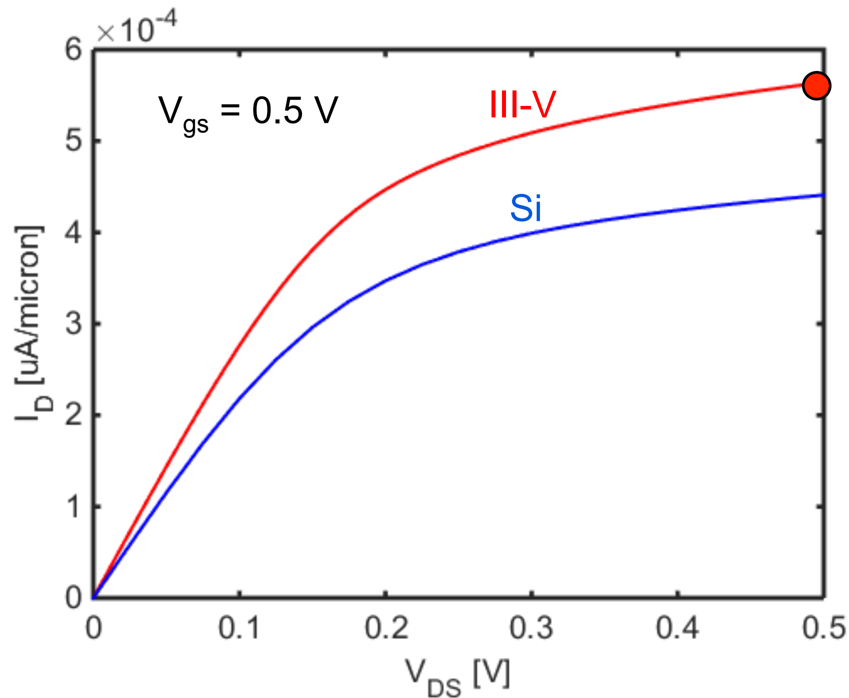
Compare a hypothetical InAs FinFET with EOT = 0.6 nm, *L* = 20 nm, to the benchmark Si device.

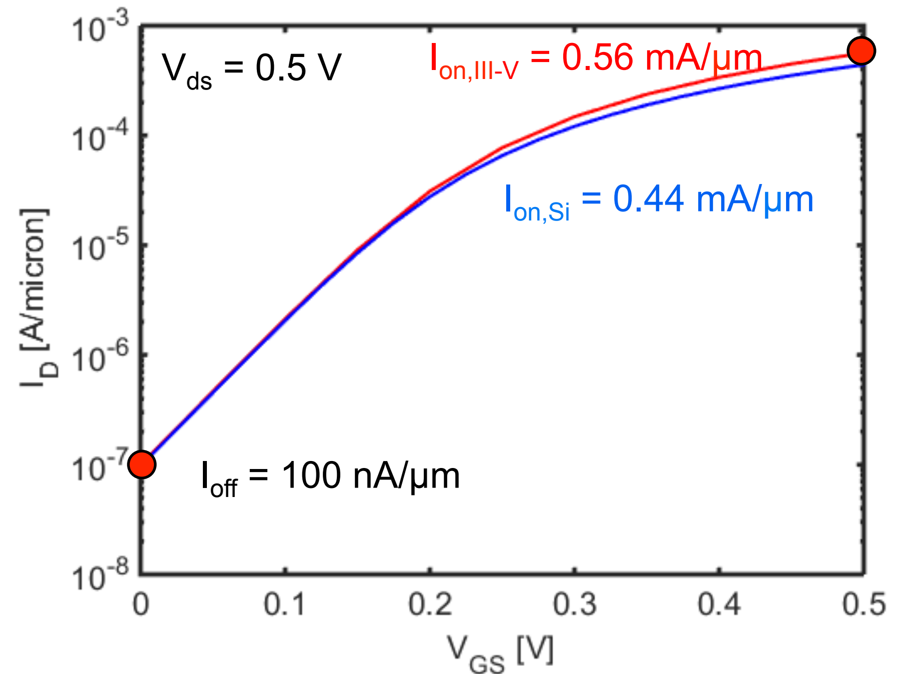
Assume the same series resistance and electrostatic parameters (SS and DIBL), but use appropriate eff. mass, non-parabolicity, and degeneracy for charge and injection velocity for **quasi-ballistic transport** in InAs.

Project High Performance and Low Power IV's with the MVS-2 model.

Lundstrom, et al. IEDM 2015

Benchmark LV/HP N-MOSFET Using MVS-2



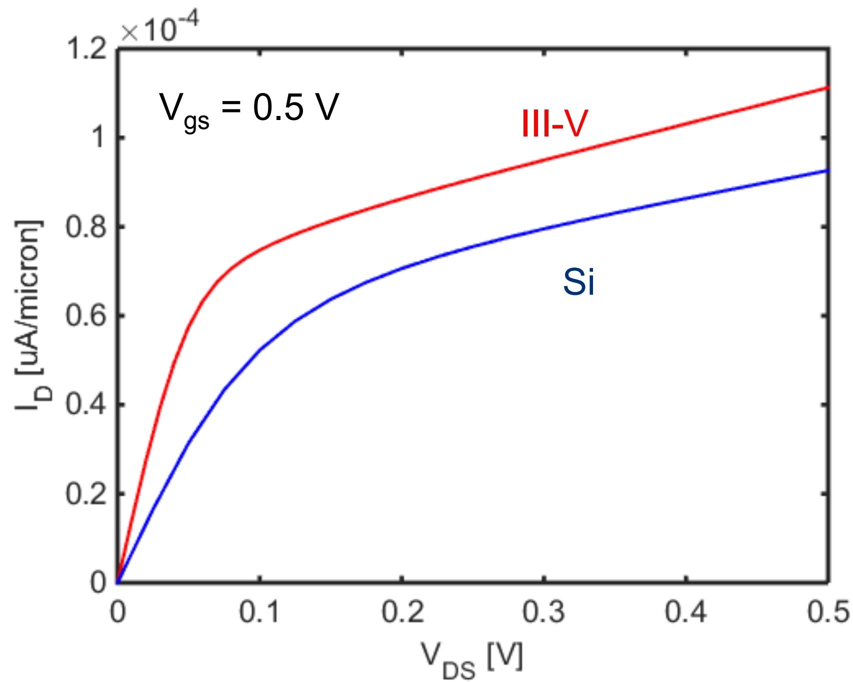


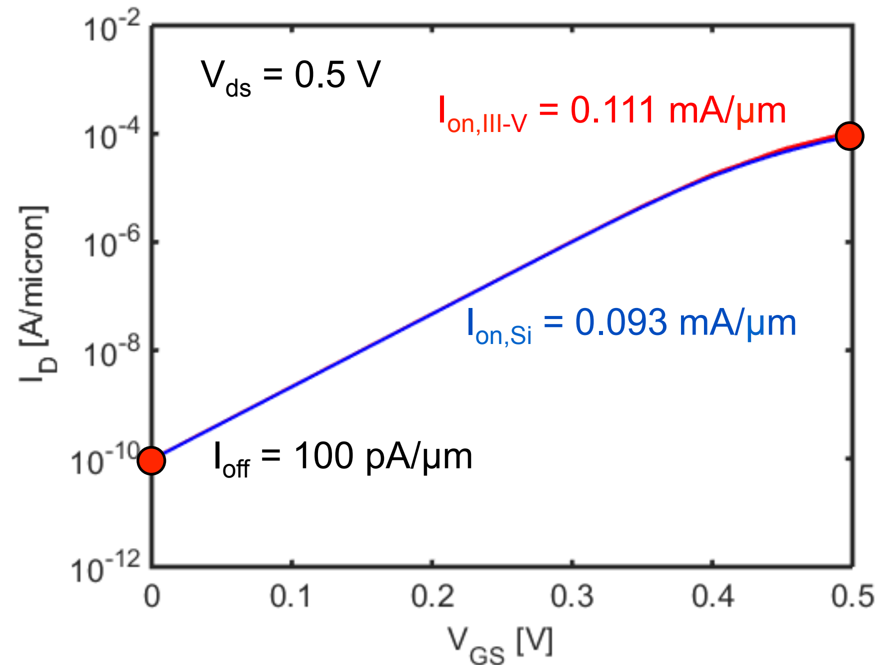
Key parameters for InAs

EOT = 0.6 nm / L_{eff} = 20 nm
Subthreshold Swing = 75 mV/decade
DIBL = 50 mV/V
R_S, R_D=100 ohm.μm

Effective mobility = 10000 cm^2/V.s
m* = $0.035m_0$ ->
$v_T = 2.88 \times 10^7$ cm/s (non-degenerate):
degeneracy included in $v_{inj} \approx 3.4 \times 10^7$ cm/s

Benchmark LV/LP N-MOSFET Using MVS-2





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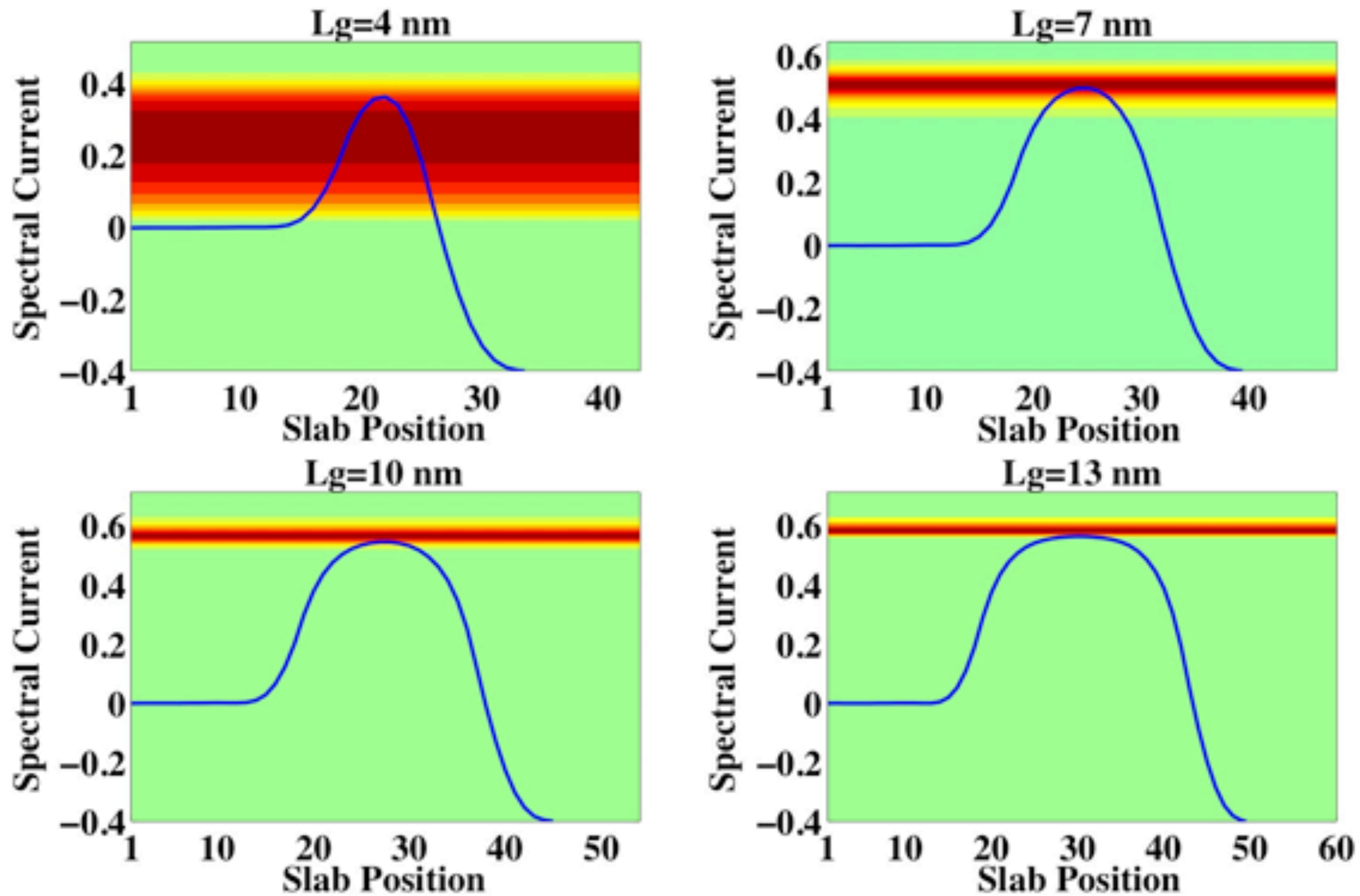
Effective mobility= 10000 cm^2/V.s
m* = $0.035m_0$ ->
v_T = 2.88×10^7 cm/s (non-degenerate):
degeneracy included in v_{inj}

High channel mobility summary

- Gate capacitance / injection velocity trade-off results in performance that is similar to silicon.
- Other materials (e.g. Ge) and bandstructure engineering to increase DOS without lowering velocity should be examined.
- Tunneling will increase leakage.

Importance of Tunneling



(Provided by M. Luisier, ETH Zurich)

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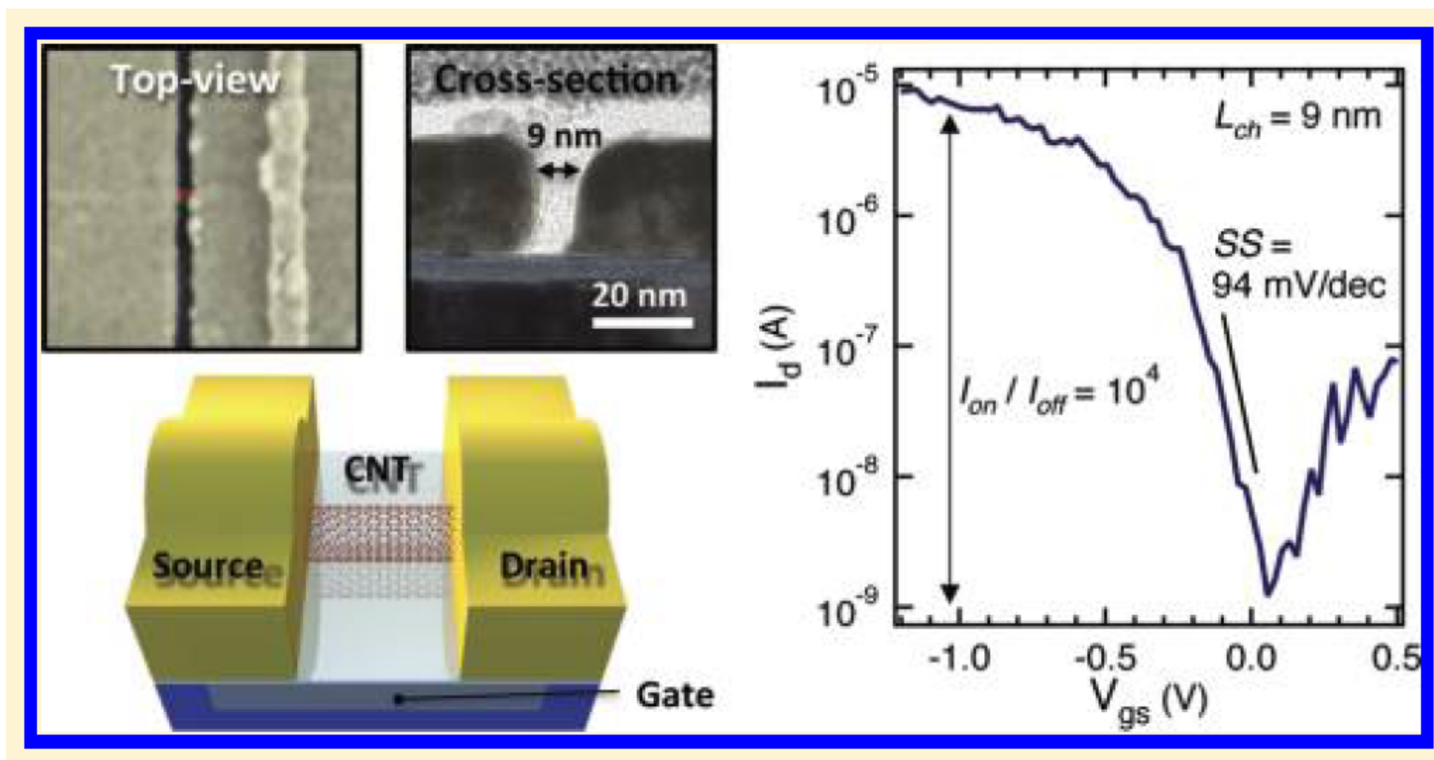
Recent results: Sub-10 nm CNTFETs



Aaron Franklin, et al., *Nano Letters*, **12**, pp. 758-762, 2012.

Nanowire FETs

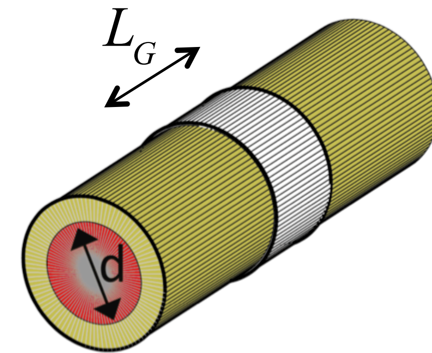
Key advantage:
-electrostatics

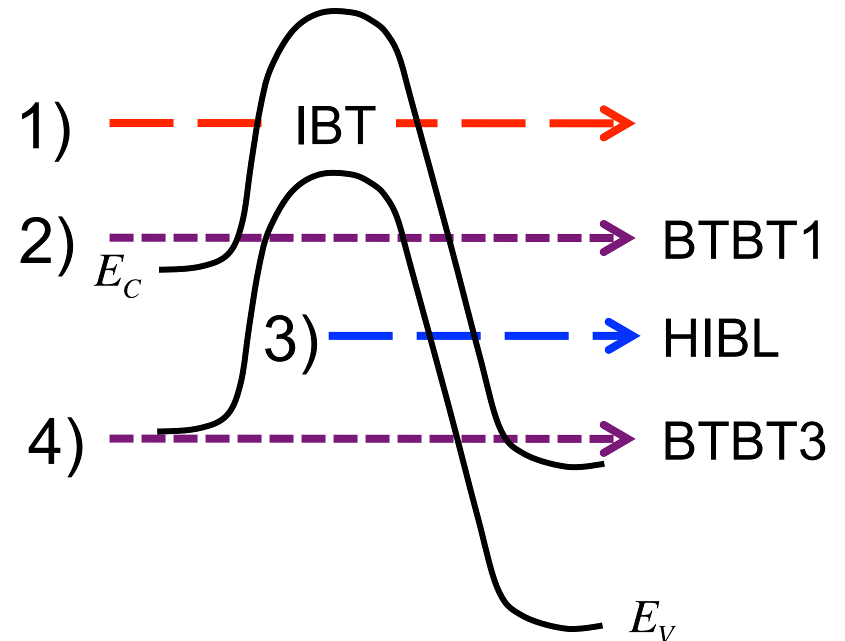
$$L_{\min} \approx 3R$$

$$L_{\min} \approx 5 \text{ nm} \quad (\text{Si})$$

$$L_{\min} \approx 10 \text{ nm} \left(\text{InGaAs}\right)$$

Bo Yu, et al, *TED*, 2008.



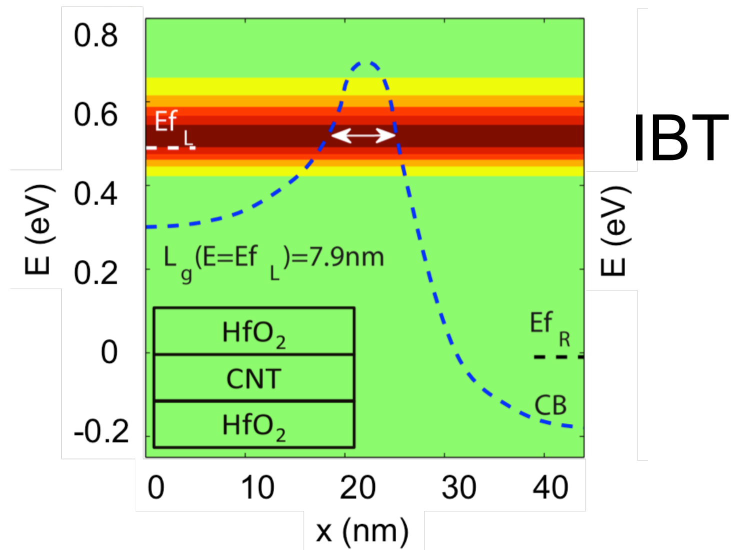


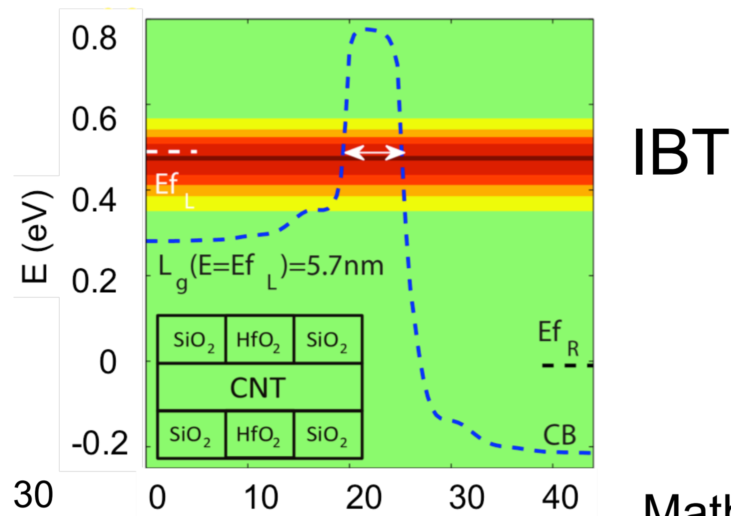
Key challenge:
-tunneling

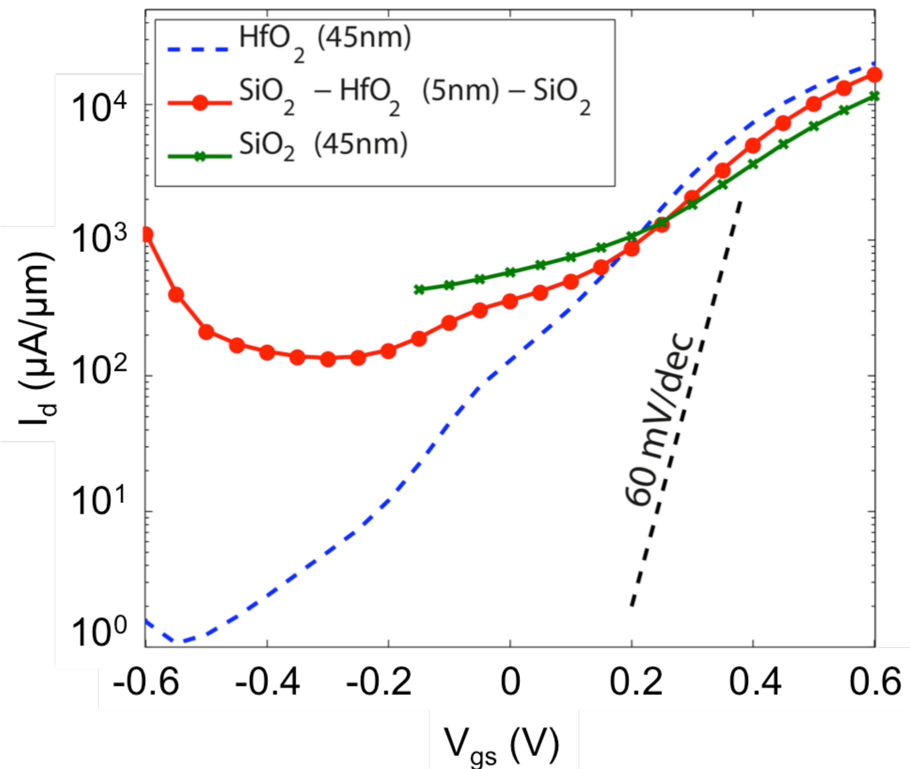
$$4)\ BTBT3 = 0 \ \text{ if } \ E_G > qV_{DS}$$

Lundstrom, et al. IEDM 2015

NW FETs: Intraband Tunneling



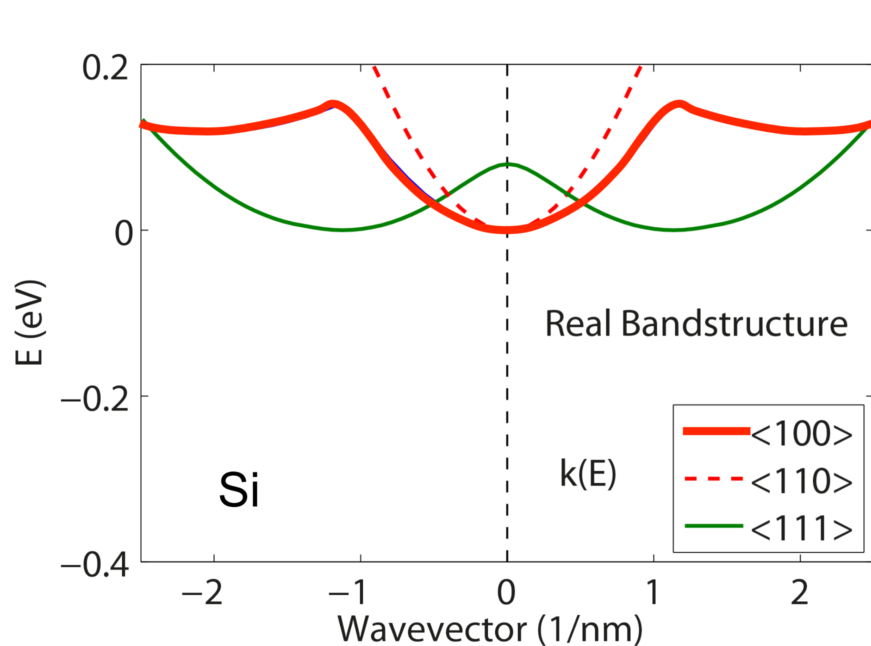


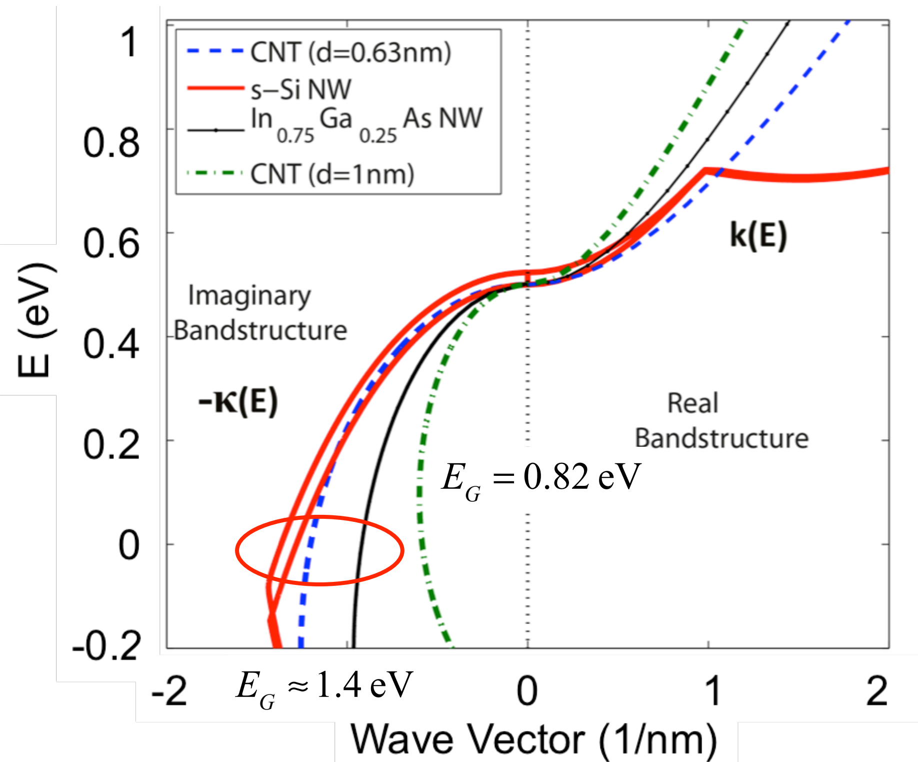


For L < 10 nm, shape of the potential barrier is critical for IBT.

Mathieu Luisier, et al., IEDM, 2011.

NW FETs: Real vs. imaginary bandstructure





$$E > E_C : \quad \psi \propto e^{ikx}$$

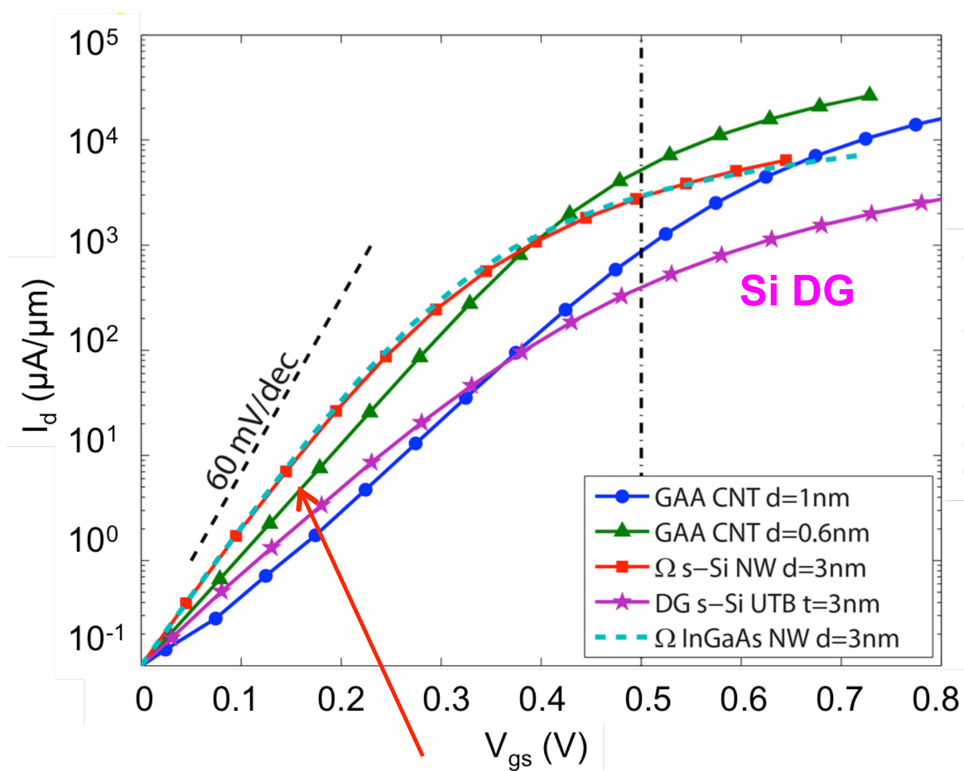
$$E_V < E < E_C : \quad \psi \propto e^{-\kappa x}$$

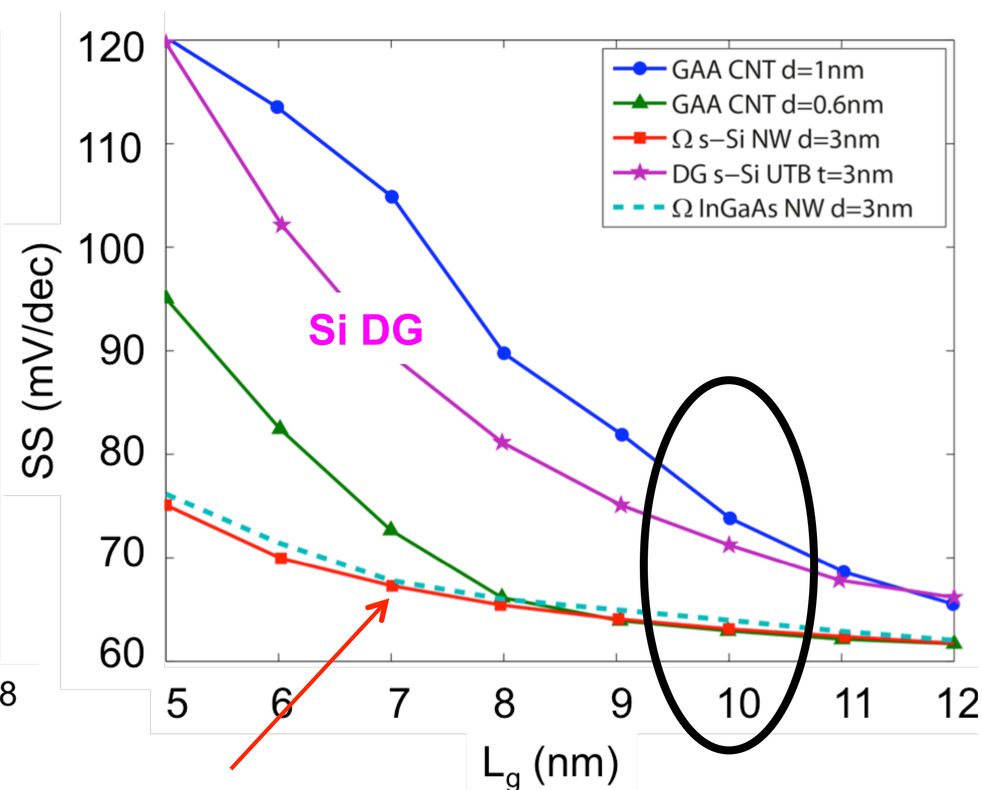
Bandgap affects Intra Band Tunneling.

Mathieu Luisier, *et al*., IEDM, 2011.

NW FETs: Performance projections

L_G = 5 nm EOT = 0.65 nm (HfO_2) V_{DD} = 0.5 V





Good performance for E_G > 1 eV.

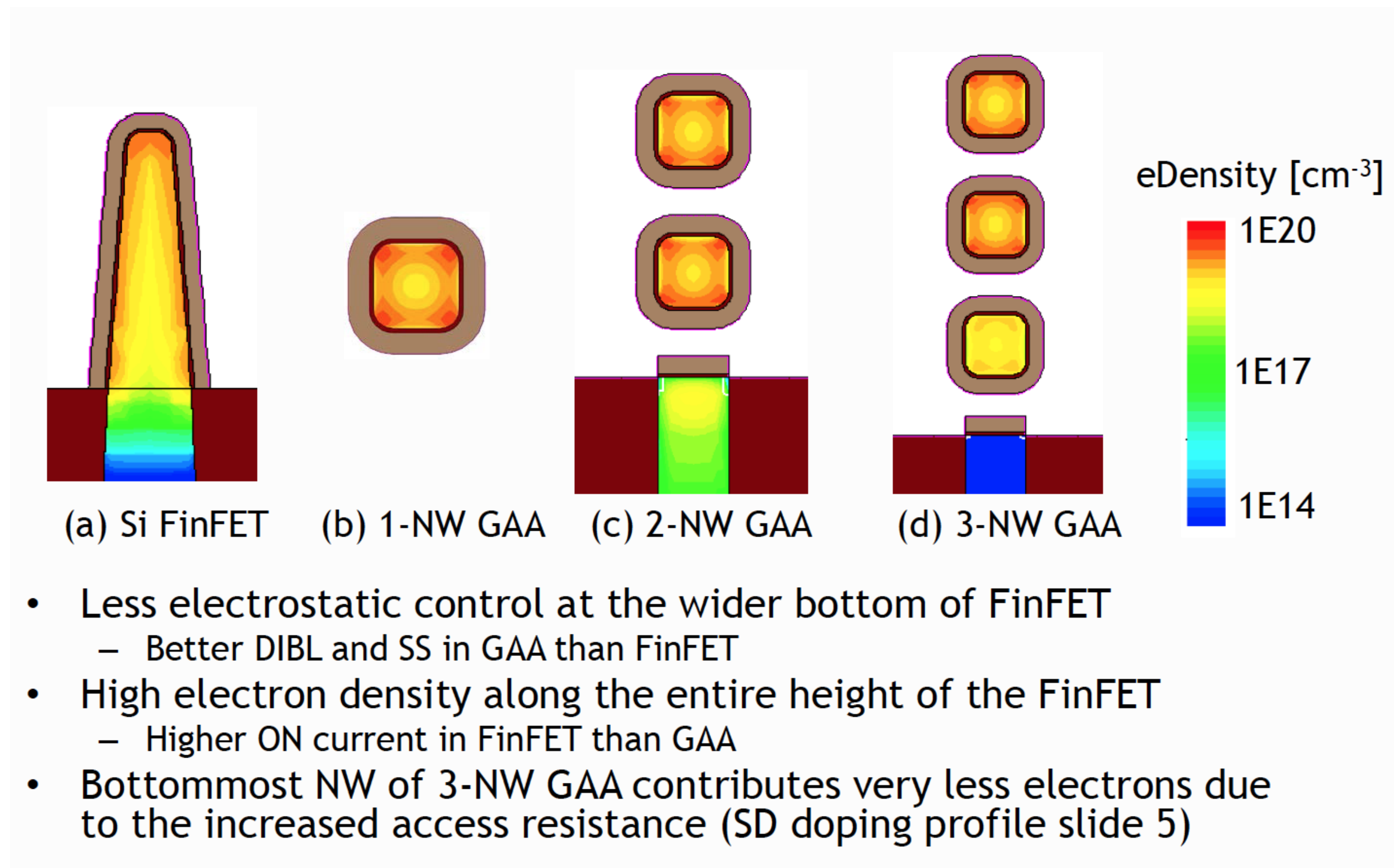
For L_G > 8 nm and E_G > 1eV, tunneling not an issue.

Mathieu Luisier, *et al*., IEDM, 2011.

NW FETs: Summary

- GAA required for L_G < 10 nm.
- Tunneling is critical for L_G < 10 nm. E_G > 1 eV is necessary. Heavy m^* gives low off-current, but light m^* gives good on-current.
- **Key technology question:** "How much effective width can be put into the required gate pitch?"

FinFETs vs. NWs



(Source: Suman Datta – see online talk)

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-iMOS

-Fe (negative capacitance) FETs

-Landau switches (FE, AFE, NEMS caps)

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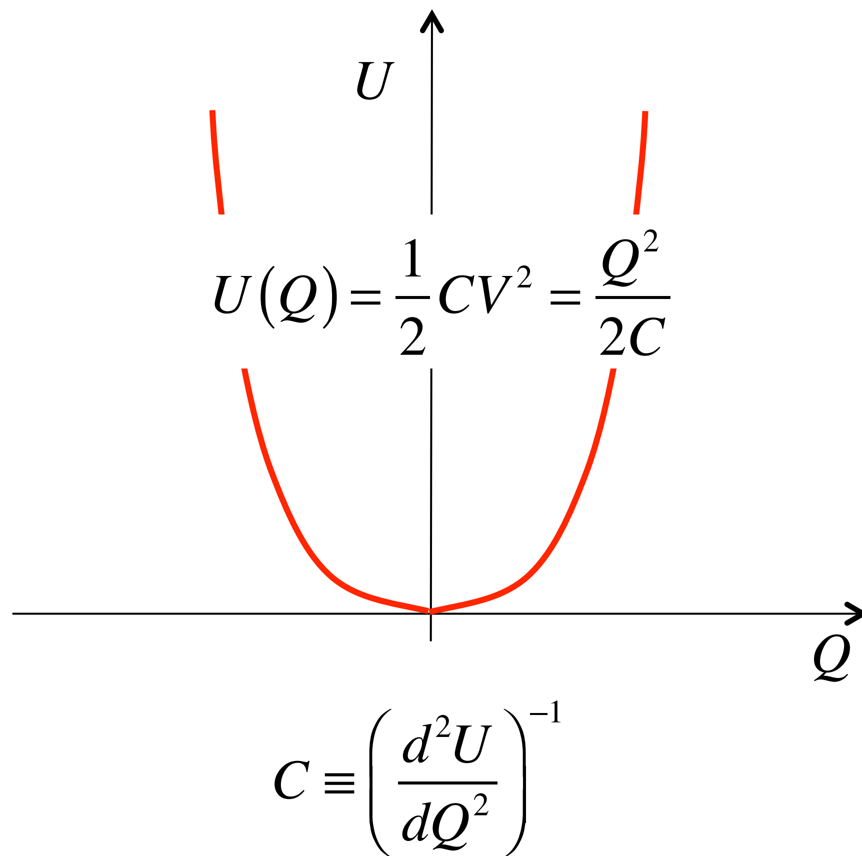
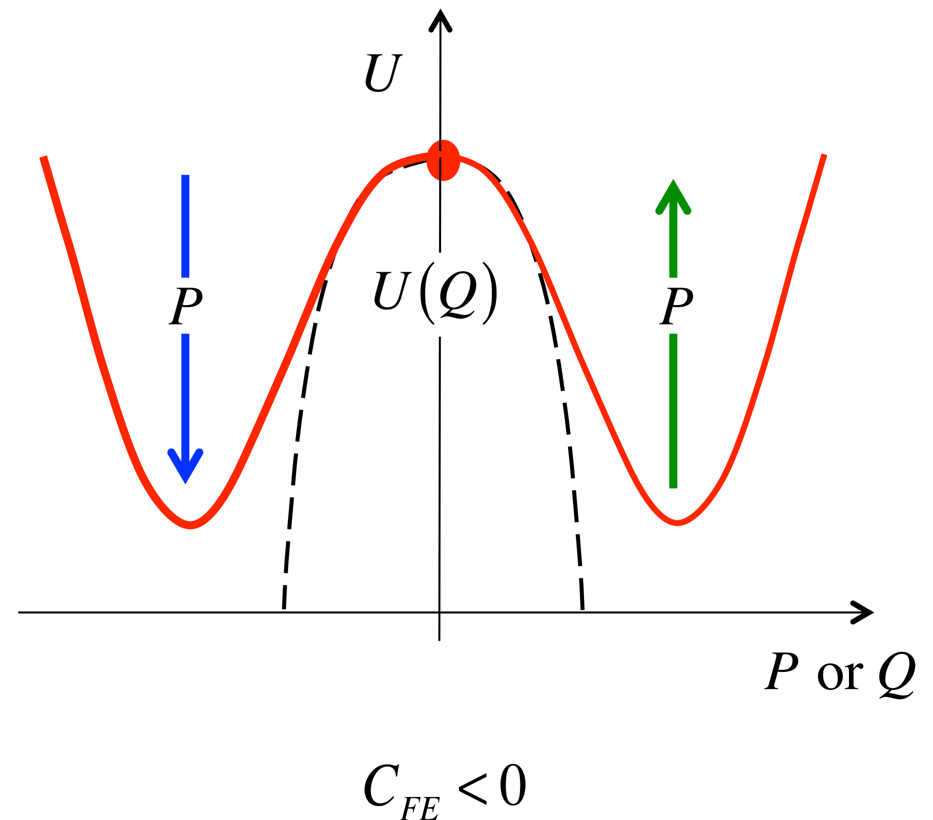
Basic Concept: Negative capacitance



$$U(Q) = \frac{1}{2}CV^2 = \frac{Q^2}{2C}$$

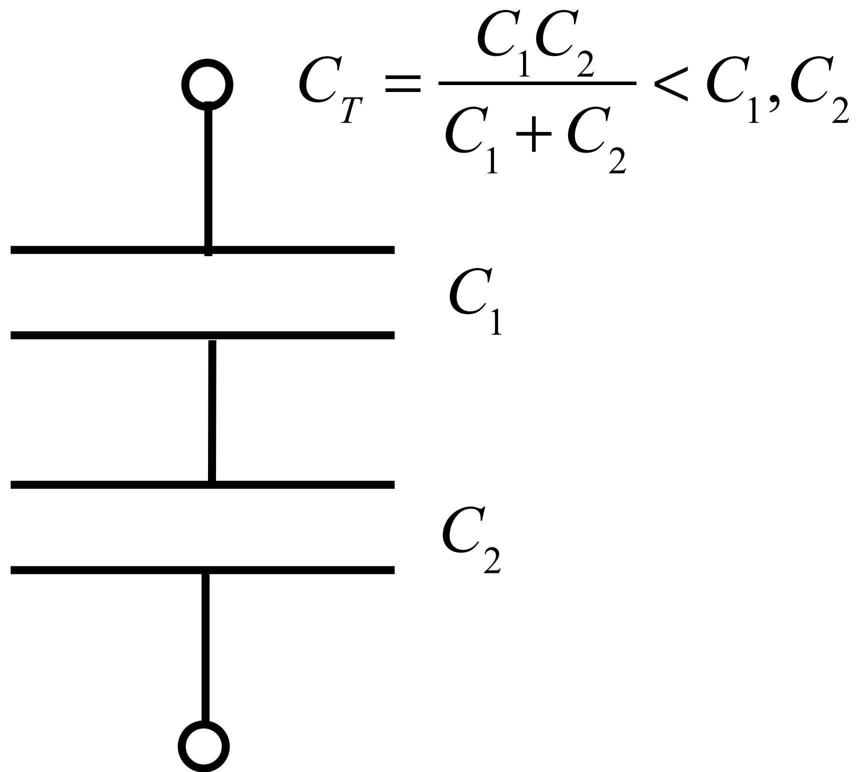
$$C \equiv \left(\frac{d^2U}{dQ^2}\right)^{-1}$$

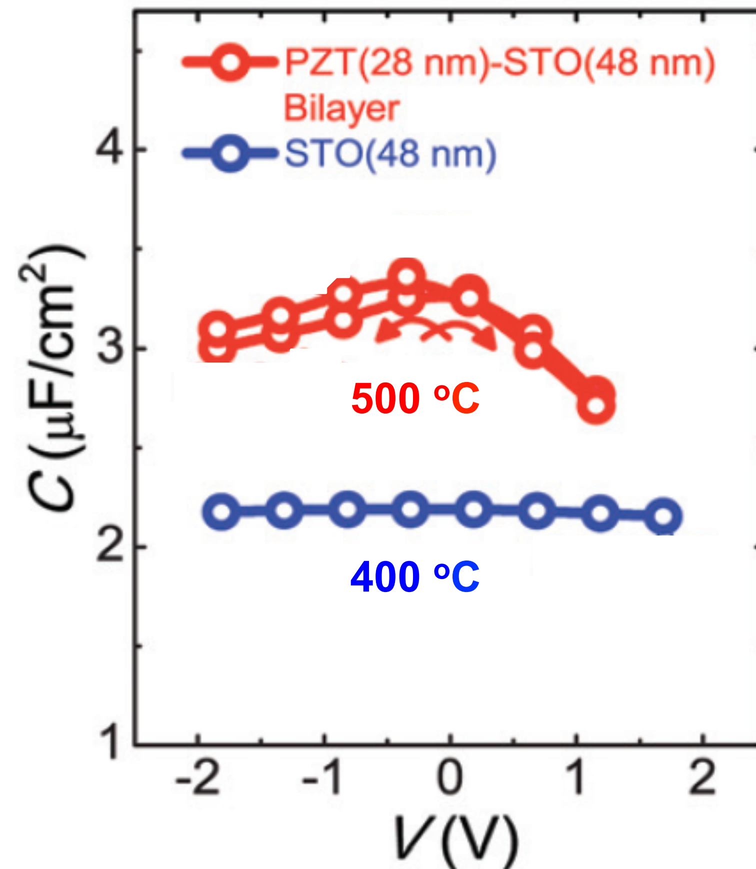


$$C_{FE} < 0$$

Lundstrom, et al. IEDM 2015

Experimental confirmation

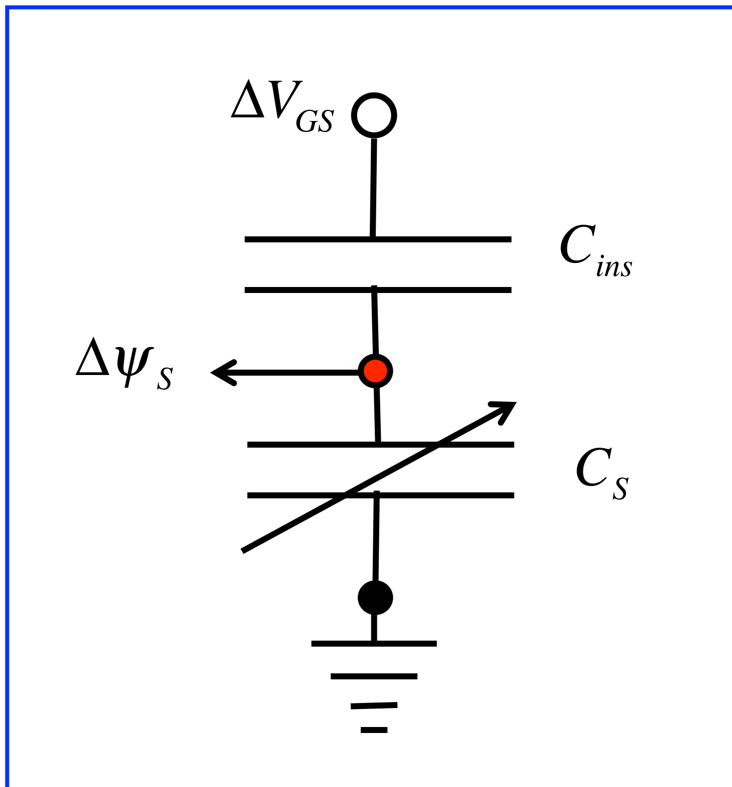




Asif Islam Khan, *et al.*, *Appl. Phys. Lett.*, 2011.

Subthreshold swing

$$SS \equiv \frac{\partial V_{GS}}{\partial(\log_{10} I_D)} = \frac{\partial \psi_S}{\partial(\log_{10} I_D)} \times \frac{dV_{GS}}{d\psi_S} = 60 \ \ \text{mV/dec} \times n$$



$$\Delta \psi_S \approx \Delta V_{GS} \frac{C_{ins}}{C_{ins} + C_S} = \frac{\Delta V_{GS}}{1 + C_S / C_{ins}}$$

$$\Delta \psi_S = \frac{\Delta V_{GS}}{n}$$

$$n = 1 + C_S / C_{ins} \geq 1$$

$$SS = 60 \times n \geq 60 \text{ mV/dec}$$

FeFET: basic concept

$$\Delta\psi_S = \frac{\Delta V_{GS}}{n} = \frac{\Delta V_{GS}}{1 + C_S / C_{ins}}$$

$$SS = 60 \text{ mV/dec} \times n$$

$$C_{ins} = C_{FE} < 0$$

$$n = 1 - C_S / \left|C_{FE}\right| < 1$$

$$\Delta\psi_S = \frac{\Delta V_{GS}}{1 - C_S / \left|C_{FE}\right|} = \beta \Delta V_{GS}$$

$$\Delta\psi_S = \beta \Delta V_{GS}$$

$$\beta = \frac{1}{1 - C_S / \left|C_{FE}\right|}$$

$$\beta >> 1 \text{ or } (n << 1) \text{ if } \left|C_{FE}\right| \approx C_S$$

FeFET: observations

$$\Delta\psi_S = \beta\,\Delta V_{GS} \qquad \beta = \frac{1}{1 - C_S/\left|C_{FE}\right|} = \frac{1}{n} \qquad \beta >> 1 \text{ or } (n << 1) \text{ if } \left|C_{FE}\right| \approx C_S$$

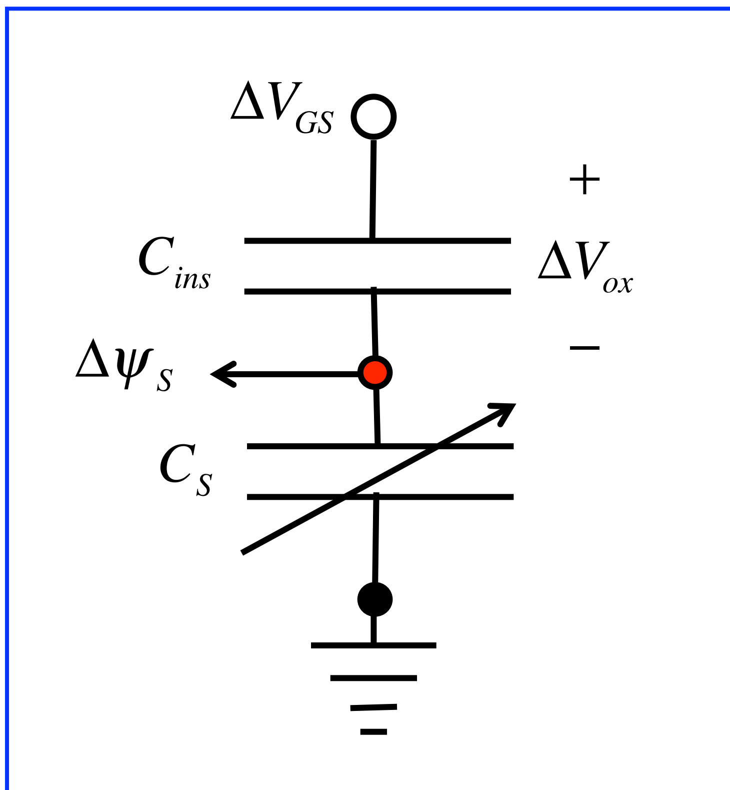
1) Must have $|C_{FE}| > C_S$ for non-hysteretic operation (i.e. positive gate capacitance)

2) Must have $|C_{FE}| \approx C_S$ for $\beta >> 1$.

3) Tricky because $C_S(V_{GS}, V_{DS})$.

4) C_{FE} and C_S not well matched. (i.e. ~250 nm for $BaTiO_3$ and ~5-10 nm for strained HfO_2).

Energy band picture



$$\Delta \psi_S \approx \Delta V_{GS} \frac{C_{ins}}{C_{ins} + C_S}$$

$$\Delta V_{ox} \approx \Delta V_{GS} \frac{C_S}{C_{ins} + C_S}$$

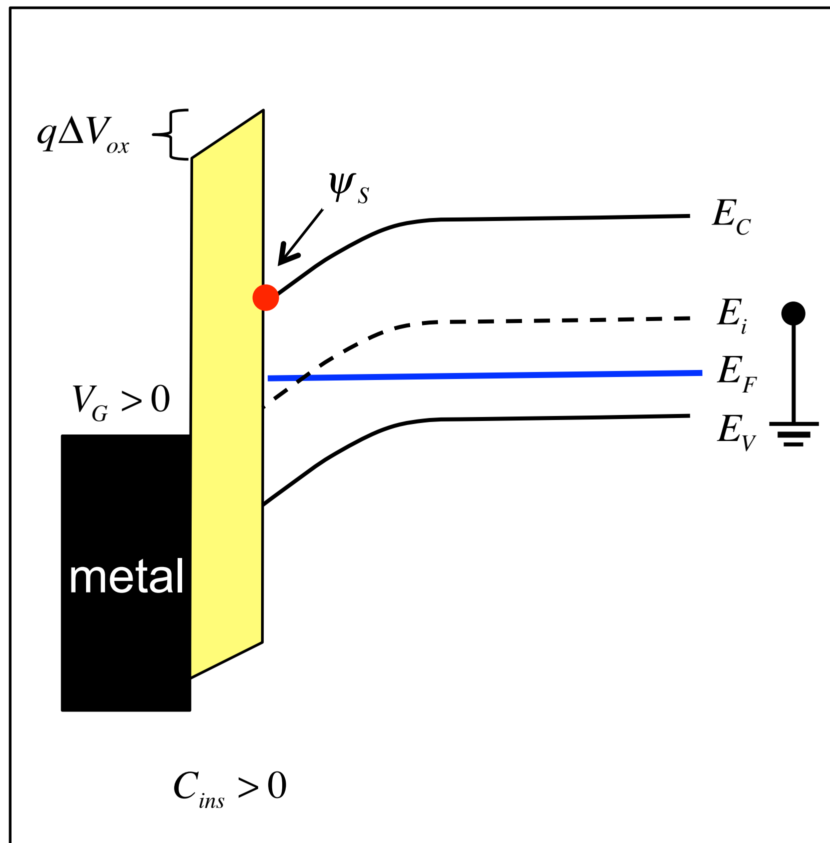
$$C_{ins} = -|C_{FE}| \qquad |C_{FE}| > C_S$$

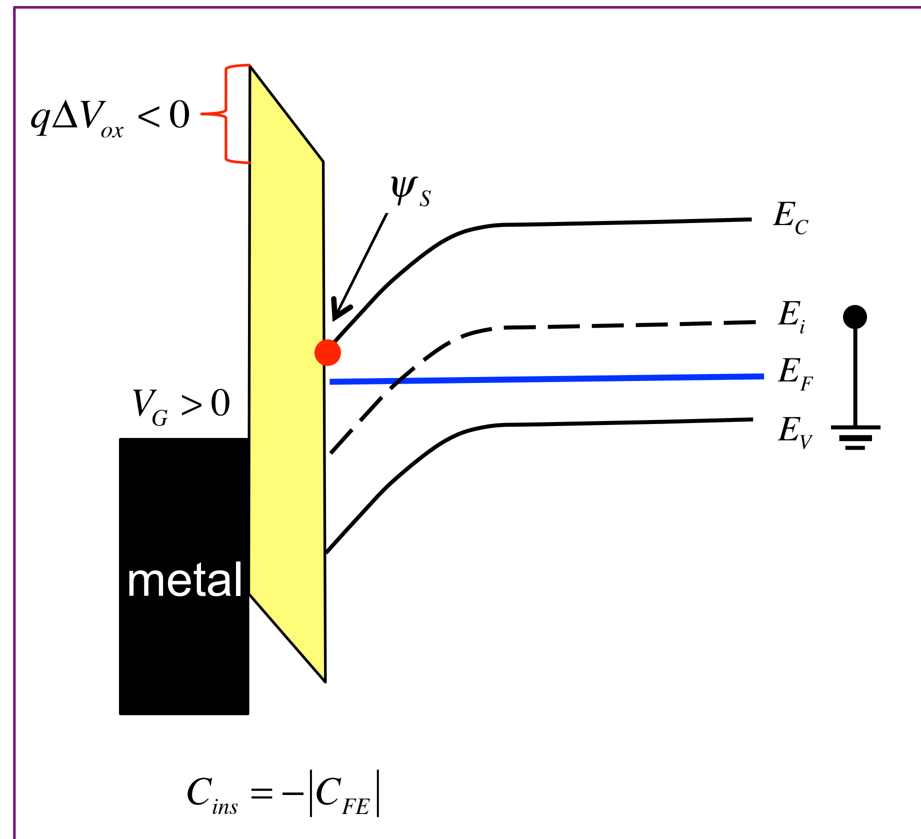
$$\Delta V_{ox} \approx \Delta V_{GS} \frac{C_S}{C_S - |C_{FE}|} < 0$$

$$\psi_S > 0$$

(source: Suman Datta)

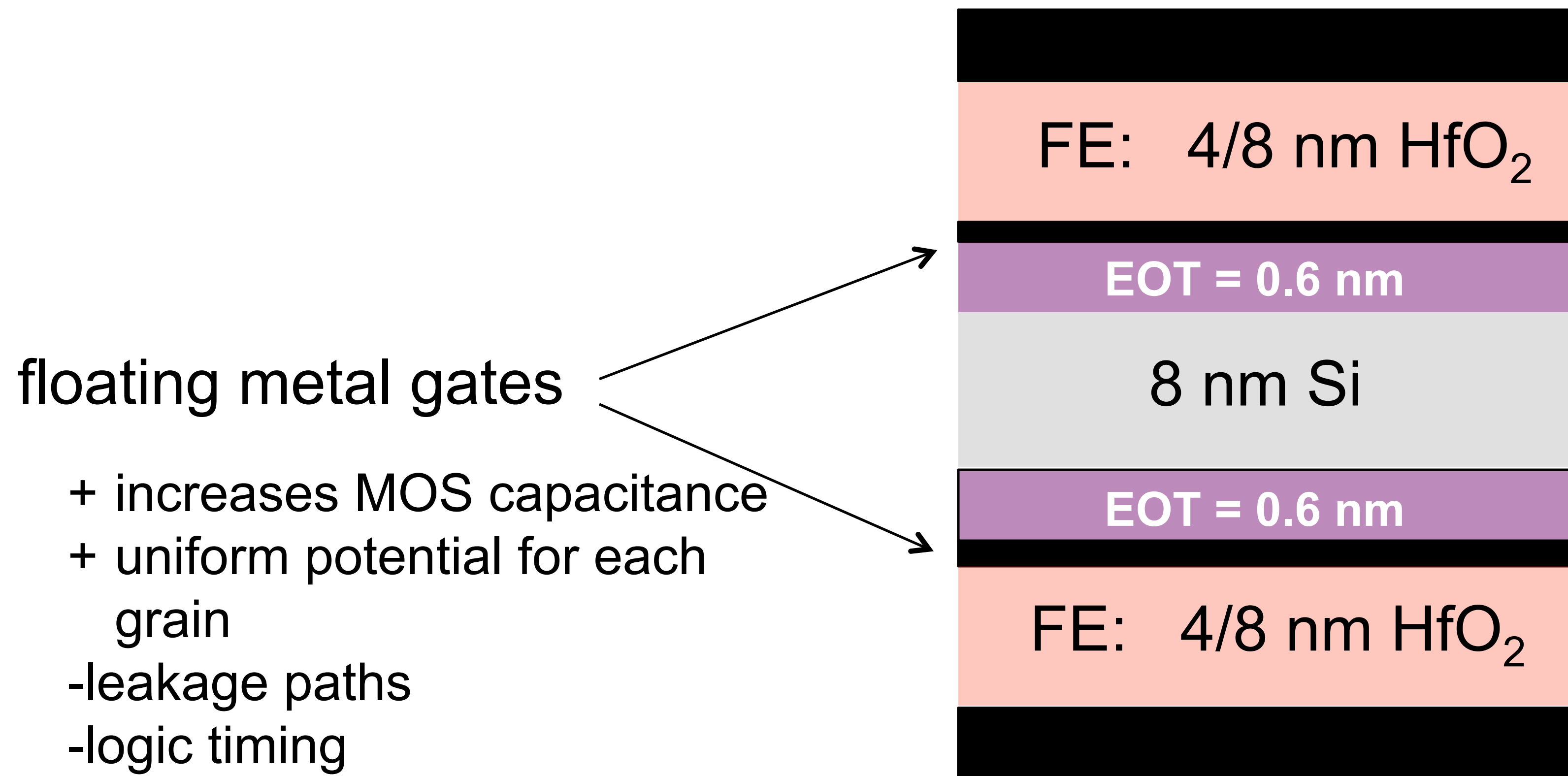
Energy band picture





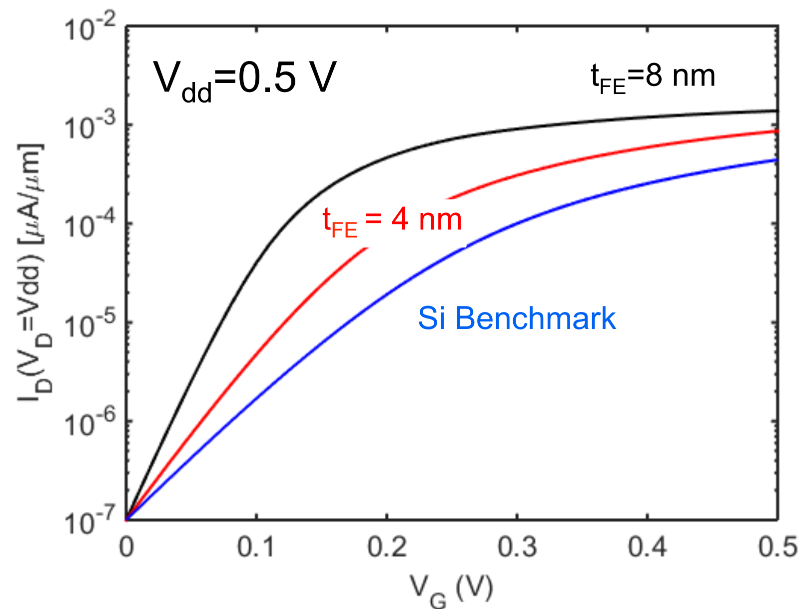
(source: Suman Datta)

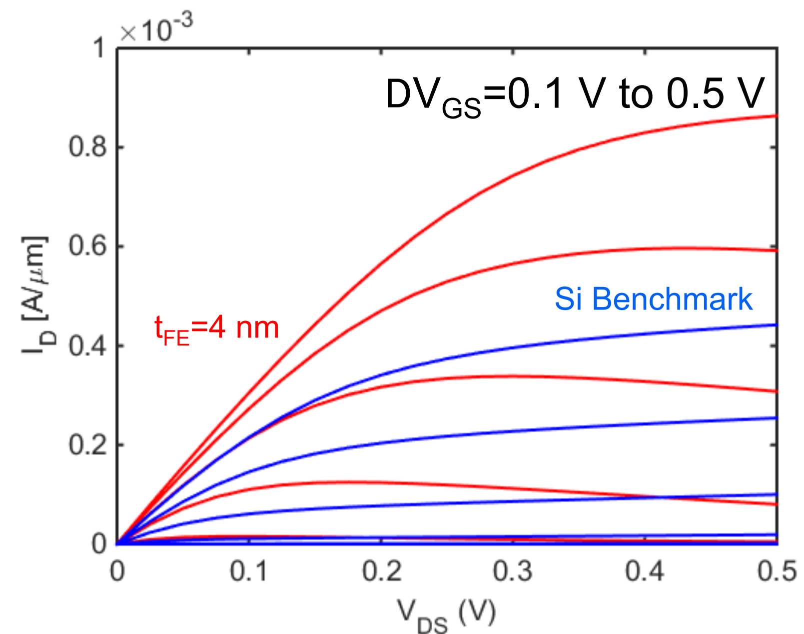
Model device structure



David J. Frank, et al., “The Quantum Metal Ferroelectric Field-Effect Transistor,” *IEEE Trans. Electron Devices*, **61**, *pp. 2145 - 2153*, 2014.

Comparison to benchmark device



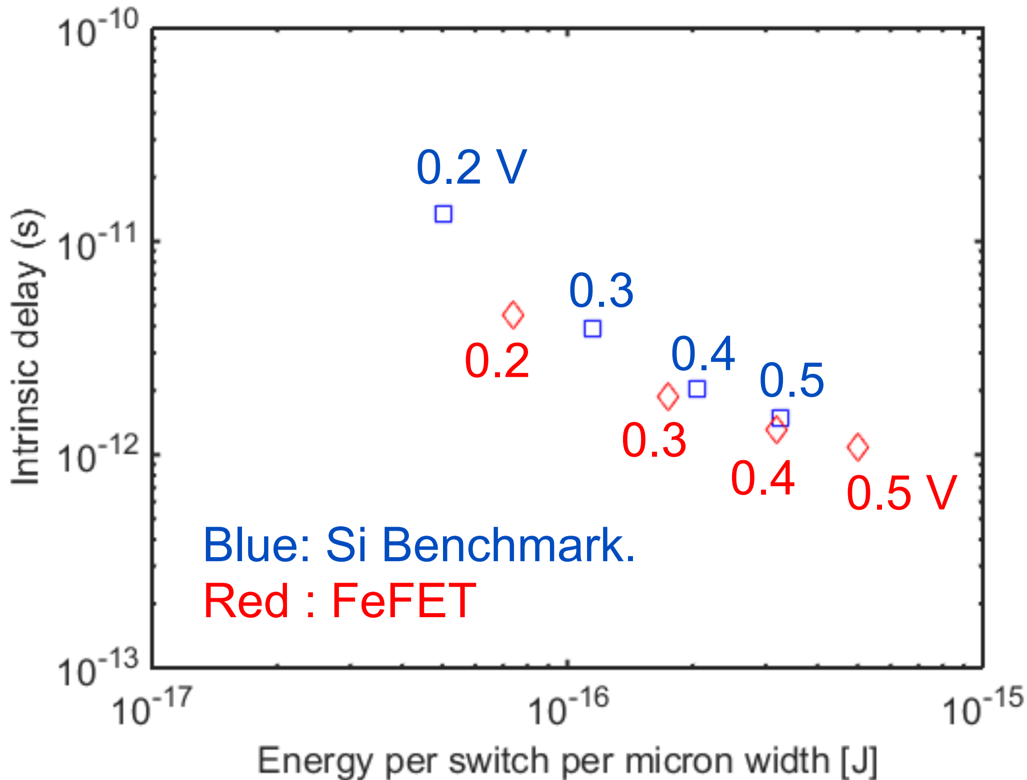


Current x2 for double gate

(Download a FeFET Verilog-A model at needs.nanoHUB.org)

Lundstrom, et al. IEDM 2015

Energy per Switch vs. Intrinsic Device Delay



$$E = CV_{DD}^2 = QV_{DD}$$

$$\tau = \frac{CV_{DD}}{I_{ON}}$$

- Intrinsic speed/energy device advantage limited by increased FeFET gate switching charge
- Significant advantage in interconnect dominated cases

Lundstrom, et al. IEDM 2015

FeFET summary

- Novel device concept with potentially significant impact.
- Encouraging results emerging.
- Significant challenges remain – materials, integration, intrinsic speed, reliability, …

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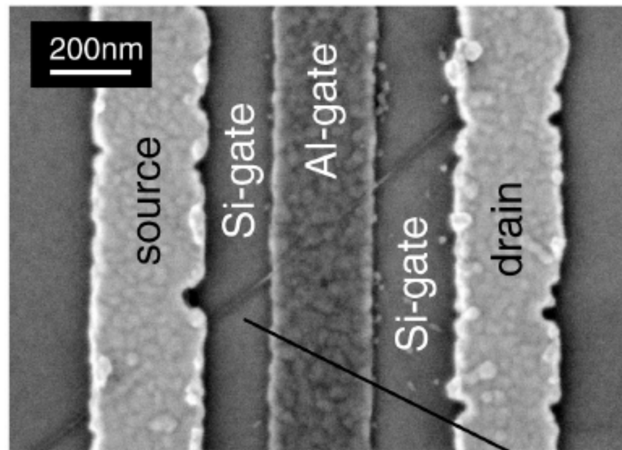
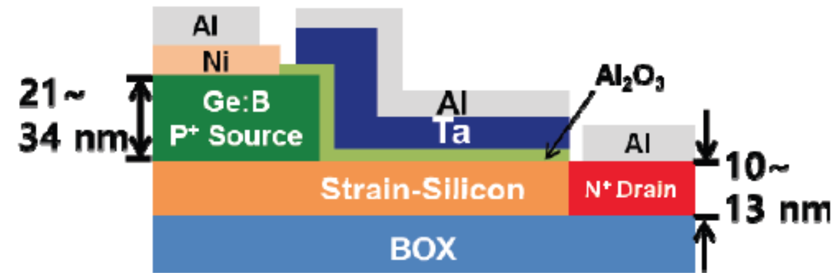
5) Internal gain FETs

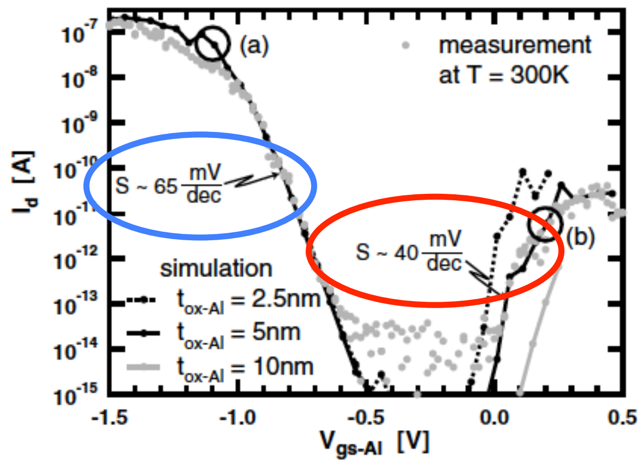
6) TFETs

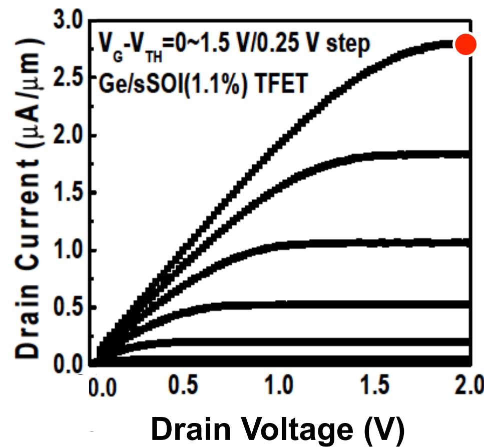
7) 2D Channel materials
8) Summary and outlook

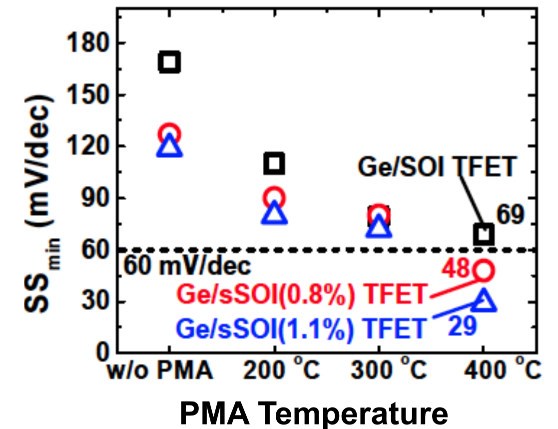
Experimental results







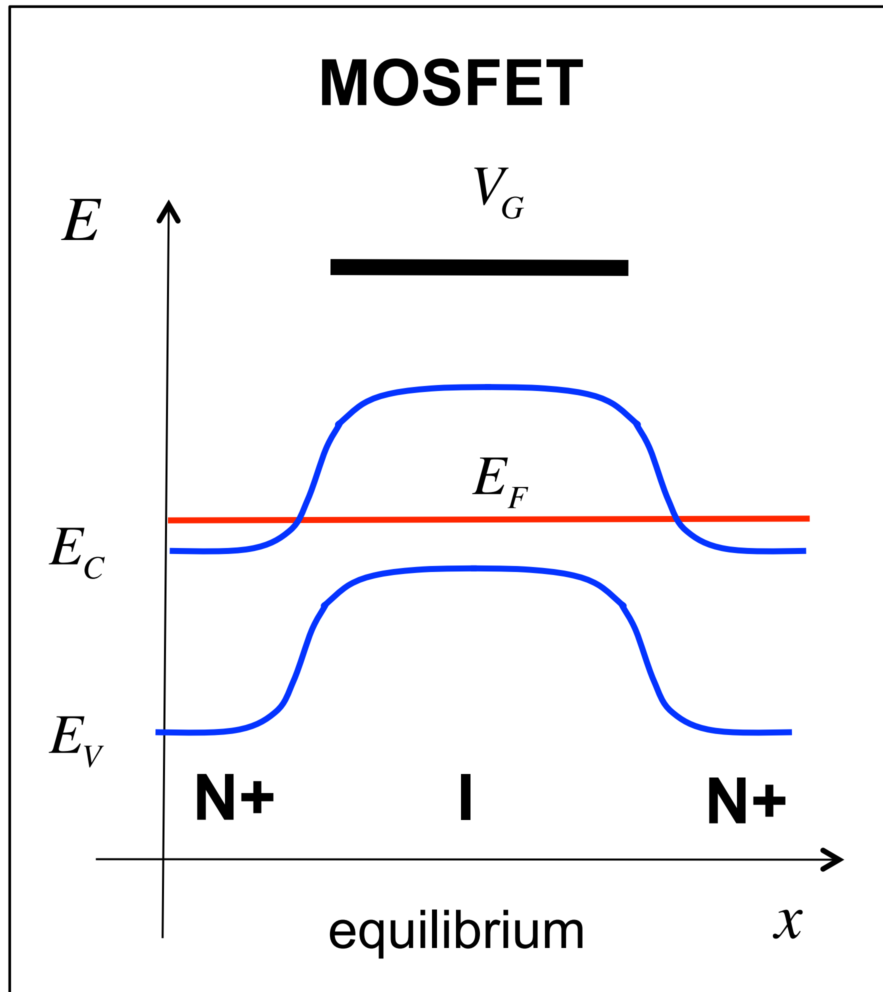


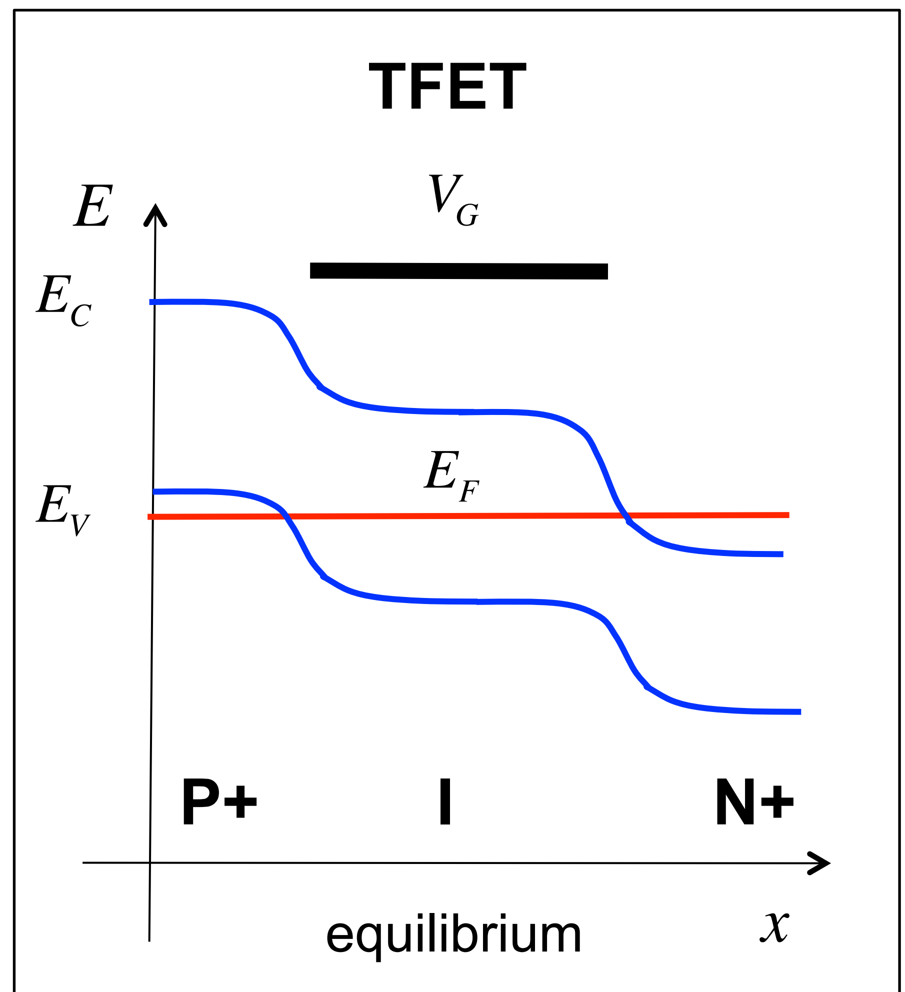


Joerg Appenzeller, *et al.*, *PRL*, **93**, 2004

Minsoo Kim, *et al.*, IEDM, 2014.

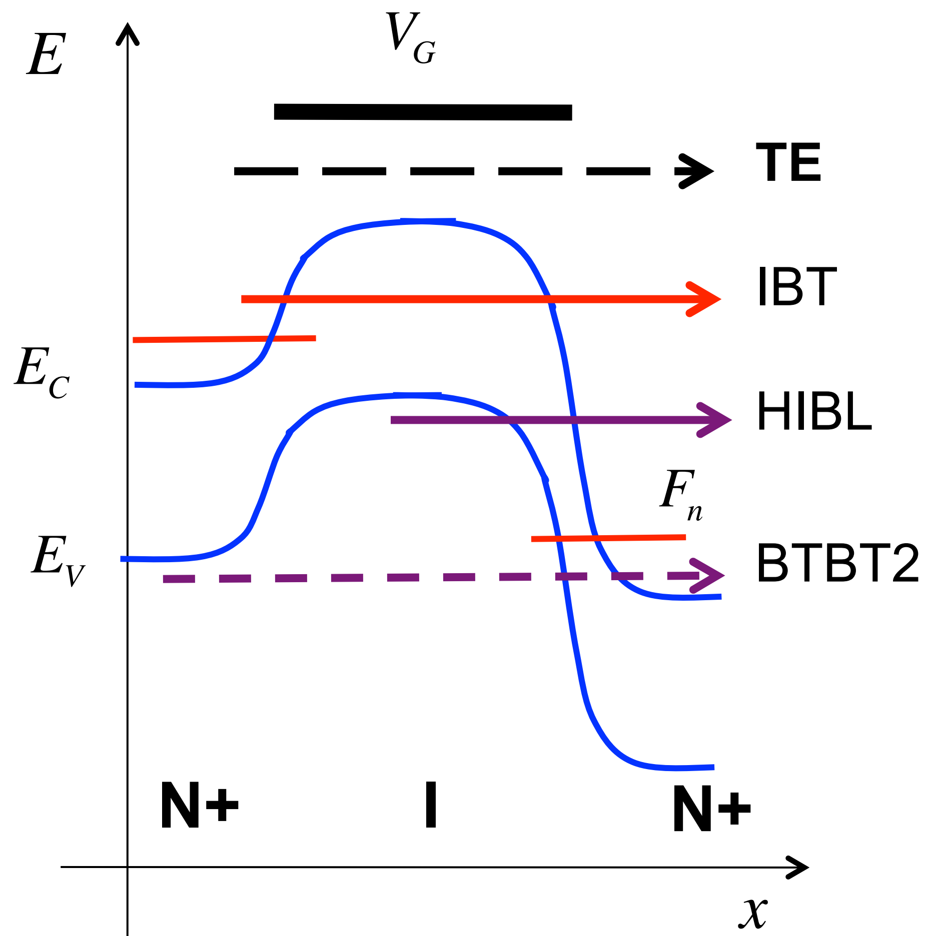
MOSFETs vs. TFETs





Lundstrom, et al. IEDM 2015

OFF-state: MOSFET

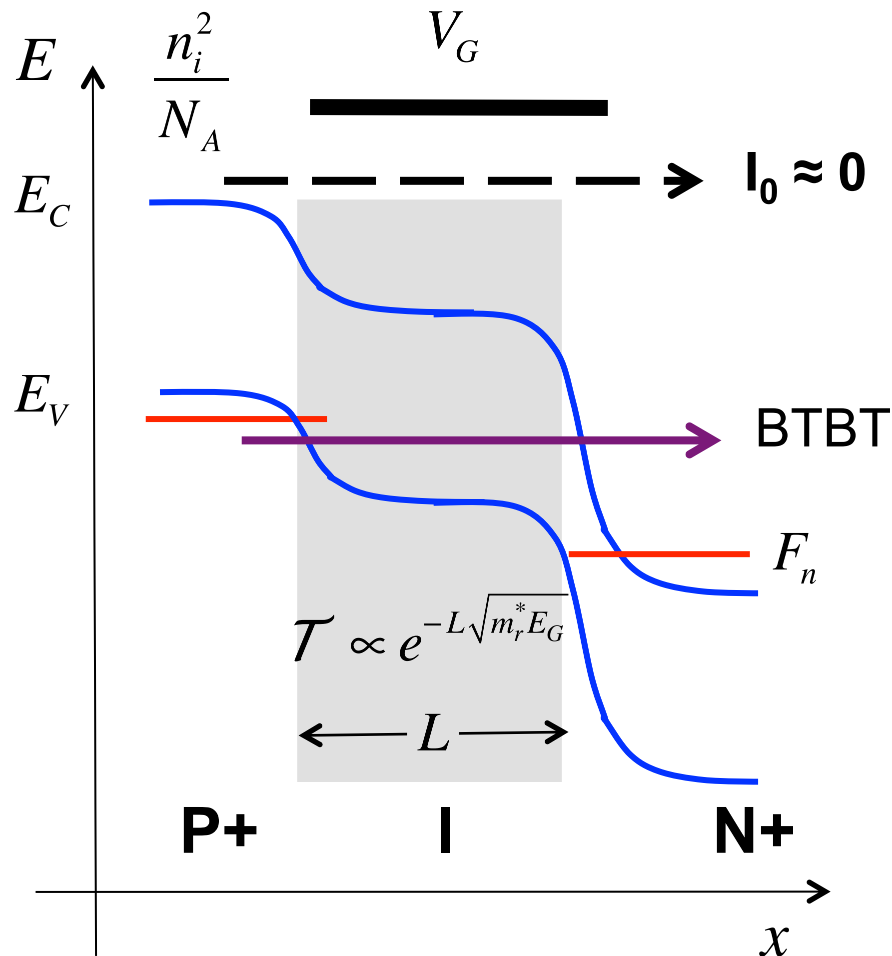


Dominated by thermal emission over the barrier (TE).

Tunnel currents become important below 10 nm.

Tunneling enhanced by small bandgaps and by small eff masses.

OFF-state: TFET



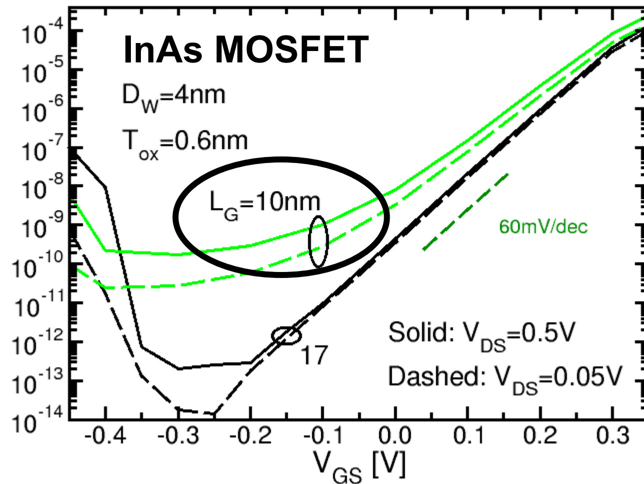
Dominant leakage current for MOSFET is suppressed.

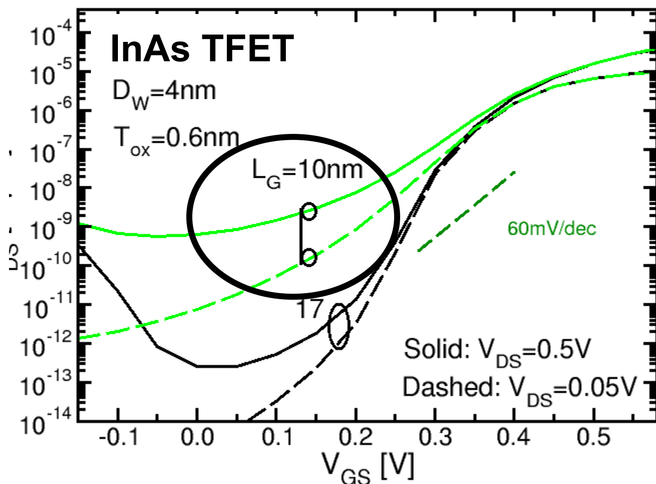
BTBT currents become important below 10 nm.

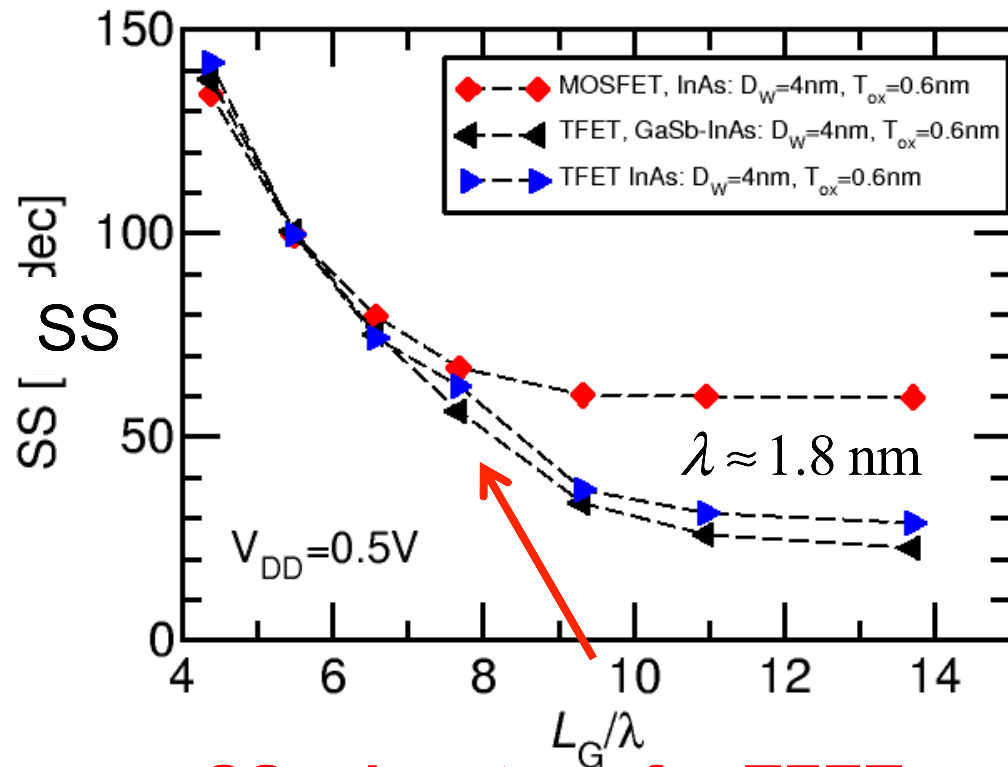
BTBT enhanced by small bandgaps and by small eff masses.

Lundstrom, et al. IEDM 2015

OFF-state calculations



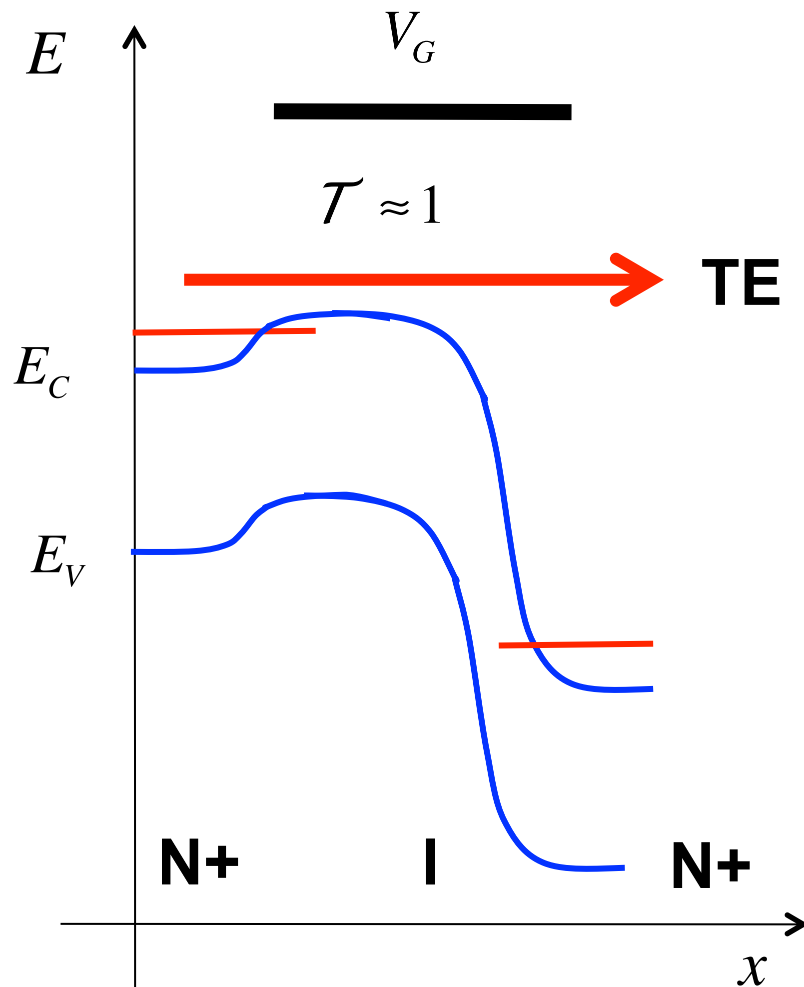




SS advantage for TFET occurs for $L_G > 8\lambda$

David Esseni, et al. *TED*, **62**, 3084, 2015.

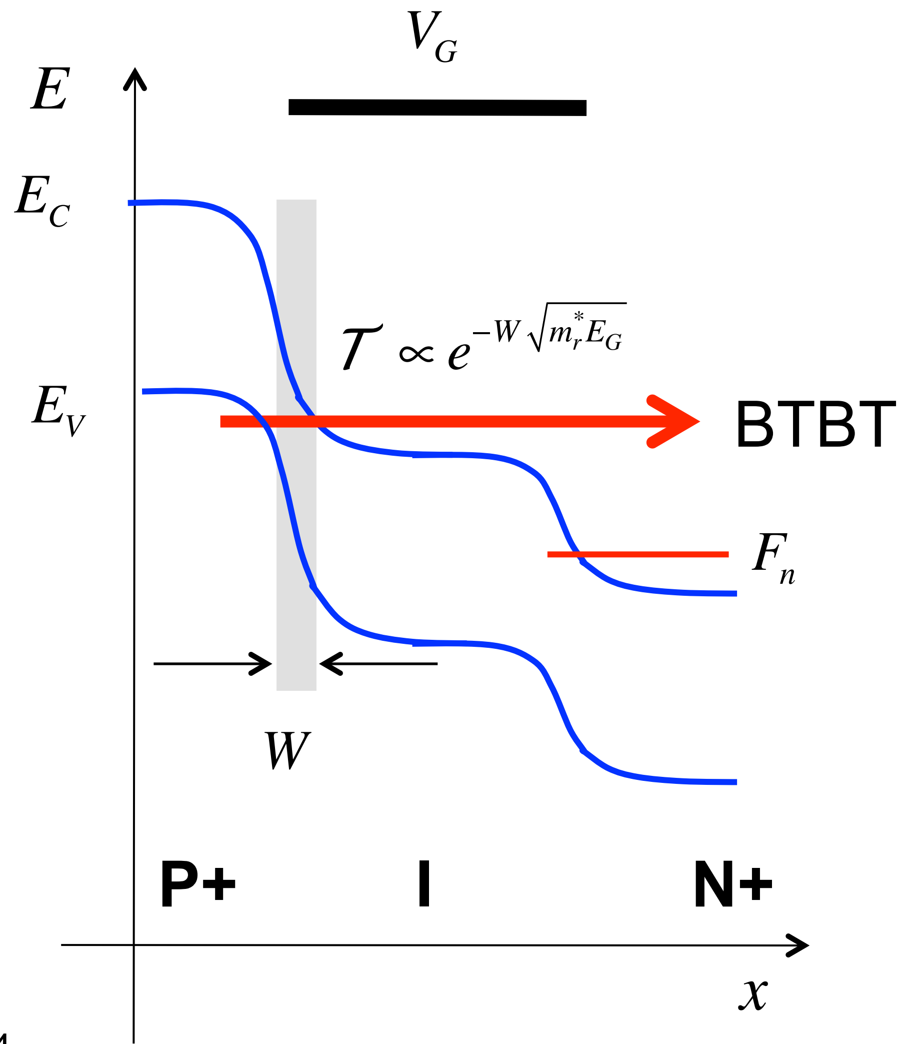
ON-state: MOSFET



ON current is a thermionic emission, over the barrier current.

Channel transmission coefficient is about one.

ON-state: TFET



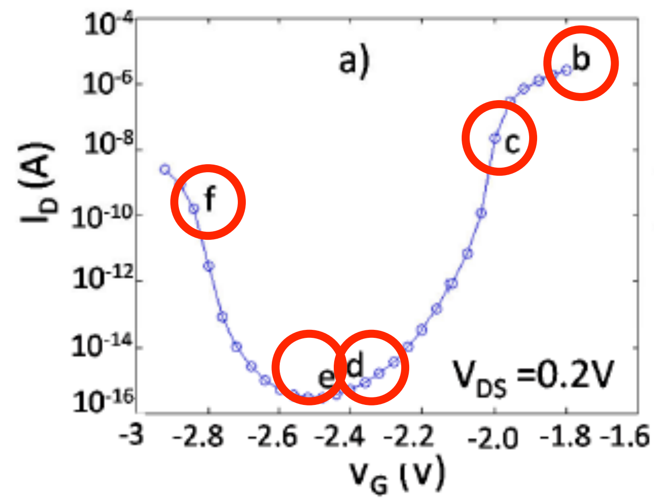
ON current is a BTBT current.

High On-current requires small bandgap, small eff mass, small tunneling width.

Steepness of turn-on controlled by source doping, phonon scattering, band tails, **defects**, …

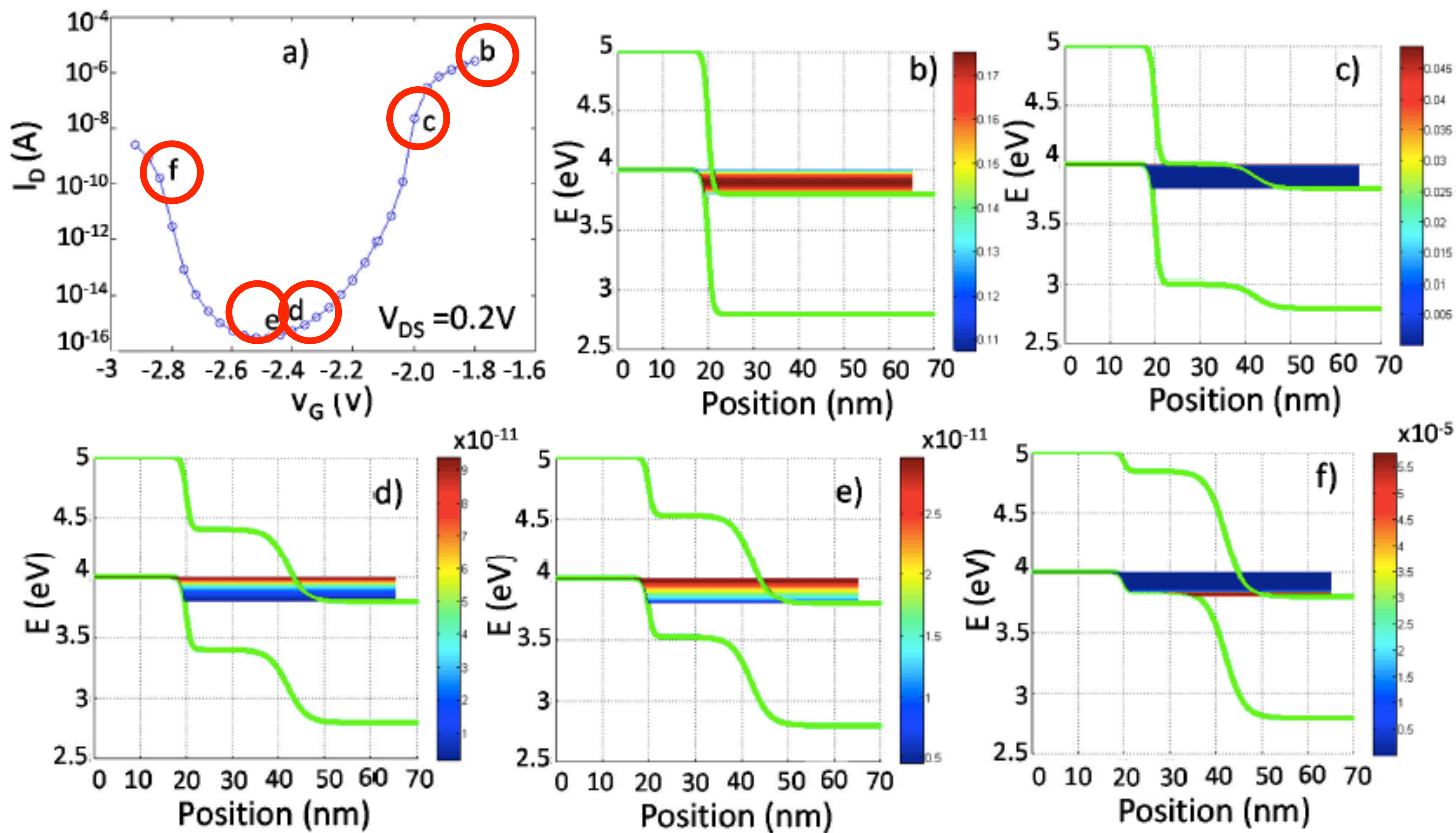
Lundstrom, et al. IEDM 2015

NEGF Simulations



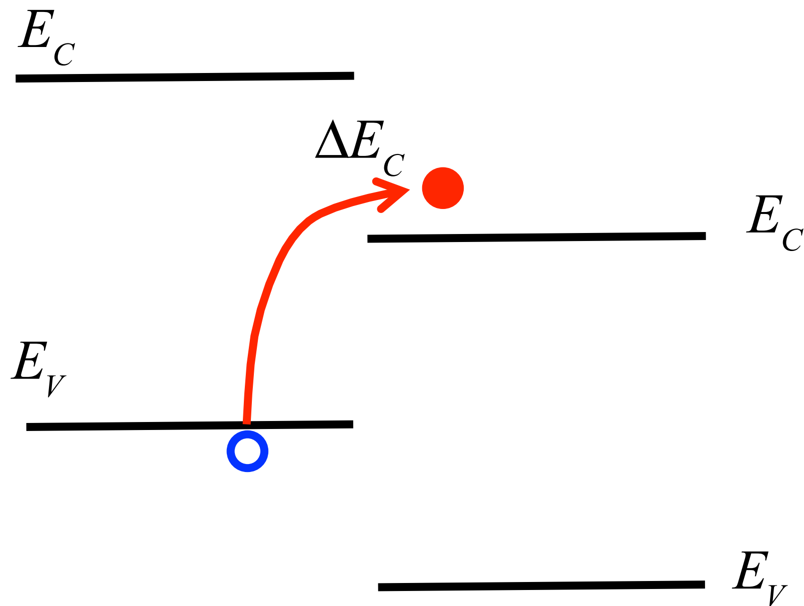
Ramon B. Salazar, *et al.*, 2015.

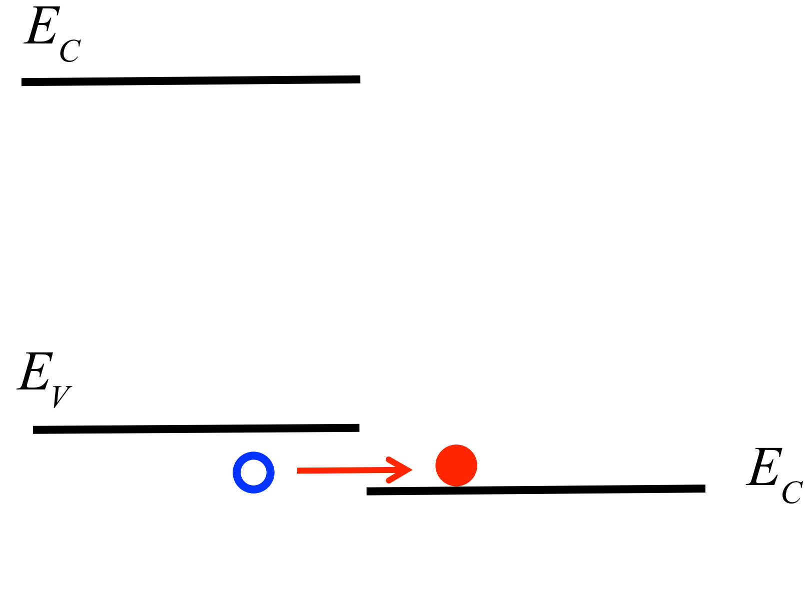
NEGF Simulations



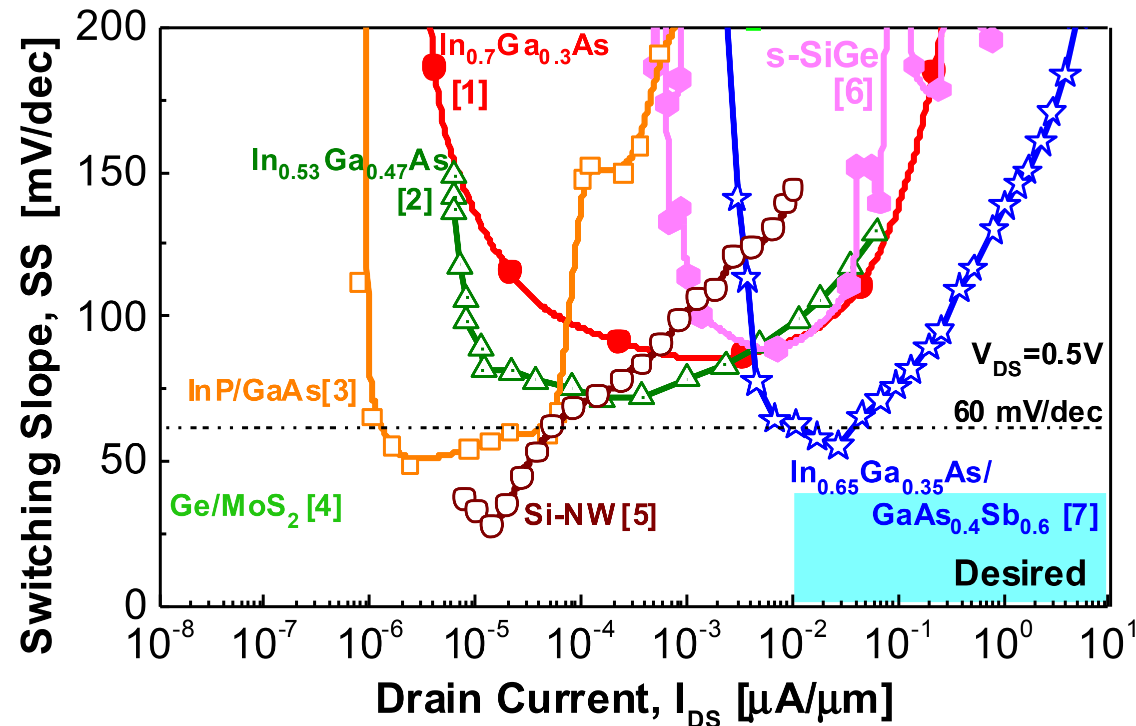
Ramon B. Salazar, *et al.*, 2015.

Staggered and broken bandgaps





Benchmarking



Source: Suman Datta

[1] H. Zhao et al, IEEE EDL, Dec. 2010

[2] M. Noguchi et al., IEDM 2013

[3] B. Ganjipour et al., ACS Nano, Apr. 2012

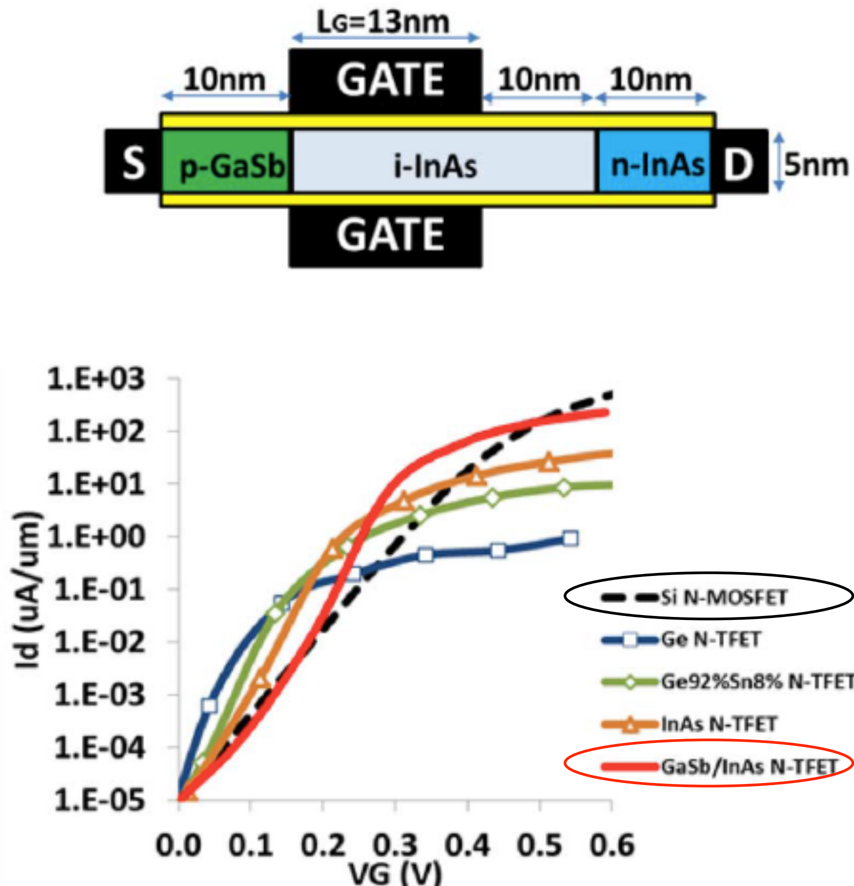
[4] D. Sarkar. et al., Nature Vol. 526, Oct. 2015

[5] L. Knoll et al., IEEE EDL, June 2013

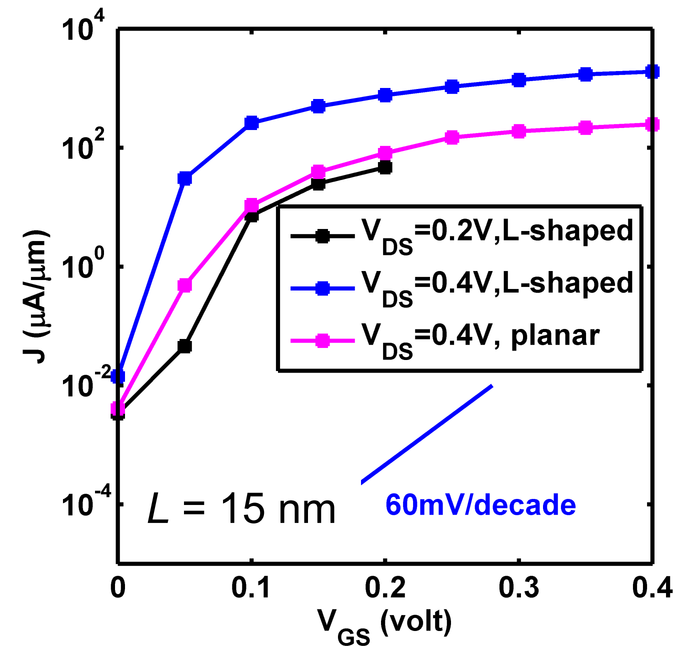
[6] A. Villalon et al., VLSI 2012

[7] R. Pandey et al., VLSI 2015

Projections and possibilities



GaN / InN / GaN TFETs



Uygar E. Avci, et al.,*J. Electron Dev. Soc.*, **3**, 2015.

W. Li, et al., *IEEE Exploratory SS Comp. Dev. and Ckts.*, **1**, 2015.

TFETs: Summary

- Interesting device concept that could out-perform subthreshold Si CMOS in ultra-low power applications.
- Significant and growing body of experimental results – still looking for a breakthrough.
- Serious challenges must be addressed – increasing on-current without increasing leakage, scaling below 10 nm, maintaining SS < 60 to high currents, …

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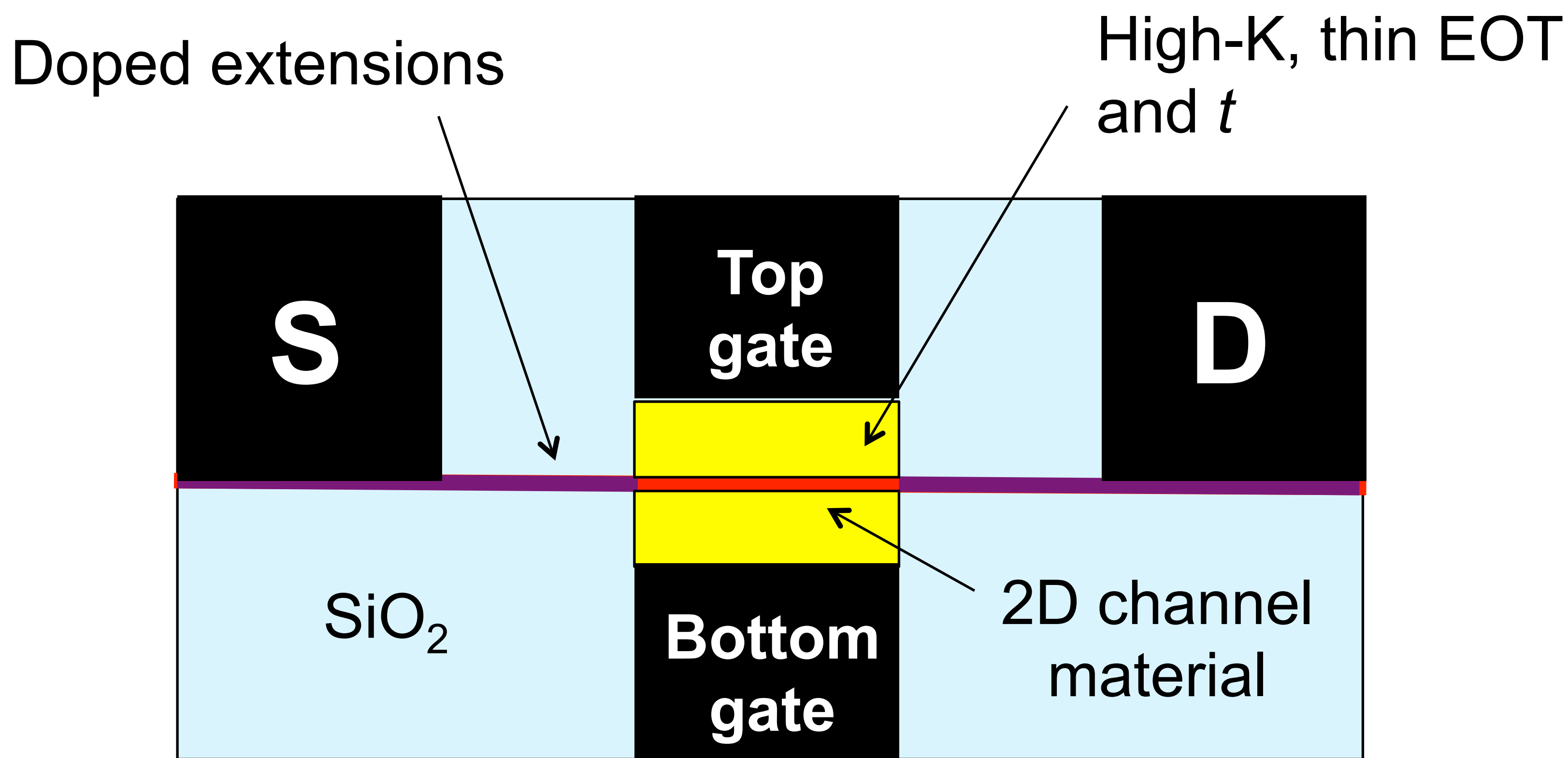
2D semiconductors

Transition metal dichalcogenides (TMD's) such as MoS_2, WSe_2 are interesting because:

- Ultra-thin (atomic scale) channels
- Atomically smooth
- No dangling bonds / stackable HJs
- Uniform thickness
- Mobility maintained for thin channels
- Relatively high effective mass – wide range of bandgaps and masses available.

Ultra-thin body 2D TMD MOSFETs

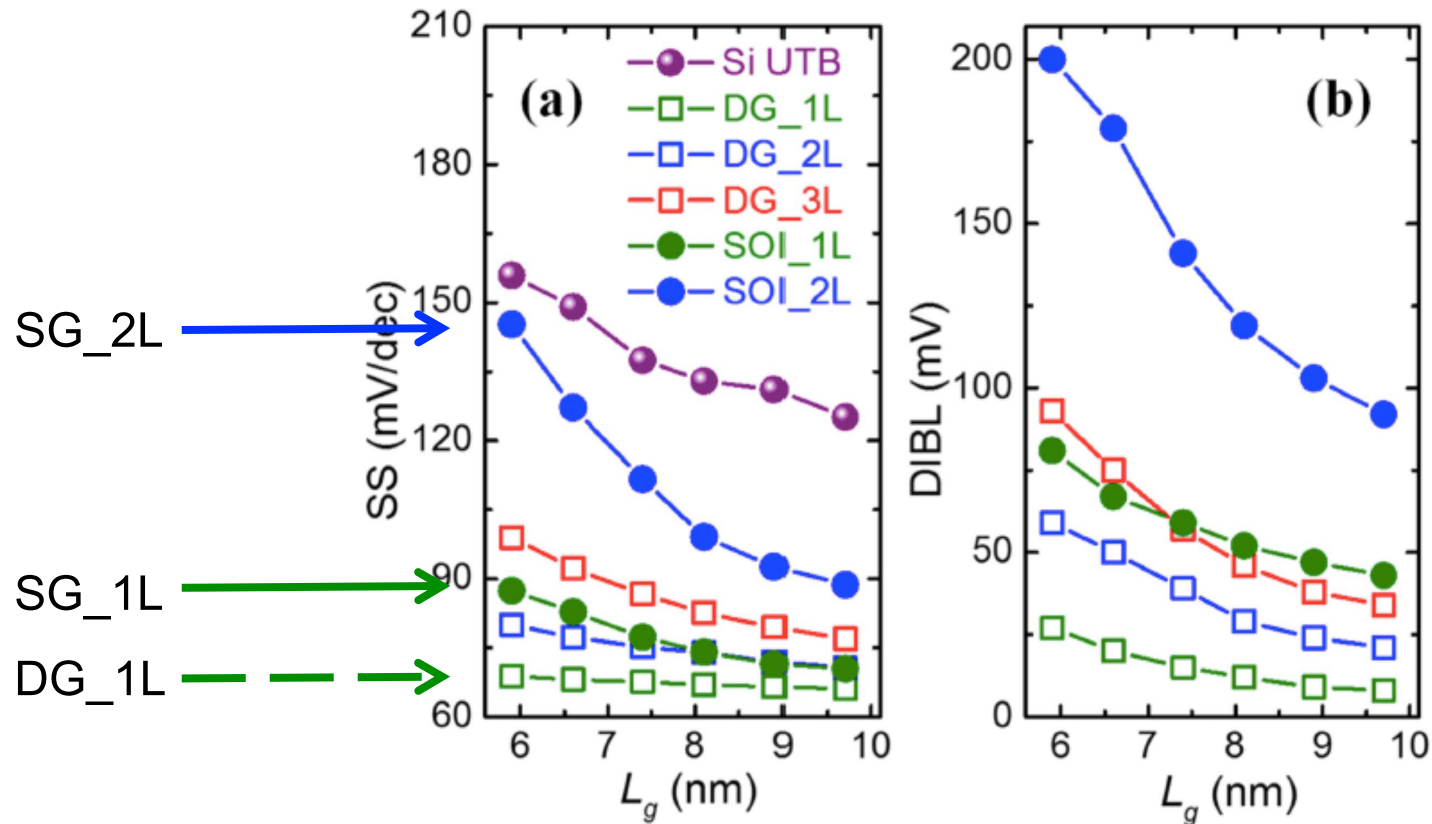


$$L_G > \Lambda = \left(T_{ch} T_{ox} \varepsilon_{ch} / \varepsilon_{ox}\right)^{1/2}$$

$$L_G > \Lambda = T_{ox} + \left(\varepsilon_{ch} / \varepsilon_{ox}\right) T_{ch}$$

D.J. Frank, et al, EDL, 1998.

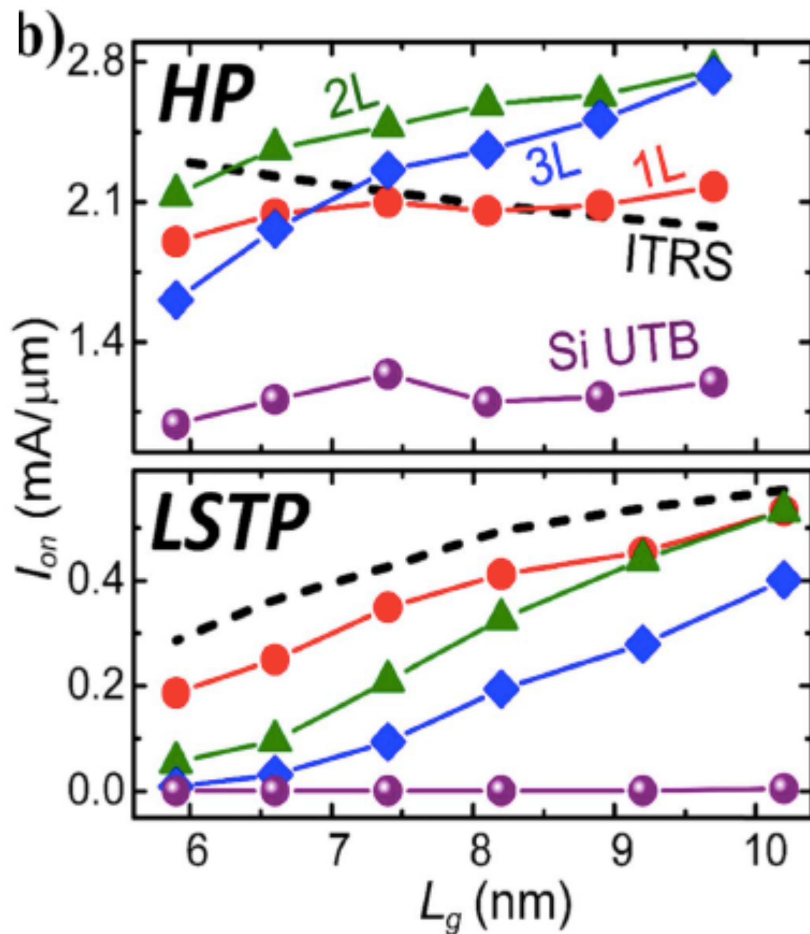
Electrostatics



DG geometry is needed to realize the promise od 2D semiconductors.

Wei Cao, et al., *IEEE TED*, **62**, 2015

On-current



HP targets achievable

LSTP challenging

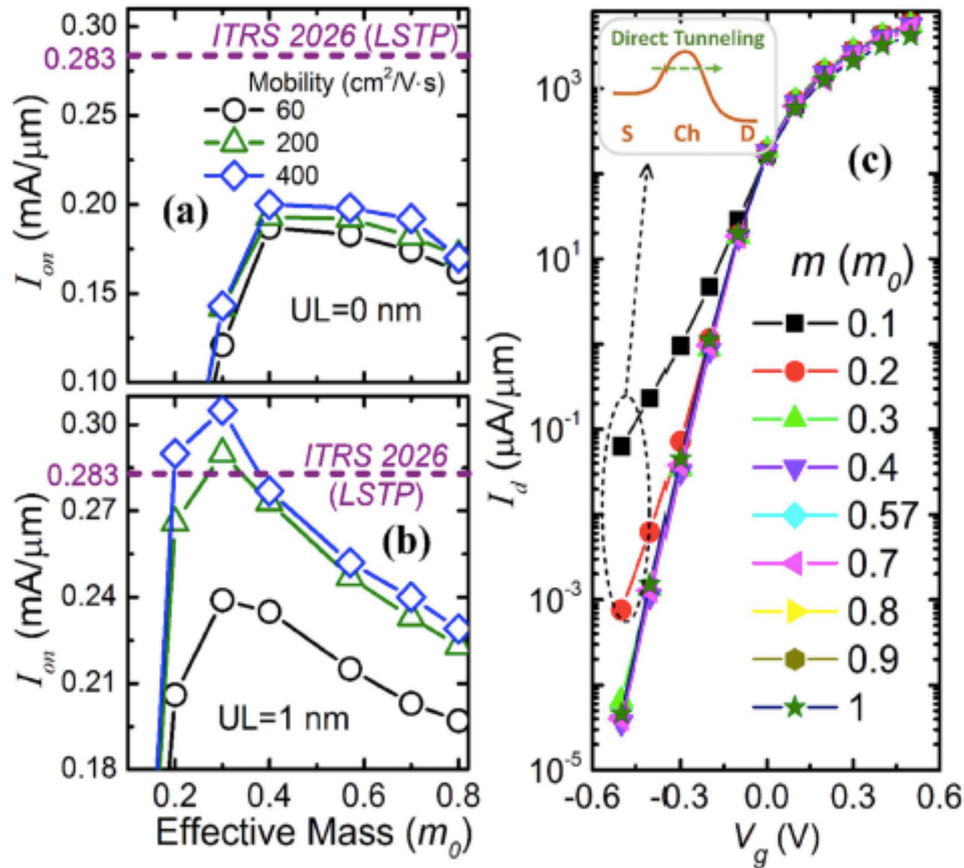
MoS_2 DG with:

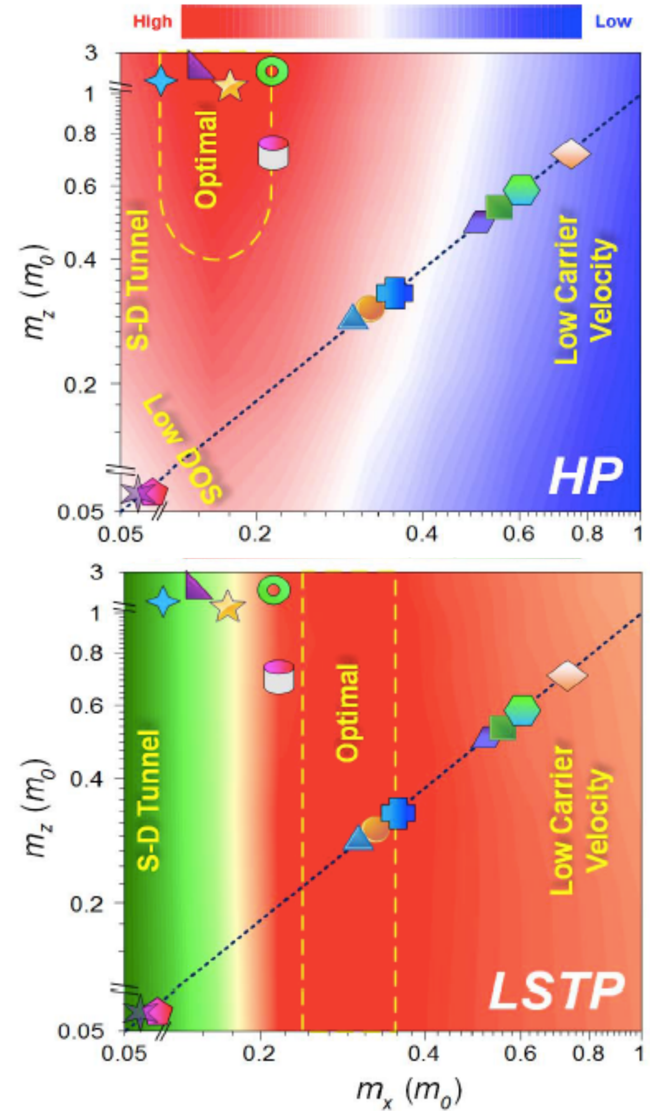
Theoretical, upper limit mobilities

Zero series resistance.

Wei Cao, et al., *IEEE TED*, **62**, 2015

Role of effective mass





Wei Cao, et al., *IEEE TED*, **62**, 2015

2D TMD MOSFETs: Summary

Excellent scaling potential in a DG implementation

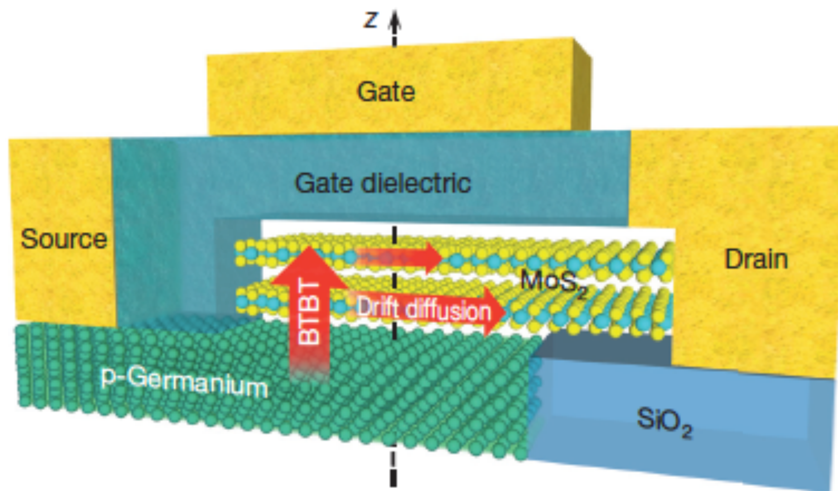
-result of ultra-thin body
-reasonably large effective mass

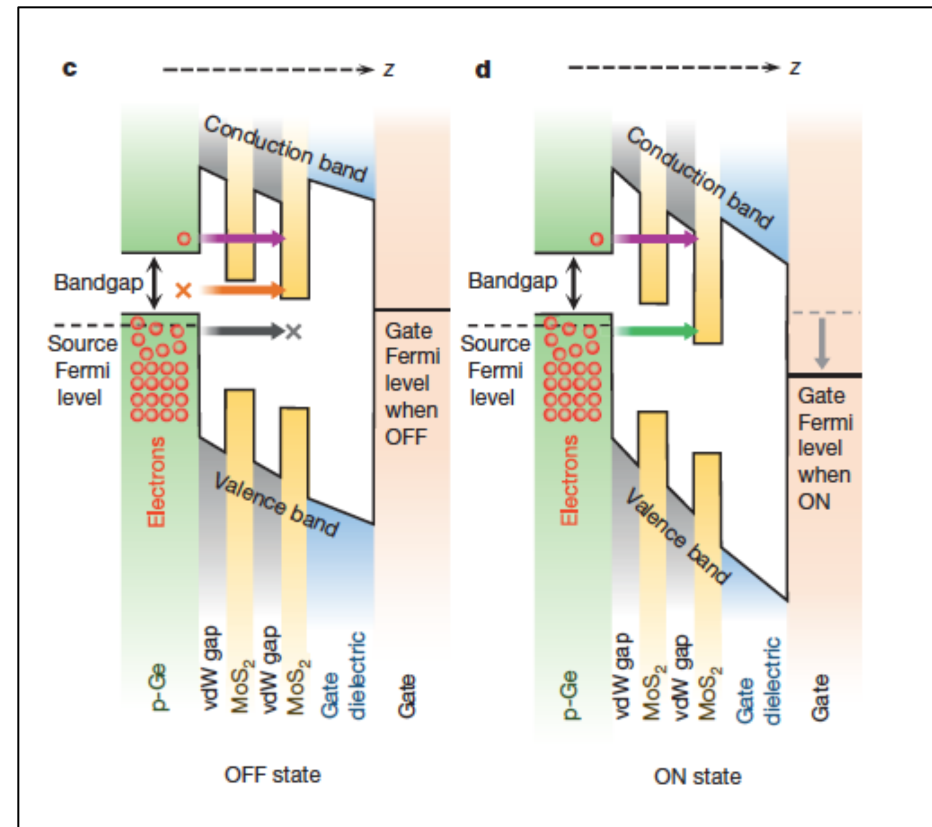
Challenges:

-DG implementation
-doping, contacts, mobility, etc.
-device optimization

2D TMD TFETs?

Vertical TFET

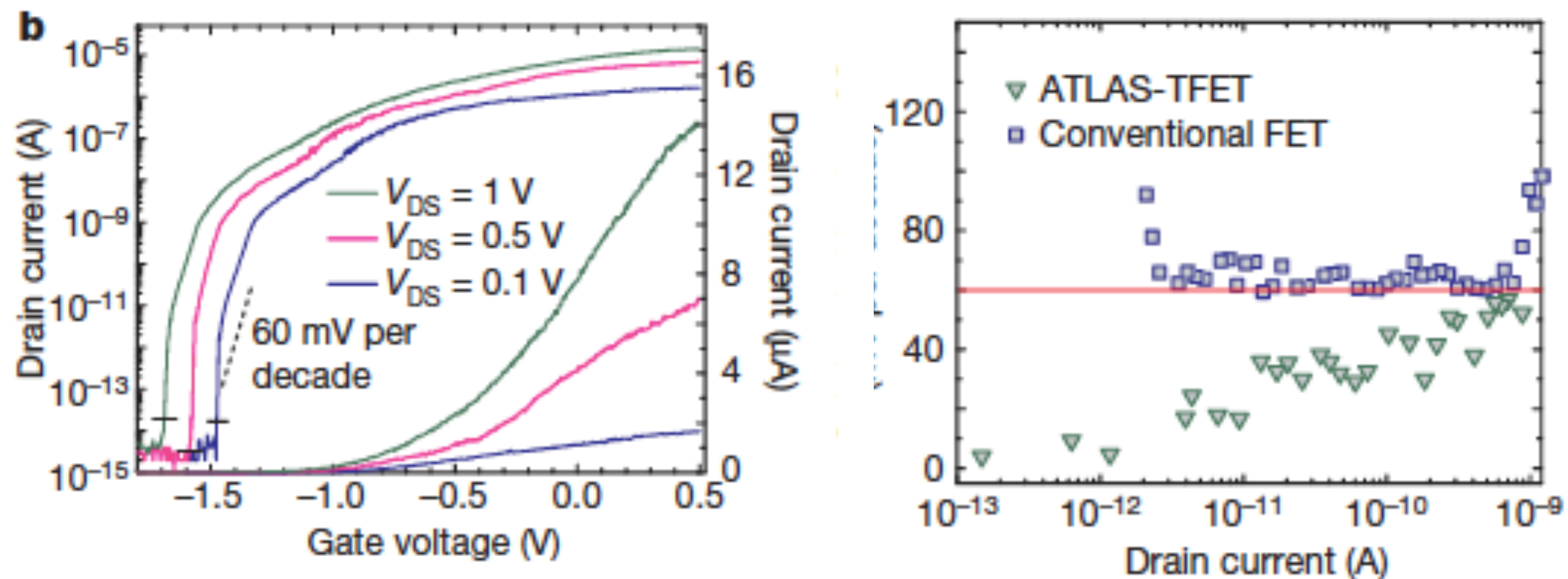




- Small tunneling distance
- Ge-MoS_2 staggered HJ
- Large tunneling area

Deblina Sarkar, et al., *Nature*, **526**, 2015.

2D TMD TFETs?



SS < 60 mV/decade for four decades

Deblina Sarkar, et al., *Nature*, **526**, 2015.

2D Semiconductors: Summary

- Interesting new materials with wide range of properties.
- Potentially suitable for MOSFETs beyond the 5 nm node.
- Especially interesting for TFETs.
- Very new field that could provide solutions beyond the 5 nm node.

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needs.nanohub.org

for more information

See appendix for references, pointers to IEDM papers, and details about MVS modeling (also see paper 28.6).

Summary

All device options face a similar set of challenges:

Cost of fabrication (esp. lithography)
Increasing role of parasitics (gate cap, series *R*)
Variability
Electrostatics
Leakage (esp. tunneling)

Difficulty of achieving desired I_{ON} at desired V_{DD} and I_{OFF}.

No device that is distinctly superior to Si has been identified.

Outlook: 5 nm node

- Si is a possibility, but will it offer enough performance?
- High mobility channels *could* work with careful consideration of trade-offs (***Ge MOSFETs?***)
- FeFETs, TFETs, 2D materials not ready for 5 nm node development, but should be watched.

Outlook: Beyond the 5 nm node

- Probably not Silicon
- Electrostatic control will require NW or ultra-ultra-thin channels in DG architecture.
- Leakage will be dominated by tunneling.
- FeFETs, TFETs, 2D materials could be the answer.

The question

14 nm   10 nm   7 nm   5 nm

CTO to senior device engineer:

> "As we begin work on the 5 nm node. Is their a new device technology we should be seriously looking at?"

Lundstrom, et al. IEDM 2015

Thank you

Bell Labs 1947

"It ain't over till it's over."

-Yogi Berra

Appendices

1) References and relevant 2015 IEDM papers

2) Additional details on MVS-2 modeling

References: High Mobility MOSFETS

S. Lee, et al., “Record Ion (0.50 mA/μm at VDD = 0.5 V and Ioff = 100 nA/μm) 25 nm-Gate-Length ZrO2/InAs/InAlAs MOSFETs,” VLSI Tech. Symp. 2014.

J. Lee, et al., “Novel Intrinsic and Extrinsic Engineering for High-Performance High-Density Self-Aligned InGaAs MOSFETs: Precise Channel Thickness Control and Sub-40-nm Metal Contacts,” IEDM, 2014.

IEDM Papers on High Mobility MOSFETS

2.1 First Demonstration of Ge Nanowire CMOS Circuits: Lowest SS of 64 mV/dec, Highest g_{max} of 1057 µS/µm in Ge nFETs and Highest Maximum Voltage Gain of 54 V/V in Ge CMOS Inverters, H. Wu, W. Wu, M. Si, and P. Ye, Purdue University

2.2 Experimental Study on Carrier Transport Properties in Extremely-Thin Body Ge-on-Insulator (GOI) p-MOSFETs with GOI Thickness Down to 2 nm, X. Yu, J. Kang, M. Takanaka, S. Takagi, The University of Tokyo

2.3 First Monolithic Integration of Ge P-FETs and InAs N-FETs on Silicon Substrate: Sub-120 nm III-V Buffer, Sub-5 nm Ultra-thin Body, Common Raised S/D, and Gate Stack Modules, S. Yadav, K.-H. Tan*, Annie, K.H. Goh*, S. Subramanian, K. Lu Low, N. Chen, B. Jia*, S.-F. Yoon*, G. Liang, X. Gong, Y.-C. Yeo, National University of Singapore, *Nanyang Technological University

2.4 Germanium-based Transistors for Future High Performance and Low Power Logic Applications (Invited), Y.-C. Yeo, X. Gong*, M. van Dal, G. Vellianitis, M. Passlack, Taiwan Semiconductor Manufacturing Company, *National University of Singapore

31.3 Quantum-size Effects in sub 10-nm fin width InGaAs FinFETs, A. Vardi, X. Zhao, and J. del Alamo, Massachusetts Institute of Technology

31.6 An InGaSb p-channel FinFET, W. Lu, J.F. Kim*, J.F. Klem*, S.D. Hawkins*, and J. A. del Alamo, Massachusetts Institute of Technology, *Sandia National Laboratories

References: NW FETS

Aaron Franklin, Mathieu Luisier, Shu-Jen Han, George Tulevski, Chris Breslin, Lynne Gignac, Mark Lundstrom, and Wilfried Haensch, “Sub-10 nm Carbon Nanotube Transistor,” in Nano Letters, Vol. 12, pp. 758-762, 2012.

Mathieu Luisier, Mark Lundstrom, Dimitri A. Antoniadis, and Jeffrey Bokor, “Ultimate device scaling: intrinsic performance comparisons of carbon-based, InGaAs, and Si field-effect transistors for 5 nm gate length,” presented at the International Electron Device Meeting, Dec., 2011.

Bo Yu, Lingquan Wang, Yu Yuan, Peter M. Asbeck, and Yuan Taur, “Scaling of Nanowire Transistors,” *IEEE Trans. Electron Dev*., **55**, pp. 2846-2858, 2008.

Raseong Kim, Uygar E. Avci, and Ian A. Young, “Ge Nanowire nMOSFET Design With Optimum Band Structure for High Ballistic Drive Current,” ” *IEEE Electron Dev. Lett*. **36**, pp. 751-753, 2015.

Peng Zheng, Daniel Connelly, Fei Ding, and Tsu-Jae King Liu, “Simulation-Based Study of the Inserted-Oxide FinFET for Future Low-Power System-on-Chip Applications,” *IEEE Electron Dev. Lett*. **36**, pp. 742-744, 2015.

IEDM Papers on NW FETs

31.1 **Gate-All-Around InGaAs Nanowire FETS with Peak Transconductance of 2200 μS/μm at 50nm Lg using a Replacement Fin RMG Flow**, N. Waldron, *et al.*, imec, *ASM, **Poongsan Inc., ***KU Leuven

31.2 **Self-Aligned, Gate-Last Process for Vertical InAs Nanowire MOSFETs on Si**, M. Berg, *et al.*, Lund University

31.4 **Single Suspended InGaAs Nanowire MOSFETs**, C. Zota, *et al.*, Lund University

34.1 **CMOS Performance Benchmarking of Si, InAs, GaAs, and Ge Nanowire n- and pMOSFETs with L_G=13 nm Based on Atomistic Quantum Transport Simulation Including Strain Effects**, R. Kim, *et al.*, Intel Corp.

34.4 **Process Variation Effect, Metal-Gate Work-Function Fluctuation and Random Dopant Fluctuation of 10-nm Gate-All-Around Silicon Nanowire MOSFET Devices**, H.-T. Chang, *et al.*, National Chiao Tung University

34.6 **InAs-GaSb/Si Heterojunction Tunnel MOSFETs: An Alternative to TFETs as Energy-Efficient Switches?** H. Carrillo-Nuñez, *et al.*, ETH Zürich

References: FE FETS

Sayeef Salahuddin and Supriyo Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices, *Nano Lett*., **8** (2), pp 405–410, 2008.

Asif Islam Khan, Korok Chatterjee, BrianWang, Steven Drapcho, Long You, Claudy Serrao,
Saidur Rahman Bakaul, Ramamoorthy Ramesh, and Sayeef Salahuddin, Negative capacitance in a ferroelectric capacitor,” Nature Materials, **14**, pp. 182–186, 2015.

Kamal Karda, Ankit Jain, Chandra Mouli, and Muhammad Ashraful Alam, “An anti-ferroelectric gated Landau transistor to achieve sub-60 mV/dec switching at low voltage and high speed,” *Appl. Phys. Lett*., **106**, 163501, 2015.

David J. Frank, Paul M. Solomon, Catherine Dubourdieu, Martin M. Frank, Vijay Narayanan,, and Thomas N. Theis, “The Quantum Metal Ferroelectric Field-Effect Transistor,” *IEEE Trans. Electron Dev*., **61**. pp. 2145-2153, 2015.

IEDM Papers on FE FETs

22.5 Prospects for Ferroelectric HfZrOx FETs with Experimentally CET=0.98nm, SS_{for}=42mV/dec, SS_{rev}=28mV/dec, Switch-OFF <0.2V, and Hysteresis-Free Strategies, M.-H. Lee, P.-G. Chen, C. Liu, K.-Y. Chu, C.-C. Cheng, M.-J. Xie, S.-N. Liu, J.-W. Lee, S.-J. Huang, M.-H. Liao*, M. Tang**, K.-S. Li***, and M.-C. Chen***, National Taiwan Normal Univ., *National Taiwan Univ., **PTEK, ***NDL

22.6 Sub-60mV-Swing Negative-Capacitance FinFET without Hysteresis, K. S. Li, P.-G. Chen*, D. Y. Lai, C. H. Lin, C.-C. Cheng**, C. C. Chen, M.-H. Liao*, M. H. Lee**, M. C. Chen, J. M. Sheih, W. K. Yeh, F. L. Yang***, Sayeef Salahuddin^, and C. Hu, National Nano Device Laboratories, *National Taiwan University, **National Taiwan Normal University, ***Academia Sinica, ^University of California, Berkeley

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12.3 Designing Band-to-Band Tunneling Field-Effect Transistors with 2D Semiconductors for Next-Generation Low-Power VLSI, W. Cao, J. Jiang, J. Kang, D. Sarkar, W. Liu, and K. Banerjee, University of California, Santa Barbara

12.5 A Computational Study of van der Waals Tunnel Transistors: Fundamental Aspects and Design Challenges, J. Cao, D. Logoteta, S. Özkaya*, B. Biel**, A. Cresti, M. Pala, and D. Esseni***, IMEP-LAHC, *Aksaray University, **University of Granada, ***DIEG-IUNET

14.3 Understanding of BTI for Tunnel FETs, W. Mizubayashi, T. Mori, K. Fukuda, Y. Ishikawa, Y. Morita, S. Migita, H. Ota, Y. Liu, S. O'uchi, J. Tsukada, H. Yamauchi, T. Matsukawa, M. Masahara, and K. Endo, AIST

22.1 Tunneling Field Effect Transistors: Device and Circuit Considerations for Energy Efficient Logic Opportunities (Invited), I. Young, U. Avci, and D. Morris, Intel Corporation

22.2 First Foundry Platform of Complementary Tunnel-FETs in CMOS Baseline Technology for Ultralow-Power IoT Applications: Manufacturability, Variability and Technology Roadmap, Q. Huang, R. Jia, C. Chen, H. Zhu, L. Guo, J. Wang, J. Wang, C. Wu, R. Wang, W. Bu*, J. Kang*, W. Wang*, H. Wu*, S.-W. Lee*, Y. Wang, and R. Huang, Peking University, *Semiconductor Manufacturing International Corporation

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27.3 2D Layered Materials: From Materials Properties to Device Applications (Invited), P. Zhao, T. Roy, M. Tosun, H. Fang, S. Desai, A. Sachid, M. Amani, C. Hu, and A. Javey, UC Berkeley

27.4 High-frequency Scaled MoS_2 Transistors (Invited), D. Krasnozhon, S. Dutt, C. Nyffeler, Y. Leblebici, and A. Kis, EPFL

27.5 Bandgap Engineering in 2D Layered Materials (Invited), T. Chu, and Z. Chen, Purdue University

27.6 van der Waals Junctions of Layered 2D Materials for Functional Devices (Invited), T. Machida, R. Moriya, Y. Sata, T.

27.7 Roll-to-Roll Synthesis and Patterning of Graphene and 2D Materials (Invited), T. Choi, S.J. Kim, S. Park, T. Hwang*, Y. Jeon*, and B.H. Hong, Seoul National University, *Samsung-Electro Mechanics

32.3 Enhancement-Mode Single-layer CVD MoS_2 FET Technology for Digital Electronics, L. Yu, D. El-Damak, S. Ha, X. Ling, Y. Lin, A. Zubair, Y.-H. Lee*, J. Kong, A. Chandrakasan, T. Palacios, Massachusetts Institute of Technology, *National Tsing-Hua University

32.1 High-Frequency Prospects of 2D Nanomaterials for Flexible Nanoelectronics from Baseband to sub-THz Devices, S. Park, W. Zhu, H.-Y. Chang, M.N. Yogeesh, R. Ghosh, S. Banerjee, and D. Akinwande, The University of Texas at Austin

Appendix: Some details of MVS-2 Modeling

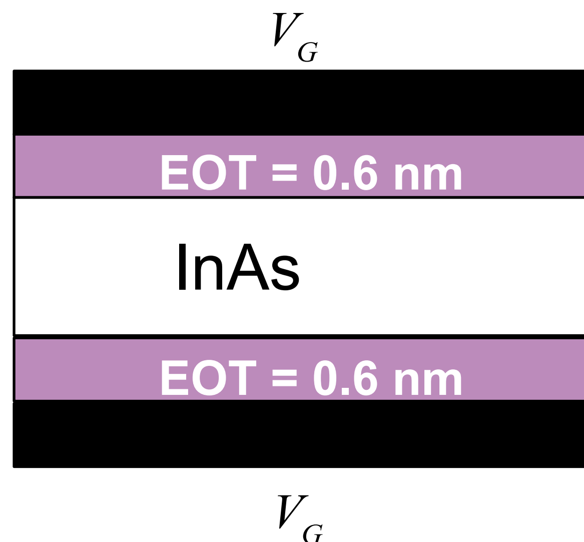
1) Comparison with Nextnano CV characteritics

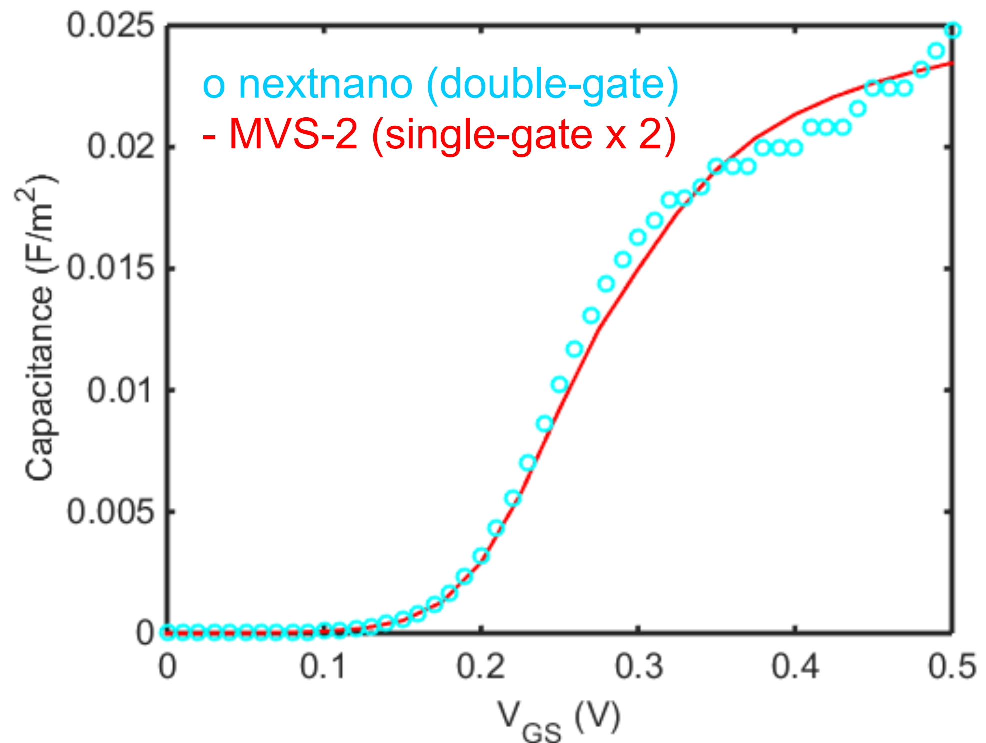
2) Injection velocity: Si vs. III-V

3) VS Capacitance and Charge - Effect of V_{DS}

4) MVS-2 Parameters in III-V simulations

III-V Channel C-V Comparison of MVS-2 with Nextnano





EOT=0.6 nm
m*=0.035
alpha=1.6 (non-parabolic energy factor)
n_0=1.00 (since Nextnano is 1-D)

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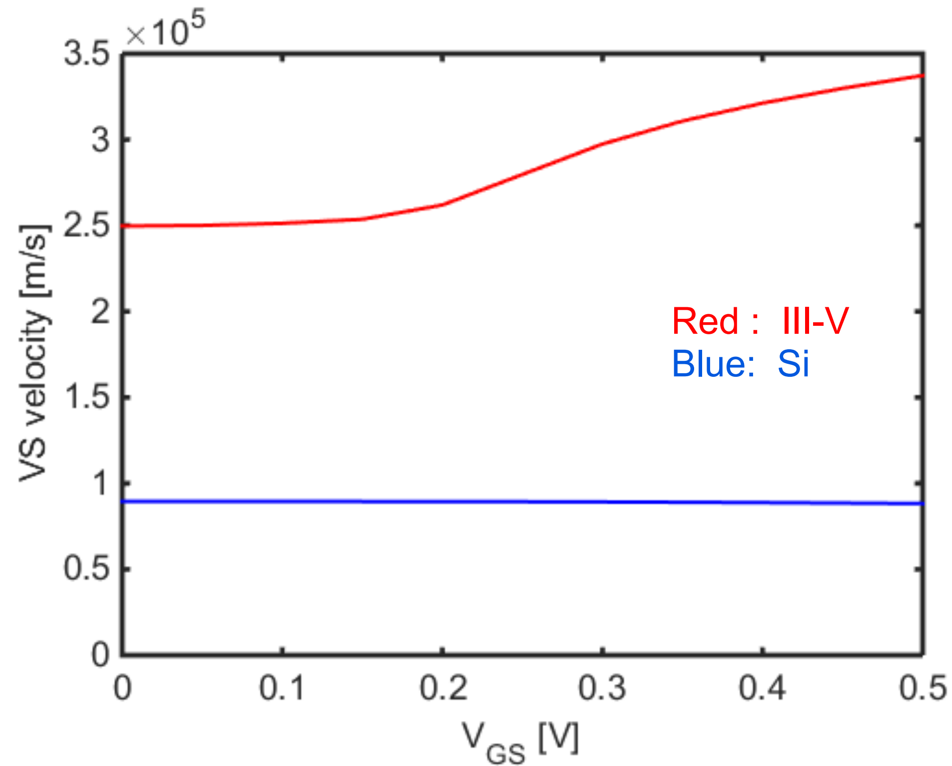
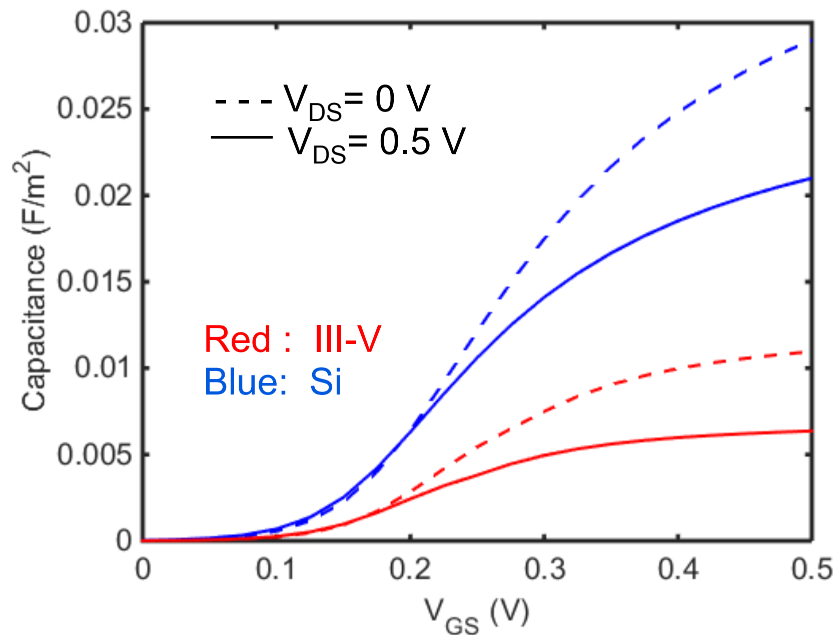
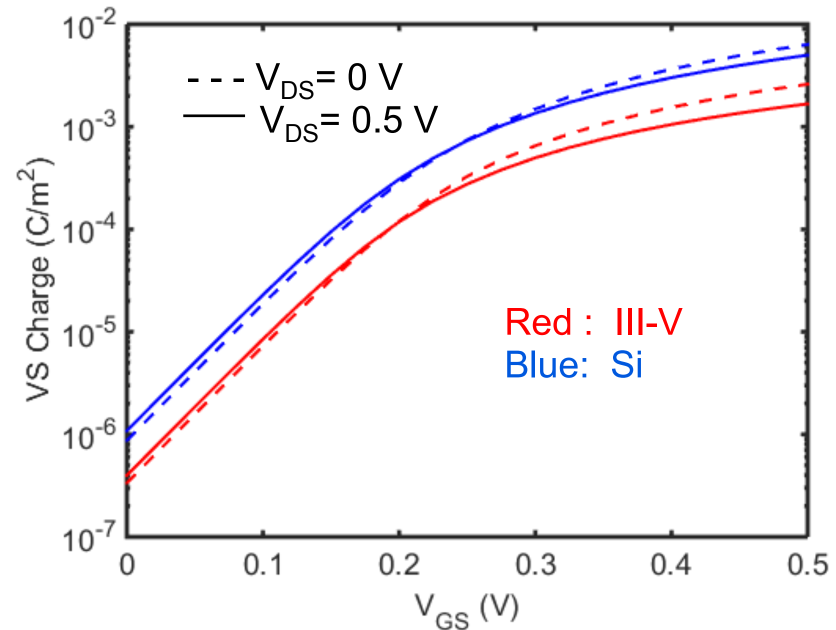
Injection Velocity – III-V vs. Si



- III-V has much higher injection velocity which also increases with degeneracy

VS Capacitance and Charge - Effect of V_{DS}





- III-V channel requires significantly lower charge for given I_{on}, I_{off}
- But, III-V charge decreases faster with increase of V_{DS} (36% vs. 21%)

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MVS-2 Parameters in III-V simulations

```
Lsd = 1e-9;        % Access-region length [m]
W=1e-6;            % Transistor width [m]
Lgdr=20e-9;        % Physical gate length [m]. This is the designed gate length for litho printing.
dLg = 0;           % Overlap length including both source and drain sides [m].
tins=0.6e-9;       % Dielectric equivalent thickness [m] (dielectric between QW and gate metal)
epins=3.9*8.85e-12;     % Effective dielectric constant of insulator [F/m]
Cins=epins/tins     % Gate-channel capacitance [F/m^2]

Vt0 = 0.582;              % LP Threshold voltage [V]
Vt0 = 0.358;              % HP Threshold voltage [V]
delta=55e-3;              % Drain induced barrier lowering (DIBL) [V/V]
n0=1.25;                  % Subthreshold swing factor [unit-less] {typically between 1.0 and 2.0}

Rc0=100 ;                 % Access region resistance for s terminal [Ohms-micron]
Qacc=qe*2.5e17;           % Access region charge [C/m^2]

meff = 0.035*m0;          % Effective mass of carriers [kg]
np_mass = 10;             % Non-parabolicity mass increase [1/eV] {m=meff*(1+np_mass*E)}
ksee = 0.1;               % Parameter for VS velocity
mu_eff=1 ;                % Long-channel effective mobility [m^2/Vs]
mu_eff_acc=mu_eff;        % Effective mobility in access region [m^2/Vs]

B=6.8e-9;                 % Stern QM correction numerator (fitted to C-V data)
dqm0=5.0e-9;              % Distance of centroid [m] (fitted to C-V data)
nq=1/3;                   % QM corr. exponent. Theoretical = 1/3.{should not be fitted. and moved to the list of constants ?}
QB=(B/dqm0)^(1/nq);       % Stern QM correction denominator term based on cetroid [C/m^2]
eps=13.6*8.5e-12;         % Permittivity of semiconductor [F/m]
Cstern=eps/dqm0;

theta1 = 0.8;             % Fitting parameter in Vdsat_acc ; NOT USED
theta2 = 2.5;             % Fitting parameter for blending Lcrit_lin and _sat
beta = 1.55;              % Fitting parameter to govern the shoulder shape of Fsat (typ. 1.5)
%beta_acc = 0.285e-3;
beta_acc = beta;
beta_crit = beta;
```

MVS-2 Parameters in III-V simulations

```
W=1e-6;                  % *** Width [m]
Lgdr= 20e-9;                % *** Gate length [m]
dLg= 0e-9;                 % *** dLg=L_g-L_c *1e-7 {default 0.3xLg_no}
EOT=0.6e-9;
Cox=3.9*8.85e-12/EOT;

Rs0  = 100e-6;                  % *** Source accessresistance [Ohm-micron]
Rd0  = Rs0;                    % *** Drain access resistance

delta = 50e-3;                 % *** DIBL [V/V]
n0    = 1.25;                  % *** Intrinsic swing n-factor at Tjun
nd    = 0;                     % *** Punch-through [1/V]

theta = 2.5 ;                  % Saturation voltage for critical length in units of phit.
beta   = 1.5;                  % Saturation parameter for the channel
beta_c = beta;                  % Saturation parameter for critical length. Right, now both beta and beta_c are same. Can be changed lat
energy_diff_volt   = -0.419;     % *** LP Threshold voltage [V]
energy_diff_volt   = -0.24;     % *** HP Threshold voltage [V]

mt = 0.19*m0;                  % *** Transverse effective mass in Si [Kg]
ml = 0.89*m0;                  % *** Longitudinal effective mass in Si [Kg]
mu_eff = 200e-4;                % *** Long-channel effective mobility [m^2/Vs]
ksee = 0.05;                   % *** Ratio of critical length to the channel length
B = 2.0e-10;                   % *** Stern QM correction numerator (fitted to C-V data)
nq = 1/3;                      % *** QM corr. exponent. Theoretical = 1/3.{should not be fitted. and moved to the list of constants ?}
dqm0 = 3e-9;                   % *** Distance of centroid [m] (fitted to C-V data)
QB = (B./dqm0)^(1/nq);          % *** Stern QM correction denominator term based on cetroid [C/m^2]
nu = 0.7;
```