Front End of Line Integration Issues and Opportunities Beyond 7nm Node

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Outline

- Introduction - 10 mins

- FEOL Integration Challenges for 5nm Node FinFET - 15 mins
  - General Performance Requirements
  - Device Menu
  - FP scaling
  - CGP scaling
  - MOL scaling

- Alternate Channel Materials - 15 mins
  - Strained SiGe
  - Strained Si
  - III V

- FEOL Integration Issues and Opportunities for Alternate Device Options - 15 mins
  - Horizontal Nano Wires
  - Vertical Nanowires
  - 3D Integration

- Conclusions – 5min
Good References

Scaled FinFETs
Holistic Technology Optimization and Key Enablers for 7nm Mobile SoC
S. C. Song, et. al., 2015 VLSI Symposium – Air Spacer, Wrap Around Contact, Fin Depopulation

Vertical FETs
Vertical Device Architecture for 5nm and Beyond: Device & Circuit Implications, A. V.-Y. Thean, D. Yakimets, et. al. imec, Belgium, 2015 VLSI Symposium

Vertical GAAFETs for the ultimate CMOS scaling

3D Integration

Micron and Samsung Memory Applications

Power benefit study for ultra-high density transistor-level monolithic 3D Ics
Young-Joon Lee, Daniel Limbrick, Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA
Proceedings of the 50th Annual Design Automation Conference Article No. 104

TFETs
III-V and Ge/strained SOI Tunneling FET Technologies for Low Power LSIs, S. Takagi, 2015 VLSI Symposium


Ge FET
Ge n-channel FinFET with optimized gate stack and contacts
H. van Dal  TSMC - IEDM 2014 – pragmatic description if issues and opportunities
Preliminaries

- Technology provides value
- Lower Cost
- Higher performance
- Any architecture must be yieldable at target ground rules
- Any new materials must be low defectivity $< 1000 \text{cm}^{-3}$
- Any new option needs to be scalable – multi generation solution
- Anything new requires very long lead time (high k, FinFET)
- Collaboration between design, technology, academia is key to success
Introduction
More aggressive nodes have tighter Gate Pitch – CPP and this results in smaller contact area ( higher Rext ), increased parasitic capacitance and less room for gate and spacer. ~ 2004 Gate Length scaling slowed.
Density Scaling

14nm (20nm)

$\text{Gate-contact spacing} \quad \text{22nm}$

$\text{CGP}=80\text{-}90\text{nm}$

10nm (14nm)

$\text{Gate-contact spacing} \quad \text{12nm}$

$\text{CGP}=60\text{-}67\text{nm}$

Aggressive pitch scaling requires $L_{\text{gate}}$, Spacer and Contact scaling.

Area shrink and performance improvement are both needed.
## Possible Technology Roadmap

<table>
<thead>
<tr>
<th>Node</th>
<th>Gate Pitch (nm)</th>
<th>Nominal L (nm)</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>170-180</td>
<td>40-45</td>
<td>2008</td>
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<td>32</td>
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_Gate, Contact and Spacer_ must get smaller to fit the pitch. Need to improve electrostatics and _resistance._
Approaches to Conventional Device Scaling L gate

- \[ \Delta V_t = \frac{2A}{W_{dm}} \left[ \sqrt{\psi_{bi}(\psi_{bi} + V_{ds})} - a(2\psi_B) \right] e^{-\frac{nL}{2}} \]
  
  [Taur and Ning, “Fundamentals of Modern VLSI, 2nd Ed. 2009]

- Decrease gate dielectric thickness, shallower extension junction depth and increase substrate doping.

- Issues:
  - Scalability of gate dielectric and junctions.
  - GIDL
  - RDF
  - Junction Leakage
  - Challenge in getting to low \( V_T \)
**Fully Depleted Device Fundamentals**

- **No Channel Doping → Better SRAMs**
  - Less doping-driven threshold fluctuation
  - Lower supply voltage ($V_{\text{min}}$) – by about 150mV
  - Lower voltages means lower power – up to 40%

- **Much better Electrostatics**
  - More abrupt junctions, and scaled dielectrics help
  - How much can we scale $T_{\text{Si}}$?

Si can be thicker for same DIBL or better DIBL for same thickness of Si
FEOL Integration
Challenges for 5nm Node
FinFET
SCE Improvement at Thinner Film

DIBL, Swing and Ieff improve with thinner channel.

Scaling

For a given DIBL – FinFET can have thicker channel
Process Flow

- Active (Fin) Formation
- Dummy Gate Deposition & RIE
- Spacer Deposition & RIE
- eSiGe(P) /eSD (N) Growth
- ILD / CMP for Node Separation
- Dummy Gate Removal
- Multi-WF Gate Stack Formation
- Self Aligned Contact (SAC) Formation
- BEOL (Cu metallization)

IBM Alliance - K-I Seo, B. Haran, VLSI 2013
Transition from 7nm Node to 5nm Node - FinFET

- CPP, FP scaling are required for area scaling
- Aggressive Lg scaling (15nm → 10nm)
- Dfin scaling limited by QC Vt variability
- Spacer thickness scaling for contact area
- Performance by parasitic cap and R reduction electrostatics, channel material?
Leakage Paths in Bulk FinFET

Perpendicular to Gate

Parallel to Gate

Bulk FinFET has similar leakage mechanisms as bulk planar

Bulk FinFET Leakage Mechanisms:
1) Sub threshold leakage
2) Gate Leakage
3) Gate Induced Drain Leakage (GIDL)
4) Junction Leakage
Final Structure of Fabricated CMOS Device

- Novel Multi-WF gate stacks implemented.
- Combined a Replacement gate process flow with Self-aligned contacts (SAC)

IBM Alliance – Early 10nm Node
K-I Seo, B. Haran, VLSI 2013
Aggressive Scaling with Innovative sub-Optical Patterning

- Sub-80nm patterning accomplished by using:
  - Sidewall image transfer (SIT)
  - Design Co-optimization of restrictive ground rules
Multi-$V_T$ – need to add alternate channel $V_T$

### FinFET Scheme 1

- **SLVT**
- **LVT**
- **RVT**
- **HVT**

**Graph:**
- $I_{OFF}$ vs $I_{EFF}$
- $I_{OFF}$ (nA/µm)
- $I_{EFF}$
- Lg
- Lg+5nm
- Lg+5nm, more doping
- Lg+15nm, more doping

### FinFET Scheme 2

- **SLVT**
- **LVT**
- **RVT**
- **HVT**

**Graph:**
- $I_{OFF}$ vs $I_{EFF}$
- $I_{OFF}$ (nA/µm)
- $I_{EFF}$
- Lg
- Lg+5nm, WF$_1$
- Lg+5nm, WF$_2$
- Lg+5nm, doping, WF$_2$

### Points:
- Density is limited by the longest Lg. Want to keep Lg small.
- Large Lg is needed to shift $V_T$ for good short channel control.
- Multi WF can reduce the length of the longest gate.
Alternate Channel Materials
Performance - Channel Strain vs Gate Pitch for e SiGe

Not much room to put e-SiGe at aggressive CGP. *SSDOI and c SiGe* channel are independent of gate pitch. *It is important to look at channel strain.*

(**SiGe desperately needed for contact resistivity)**
nMOS Performance Enhancement Option

Strained Si Directly on Insulator (SSDOI)

Tensile Strained Si

*Bulk analog is also being pursued by many researchers.*
SSOI nFET – Planar FDSOI
Low Power and High Performance Lg=20nm

SSOI nFET demonstrated with Ion 1440 μA/μm and 1120 μA/μm at Ioff=100nA/μm and 1nA/μm respectively and 0.9V 0.75V and Ioff=1nA/μm Ion=1120 and 760 μA/μm. Tsi ~ 5nm

Q.Liu IEDM 2014
20% SSDOI FinFETs --- nFET

- SSDOI nFinFETs show > 25% Ieff improvement
- SSDOI benefit is independent of gate pitch – Channel Strain
- Bulk analog will behave similarly

A. Khakifirooz et. al. S3S Conference 2014
Stress vs. Device Width

Large width: Biaxial stress
Narrow width: Uniaxial stress

Relaxation in transverse and increased strain in longitudinal direction leads to extremely high mobility enhancement.
As device W gets narrow mobility increases. Drive current is 60% higher for narrow W.

*This is not simulation, this is 25% SiGe FDSOI device data.*

Although this is planar data FinFET will have similar benefits.
We converted the SSDOI into SGOI by SiGe condensation process.

Si 20% SSDOI pFET with strained 20% SiGe is same as Si pFET.

First demonstration of relaxing SSDOI strain in a controlled manner.

There is a way to overcome tensile strain SSDOI with SiGe for pFETs!
Starting with SSDOI made using 20% SiGe we do condensation with 35% to 50% SiGe.

This leads to the strain equivalent of 15% to 25% SiGe pMOS.

Tensile and Compressive stress is additive!

Reciprocal Space Map showing strain on SSDOI after condensation process on SSDOI.
We turned tensile strain in SSDOI into compressive strain.
Device data shows the Ge concentration is increased to 35% to compensate 20% SSDOI the strain in pFET looks like 15% SGOI starting with neutral Si. Lg~20nm, Tsi~5nm

Q.Liu IEDM 2014
Parasitic Resistance Reduction with Epitaxial Extensions

- Due to low temp process, implanted extensions introduce damage and have limited activation (high Rs).
- Compared to implanted extensions, epitaxial extensions leads to $\sim 10x$ lower $I_{OFF}$ floor due to less damage at channel-to-contact (p-n) junction.

Y. Sun, A. Majumdar, et al, IEDM 2013
Peak Gmsat shows significant improvement from 2013 to 2014

Rext also improved dramatically

Device characteristic Improvement is a direct result of process improvements.

Key Challenges: Materials Processing including III V, Gate Stack, Junctions, Contacts

Y. Sun, A. Majumdar, et al, IEDM 2013, IEDM 2014
III V – IBM Materials Improvements

- Defect density is continuously improving.

**Plan View TEM**

- **Typical**: $2 \times 10^9$ cm$^{-2}$
- **Improved**: $4 \times 10^8$ cm$^{-2}$

Target is close to $<1000$ cm$^{-2}$

Y. Sun, A. Majumdar, et al, IEDM 2013, IEDM 2014
Strained SiGe has lower hole effective mass than Si due to both Ge content as well as uniaxial compression.

Simulations show the impact of strain is more than increasing Ge fraction.

- Strained Si\textsubscript{1-x}Ge\textsubscript{x} with moderate Ge content can offer lower effective mass than even pure Ge, while avoiding significant bandgap shrinkage at higher Ge %.
As SiGe concentration increases gate stack is key challenge (Dit increases, SS degrades). At very high SiGe concentrations, new processes are needed for junctions, contacts.

Transfer characteristics of an electrostatically long channel \((L_G=95\text{nm})\) s-SiGe pMOS FinFET with regular (dashed) and new (solid) passivation scheme, showing the impact of the new passivation scheme to improve the on current and SS.
Impact of New Passivation Scheme on $I_{on}$-$I_{off}$

- $I_{off}$ vs. $I_{on}$, for two passivation schemes measured at $V_{DD}=0.9V$
- The new passivation improves drive current by 20% at $I_{off} = 100nA/\mu m$

P. Hashemi VLSI 2014
Most-aggressively-scaled SiGe finFET $L_G=15\text{nm}$, $W_{\text{FIN}}=8\text{nm}$ and $H_{\text{FIN}}=20\text{nm}$

High performance is maintained at the aggressively scaled gate lengths ($I_{\text{on}}/I_{\text{eff}}=1.28/0.74 \text{ mA/\mu m}$ at $I_{\text{off}}=80 \text{ nA/\mu m}$ at $V_{\text{DD}}=1\text{V}$)

P. Hashemi VLSI 2014
SiGe Fin – 70% Ge

Interface control – low Dit, gate stack optimization at very thin Tinv.

P. Hashemi VLSI 2015
FEOL Integration Issues and Opportunities for Alternate Device Architectures
## Scaling Beyond 7nm Node

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<th>Node</th>
<th>Gate Pitch (nm)</th>
<th>Nominal L (nm)</th>
<th>Spacer (nm)</th>
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*New device architecture is needed ~ 5-3nm Node. Tsi ~1/2Lg for FinFETs*
Nano Wire – For Improved Electrostatics - Lg scaling.

- Fin is capable of delivering more current per footprint. Single wire is not competitive.
- Stacked and wider can resolve the Weff issue.
- How much Lg scaling is possible?
- Nano Wires are still CPP constrained.
- Wider wires have less electrostatic improvement.
- Can we have multiple generations of Nano Wire?

I. Laurer  VLSI 2015
Vertical Nanowires – Lg and spacer dimension are decoupled from the gate pitch. Density is determined by distance between the wires. Many process challenges.
Monolithic 3D principle

Scaling can be achieved by using Previous node ground rules and stacking another device layer on top of the first device layer.

Different than TSV approach. No alignment issues.

Bonded layer is patterned after bonding not before.

O. Faynot, M. Vinet – LETI
IBM – LETI – ST JDP
Versatility of Monolithic 3D: 2 main options

- CMOS over CMOS

<table>
<thead>
<tr>
<th>Bottom transistor</th>
<th>Top transistor</th>
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<tr>
<td>Bulk</td>
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<tr>
<td>Bulk FinFET</td>
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<tr>
<td>SOI FinFET</td>
<td>SOI FinFET</td>
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<tr>
<td>SOI Trigate/NW</td>
<td>SOI Trigate/NW</td>
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<tr>
<td>FDSOI</td>
<td>FDSOI</td>
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- N over P

\[
\frac{7\text{nm}}{7\text{nm}} = 5\text{nm}
\]

+ Mixing of FinFET, NW, FDSOI with various materials/orientations
+ N and PMOS optimized independently

O. Faynot, M. Vinet – LETI IBM – LETI – ST JDP
CMOS/CMOS: PPA Analysis at 14nm vs 2D

- FPGA applications
- 2 stacked FDSOI layers
- W used for interconnects (2 Metal levels)
- Main results for 6 circuits/ planar
  - **Area gain** = 55%
  - **Perf gain** = 23%

O. Faynot, M. Vinet – LETI
IBM – LETI – ST JDP

DAC 2014
Monolithic 3D - Integration challenges

Low temp top MOSFET
- Gate stack
- Dopant activation
- Epitaxy

Local Interconnect Level
- Thermal stability and low resistivity
- Manufacturing compatibility

Salicide thermal stability

O. Faynot, M. Vinet – LETI
Monolithic 3D - Material co-integration

- Already demonstrated: Ge over Si, Si (110) over Si (100)
- Next step: InGaAs over Ge

COMPOSE3 between IBM Zurich and LETI.

P. Batude et al., VLSI 2009; [27]: P. Batude et al., IEDM 2009
Conclusions
Conclusions

- FinFET scaling is limited by Tsi scaling and CPP.
- High mobility channel materials and low resistance contacts are needed to continue performance trend.
- Nanowires offers scaling beyond FinFET.
- Vertical Nanowires can enable density scaling.
- 3D Integration may be an attractive option to provide density improvement.
Successful Technology Implementation

- We are living in a very exciting era.
- There are many interesting and important topics to work on.
- Many small steps are needed to arrive at our destination so start early.
- Collaboration with Academia, Industrial Research- Development and Manufacturing is key.
- Please continue to work on Ge, III-V, TFET, MoS2, Nanotubes and others.
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