BEOL Process Challenges

2015 IEDM Short Course #1
Emerging CMOS Technology at 5nm and beyond
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Takeshi Nogami

IBM Research @ Albany Nano Tech Center
IBM Corporation, NY, USA
tnogami@us.ibm.com

Acknowledgements to IBM Alliance Team members

Terry Spooner
Daniel Edelstein
Larry Clevenger
Benjamin Briggs
Griselda Bonilla
Eric G Liniger
Son Nguyen
James J Kelly
Huai Huang
Vamsi Paruchuri

** Sevim Korkmaz
Moosung Chae[1]
Christopher Penny
Juntao Li
Wei Wang
Paul S McLaughlin
* Christopher Parks
* Anita Madan
Stephan Cohen
Thomas Shaw
Deepika Priyadarshini
Hosadurga Shobha
Raghuveer Patlolla
Xunyuan Zhang[4]
Donald Canaperi
Theodorus Standaert
Elbert Huang

IBM Research
[1] GLOBALFOUNDRIES Inc.

*currently GLOBALFOUNDRIES Inc.
**currently Micron Technology

IEDM 2006 32nm BEOL Short Course - Bob Wisnieff / IBM

Did not happen in 32 nm to 10 nm

1. Cu resistance:
   1. Minimize barrier thickness
   2. Maximize Cu grain size
2. Capacitance:
   1. Spin-on dielectric, SiLK
   2. SiLK Hybrid low-k process
3. Carbon-Nanotube
4. Superconducting materials
5. Supercritical fluids for cleans and strip
6. ECMP
7. CVD Cu Seed
8. Direct electroplating on Ru barrier
9. Electroless plating / seed repair

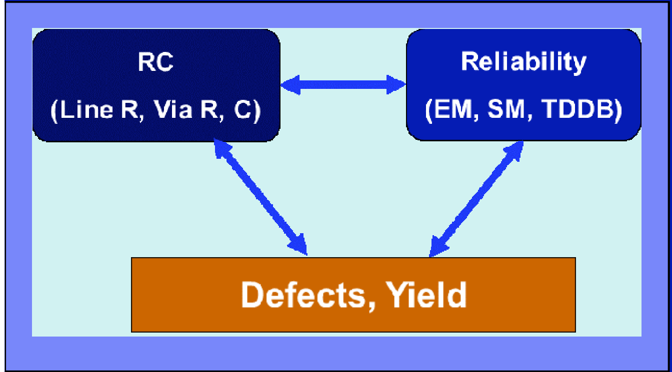
Happened in 32 nm to 10 nm

1. Porous PECVD-SiCOH (22 nm BEOL)
2. Air gap
3. Electroless deposition of CoWP
4. ALD-TaN

Not mentioned, but happened.

1. CuMn alloy seed (32 nm and beyond)
2. CVD-Co wetting layer
3. Selective CVD-Co cap

Common approaches vs. Innovative approaches



Innovation to achieve these three simultaneously

Fundamentals that we need to understand
1. Line Resistance
2. Via Resistance
3. Capacitance
4. Electromigration
5. TDDB
6. Cu gap fill
7. Barrier test
8. RC Variation

Common approaches
1. Stress-liner capped anneal for Line R
2. Tall metal for Line R
3. Self Forming Barrier for Line R
4. Lower-k integration and air gap for C
5. Selective Co cap for EM
6. Cu alloys for EM
7. CVD-Co, Ru for Cu gap fill

Innovative approaches
1. Integrated solution with alternative barrier
2. Co plug to reduce the aspect ratio of Cu
3. Alternative conductors
4. Alternative diffusion barriers

Understanding fundamentals of these three components

Innovation to achieve these three simultaneously

1. Common approaches
2. Innovative approaches

3. Radical technologies (graphene etc.) → Prof. Saraswat in the afternoon

OUTLINE

1. **Technology Scaling and BEOL**
2. **BEOL Challenges**
   - ❖ **Tradeoff's**
3. **Potential Solutions**
   - ❖ **Fundamentals**
   - ❖ **Common Approaches**
   - ❖ **Innovative Approaches**
4. **Summary**

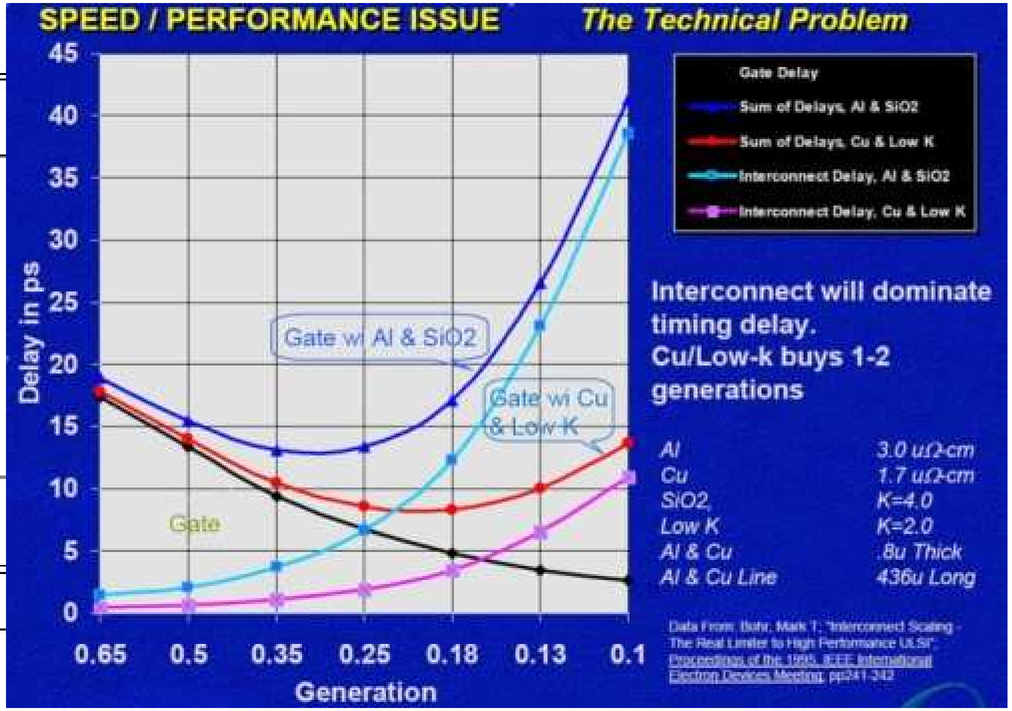
BEOL has started to void FEOL scaling benefits

Scaling Results for Circuit Performance

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Scaling Results for Interconnection Lines

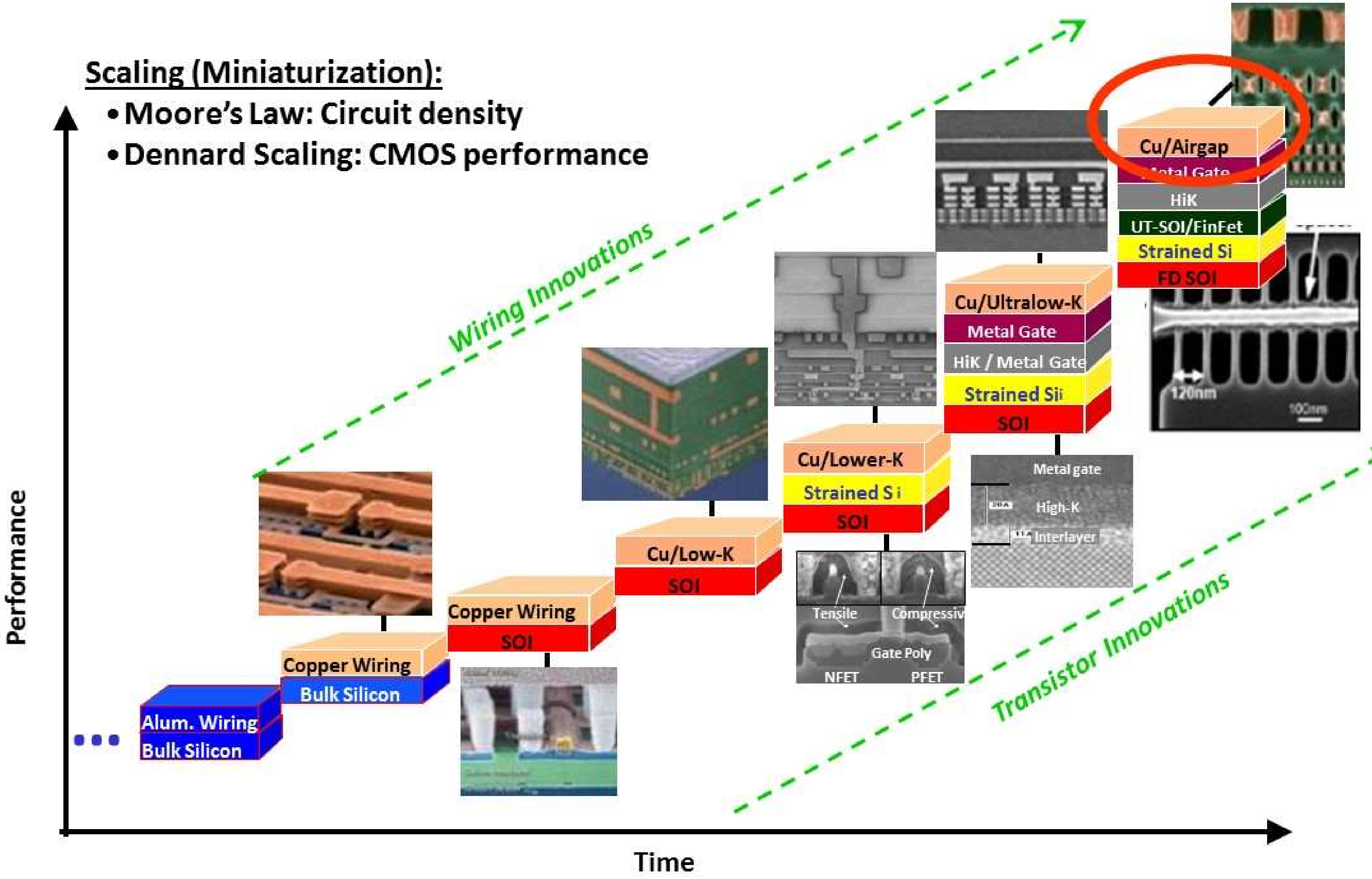
Parameter	Scaling Factor
Line resistance, $R_L = \rho L/Wt$	κ
Normalized voltage drop IR_L/V	κ
Line response time $R_L C$	1
Line current density I/A	κ



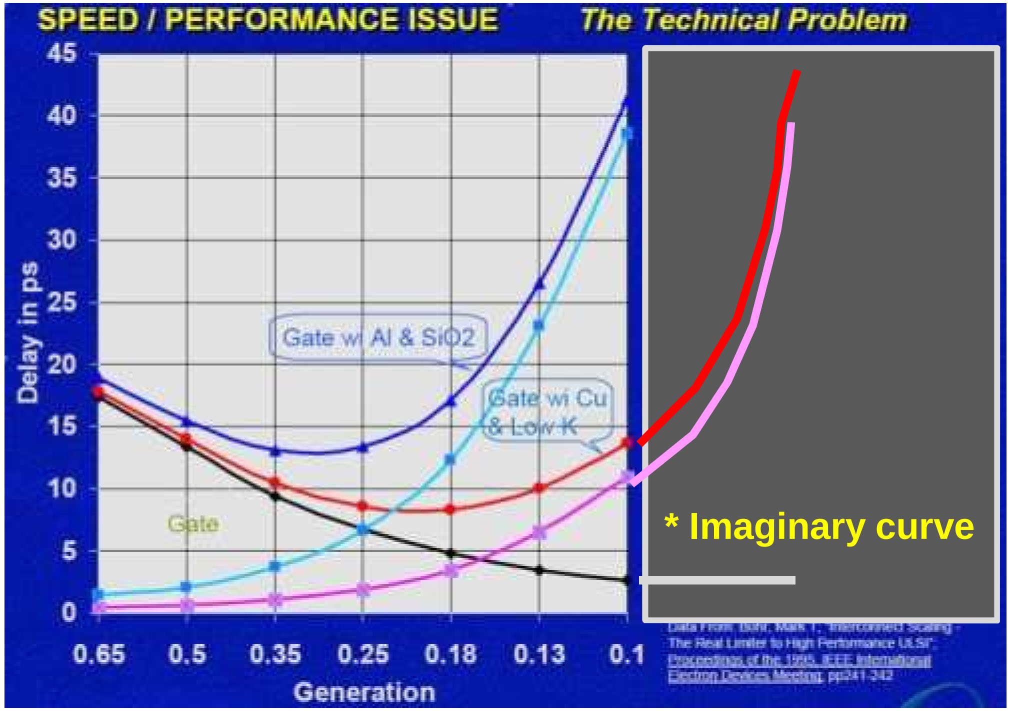
Scaling factor of Interconnect is no longer *k*, but n*k* (n>1)

Interconnect RC started to dominate the delay.
It started already from 10 nm CMOS.

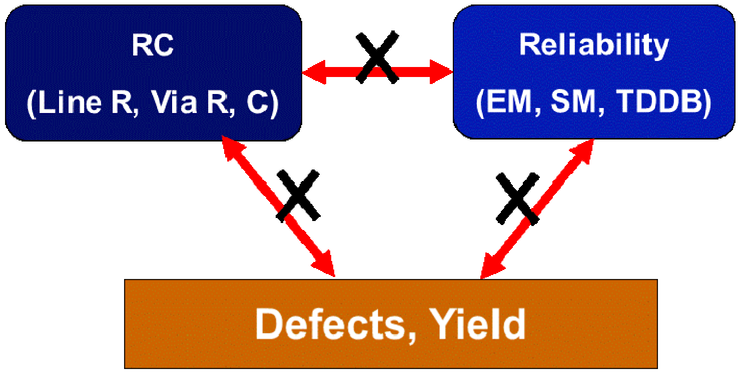
15+ year continuous BEOL innovations



BEOL has started to void FEOL scaling benefits



Tradeoff's



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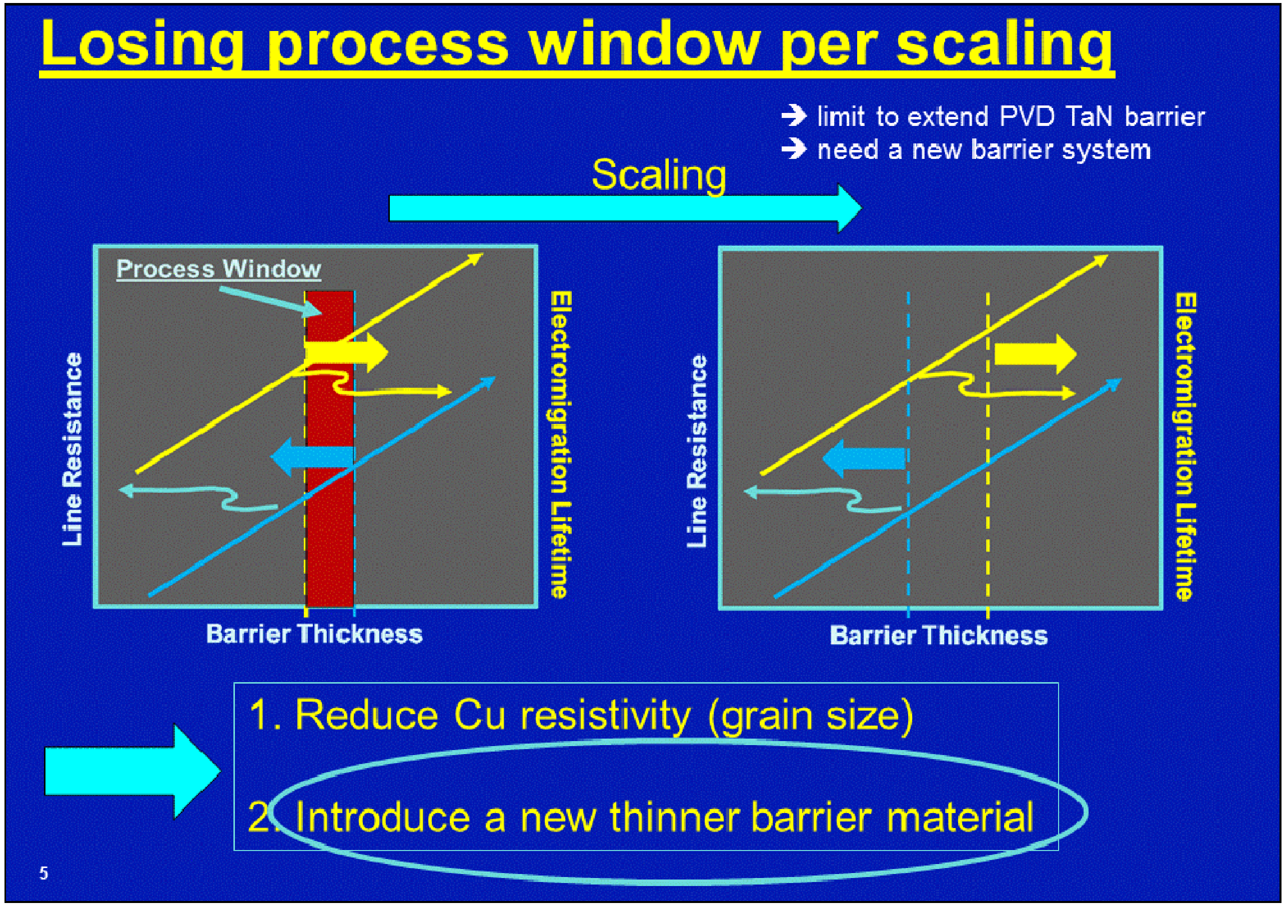
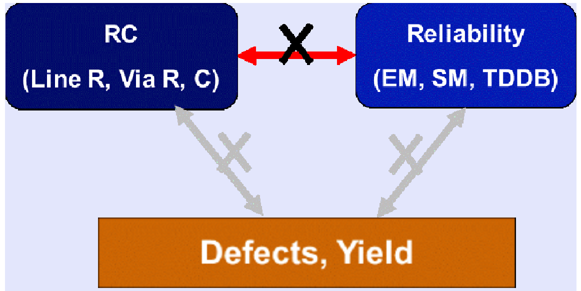
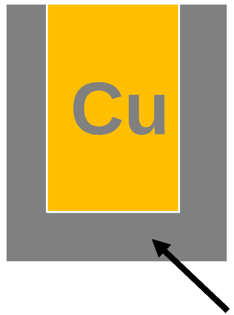
Tradeoff between Line R vs. EM



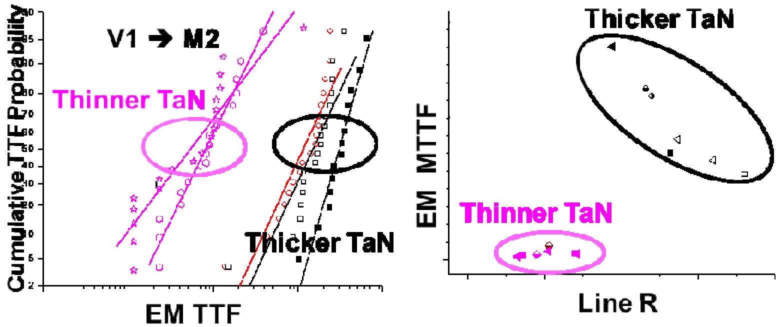




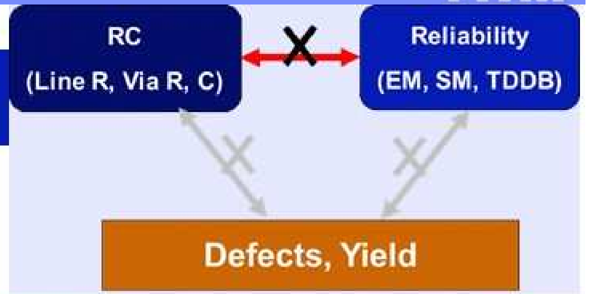
Barrier/Liner

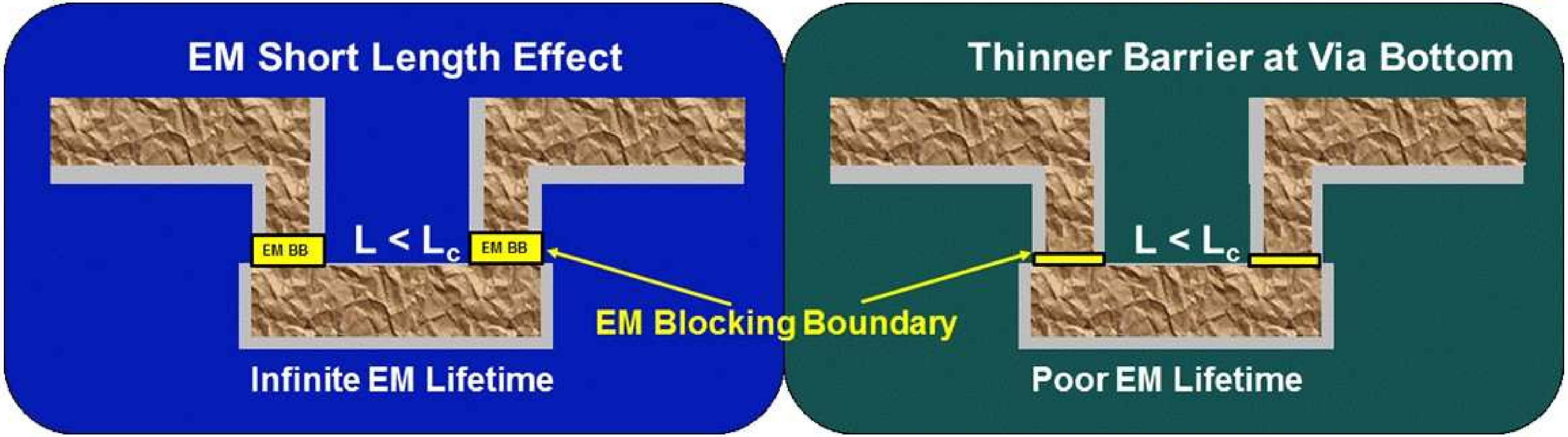
IEDM 2015 T. Nogami et. al

Reduce Line R ➔ Larger Cu Volume ➔ Thinner Barrier ⬅ Poor EM



Tradeoff between Via R vs. EM Reliability

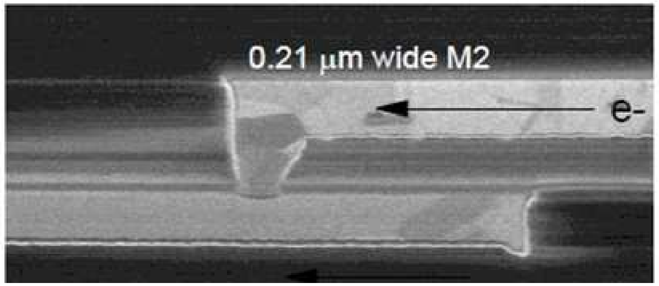




$$\frac{\partial n}{\partial t} = -\left(\frac{\partial}{\partial x}\{D\left(\partial n/\partial x\right) - n\frac{D}{kT}Z^* e\rho j\}\right)$$

$$v_{net} = 0$$

$$Z^* e\rho j L = \Omega\sigma$$

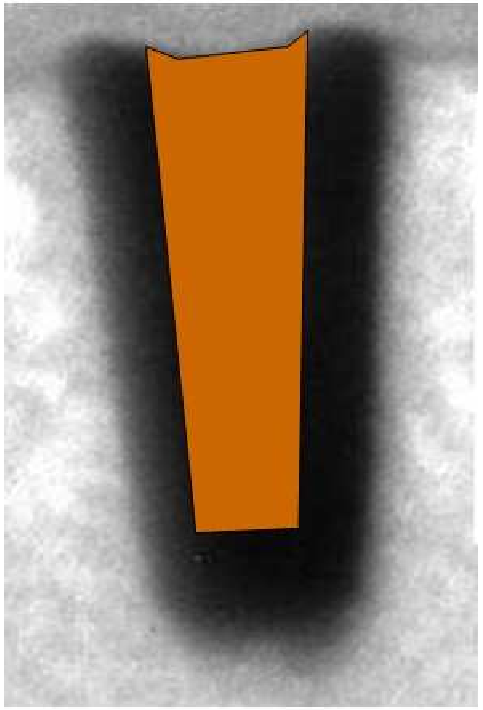


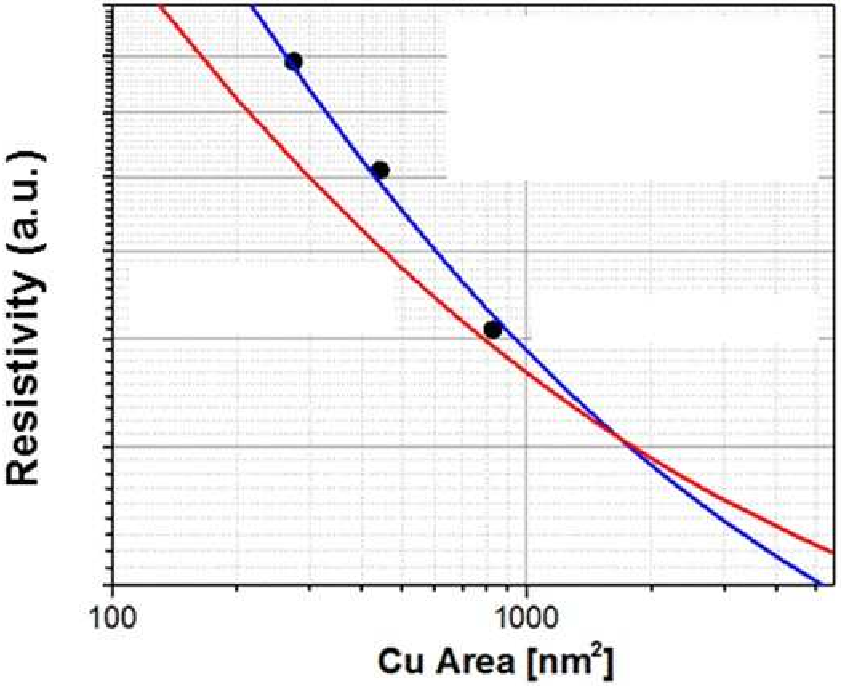
$$v_{net} = \frac{D}{kT}Z^* e\rho j - D\left(\frac{1}{n}\partial n/\partial x\right) = \frac{D}{kT}\{Z^* e\rho j - \left(\Omega\partial\sigma/\partial x\right)\}$$

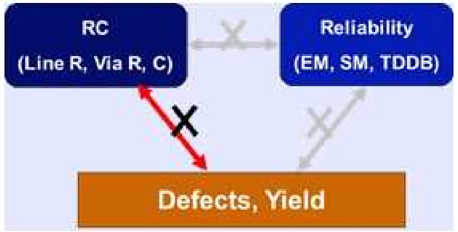
C. K. Hu et al., ECD 2000

Low Via R ➔ Thinner Barrier at Via Bottom ← Insufficient EM Blocking Boundary

Tradeoff between Cu Gap Fill vs. Line Resistance

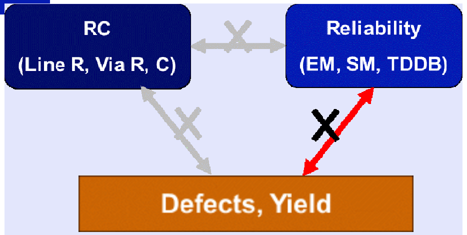


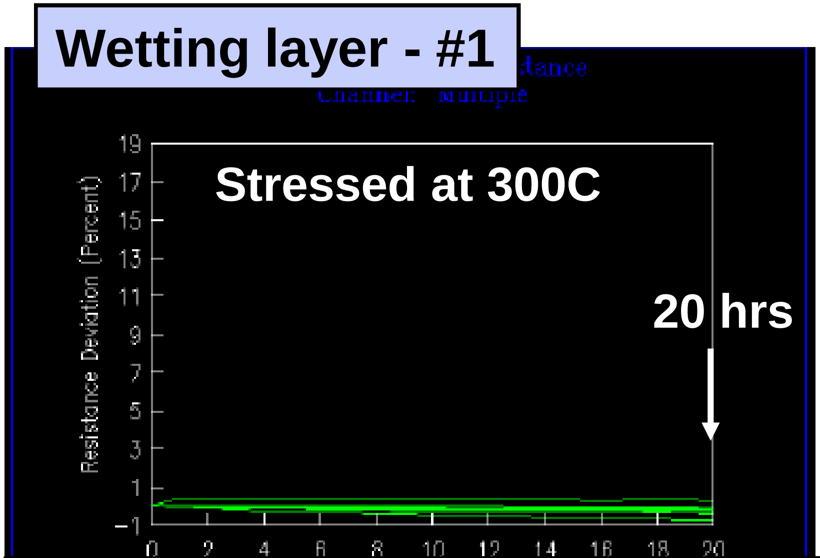


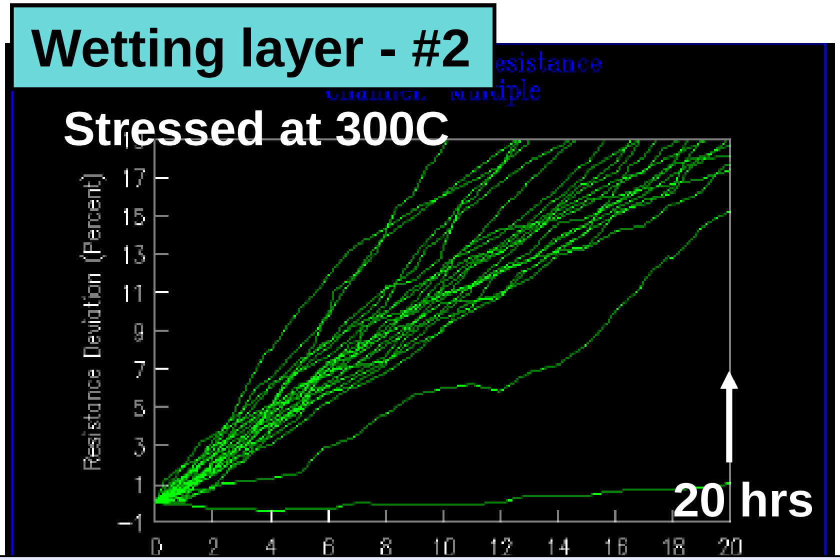


Cu Dual Damascene BEOL requires a Wetting Layer in addition to Diffusion Barrier.
Barrier Layer + Wetting Layer occupies significant volume which reduces Cu volume ← High Line R

Tradeoff between Cu Gap Fill vs. EM Reliability

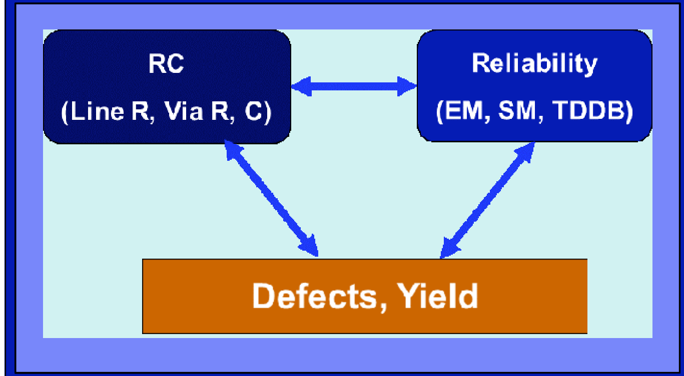






Wetting layer-#2 shows a higher potential for Cu gap fill than Wetting layer-#1.
However, the line R increase during EM stress test suggests a faster diffusion of Cu at the wetting layer/Cu interface.
Cu Gap Fill ➔ Better Wetting Layer –B 🡐 Poor EM Reliability

Common approaches and Innovative approaches for 5 nm BEOL



Innovation to achieve these three simultaneously

Understanding fundamentals

Fundamentals that we need to understand

1. Line Resistance
2. Via Resistance
3. Capacitance
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1. Common approaches

Common approaches

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2. Tall metal for Line R
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2. Innovative approaches

Innovative approaches

1. Integrated solution with alternative barrier
2. Co plug to reduce the aspect ratio of Cu
3. Alternative conductors
4. Alternative diffusion barriers

OUTLINE

1. Technology Scaling and BEOL
2. BEOL Challenges
   ❖ Tradeoff's
3. Potential Solutions
   ❖ Fundamentals
      1. Line Resistance
      2. Via Resistance
      3. Capacitance
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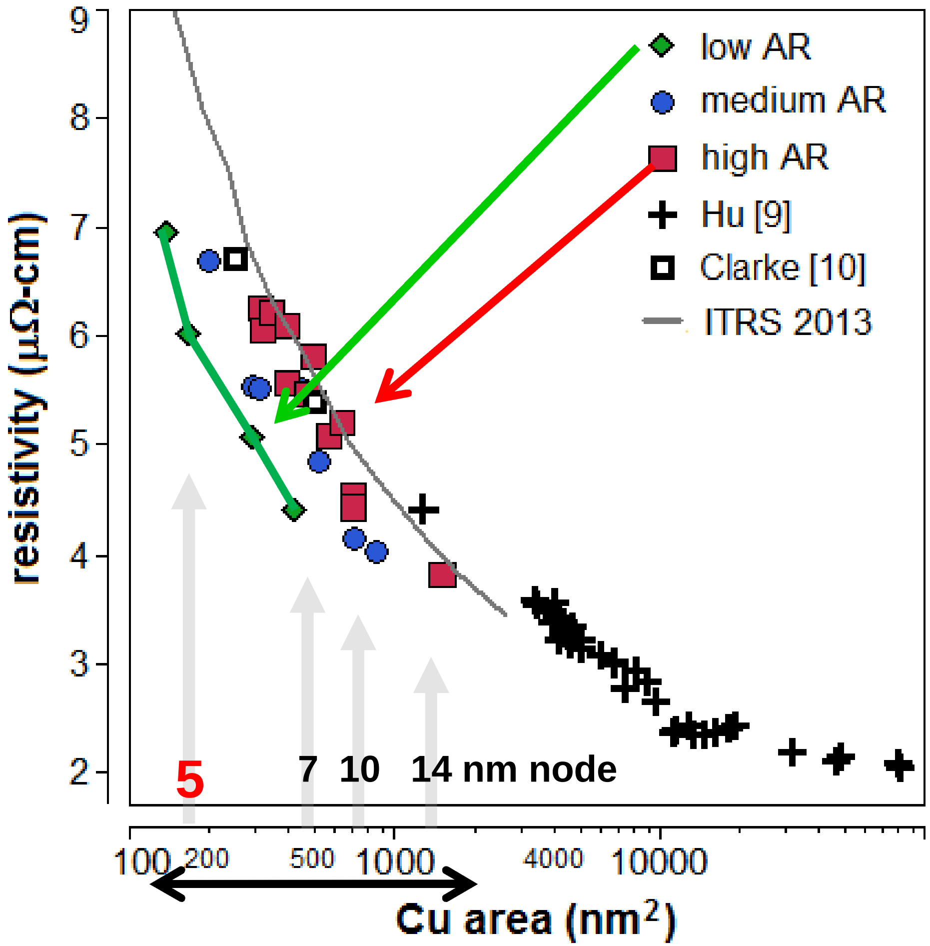
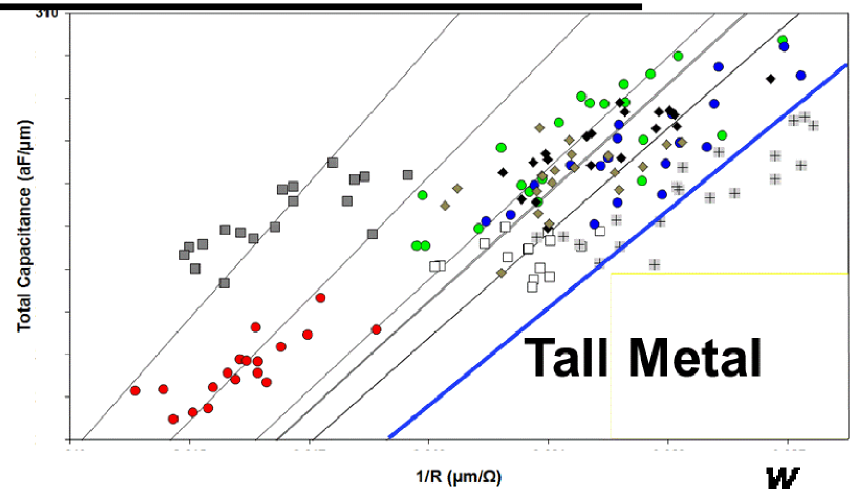
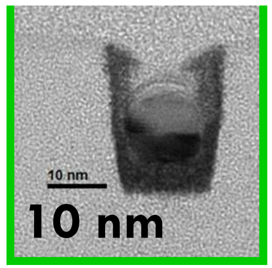
      6. Cu gap fill
      7. Barrier test
      8. RC Variation
   ❖ Common Approaches
   ❖ Innovative Approaches
4. Summary

Line Resistance

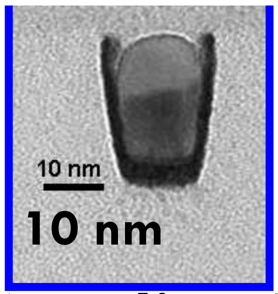
Cu line resistivity, resistance vs. Dimension



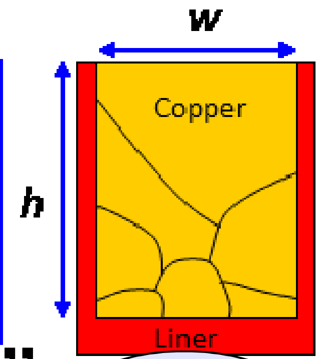




“low”



“medium”



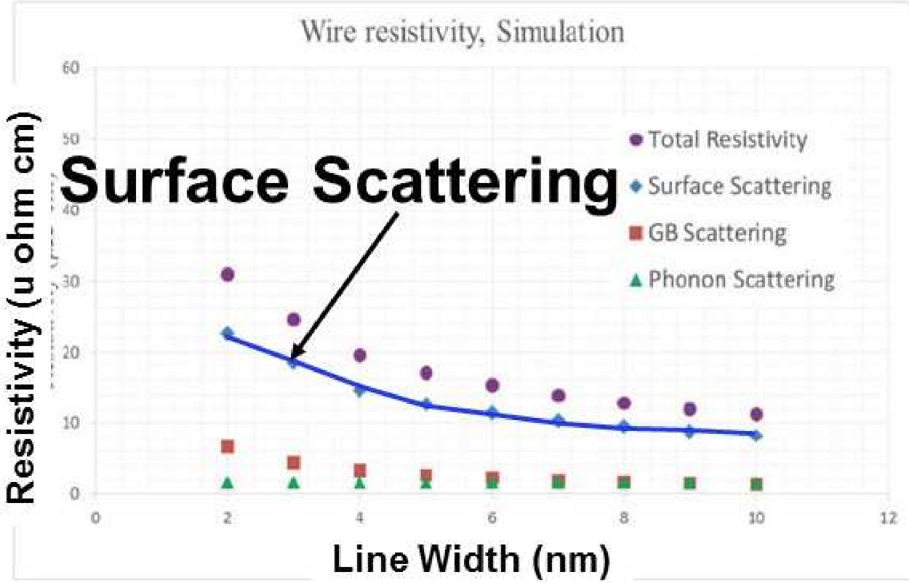
$$R = \frac{\rho}{w \cdot h}$$

Cu resistivity is not just simply determined by Cu volume. IC spec is Cu line resistance, not resistivity. That means we need both an acceptable resistivity, and acceptable line area (e.g. aspect ratio at a given pitch).

Fundamental-1

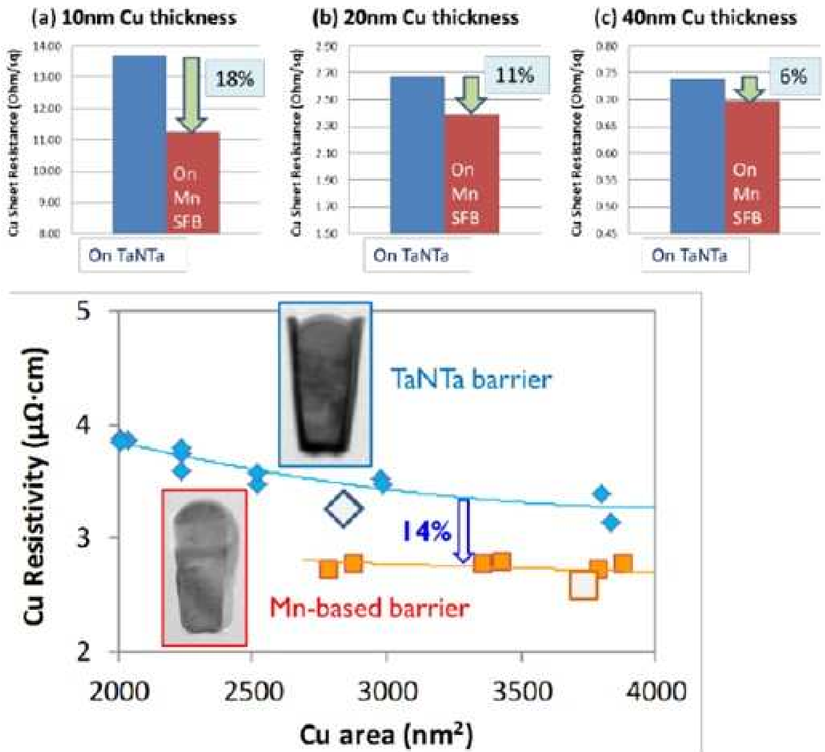
Line Resistance

Surface scattering of MnSiO3/Cu interface



Surface scattering dominates the Cu resistivity.

J. Roberts et. al, IITC 2015 Intel



Lower surface scattering with $MnSiO_3$ than Ta

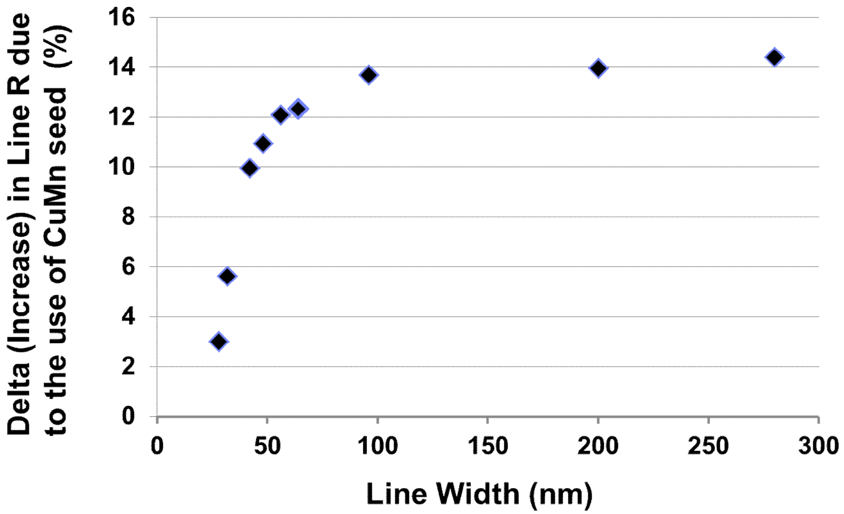
Y. Siew et. al, IITC 2014 IMEC

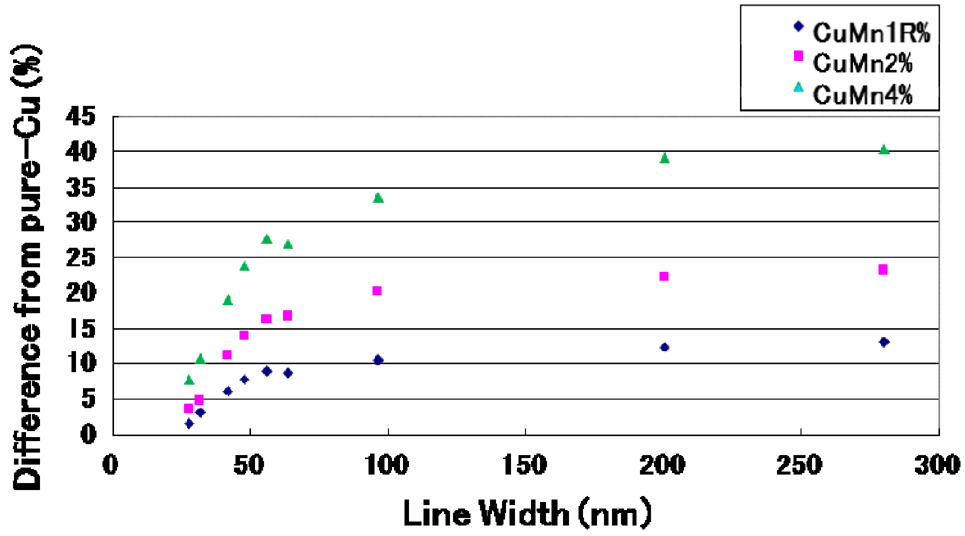
(1) Surface scattering is the major cause.
(2) Grain boundary scattering is the second cause.
(3) Larger Cu volume reduces the contribution of (1) and (2).

Line Resistance

Impurity Scattering and Cu Alloy

Relative decrease in line R penalty in finer dimensions



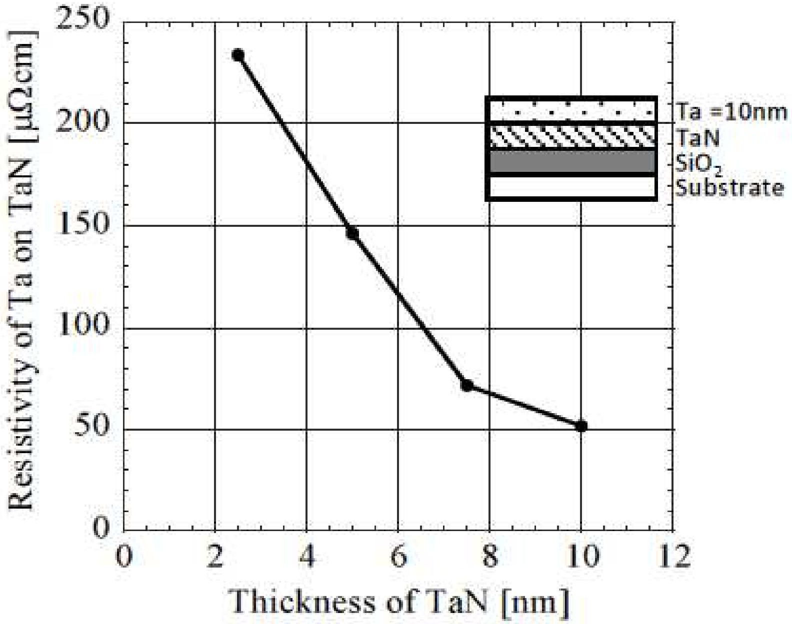


T. Nogami et. al, IITC 2013 IBM

1. CuMn alloy leads to <10% higher Cu line R, however,
2. The penalty is reduced to <3% in 10 nm BEOL.
3. Higher Mn % in finer dimensions with less R penalty.

Fundamental-2

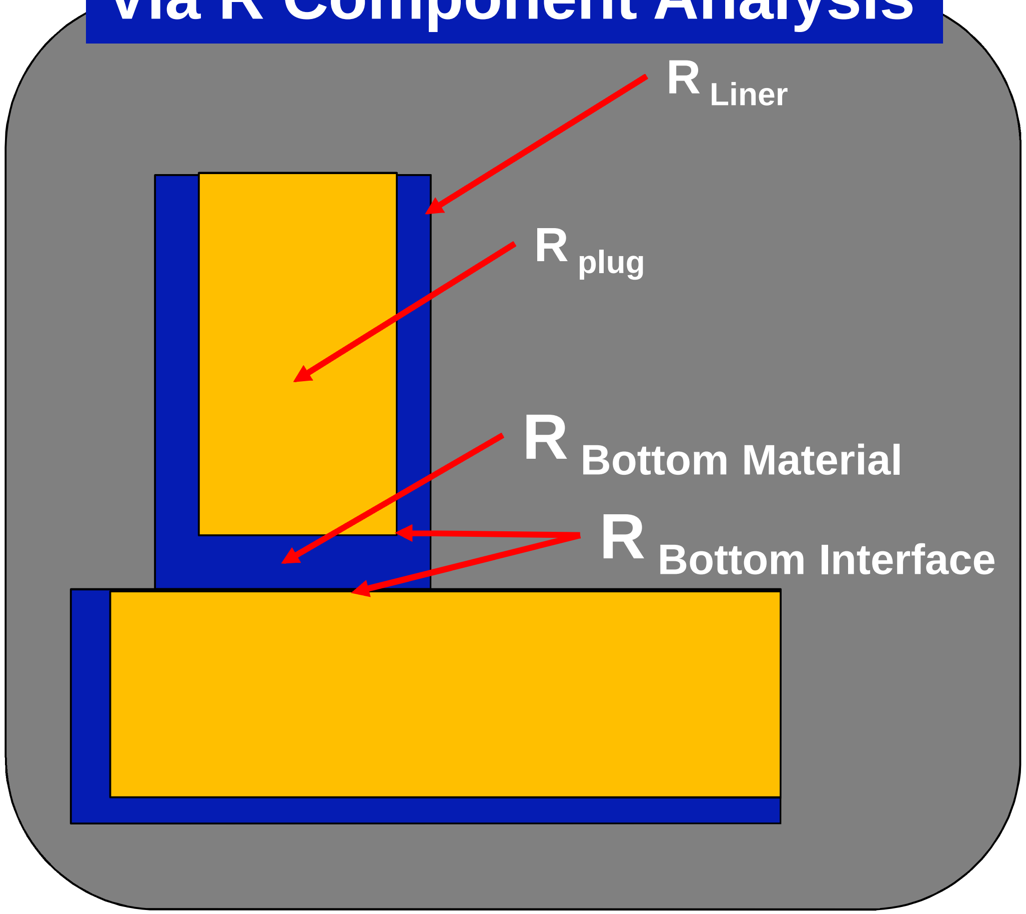
Via Resistance



Estimated thickness of TaN at via-bottom [nm]	2.2	3.6	3.7	6.0	7.2	7.3	9.0
Crystal Phase of Ta	β-Ta			α-Ta + β-Ta		α-Ta	

K. Ohmori et. al, IITC 2014

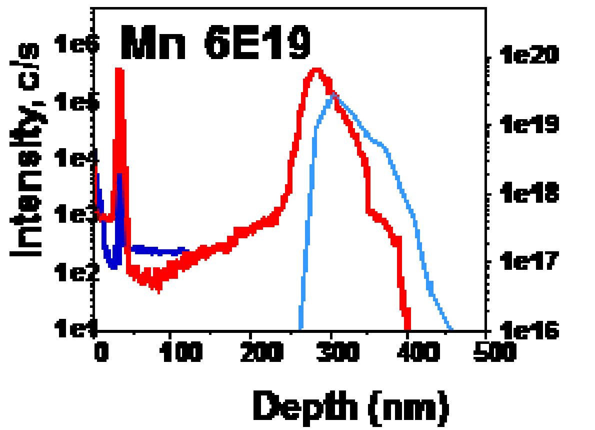
Via R Component Analysis



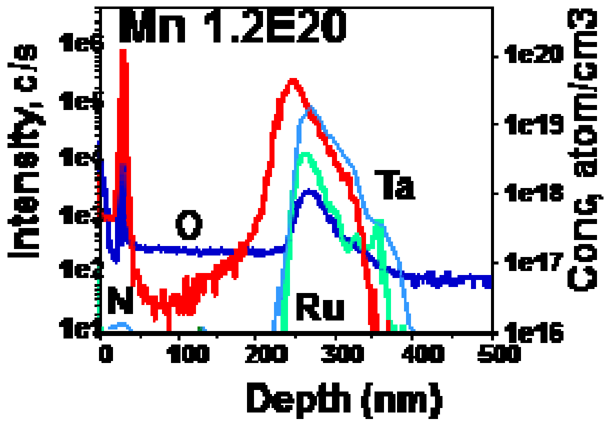
1. R(bottom material) and R(bottom interface) are dominant R components.
2. Material design of the R(bottom material) is one of the keys to lower via R.

Via Resistance

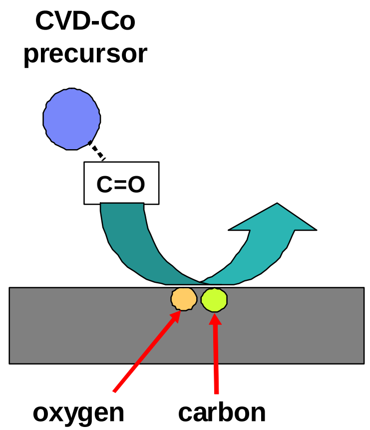
Via Interface Material due to Wetting Layer

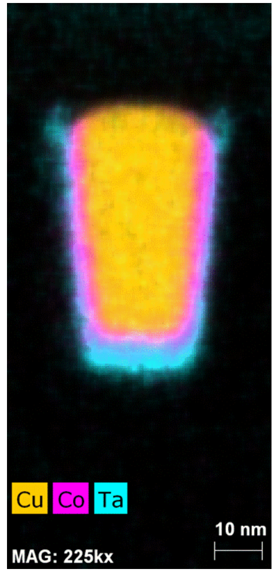


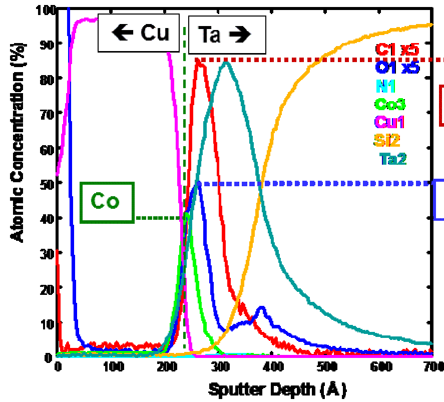
CuMn0.7R% on PVDRu

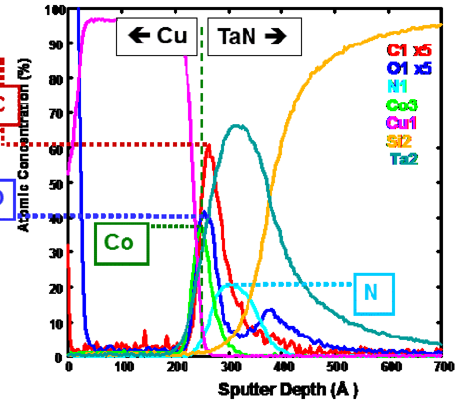


T. Nogami et al, IEDM 2010 IBM









T. Nogami et al, IITC 2010 IBM

1. CVD-Co, CVD-Ru on Ta(N) may create high R material at via bottom.
2. Decomposition of precursors for Co and Ru may contaminate the interface.

Dielectric (LK, ULK) materials

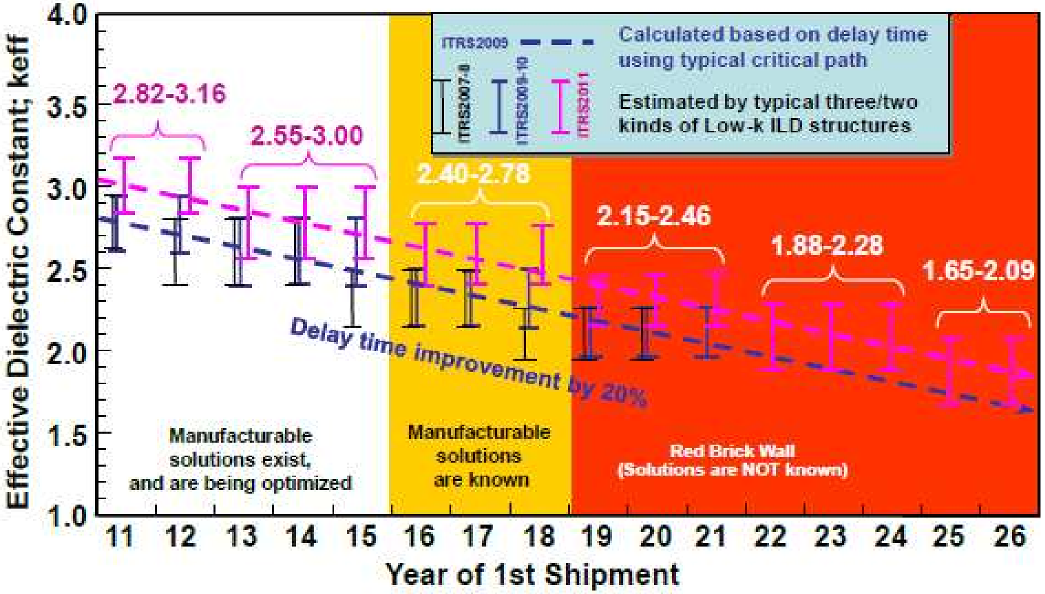
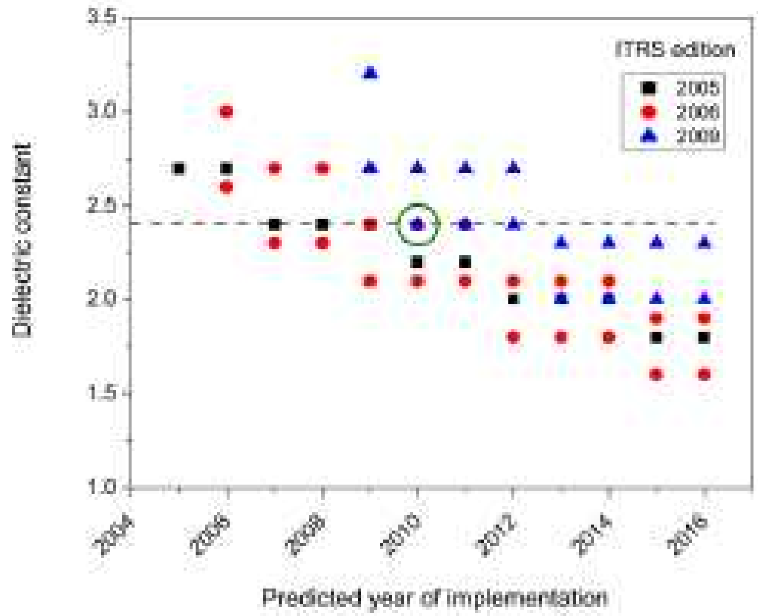


Figure INTC11 Low-κ Roadmap Progression

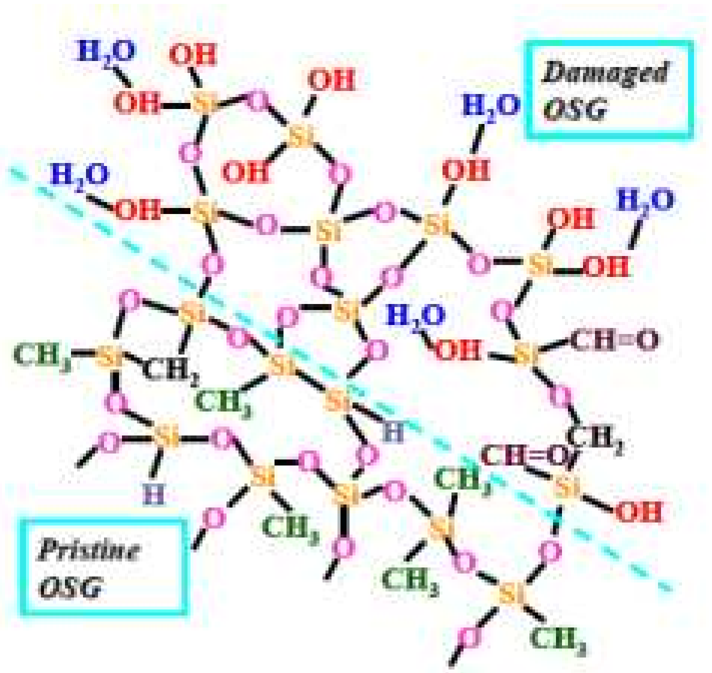


Source: ITRS, 2011

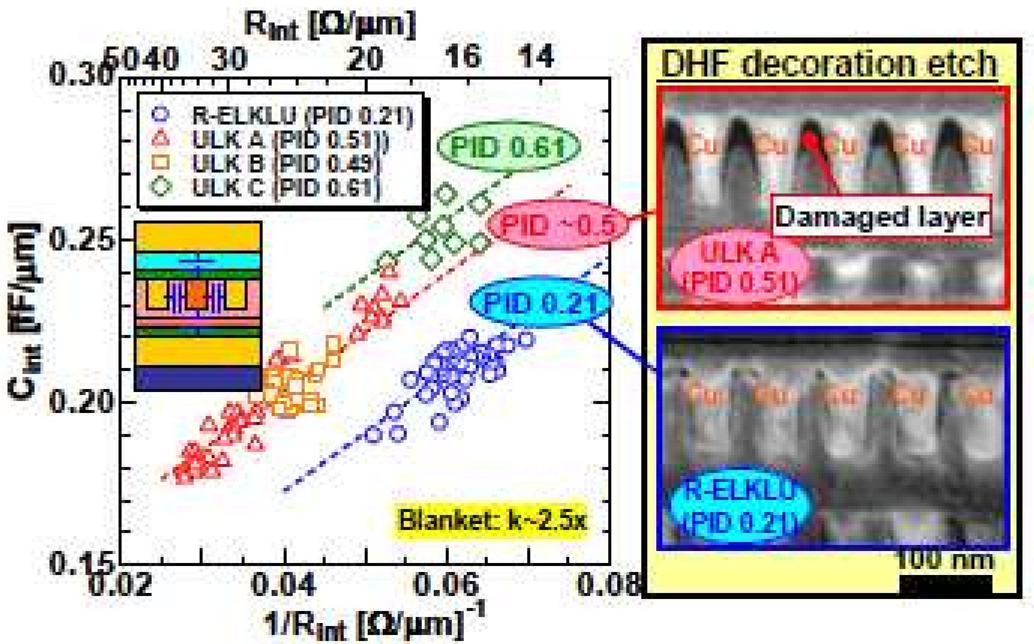
A. Grill et al, App. Phys. Rev, 2014 IBM

- ~ 150 different materials identified in the mid-90's (spin-on glasses, fluorinated silicate glass (FSG), diamond like carbon (DLC), organosilicate glass (OSG, SiCOH)).
- Delays observed with ULK implementation due to several integration challenges.
- PECVD SiCOH based materials are most prevalent today.

Dielectric damage



H. Huang, U. Texas Ph.D. thesis, 2012



N. Inoue et al, IITC 2013

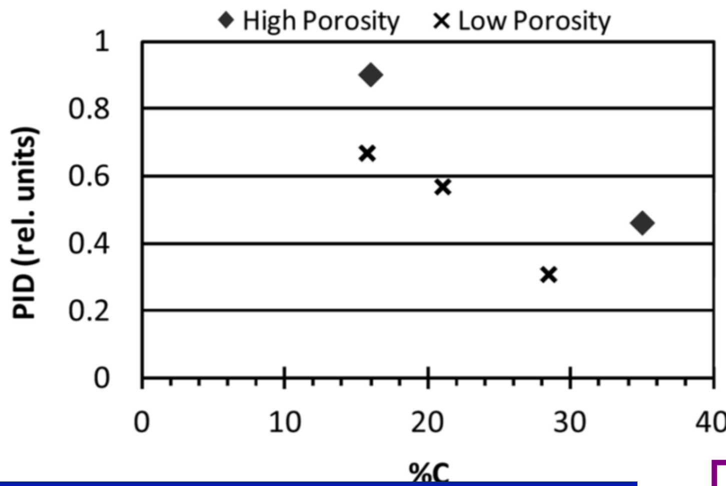
Dielectric materials can be damaged by many steps in the process flow. Damage results in increased capacitance and susceptibility to yield and reliability failure.

Fundamental-3

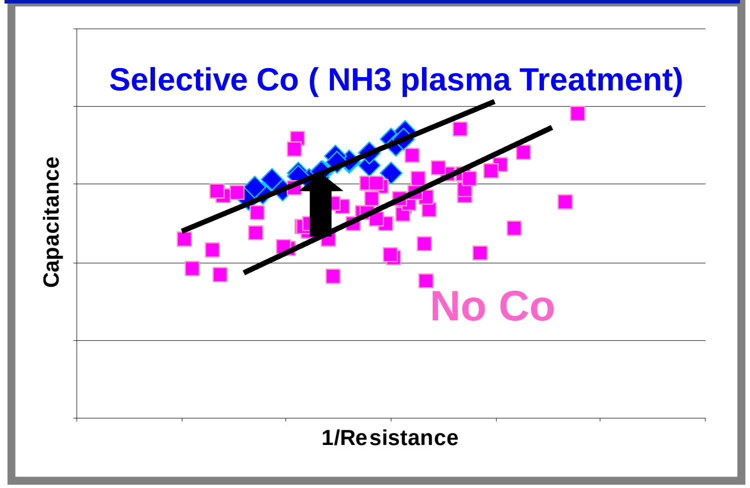
Capacitance

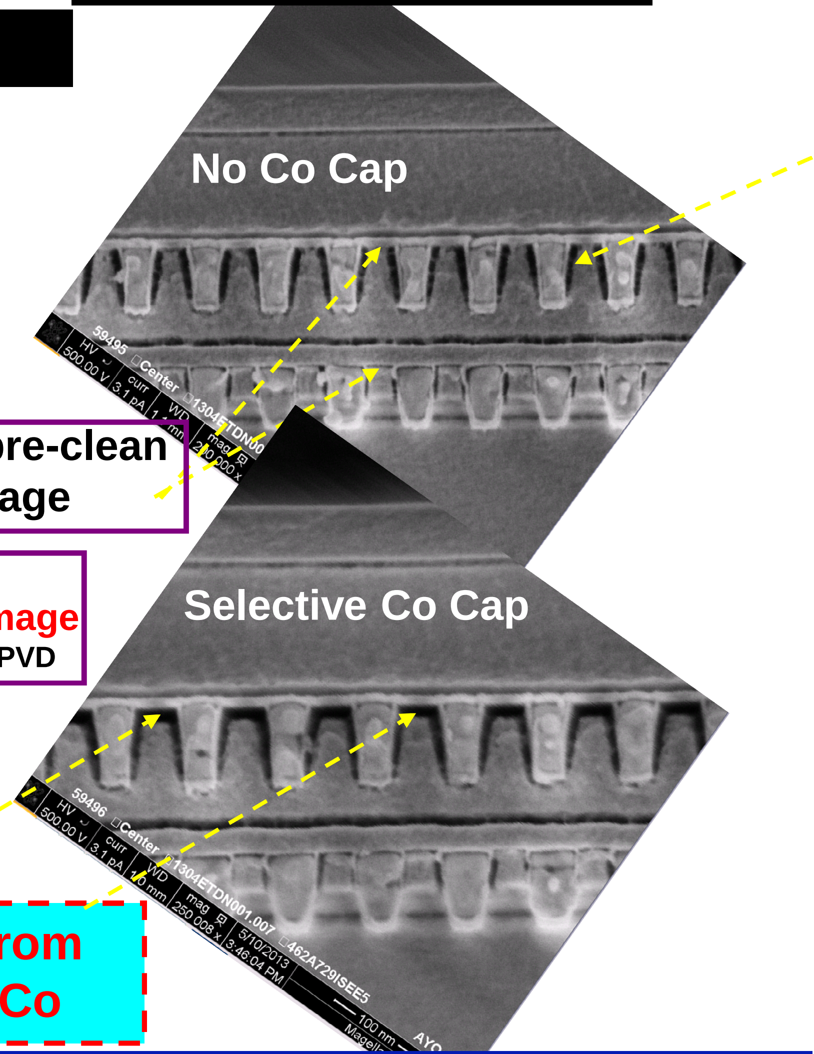
FIB-SEM with DHF decoration

Plasma Damage in ULK: Capacitance Impact



A. Grill et al., Appl. Phys. Rev 2014 IBM





Cu pre-clean damage

Plasma damage
From RIE and PVD

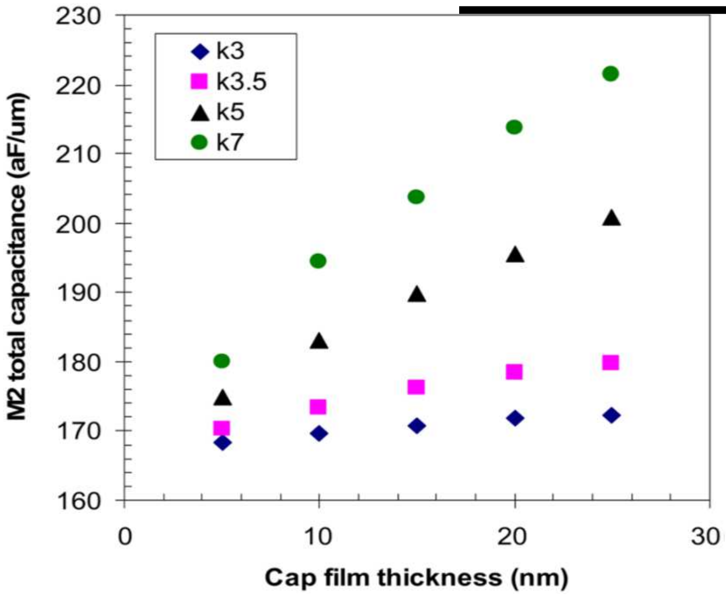
Damage from Selective Co

D. Priyadarshini /Nguyen et al., IITC 2014 IBM

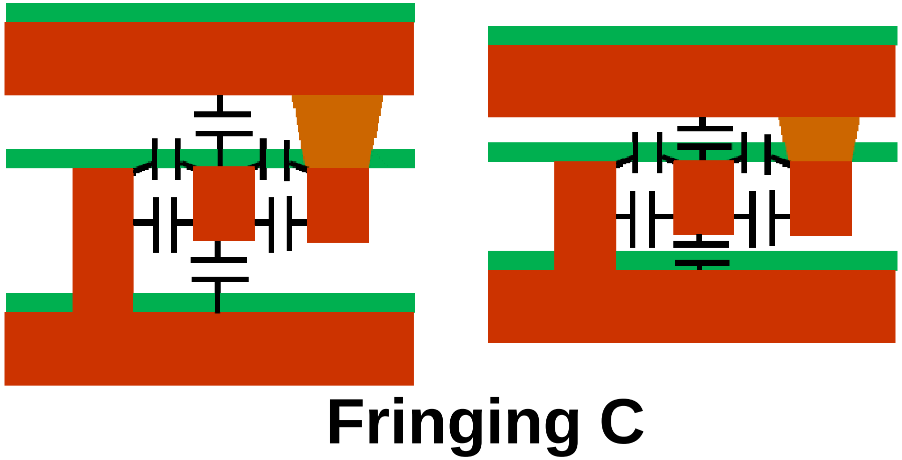
The degree of damage decreases as the %C in the film increases.
Selective CVD-Co pre-clean damage on top. PVD liner cause damage on Sidewall

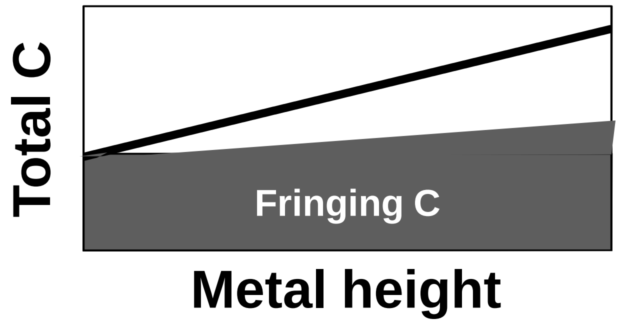
Capacitance

Dielectric Cap



A. Grill et al., Appl. Phys. Rev 2014 IBM

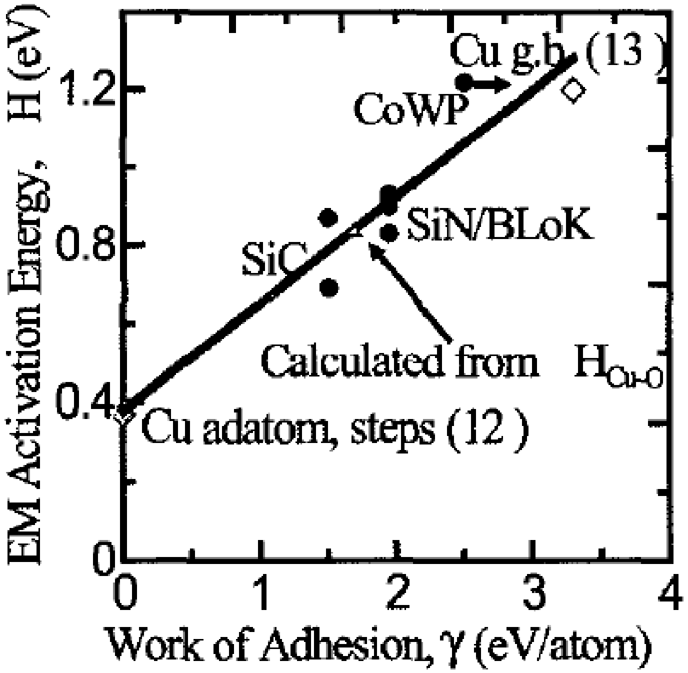


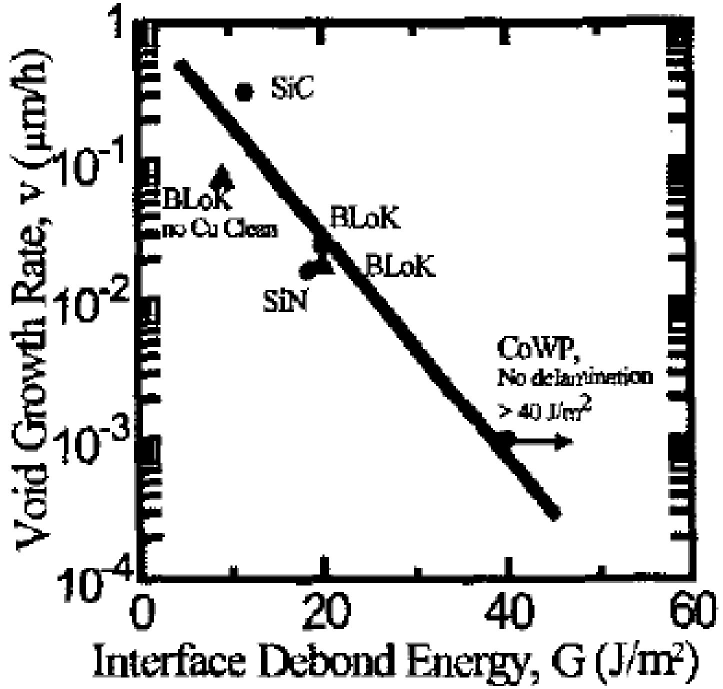


The additional C impact of non-scaling cap thickness is that next-level trench bottoms get too close to the cap, and penetrate fringing fields (Via height becomes too small vs. cap thickness).

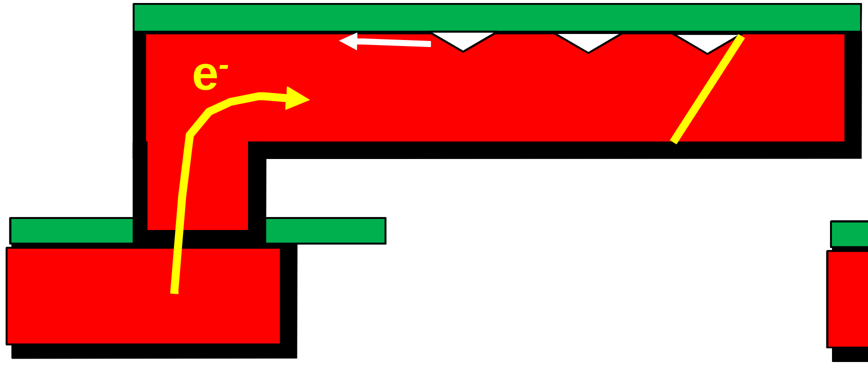
Electromigration

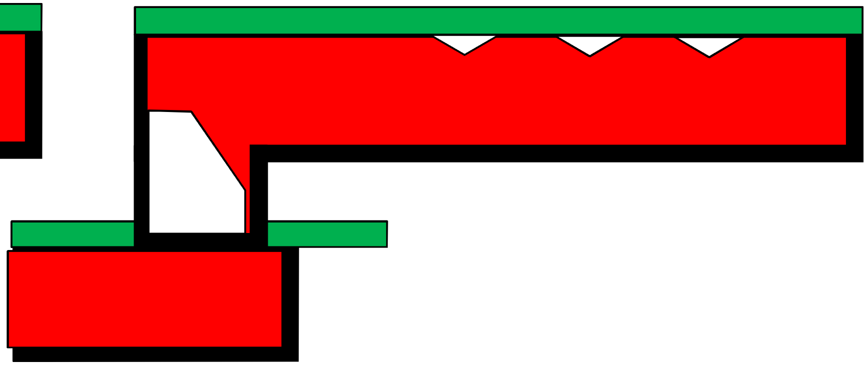
Cu top surface



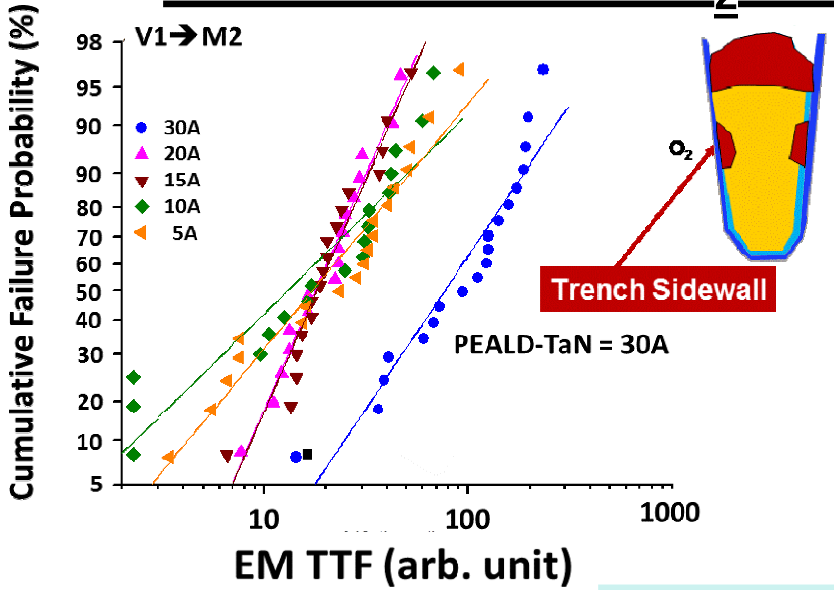


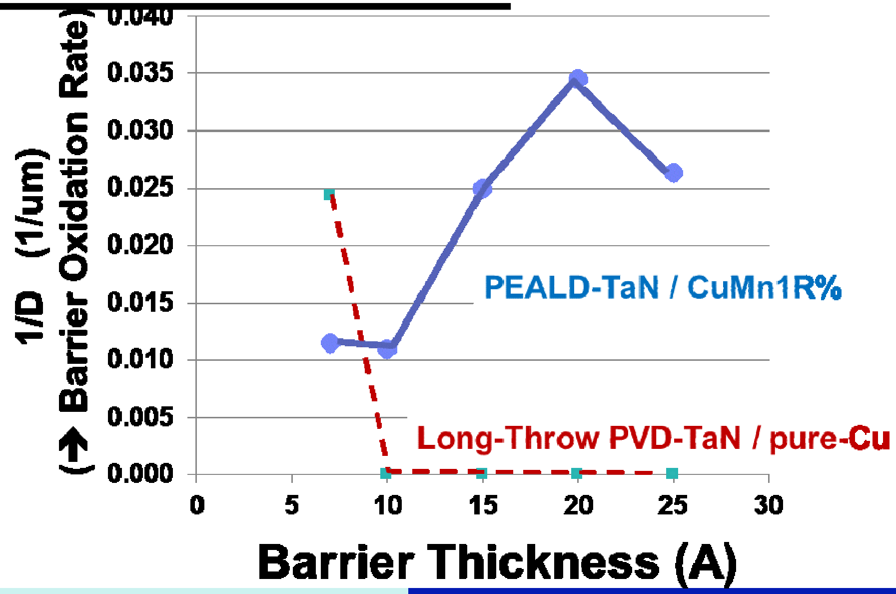
M. Lane, et al. Integ. Rel. 2002 IBM





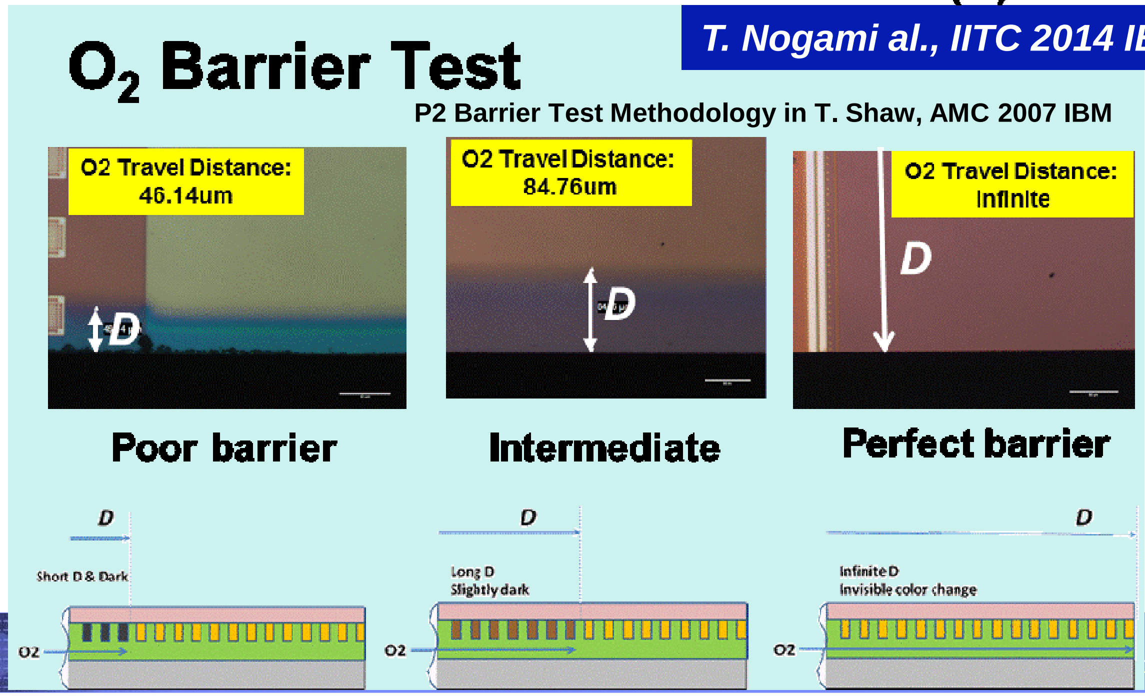
Trench Sidewall O_2 Barrier Performance





T. Nogami al., IITC 2014 IBM

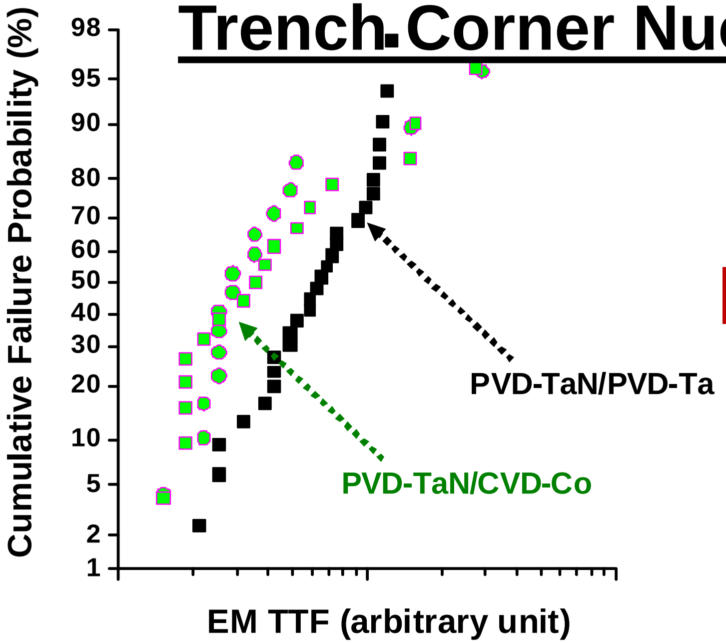
Correlation between barrier oxidation and EM

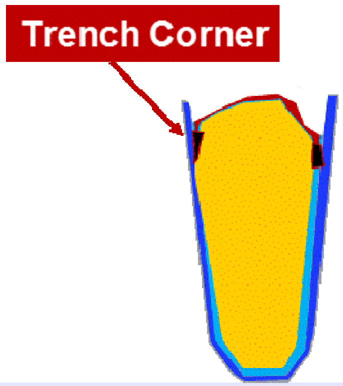


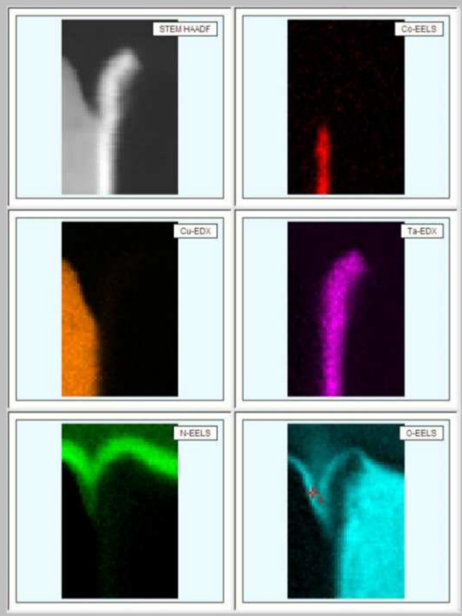
Fundamental-4

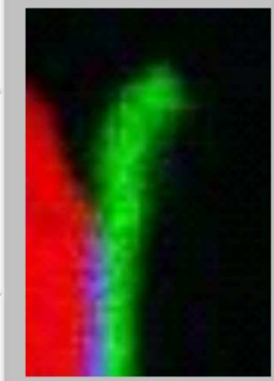
Electromigration

Trench Corner Nucleation Site



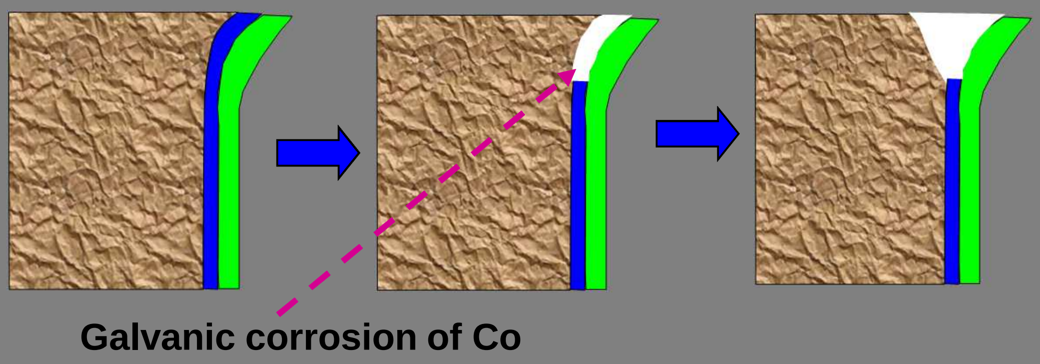


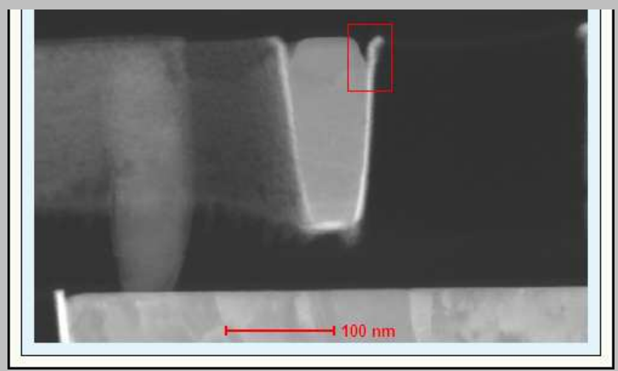




Poorer EM with CVD-Co and Suspected Cause – Slit Void Formation due to Galvanic Corrosion.

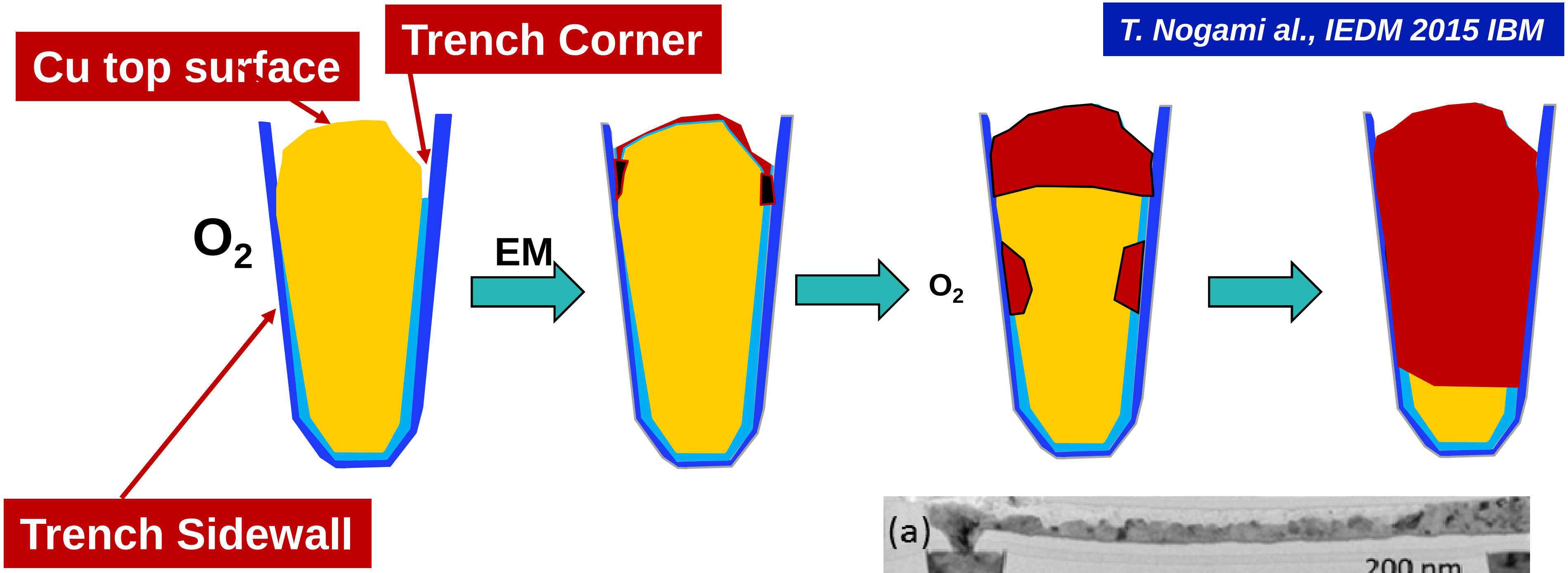
T. Nogami al., IITC 2010 IBM

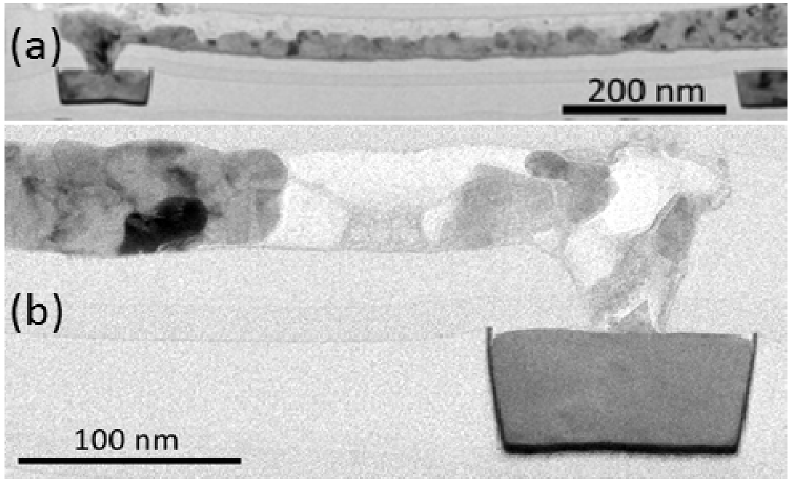




EM Void Nucleation Site and Fast Diffusion Path

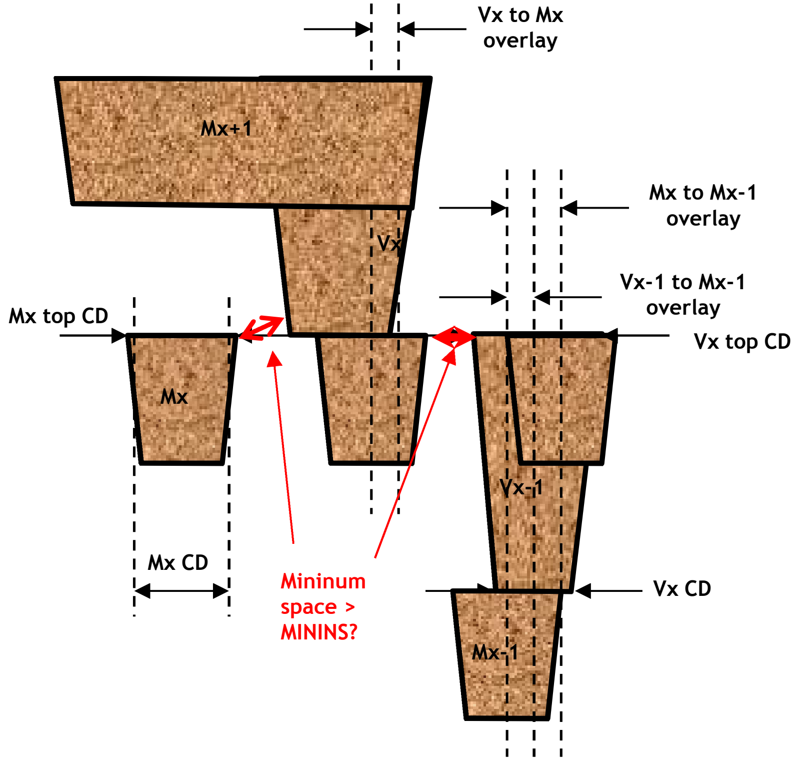
T. Nogami al., IEDM 2015 IBM

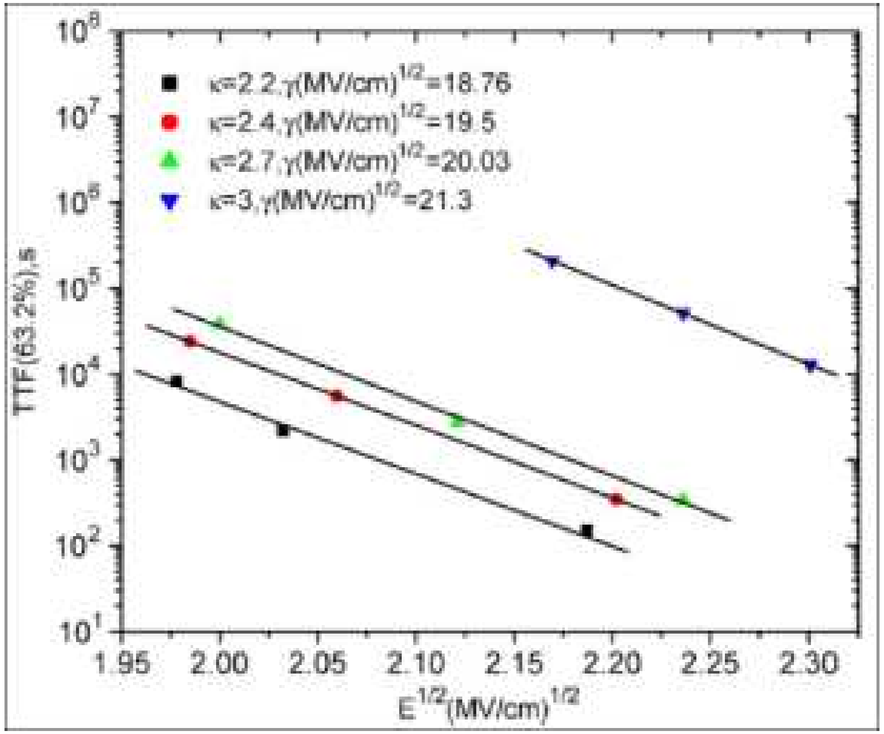




#1 Cu top surface
#2 Trench corner
#3 Trench sidewall/bottom

Fundamental-5 TDDB





R. Achanta et al, IEEE Trans. Dev. & Mat. Rel. 2011

The major diffusion path is the low-k/cap-dielectric interface. TDDB is affected by spacing, low-k dielectric materials, CVD-Ru wetting layer, CMP process, Sel-Co cap, etc.

TDDB

Lifetime Prediction Model

E. Liniger G. Bonilla et al, IRPS 2014 IBM

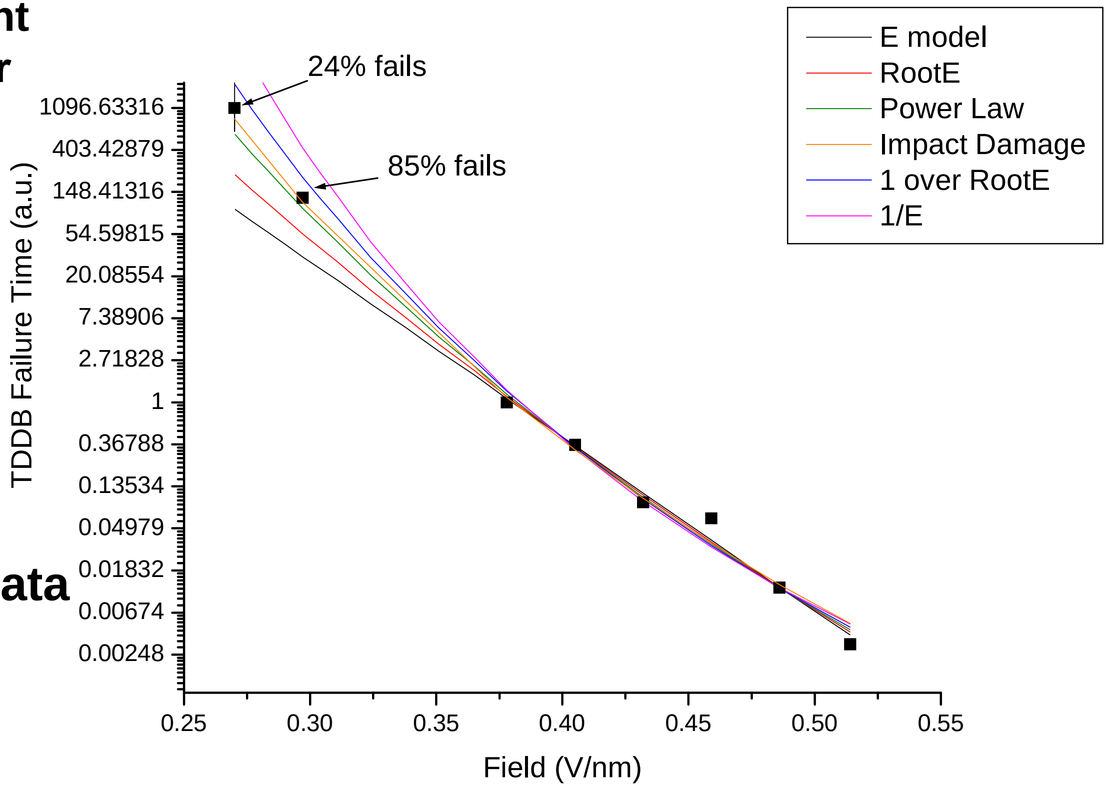
Root-E : $TBD = A_{RE} \exp(-\gamma_{RE} E^{1/2})$
➔
Power Law: $TBD = A_{PL} E^{-n}$

Cu ion drift playing an important secondary role in breakdown

hydrogen playing a critical role in defect creation

TBD: Time to breakdown
A: Pre-exponential constant
γ: Field acceleration factor
N: Power law exponent
E: Electric field

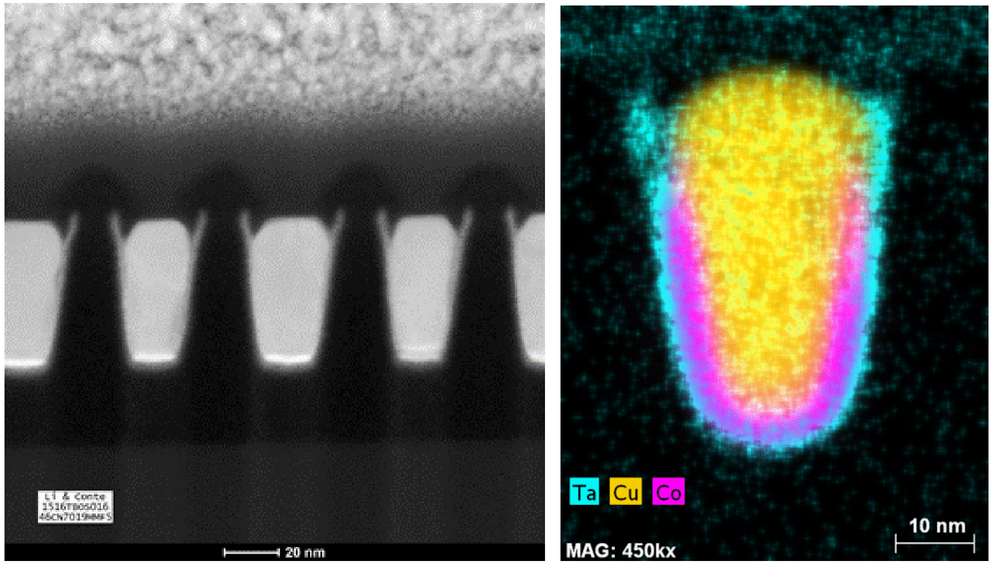
Low-field TDDB reliability data



Root-E model is overly conservative.

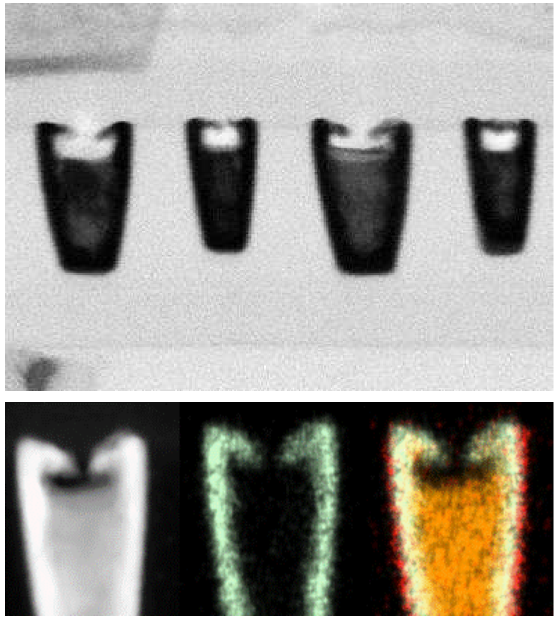
CMP issues of Co and Ru wetting layers

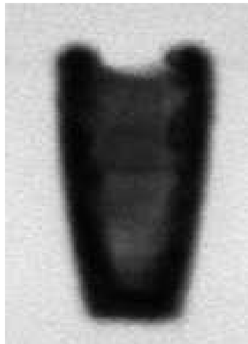
Co CMP Divot



T. Nogami IITC 2013 IBM

Ru CMP Cu-recess





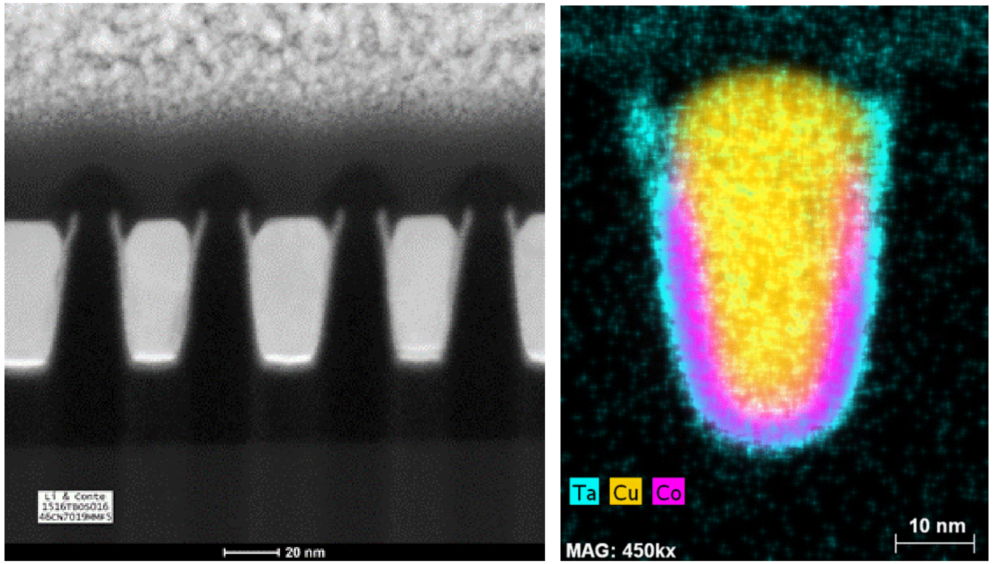
R. Patlolla et al., ICPT 2015 IBM

1. Co liner is lost along the sidewall, being followed by Cu divot formation.
2. Cu shows faster dissolution in the presence of Ru which results in Cu recess.

Cu Gap Fill

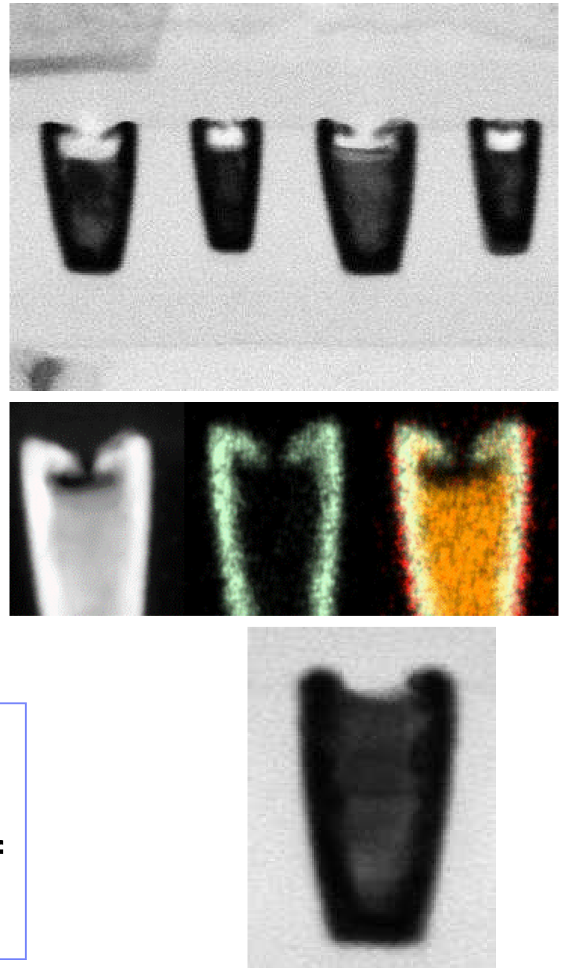
CMP issues of Co and Ru wetting layers

Co CMP Divot



T. Nogami IITC 2013 IBM

Ru CMP Cu-recess



R. Patlolla et al., ICPT 2015 IBM

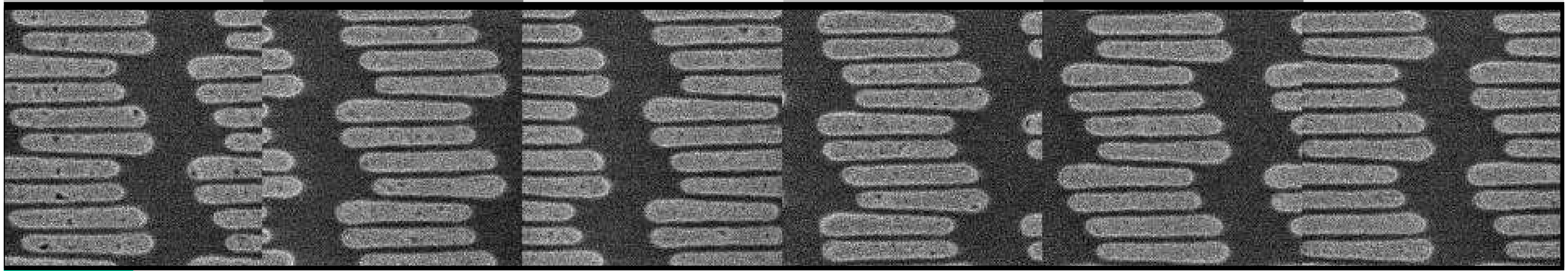
1. Co liner is lost along the sidewall, being followed by Cu divot formation.
2. Cu shows faster dissolution in the presence of Ru which results in Cu recess.

Cu Gap Fill

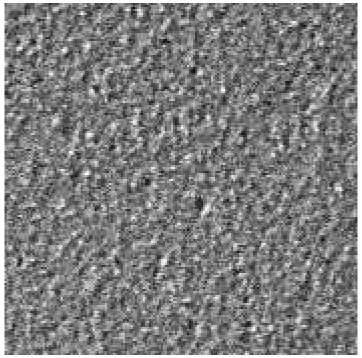
Post CMP Cu Fill Improvement with Cu Chemistry

- **PVD TaN/Co/Cu**

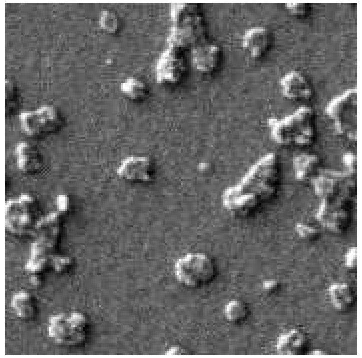
Baseline chemistry			Modified chemistry		
Waveform 1	Waveform 2	Waveform 3	Waveform 1	Waveform 2	Waveform 3



center



4nm plated Cu on PVD Cu/Co (with 20nm Cu underlayer)

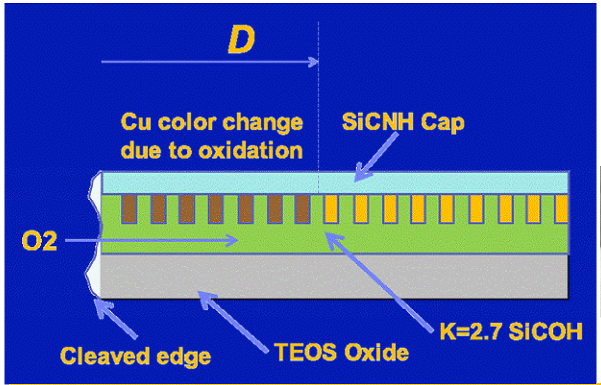


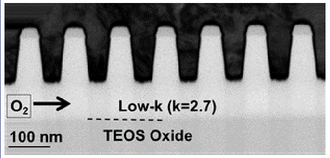
4nm plated Cu on PVD Cu/Ta (with 20nm Cu underlayer)

J. Kelly et al., ECS 2013 IBM

Diffusion Barrier Test

O_2 Barrier Test

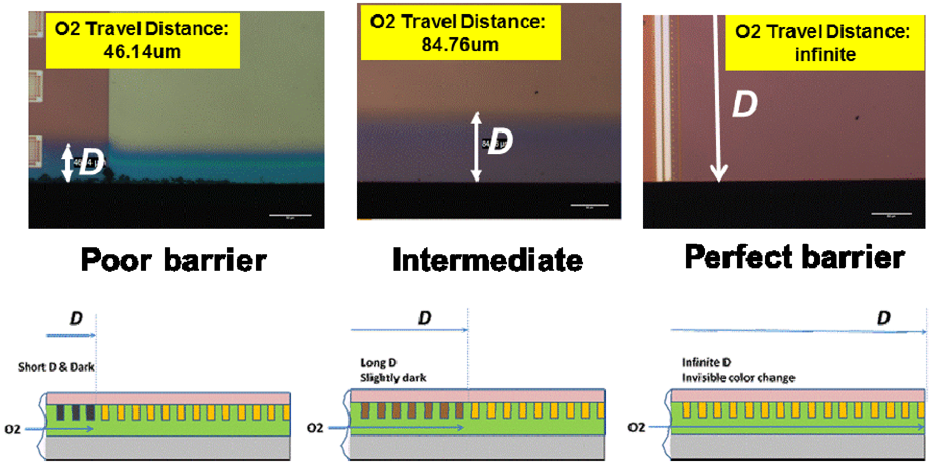




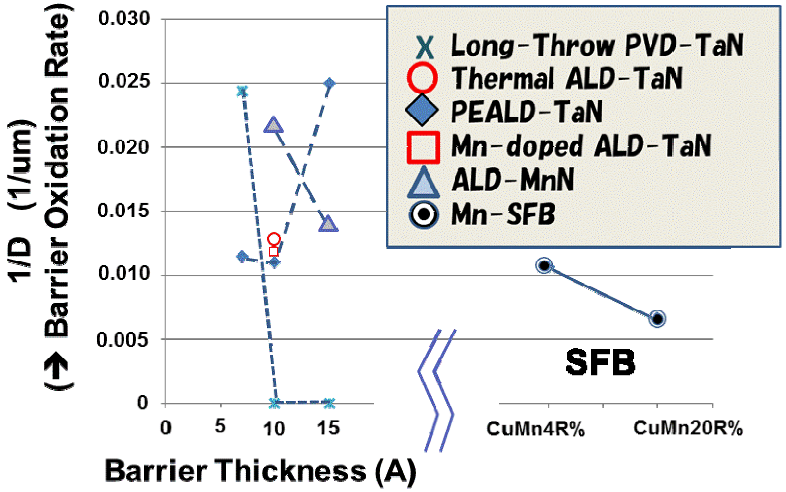
Oxidation results from two competing processes of
(1) O_2 diffusion through the material and
(2) O_2 consumption by barrier/Cu reaction.

O2 Barrier Test Methodology by T. Shaw, AMC 2007 IBM

O_2 Barrier Test



O_2 Barrier of Alternative Barriers



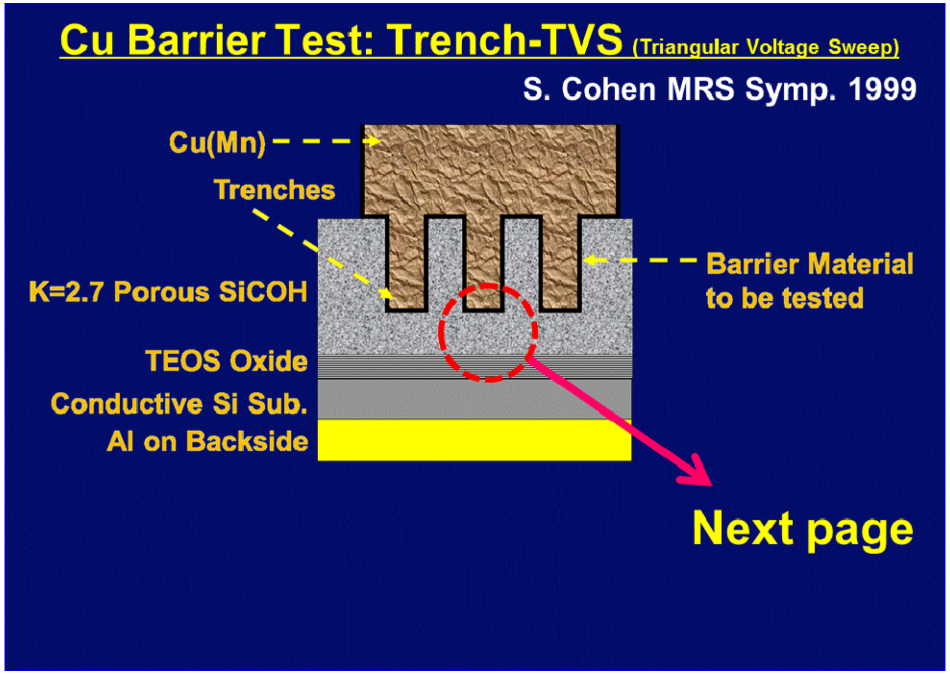
All alternative barriers showed imperfect O_2 Barrier.

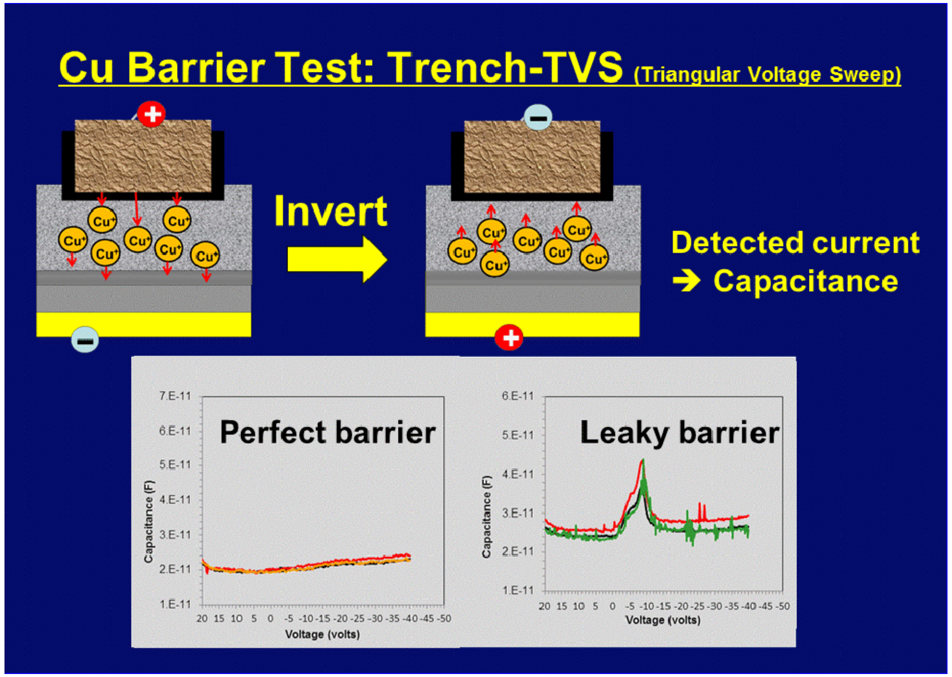
Diffusion barrier needs to work as a diffusion barrier to oxygen, not just as a diffusion barrier to copper. Conventional PVD-TaN and alternative barrier metal candidates are examined in the O_2 barrier test.

T. Nogami al., IITC 2014 IBM

Diffusion Barrier Test

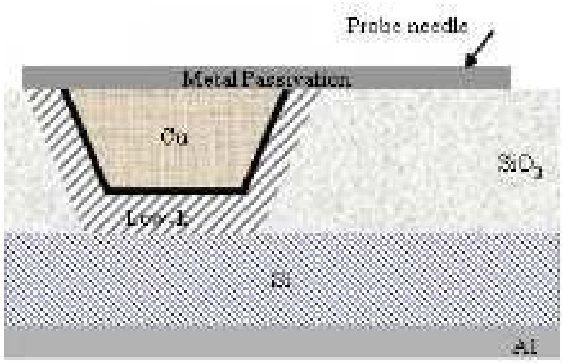
Cu ion diffusion





barrier performance in geometry close to actual

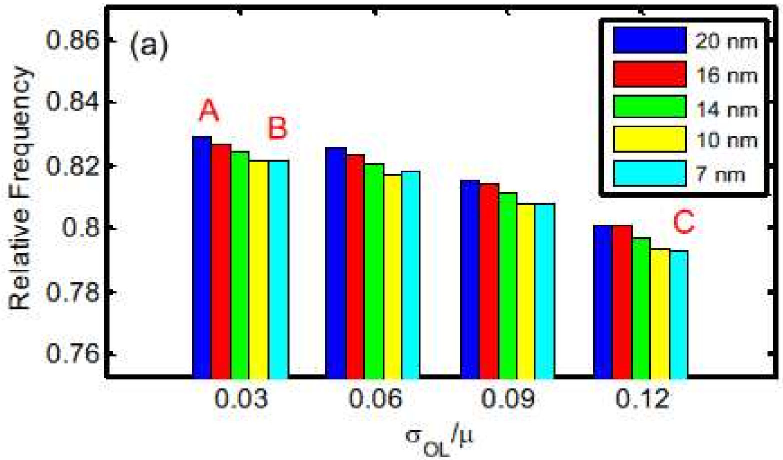
T. Nogami al., IITC 2014 IBM



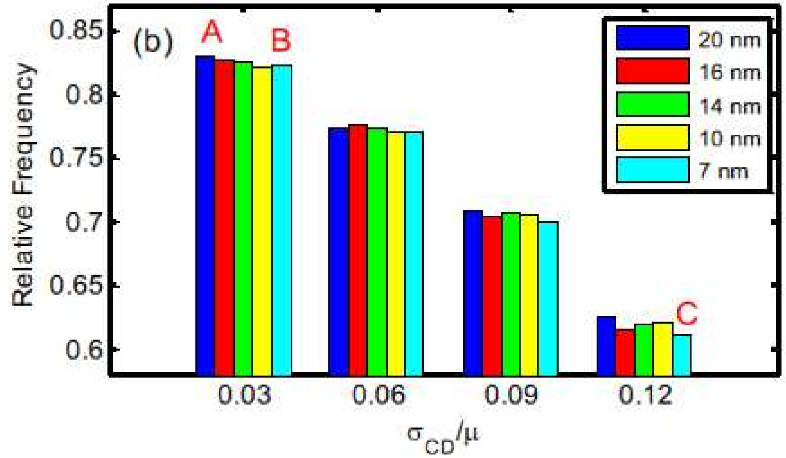
Intrinsic barrier performance

L. Zhao al., IITC 2011 Intel

RC variation impact on circuit performance

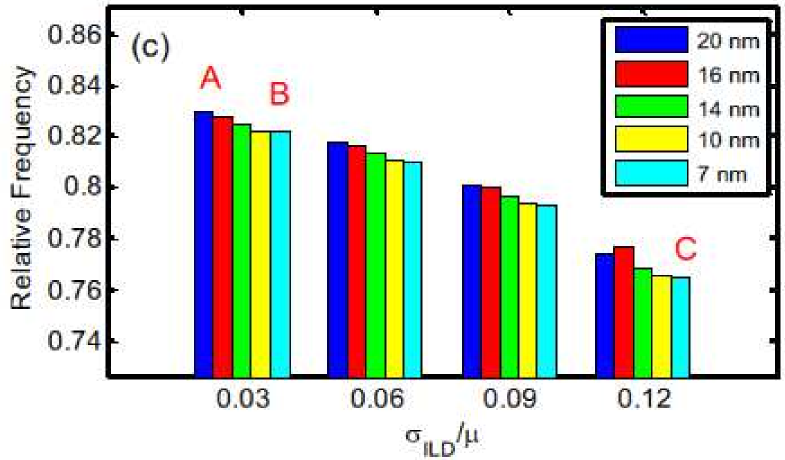


Overlay variation



CD variation

C. Pan, A. Naeem et al, IITC, 2014, Intel

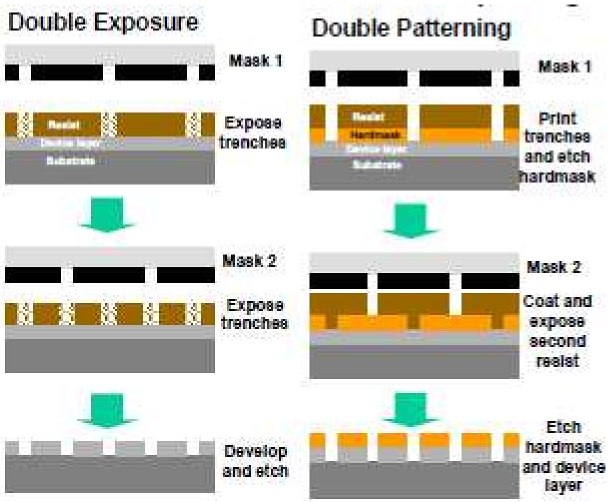


ILT variation

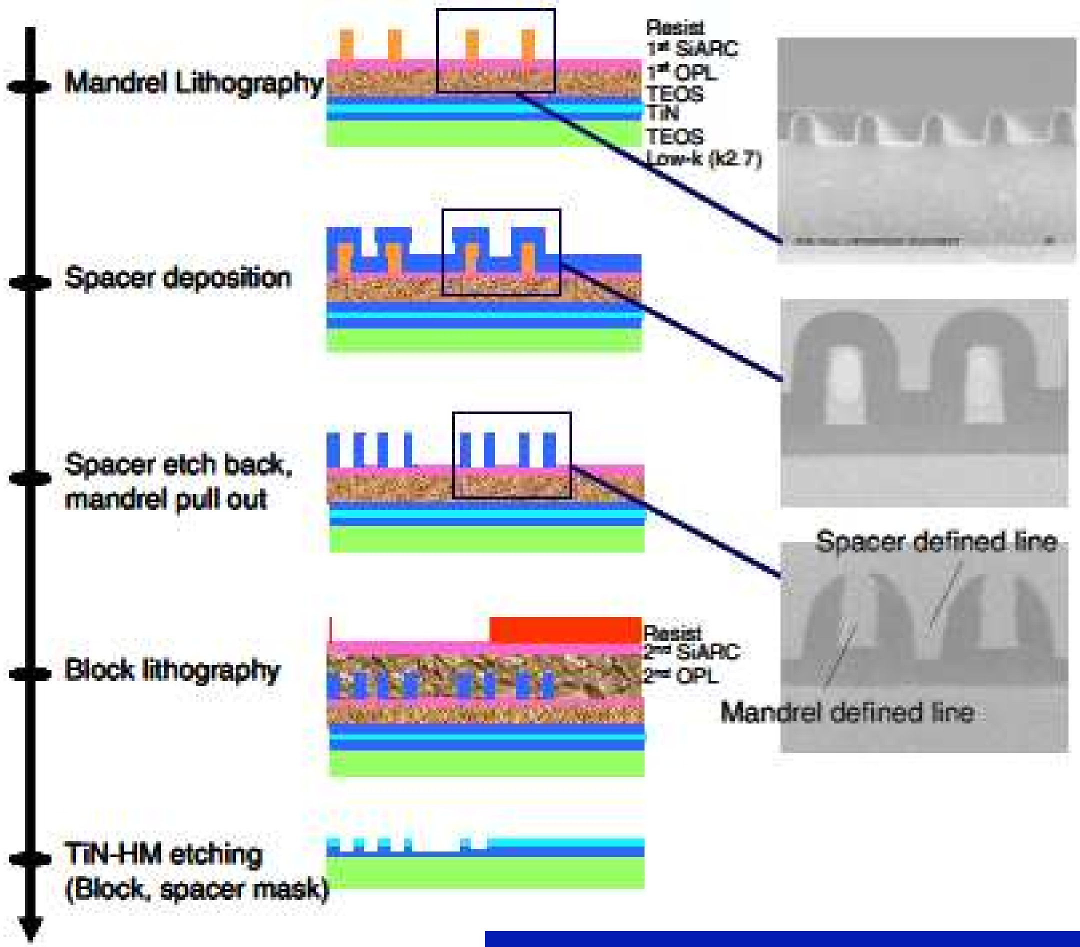
Interconnect variation comes from lithography, alignment, etching, polishing, and orientation

RC variation by multiple patterning

Pitch Splits (LELE…)



Sidewall Image Transfer

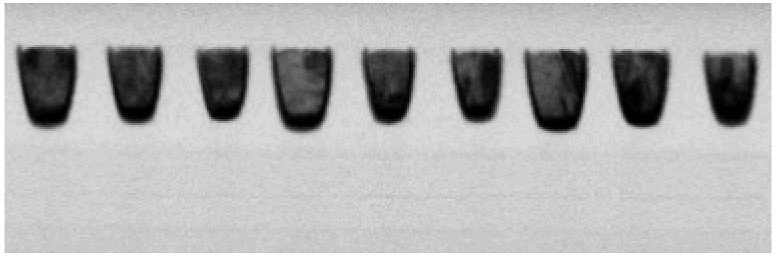


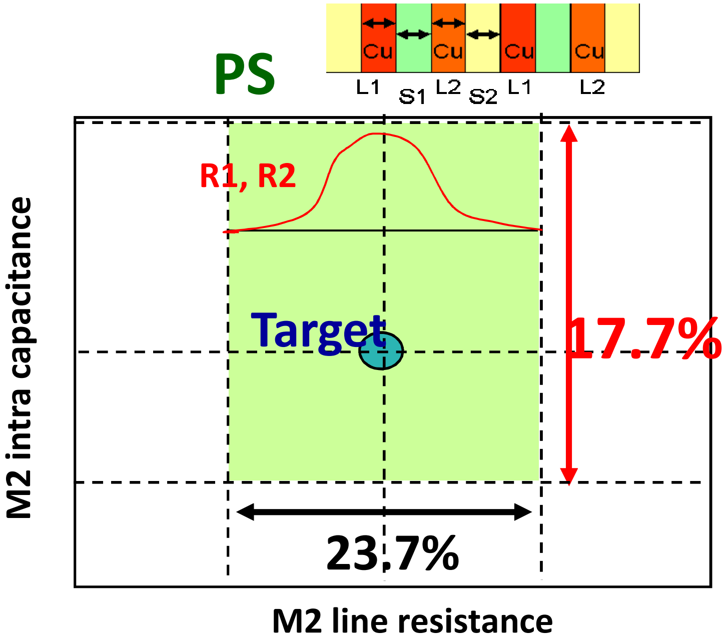
Interconnect variation comes from lithography, alignment, etching, polishing, and orientation

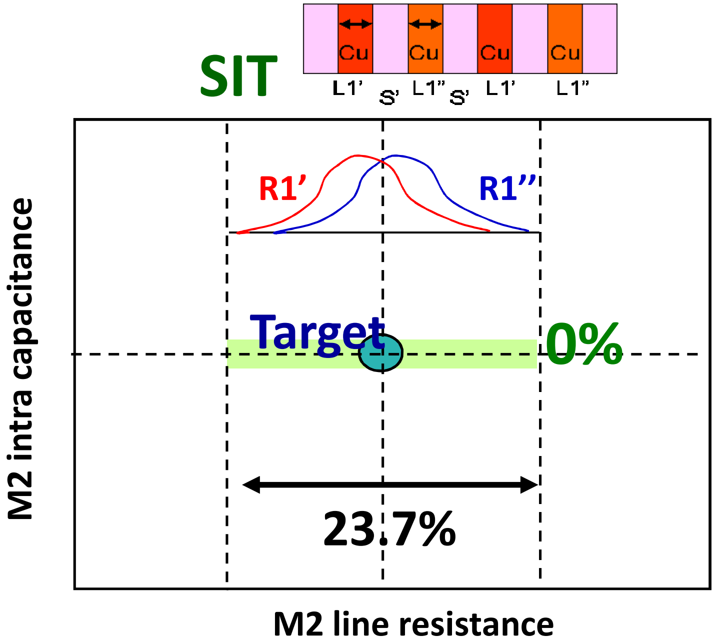
M. Tagami et al, IITC, 2012, IBM

RC variation by multiple patterning

- **Illustration of line dimension (width, height) with multiple patterning (LEx)**



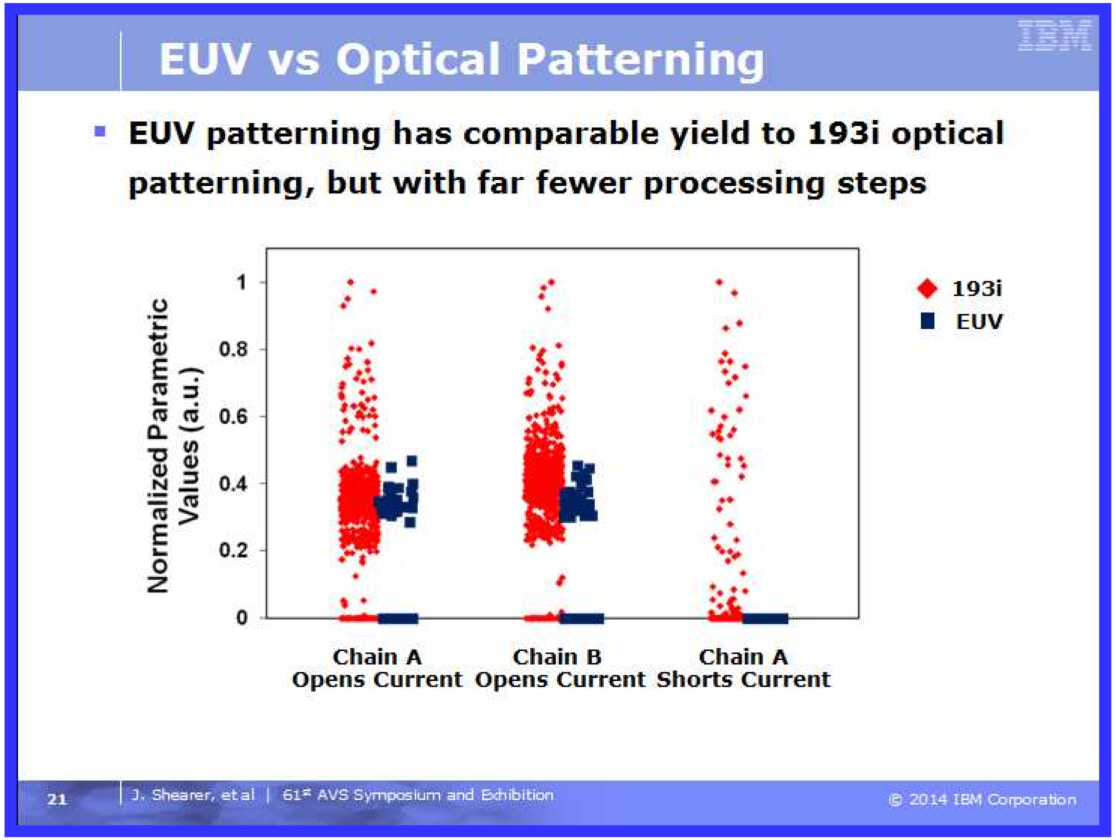


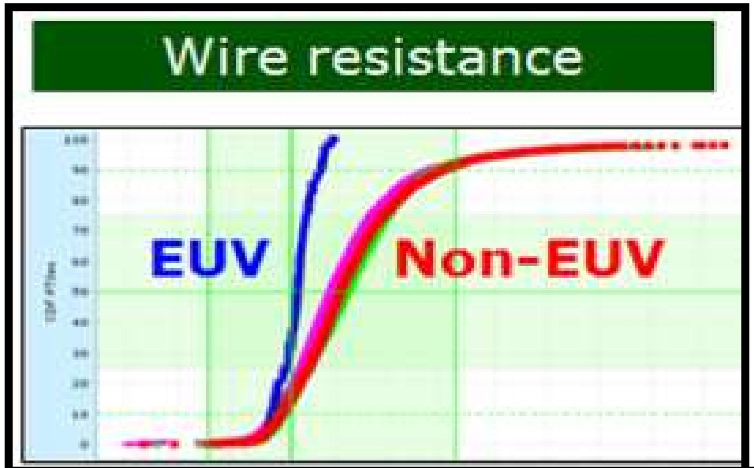


M. Tagami et al, IITC, 2012 IBM

RC variation

Performance Improvement for BEOL Resistance Due to EUV





EUV 10nm single exposure wires have tighter R distribution than 2x-patterning
(J. Shearer et al, AVS 2014)

10NM wafers with single exposure EUV have tighter distribution than with multiple patterning.

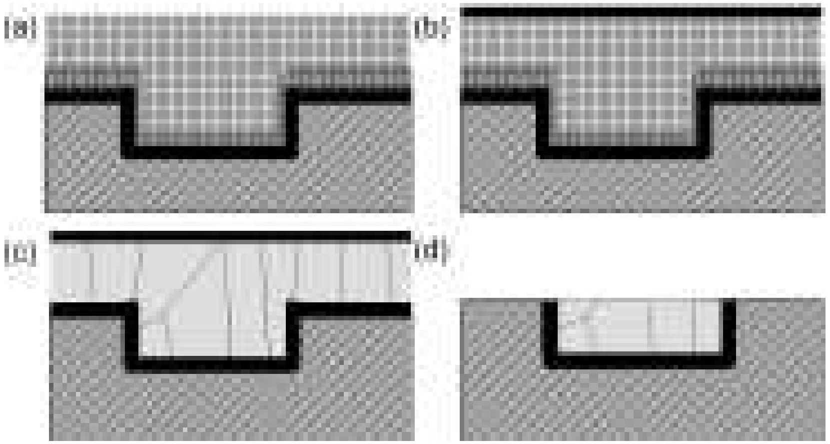
Improved variability observed for line and via resistance compared to multiple patterning 193 approaches

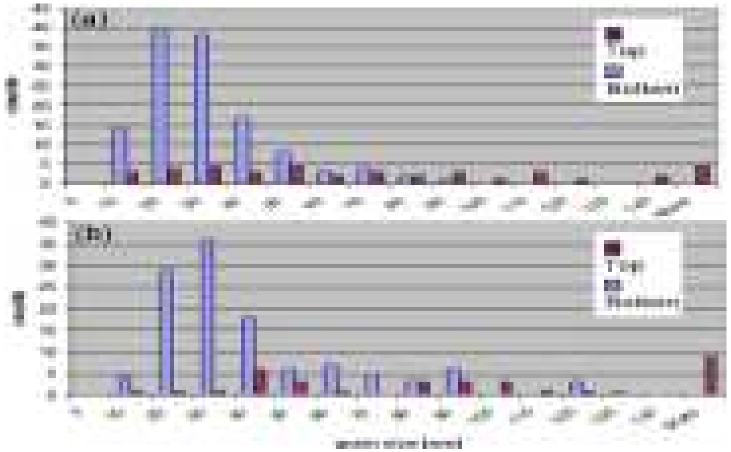
OUTLINE

1. **Technology Scaling and BEOL**
2. **BEOL Challenges**
   - ❖ **Tradeoff's**
3. **Potential Solutions**
   - ❖ **Fundamentals**
   - ❖ **Common Approaches**
     1. **Stress-liner capped anneal for Line R**
     2. **Tall metal for Line R**
     3. **Self Forming Barrier for Line R**
     4. **Lower-k integration and air gap for C**
     5. **Selective Co cap for EM**
     6. **Cu alloys for EM**
     7. **CVD-Co, Ru for Cu gap fill**
   - ❖ **Innovative Approaches**
4. **Summary**

Line Resistance

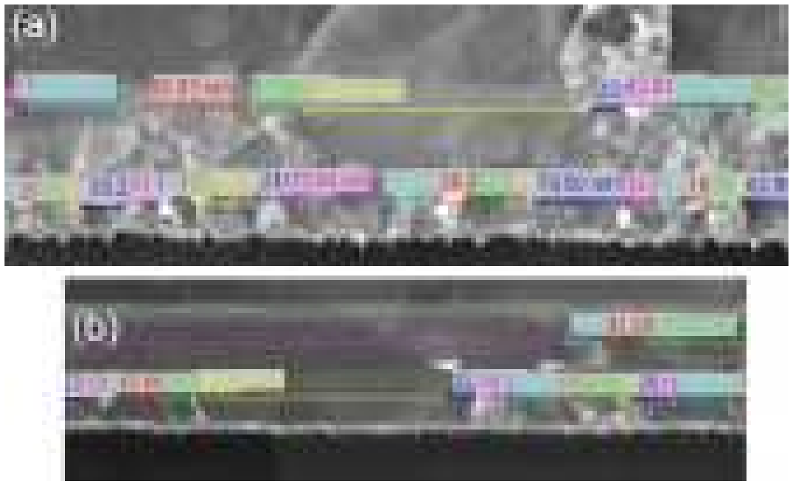
Thermal stress control in Cu Interconnects





100C

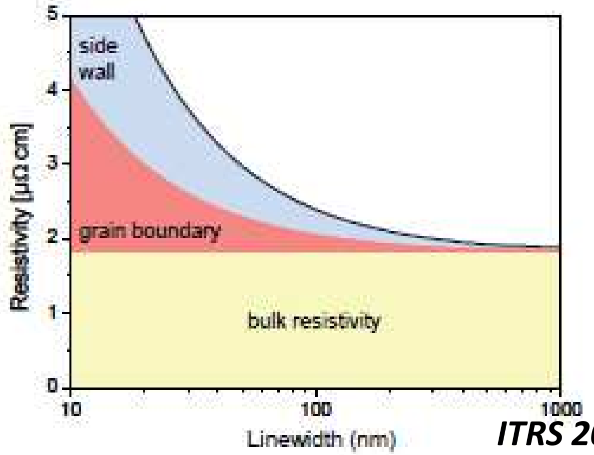
250C



100C

250C

CC Yang et. al, IITC 2014 IBM

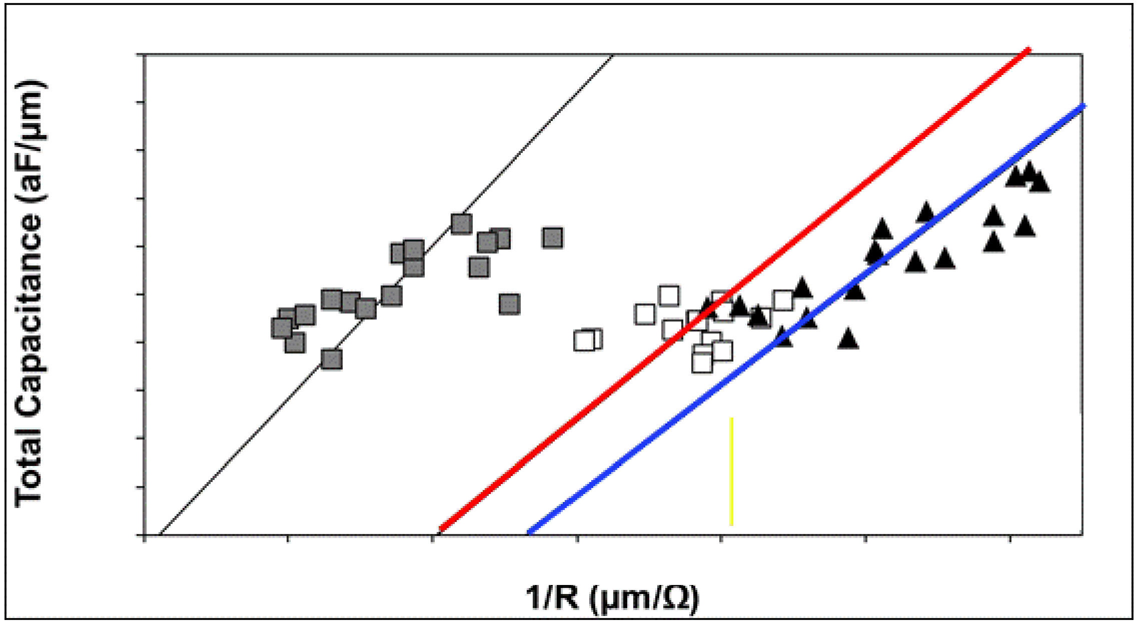


ITRS 2007

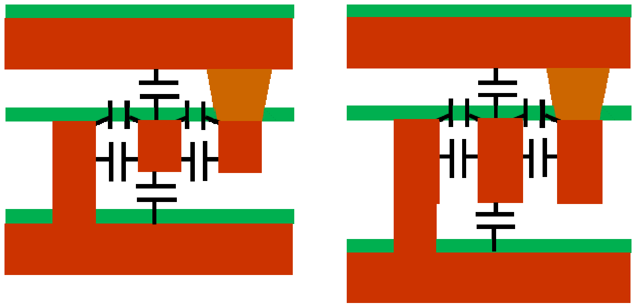
TaN stress-liner on top of plated Cu enables higher temperature post-plating anneal to lead to larger grains and lower Cu resistivity.

Line Resistance

Tall Metal (High Aspect Ratio Metal)



Line Height 10.3% up
RC dropped by 9.3%

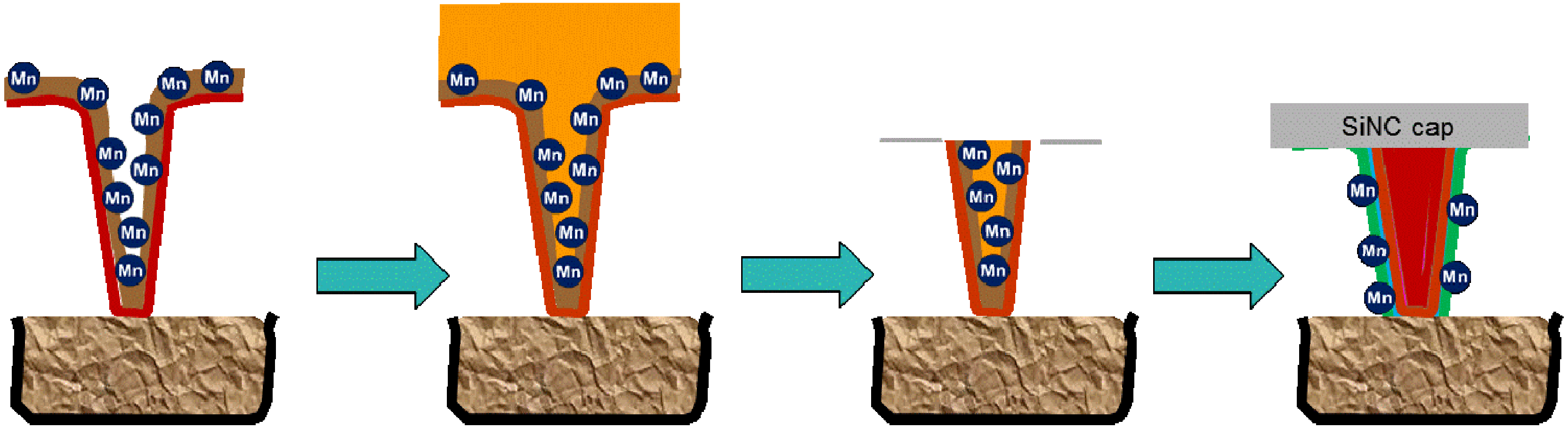


Fringing C

R decreases with metal height, while C does not increase as much because of fringing C contribution.

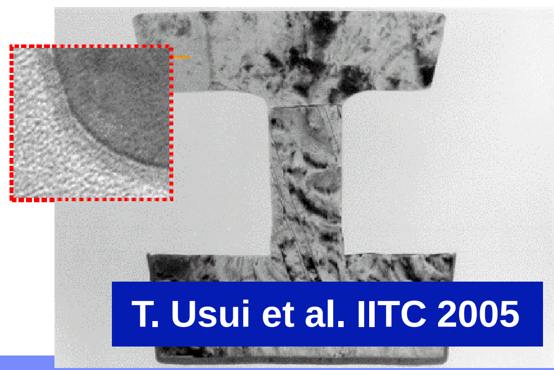
1. **Contribution of cap material is significant**
2. **In other words, taller metal does not impact C proportionally and is advantageous for RC.**

Conventional Self-Forming Barrier



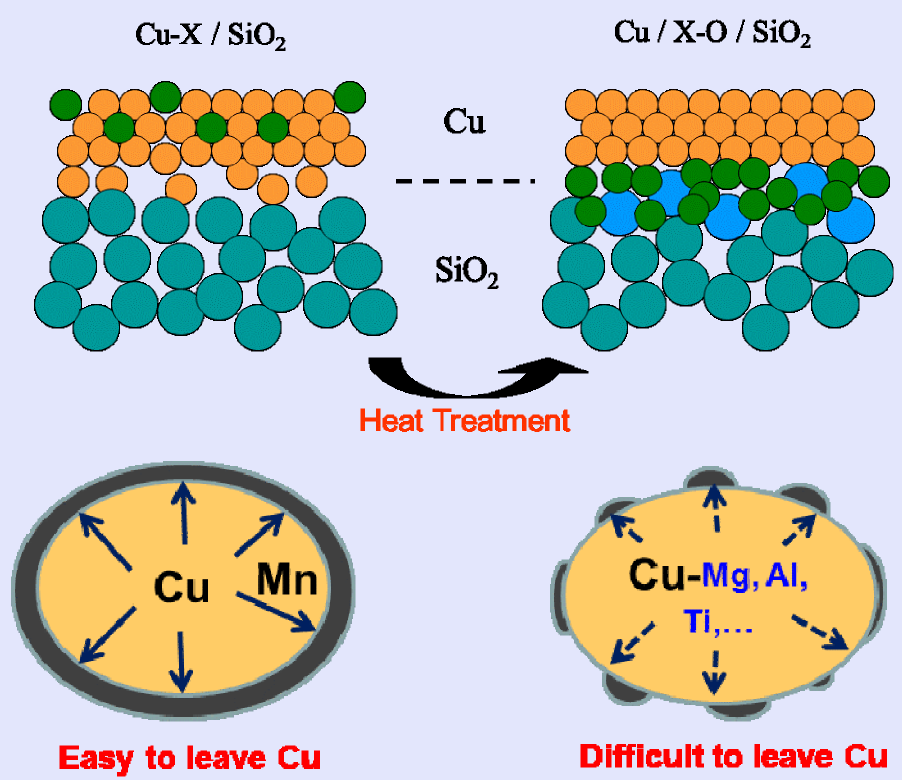
CuMn-seed → **Cu Plating & ppA** → **CMP** → **$MnSiO_3$ SFB Formation**

TEOS Oxide

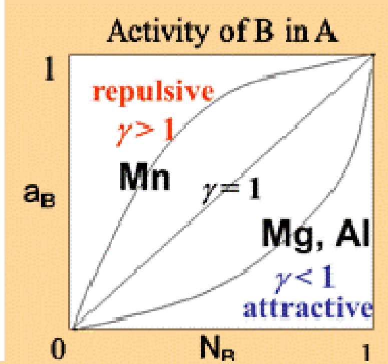


Line Resistance

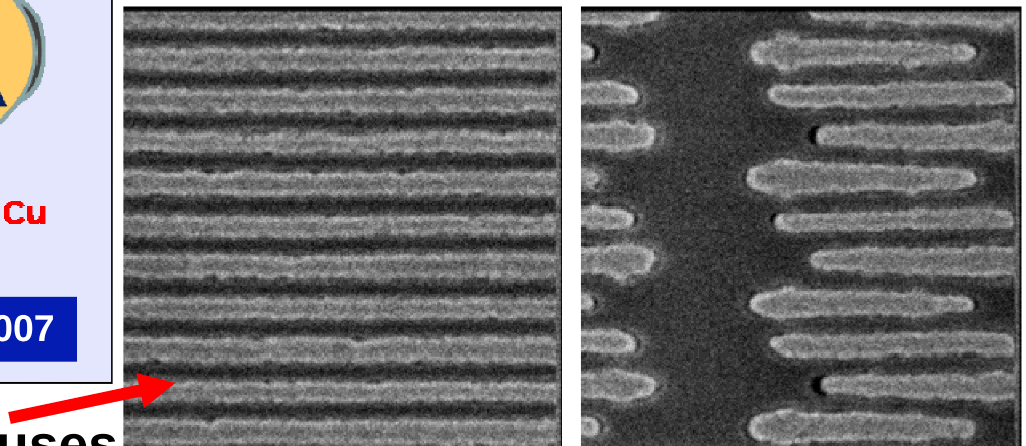
Self-forming barrier (SFB)



J. Koike AMC 2007



Activity $a_i = \gamma_i N_i$



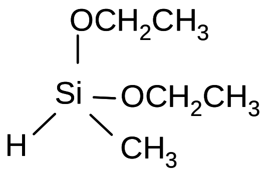
However, CMP in SFB process causes voiding and delamination when it was integrated with ultra low-k.

T. Nogami et al., IEDM 2015 IBM

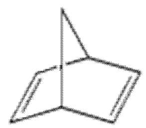
Capacitance

Dielectric (LK, ULK) materials

Precursor (A) + BCHD



DEMS



BCHD

v1
(k=2.55, 13%

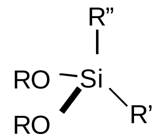
v1.0
(k = 2.4, 17%C)

v1.3
(k = 2.2, 19%C)

Plasma

Single Precursor (BCHD optional)

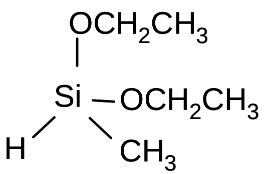
For example,



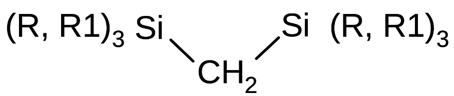
R" = porogen

Plasma

Precursor (A) + Precursor (B) + BCHD



DEMS



Carbosilane 2
CS-2

V2c
(k=2.55, 21%C

v2b
(k = 2.4, 27%C)

v2.1
(k = 2.2, 35%C)

US 7,202,563 B2 S. Nguyen, T. Nogami 2006, IBM

G. Dubois et al., Adv. Mat 2007, IBM

Plasma

Composite Film

Porogen Removal (UV cure)

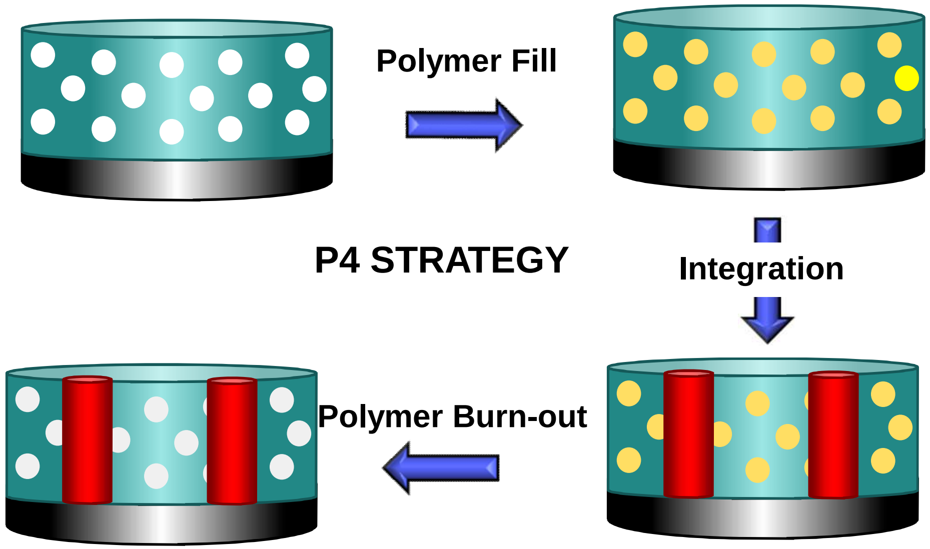
Nanoporous Film with variable carbon content

E.T. Ryan, et al. AMC 2011

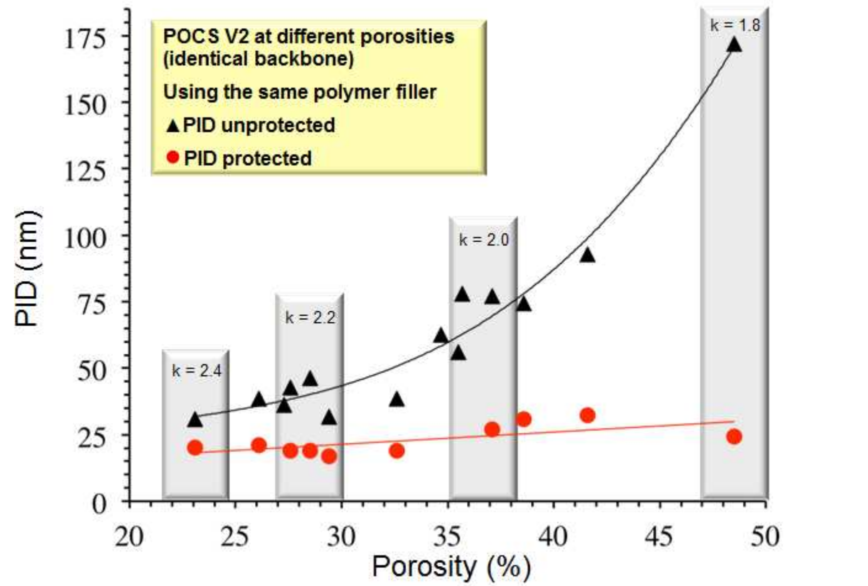
- **Tune ULK film composition and properties using chemistry, plasma conditions, and curing conditions.**

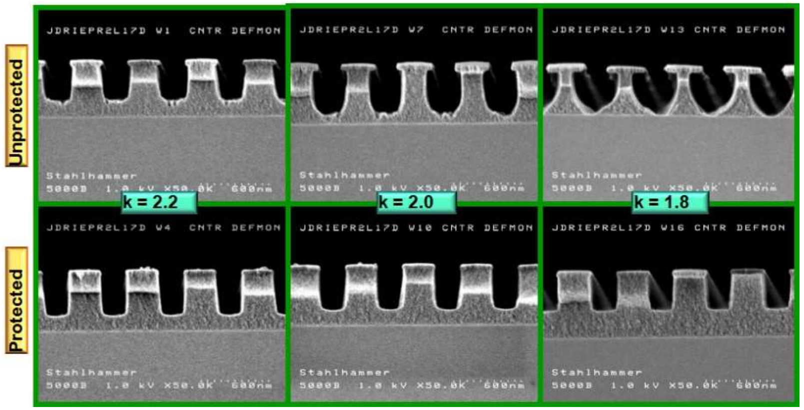
Capacitance

Post Porosity Plasma Protection (P4) to reduce PID



T. Frot, G. Dubois, et al. Adv. Mat. 2011 IBM





PLASMA DAMAGE OF ULK REMAINS VIRTUALLY CONSTANT

US 8,314,005 , US 8,492,239, US 8,541,301
US 201300117682 A1, US 201300117688 A1, US 20130045608 A1

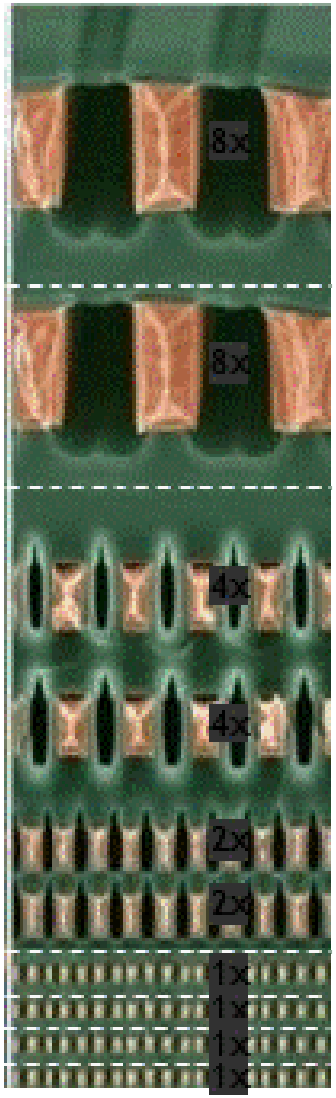
T. Frot et al, Adv. Mat. 2011, 23, 2828-2832.

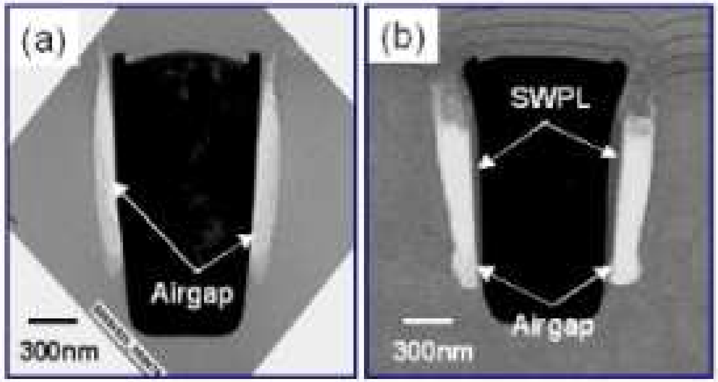
T. Frot et al, Adv. Funct. Mat. 2012, 14, 3043-3050.

- **Porefilling can reduce integrated k and improve device reliability by minimizing process damage to ULK and maintaining etch profile.**
- **Porefilling may enable lower k dielectric in future technology node.**

Capacitance

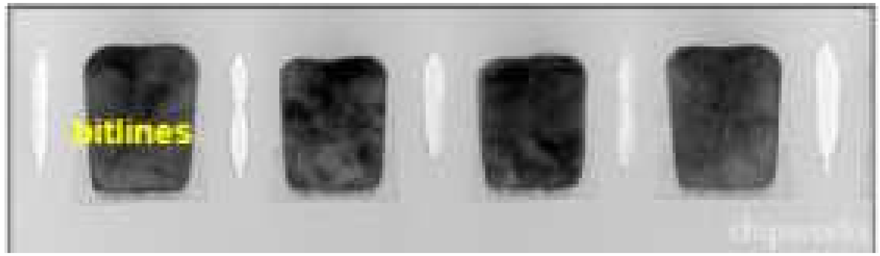
Airgap enables further C reduction





H-W Chen et al, IITC 2008 TSMC

Samsung 4 Gbit DDR3 SDRAM (26-nm)



Intel/Micron 64-Gbit Planar Flash (20-nm)

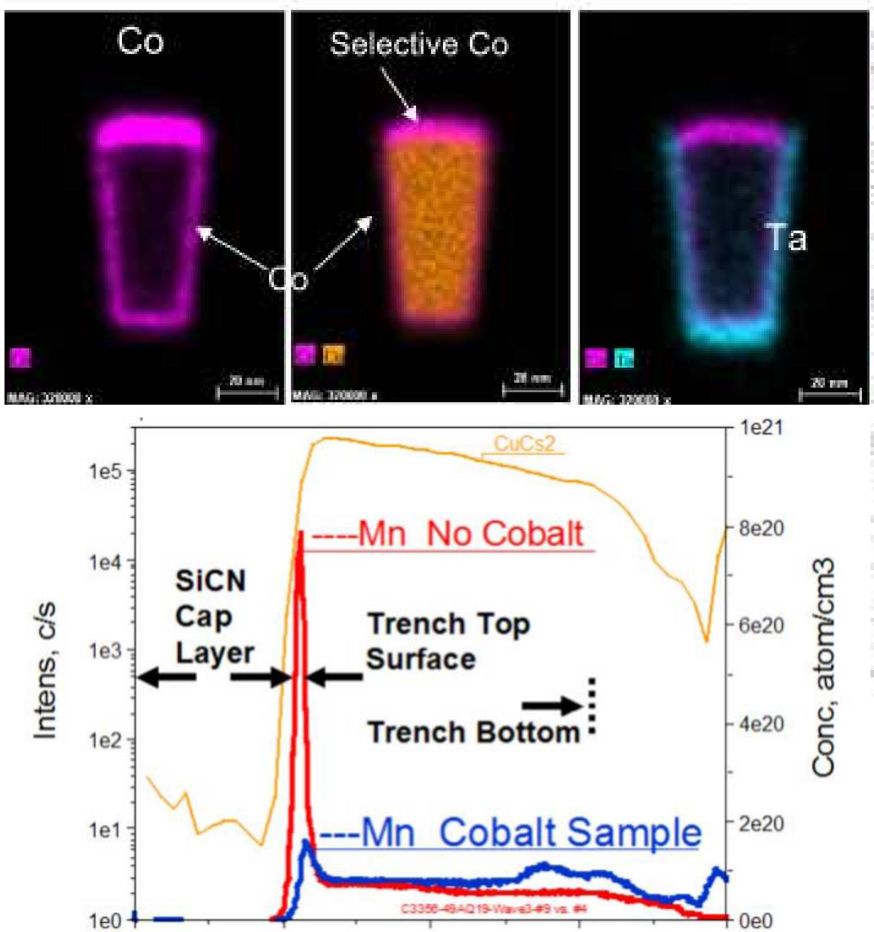
Source: D. James, CSTIC 2014.

D. Edelstein et al, AMC 2005, IBM

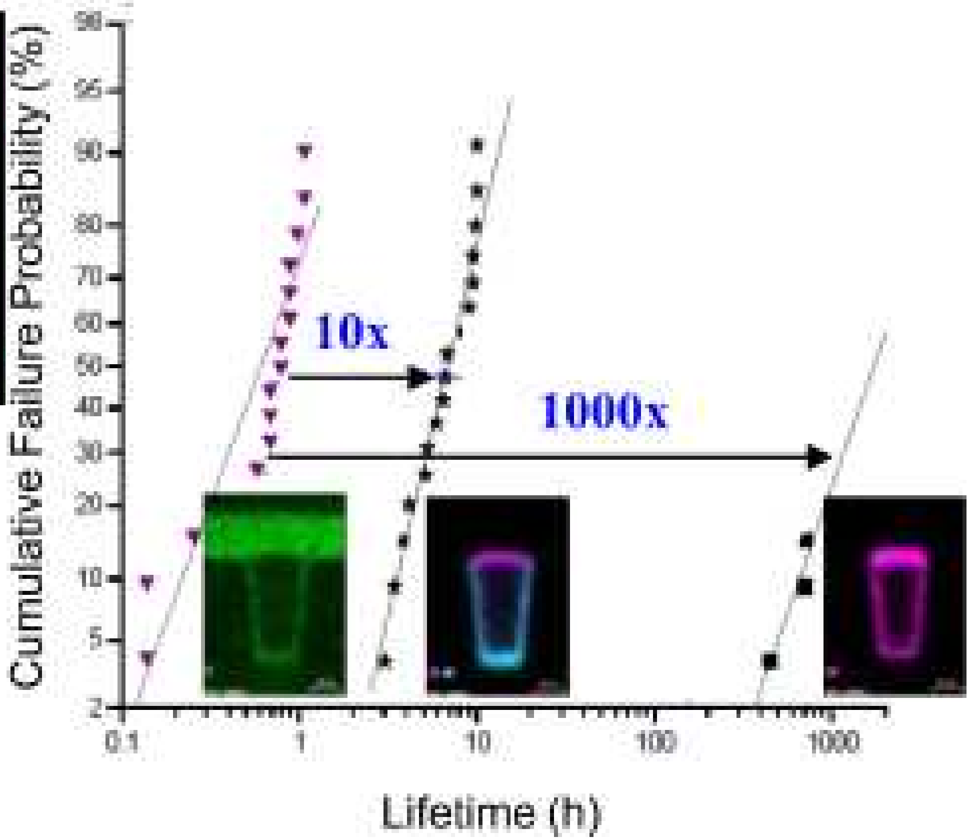
Significant capacitance reduction demonstrated with insertion of air gap.

Electromigration

Cu top surface (Selective Co Cap)



A. Simon et al, IRPS 2013 IBM

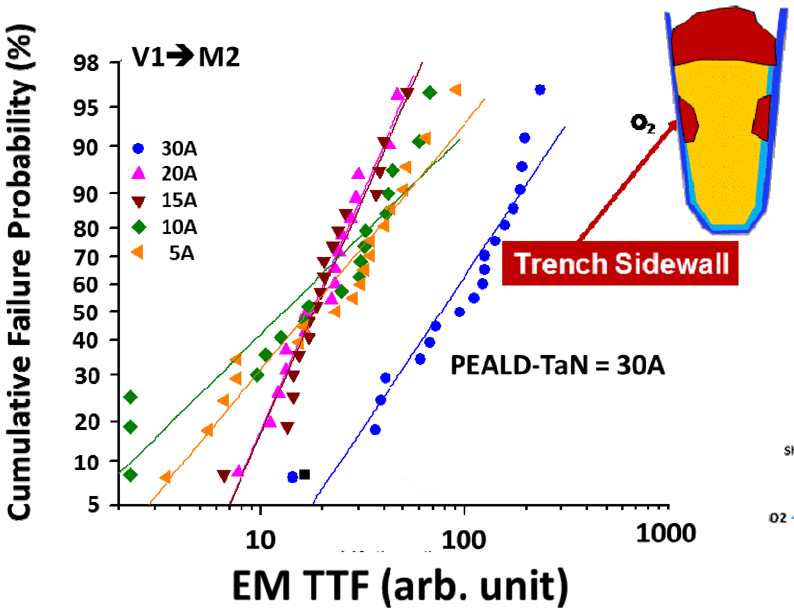


A. Grill et al, App. Phys. Rev,.2014 IBM

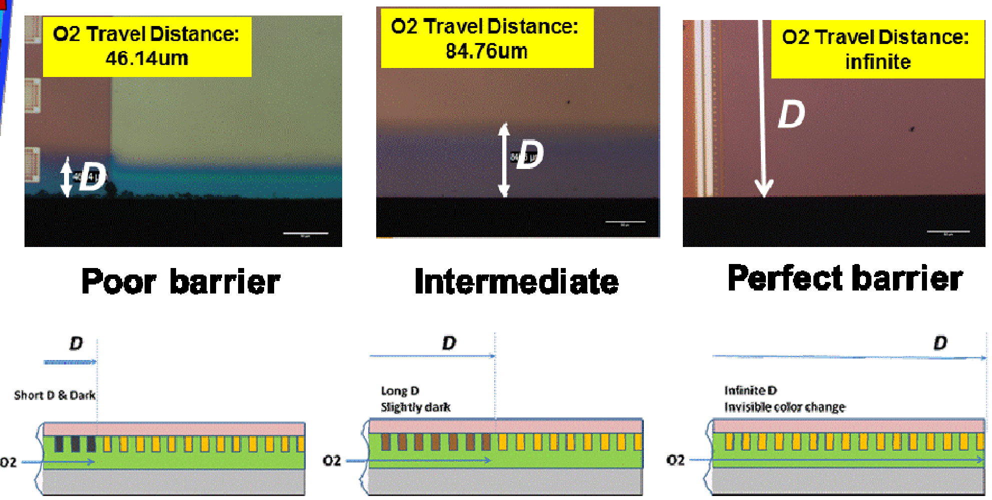
Metal/Cu interface has less EM void nucleation and less Cu diffusion. Selective CVD-Co, CVD-Ru and Selective electro-less CoWP have been proposed or used in production.

Electromigration

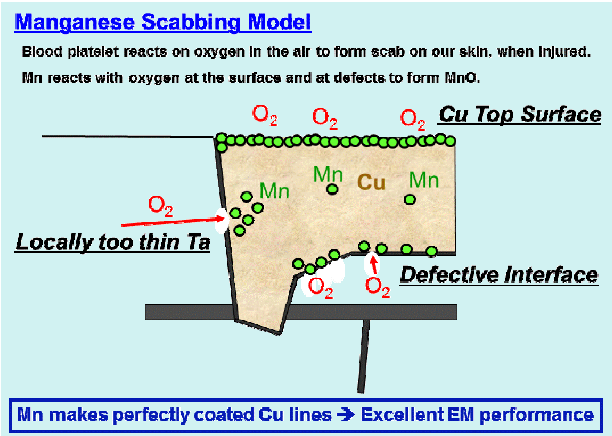
Trench Sidewall O_2 Barrier Performance

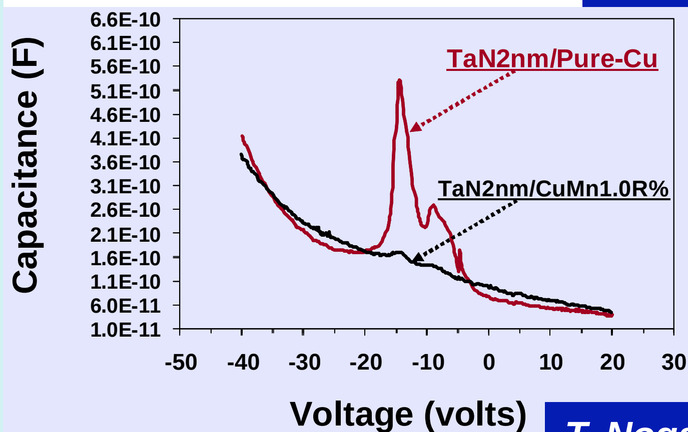


O_2 Barrier Test



T. Nogami al., IITC 2014 IBM



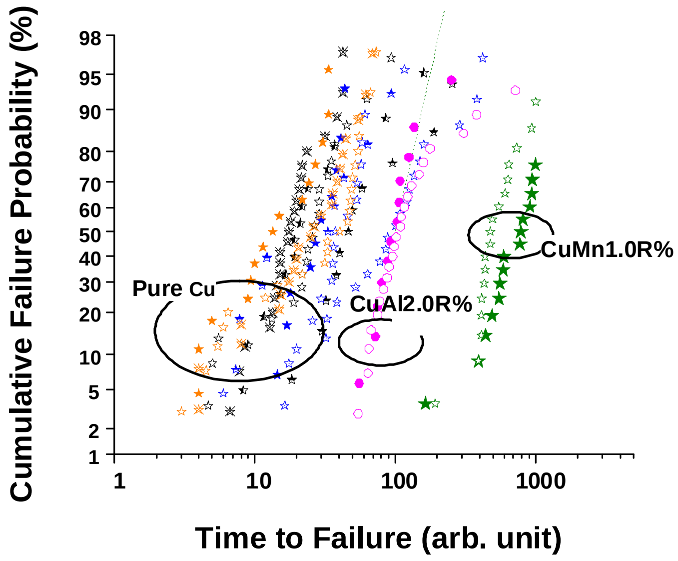


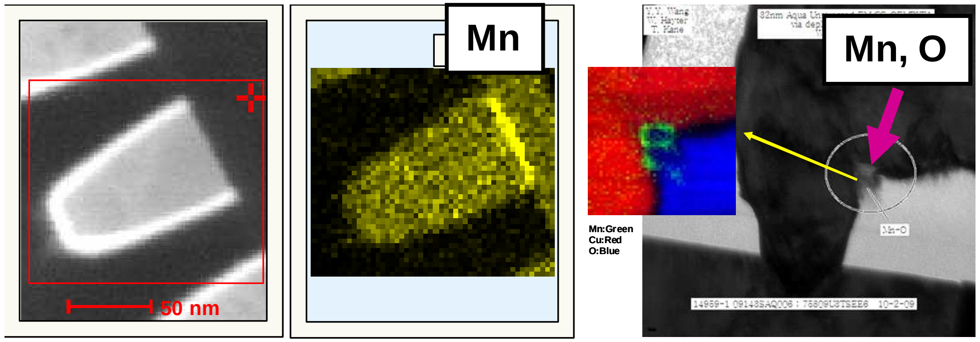
Mn scabbing

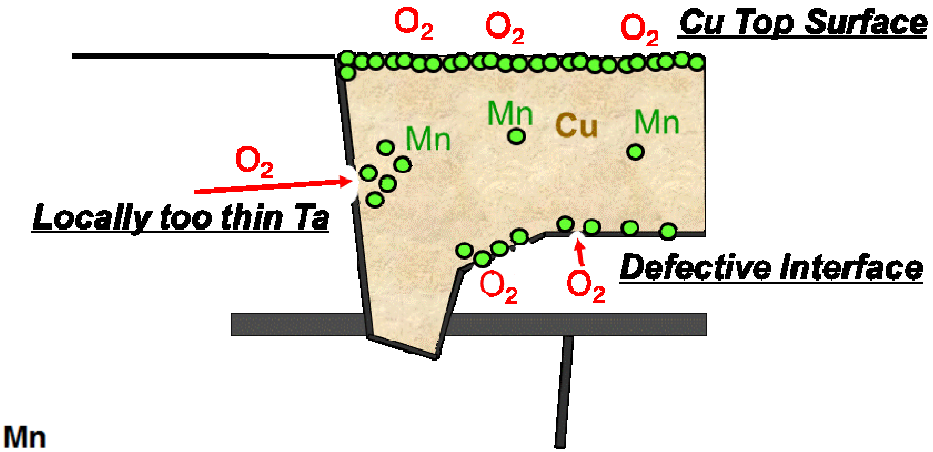
T. Nogami al., IEDM 2010 IBM

Electromigration

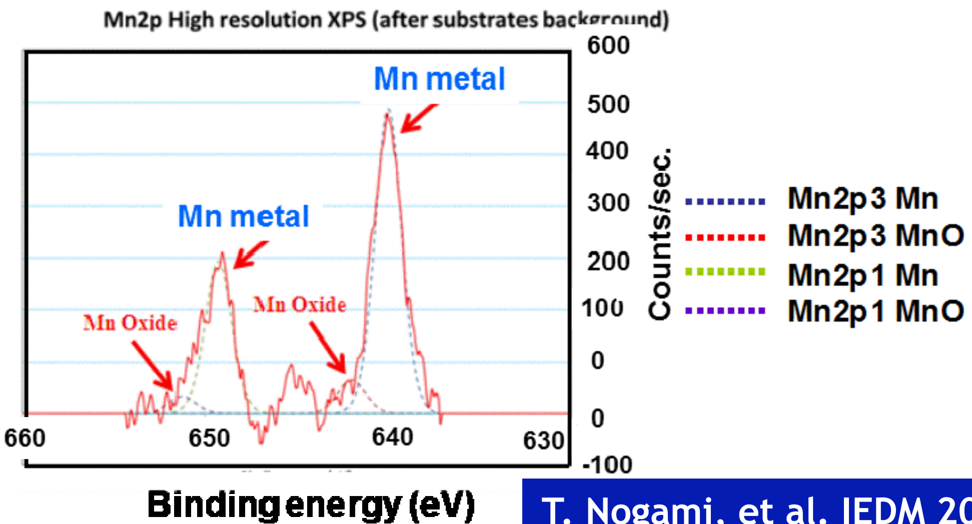
Cu Alloys (Mn, Al)







T. Nogami, et al. IEDM 2010 IBM

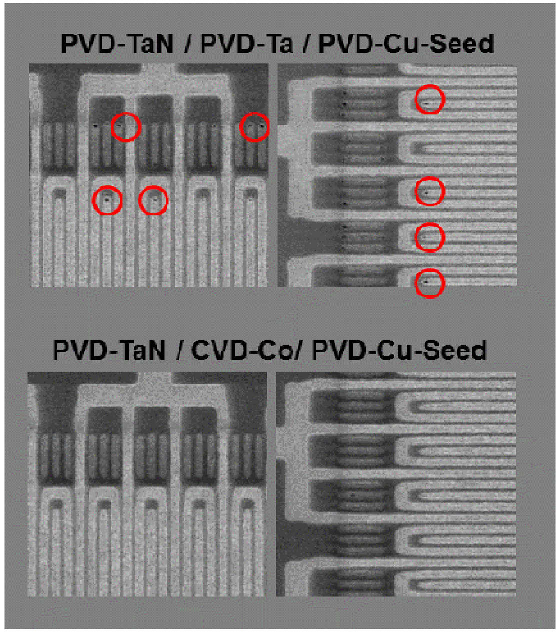


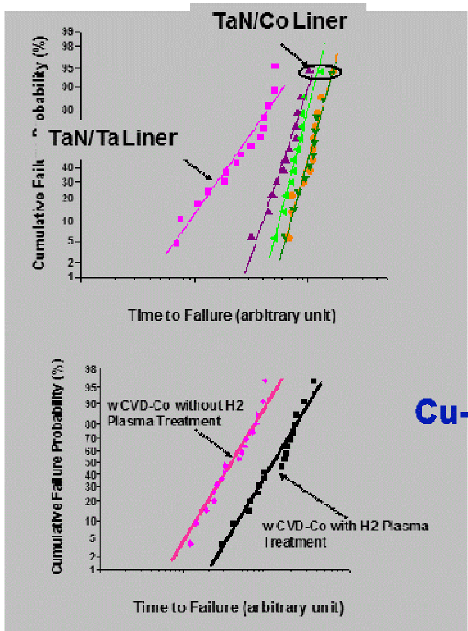
T. Nogami, et al. IEDM 2012 IBM

Cu Gap Fill

CVD-Co wetting layer

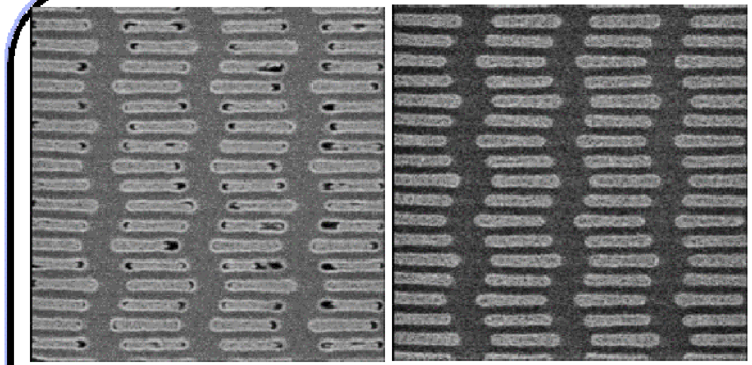
Gap Fill and EM Improvement in 22nm in k=2.4 SiCOH with CVD-Co





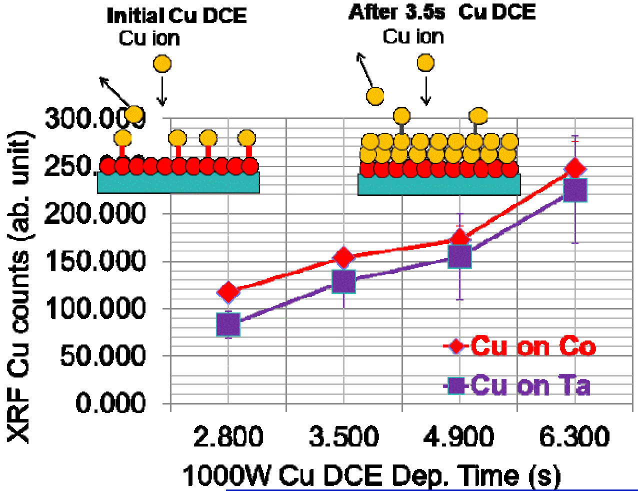
H-post-treatment as recommended

T. Nogami al., IITC 2010 IBM



48 nm pitch DD Cu gap-fill comparison, with: a) TaN/Ta liner, vs. b) TaN/Co liner

Cu-Co sticking coefficient > Cu-Ta sticking coefficient



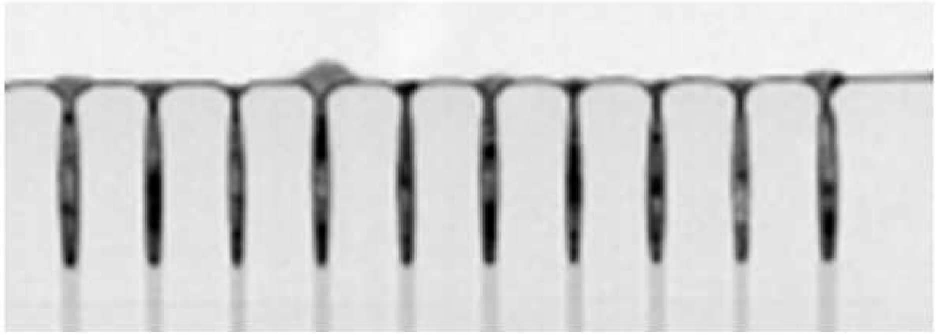
T. Nogami al., IITC 2013 IBM

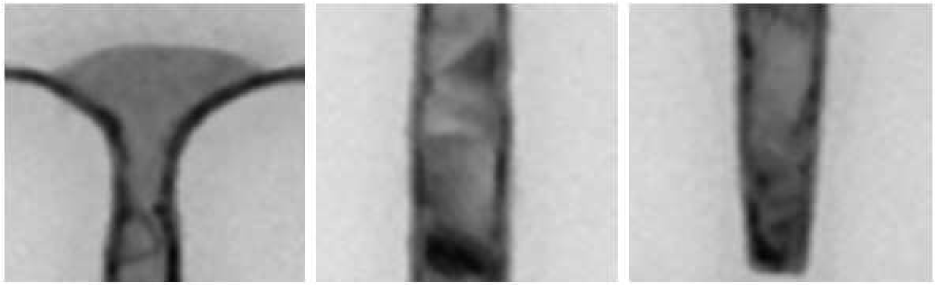
Common Approach-5

Cu Gap Fill

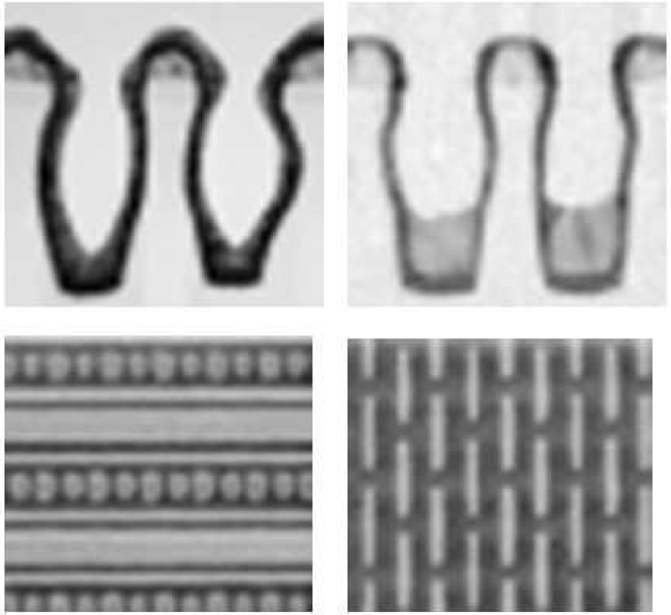
Cu Reflow on CVD-Ru

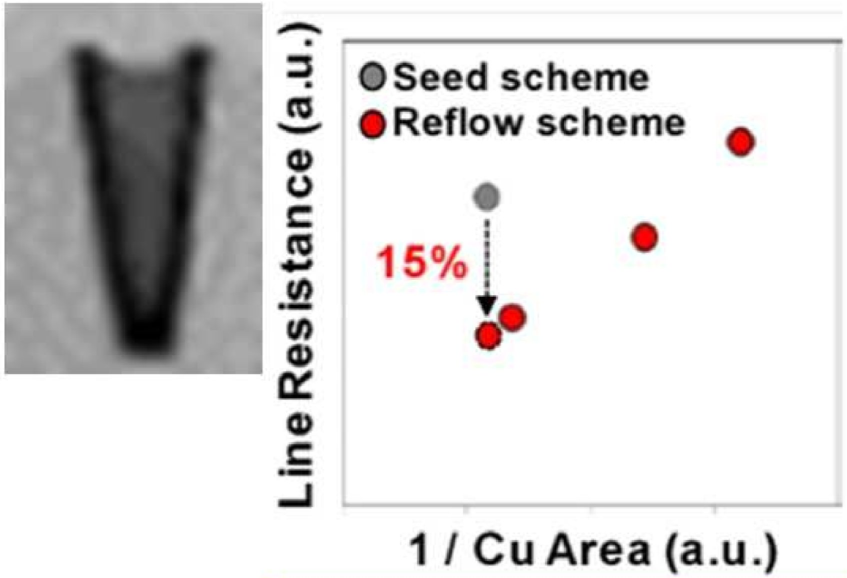
Gap Fill and EM Improvement in 22nm in k=2.4 SiCOH with CVD-Co





K. Yu, et al., IITC 2014 TEL





R-H Kim al., IITC 2015 Samsung

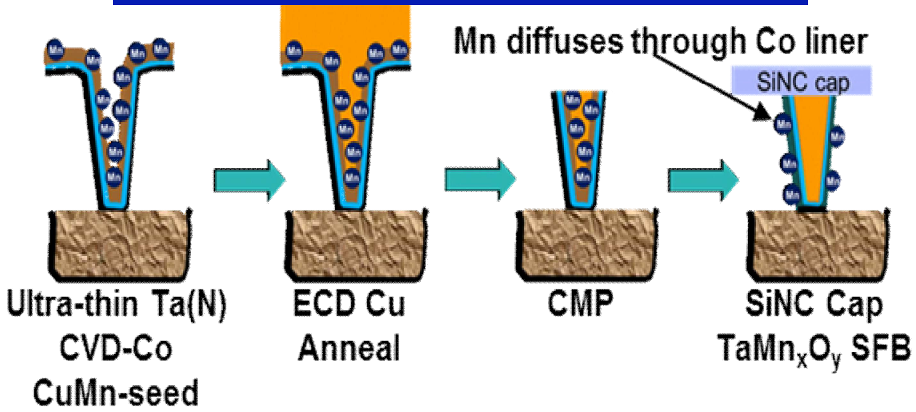
OUTLINE

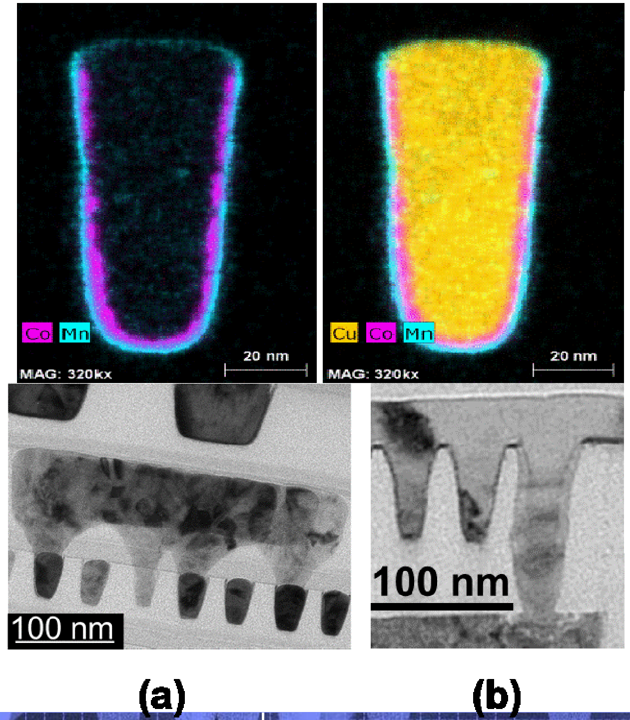
1. **Technology Scaling and BEOL**
2. **BEOL Challenges**
   - ❖ **Tradeoff's**
3. **Potential Solutions**
   - ❖ **Fundamentals**
   - ❖ **Common Approaches**
   - ❖ **Innovative Approaches**
     1. **Integrated solution with alternative barrier**
     2. **Co plug formation to reduce the aspect ratio of Cu**
     3. **Alternative conductors**
     4. **Alternative diffusion barriers**
4. **Summary**

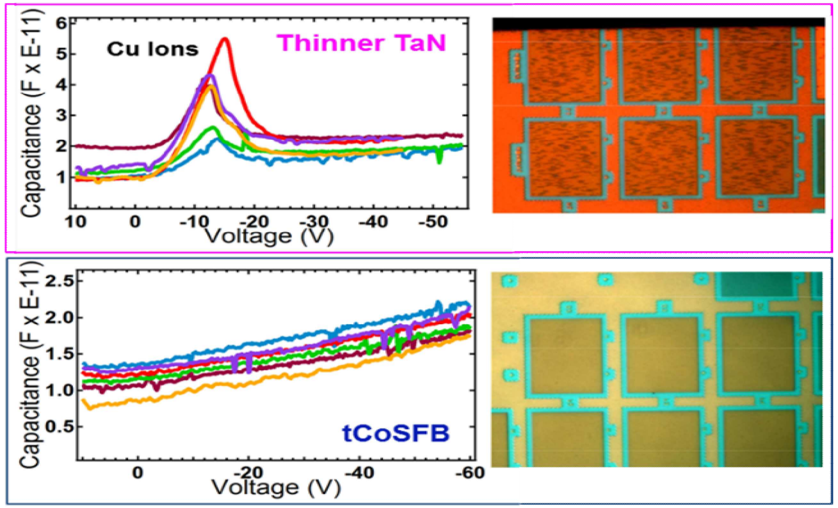
Integrated Solution

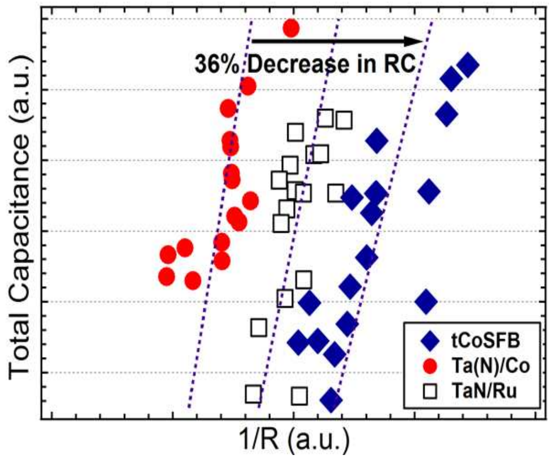
Reduced RC with EM reliability and Cu gap fill simultaneouly

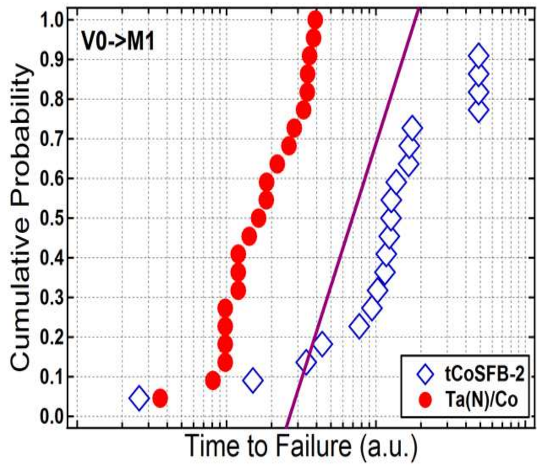
Through-Cobalt Self Forming Barrier











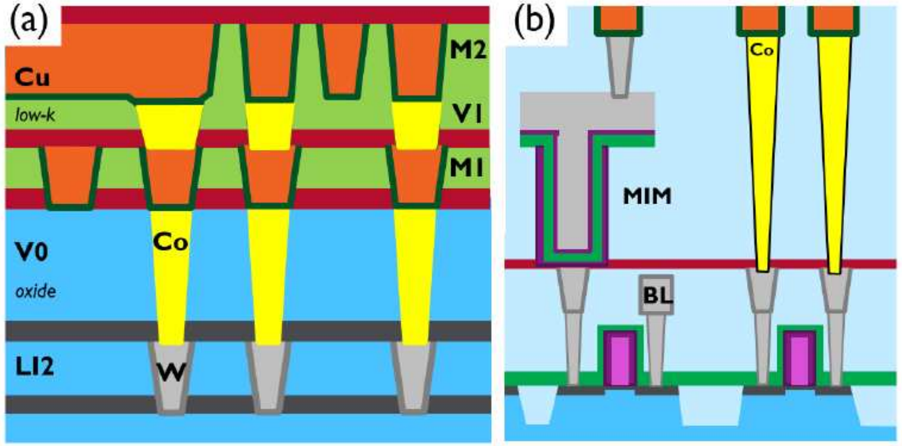
IEDM 2015 T. Nogami et. al, IBM

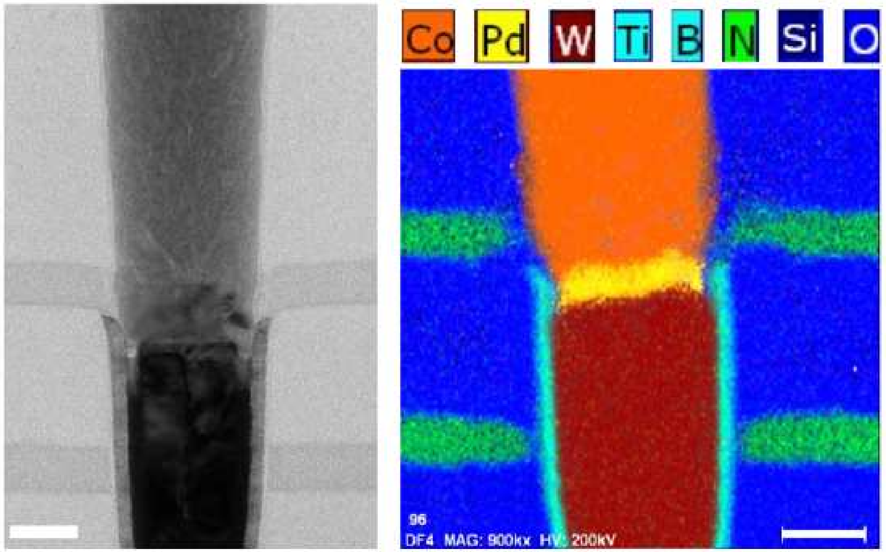
Session-8 Mon 1:35PM

Cu Gap Fill / EM / Via R

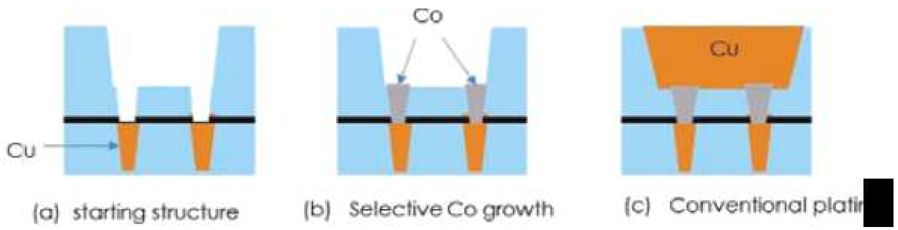
Cobalt Bottom-Up Contact and Via Prefill

J-F. Zheng, et. Al., IITC 2015 LAM Research, IMEC





M. Veen, et. Al., IITC 2015 Entegris, IMEC



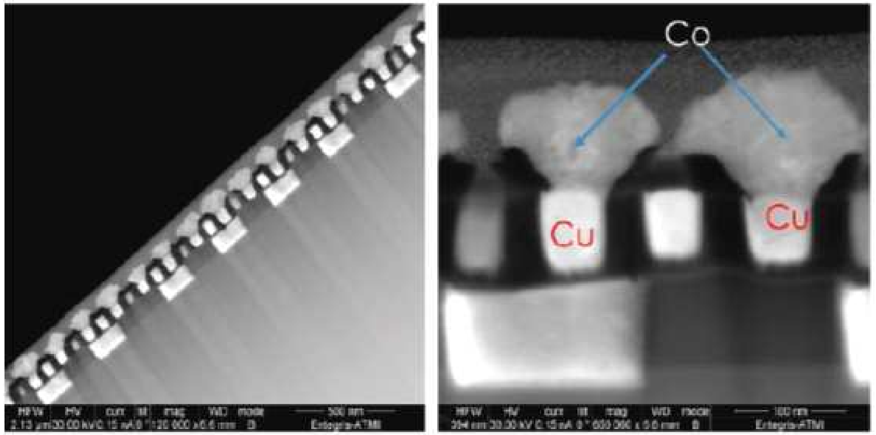
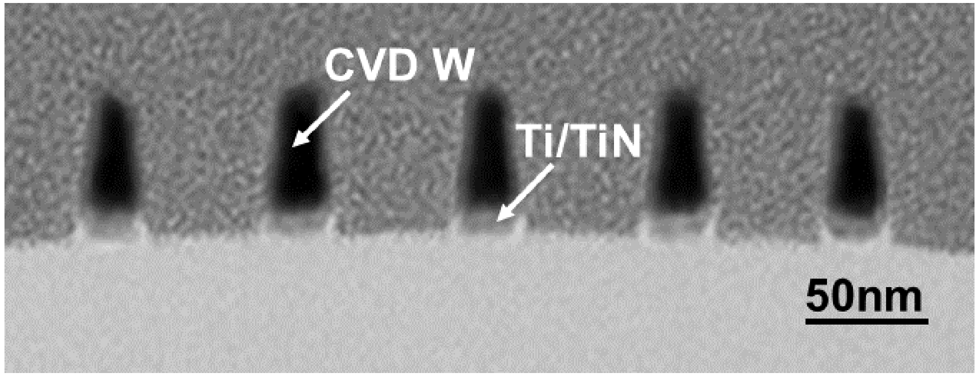


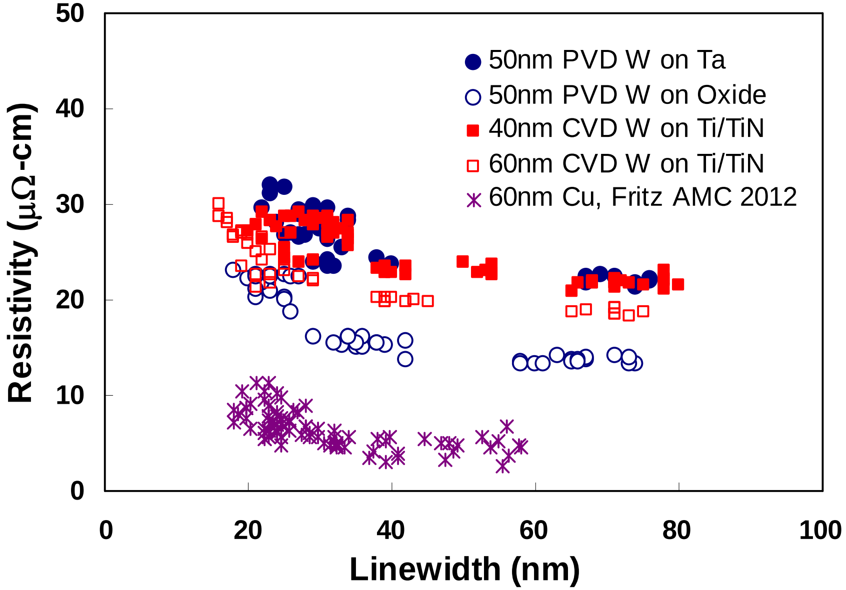
Fig.8a Cross-sectional SEM view of Co fill of via arrays.

Fig.8b Zoomed Cross-sectional SEM view of Co fill of vias

Alternative conductors to Cu

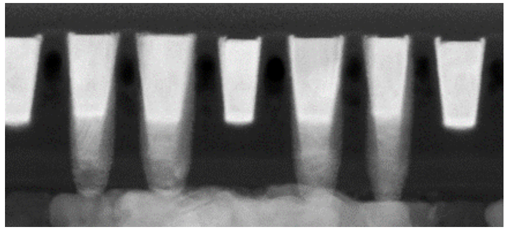
W interconnect

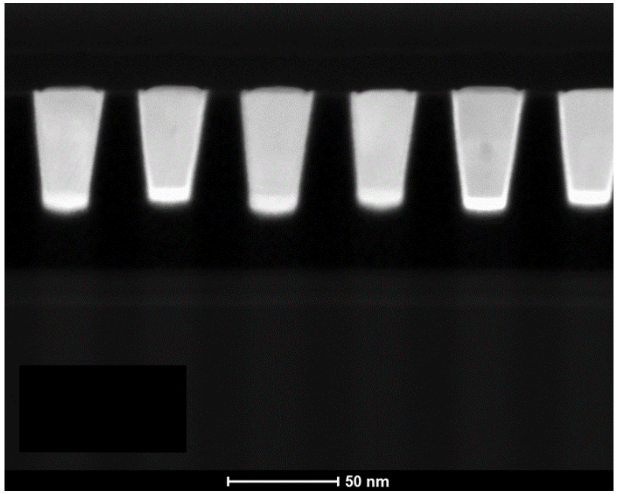




F. Liu, IEEE IITC 2014, IBM

Co interconnect





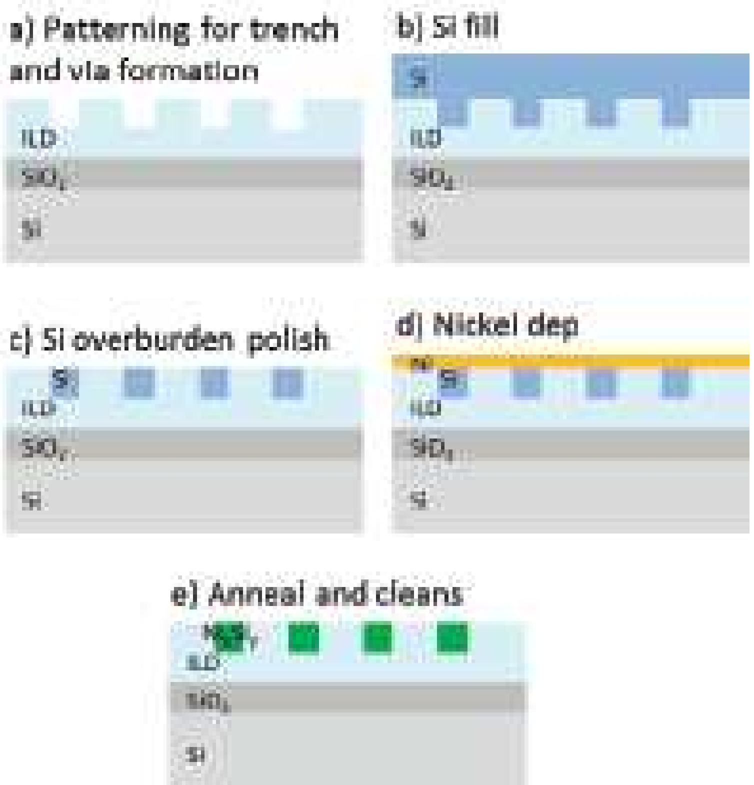
Innovative approach-4

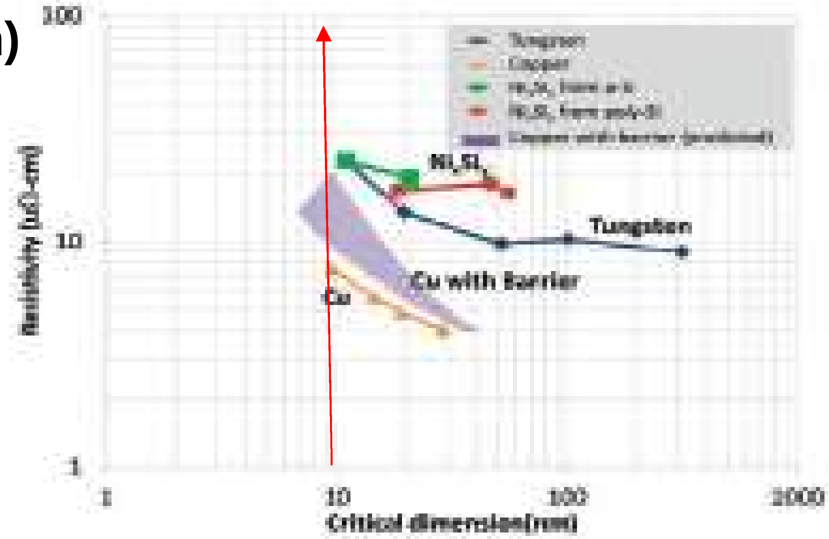
Alternative conductors to Cu

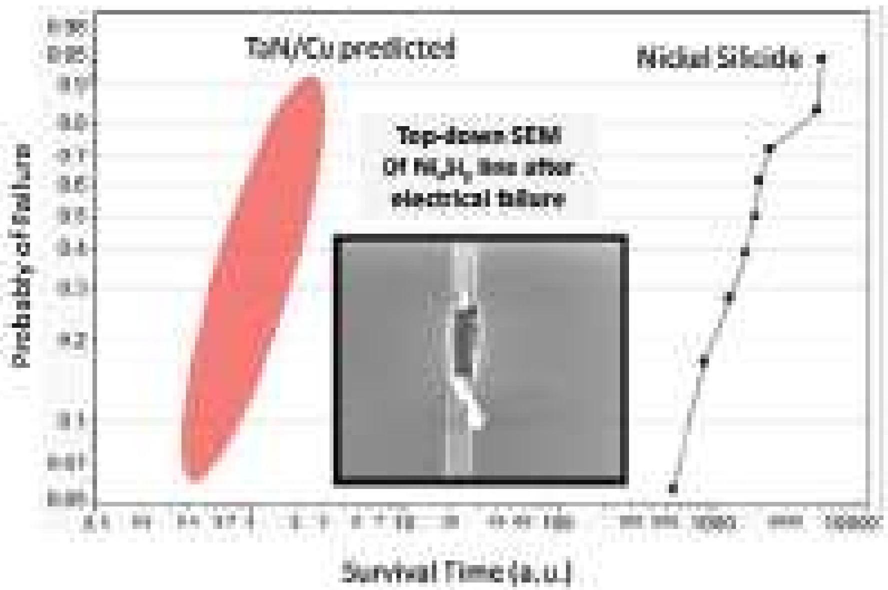
Nickel silicide

K. L. Lin, IITC 2015, Intel

Nickel silicide (resistivity 10 – 20 u ohm cm)
Electron mean free path <10 nm
Predicted to have good EM resistance
Preclude the need for diffusion barrier





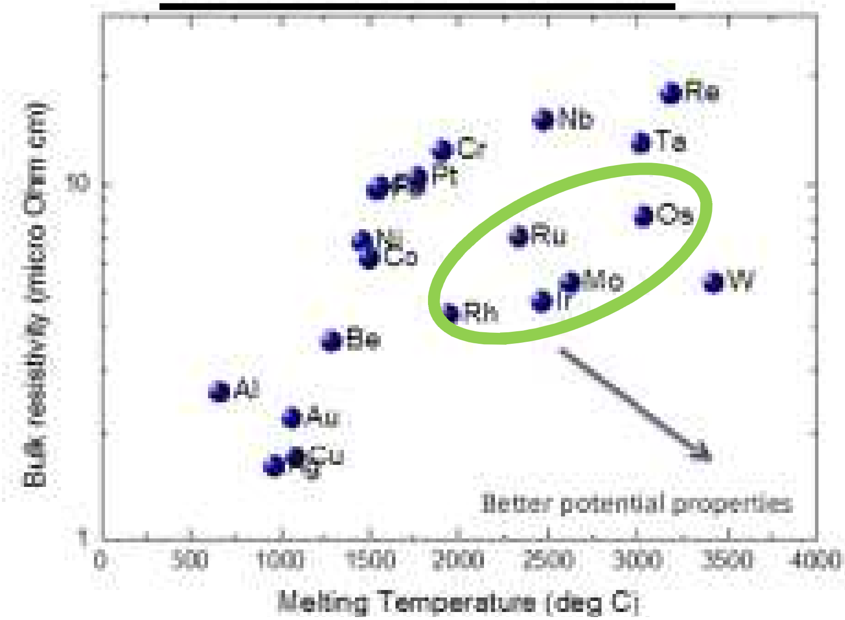


Innovative approach-4

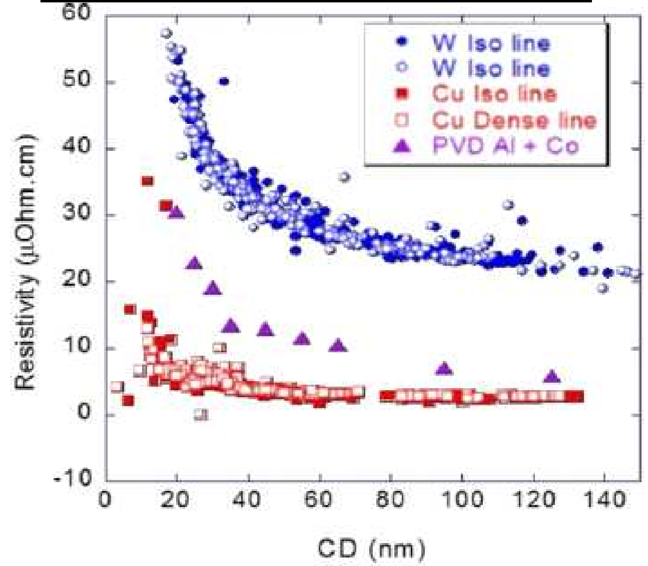
Alternative conductors to Cu

C. Adelmann, et. al, IITC 2015, IMEC

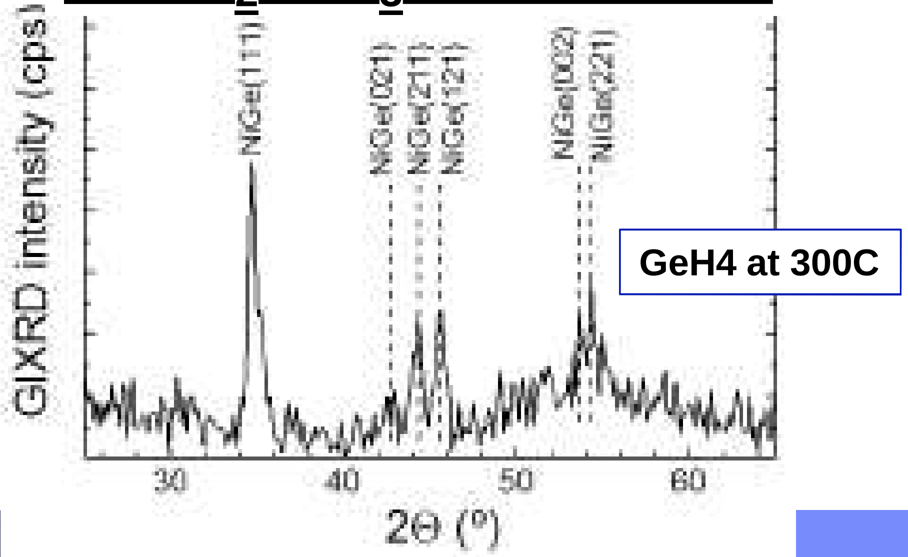
elemental metals

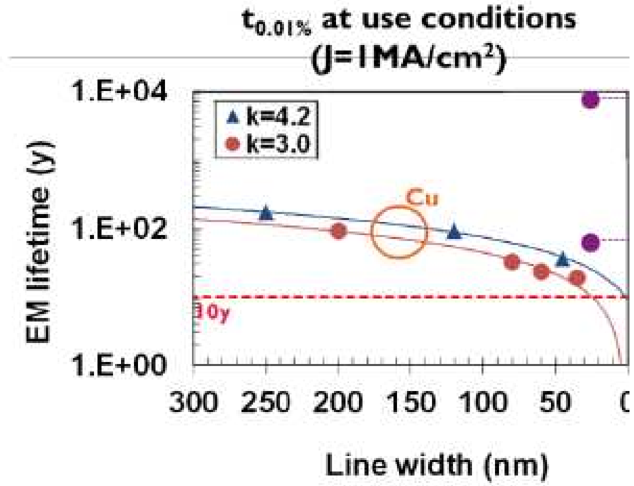


AlCo interconnect



CoGe$_2$, Cu$_3$Ge, or NiGe.





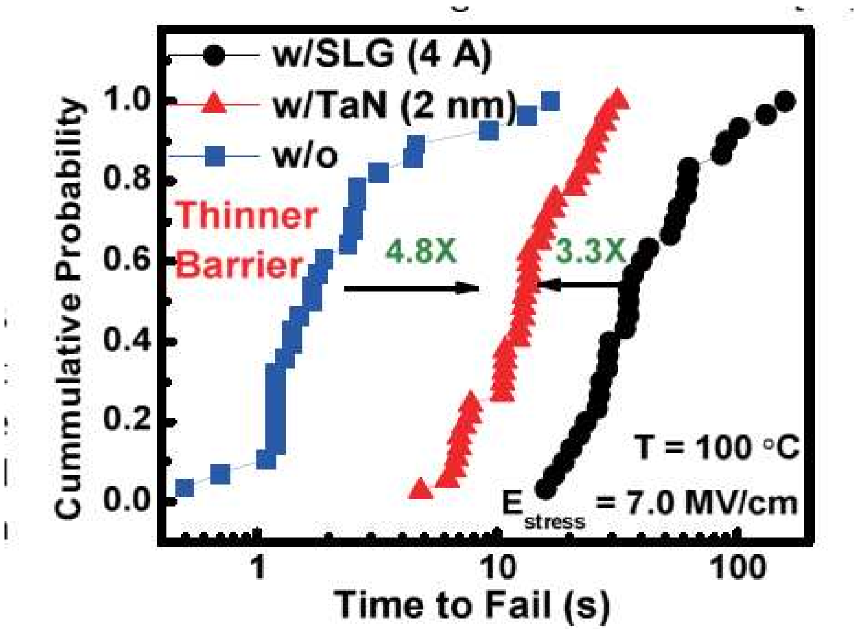
CoAl resistivity is half of W.
CoAl EM is better than Cu.

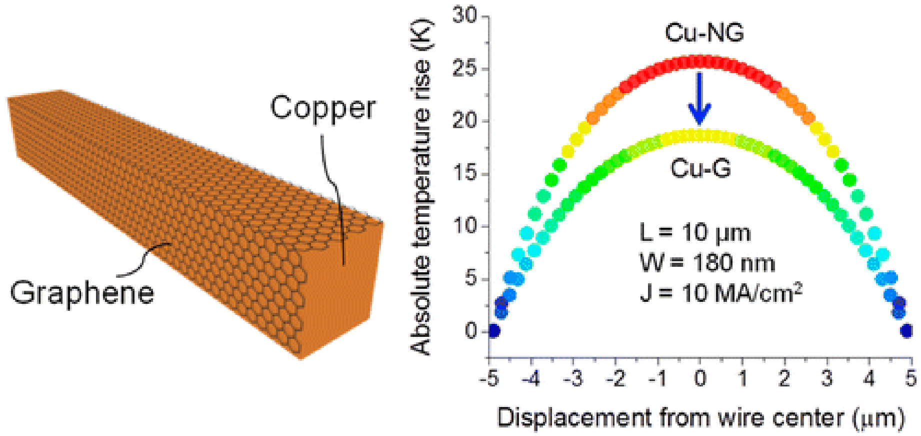
Alternative Barrier

Cu diffusion barrier: graphene

Ling Li, et. Al., VLSI Symposium 2015, Stanford Univ., Univ. of Wisconsin

R. Mehta et al., Nano Lett., 2015 Purdue Univ.





strong enhancement of electrical and thermal conductivity

3 Å single-layer graphene (SLG) gives 3.3X longer TDDB MTTF than 2 nm TaN

Low-temperature deposition of graphene around Cu

OUTLINE

1. **Technology Scaling and BEOL**
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4. **Summary**

Summary

1. 5 nm BEOL spec's are likely to be achievable with a Cu process by introducing innovative technology and by common process improvements.

2. Three tradeoff's of RC, Reliability and Defectivity need to be balanced and resolved by innovation and improvement.

3. Some alternate conductors have 2x line R, but have other potential benefits such as EM and become competitive to Cu.

Acknowledgement

This work was performed by the Research and Development Alliance Teams at various IBM Research and Development Facilities.

The presenter thanks to all coworkers of IBM and IBM Alliance for their cooperation.

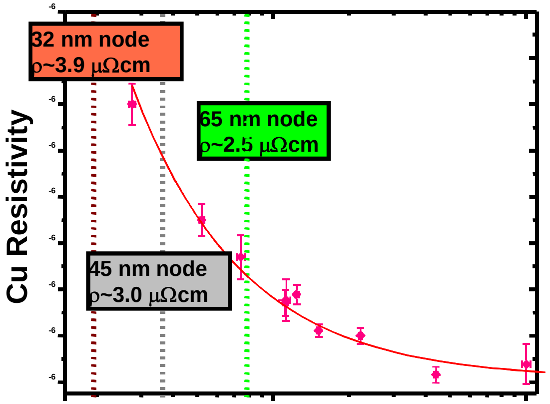
Back up

D. Edelstein, IITC 2012

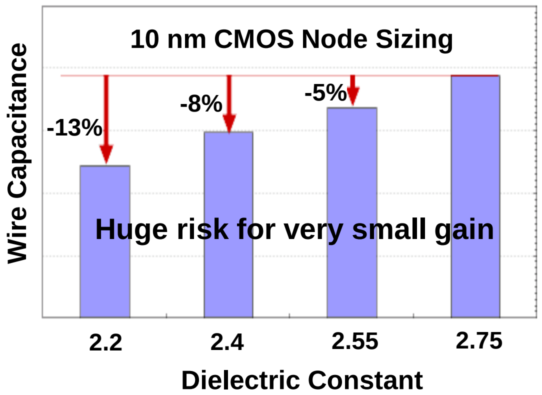
Scaling Challenges for On-Chip Cu/Low-k Multilevel Wiring (BEOL)

Scaling has always gone against wiring performance and reliability.
The problems are not new, but grow more acute the deeper we go into the nanoscale.

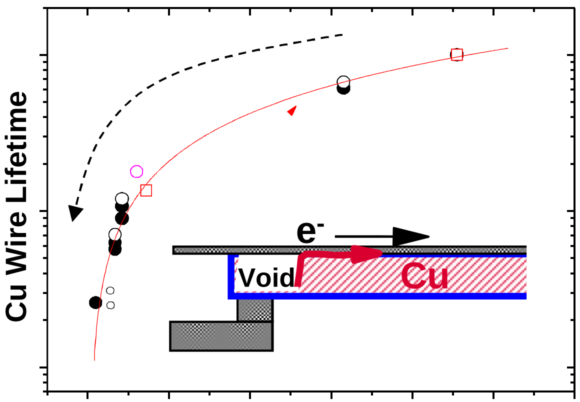
Performance (R and C)



Scaling

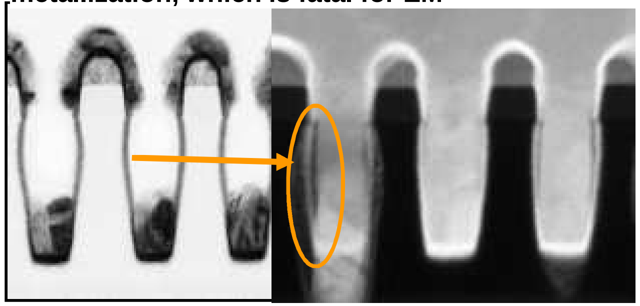


Metal Reliability (Electromigration)

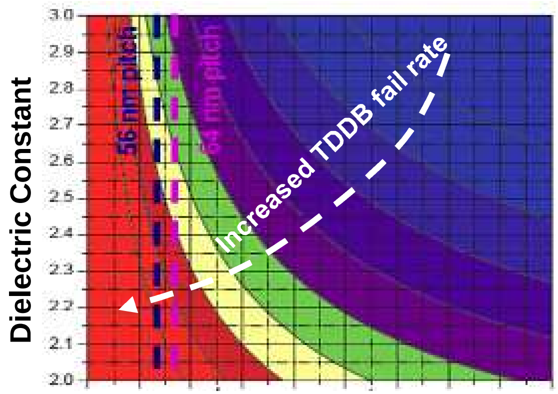


Scaling

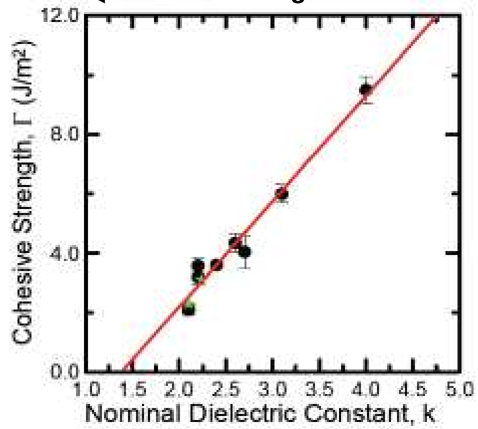
Nanoscale patterning can lead to defective Cu metallization, which is fatal for EM



Insulator Reliability (TDDB)



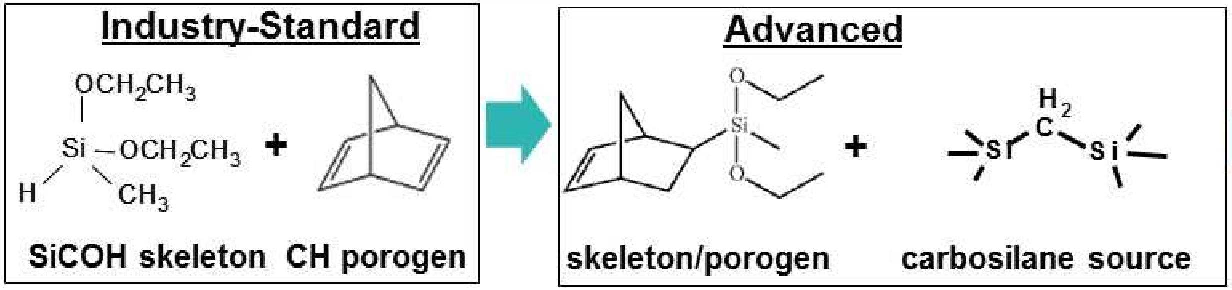
Scaling

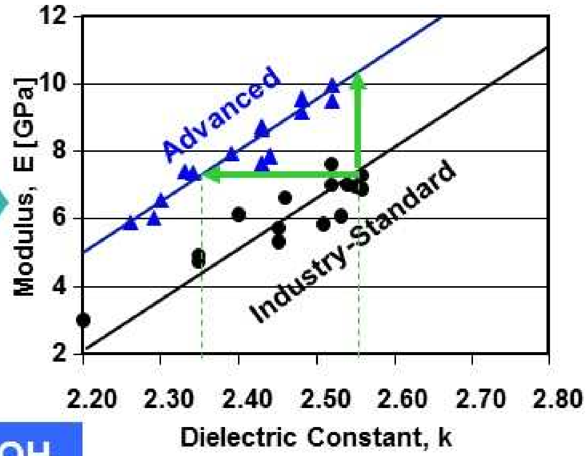


D. Edelstein, IITC 2012

Innovations for Low-k Insulator Performance and Reliability

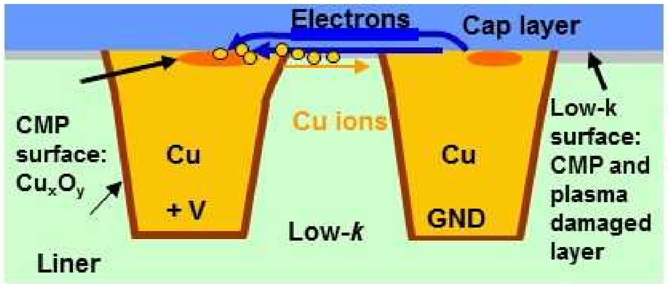
- Increasing the Mechanical Strength of Ultralow-k Porous SiCOH



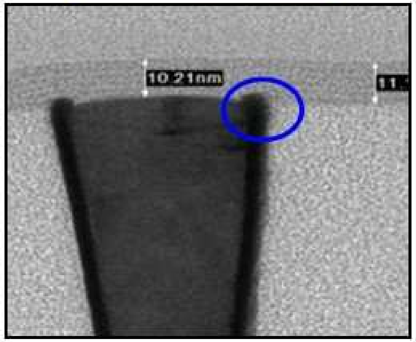


- Increasing TDDB Reliability with Advanced Low-k Cap and Porous SiCOH.
- Cu containment, and dielectric strength lead to higher TDDB reliability.
- All with equal or slight reduction in overall effective dielectric constant.

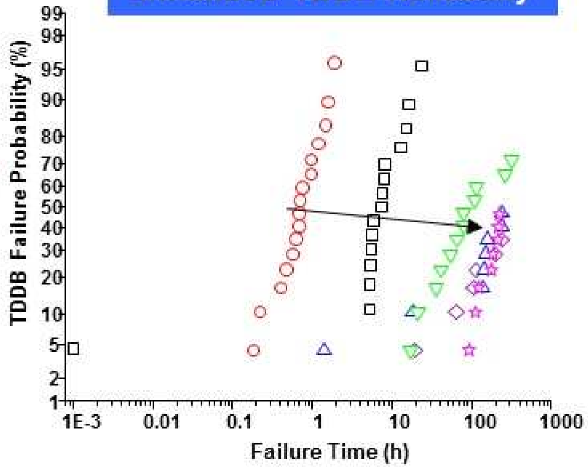
Fundamental TDDB Mechanisms



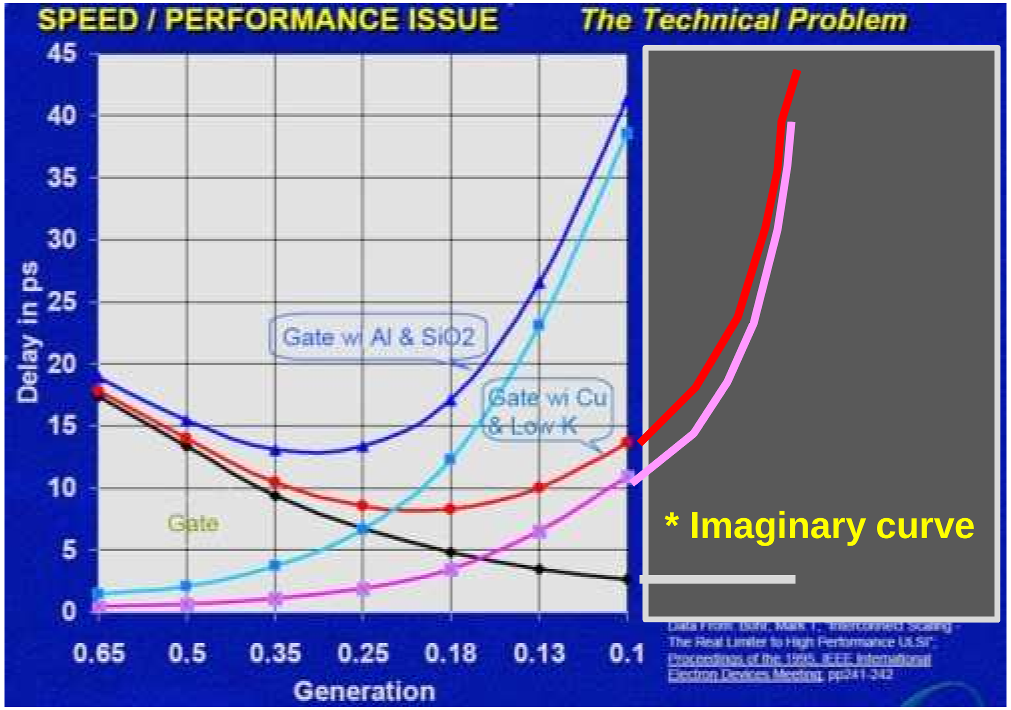
Advanced Cap

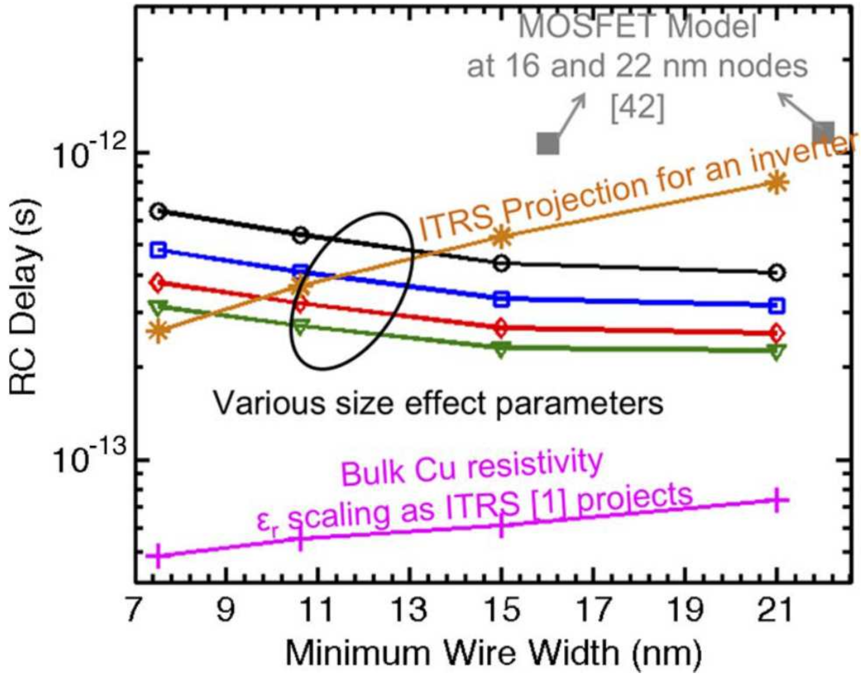


Enhanced TDDB Reliability



BEOL has started to void FEOL scaling benefits





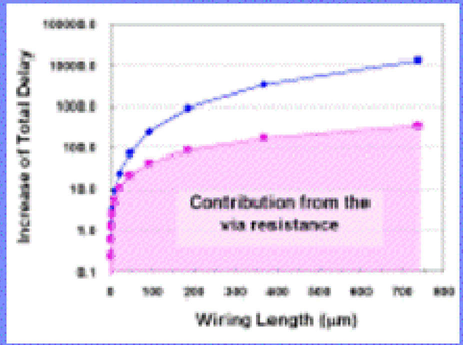
A. Ceyhan, A. Naeemi, Trans. ED 2013

Scaling factor of Interconnect is no longer *k*, but n*k* (n>1)

Interconnect RC started to dominate the delay.
It started already from 10 nm CMOS.

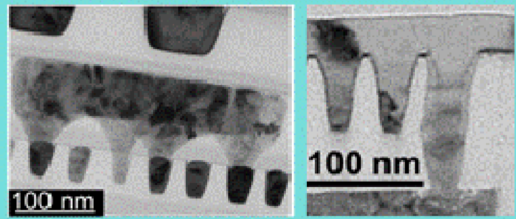
Critical elements in 7nm and 5nm BEOL

RC, Via R



J. HC Chen, IITC2014, IBM

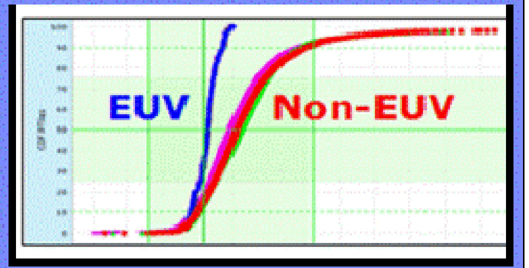
Cu Gap Fill



(a) (b)

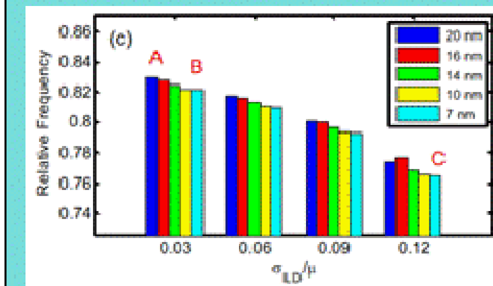
T. Nogami IEDM 2015 IBM

Litho/RIE



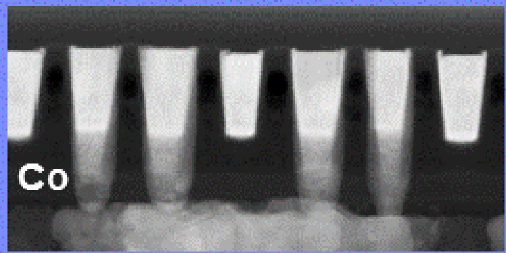
J. Shearer AVS 2014

CD Variation

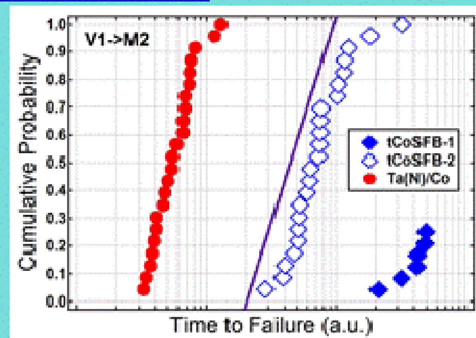


C. Pan et al., IITC 2014

Alternative metal



EM, TDDB



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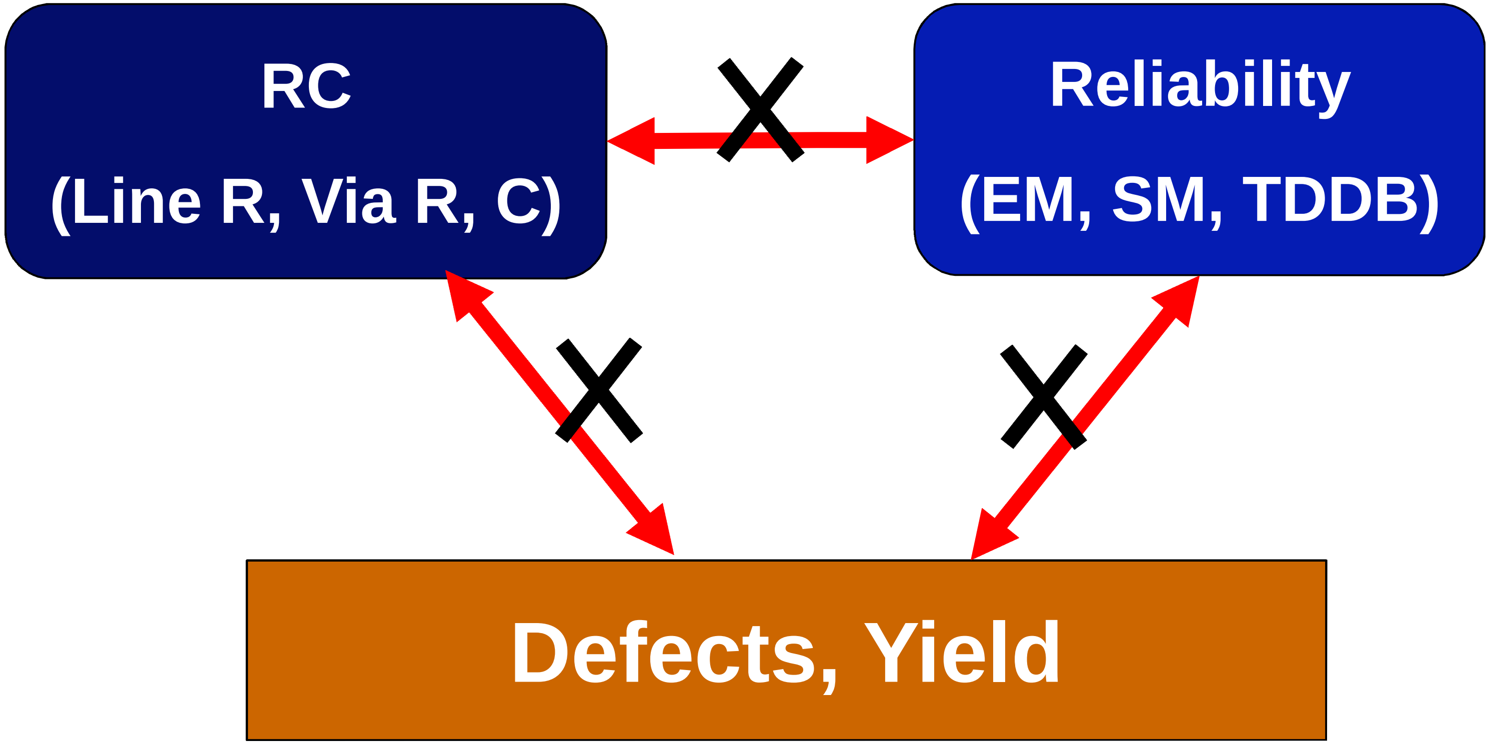
Tradeoff's among RC, Reliability and Cu Gap Fill



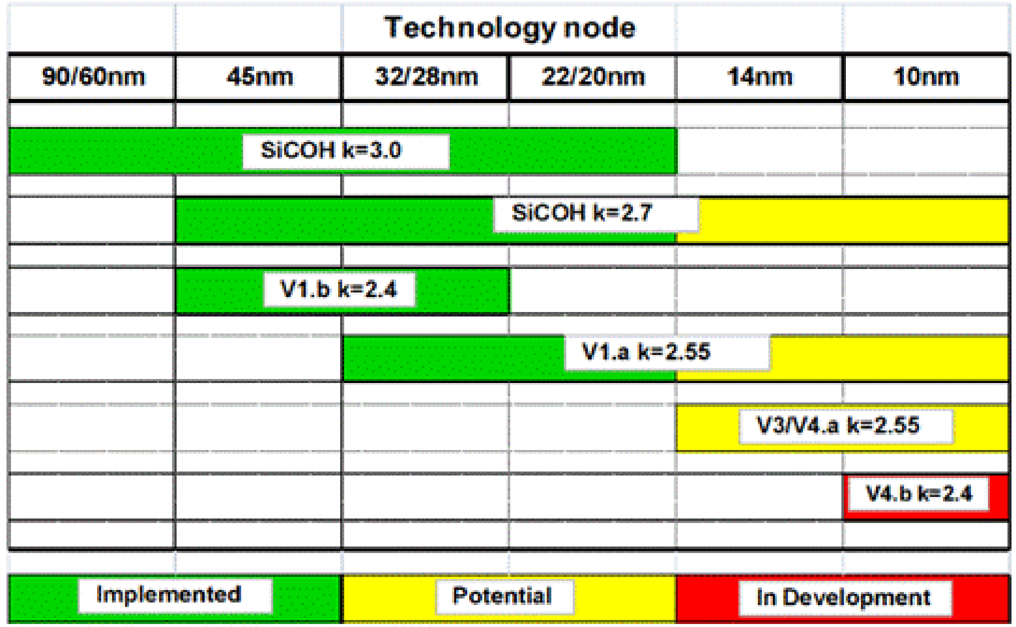
We need to reduce the line R, via R, and capacitance.
At the same time, reliability (EM, TDDB) needs to be maintained.
Before these, defect-free Cu gap fill is a prerequisite.

Interconnect dielectrics

Dielectric	V1.a	V1.b	V3	V4.a	V4.b
Precursor	DEMS+BCHD		Embedded porogen	Embedded porogen+Carbosilane	
k (@ 150C)	2.53	2.4	2.46	2.53	2.42
Breakdown voltage (MV/cm)	>7.3	> 6.0	> 7	7	
E (GPa)	7.2	4.9	6.64	10.2	6.64
Adhesion (J/cm2)	4.5	4.4	3.9	4.4	3.9
C%	15.7	15.5	21.1	16.3	17.4
Porosity (%)	16.3	24.5	14.4	17.9	19.7
Pore diameter (nm)	1.2	1.2	1	1.1	1.3
PID	0.67	0.9	0.57	0.49	0.65

Dielectrics and selected properties

S. Nguyen et.al., MRS 12015 IBM



Dielectrics implemented by IBM and Alliance partners

A. Grill et.al., Appl.Phys.Rev., 12014 IBM