Emerging Interconnect Technologies

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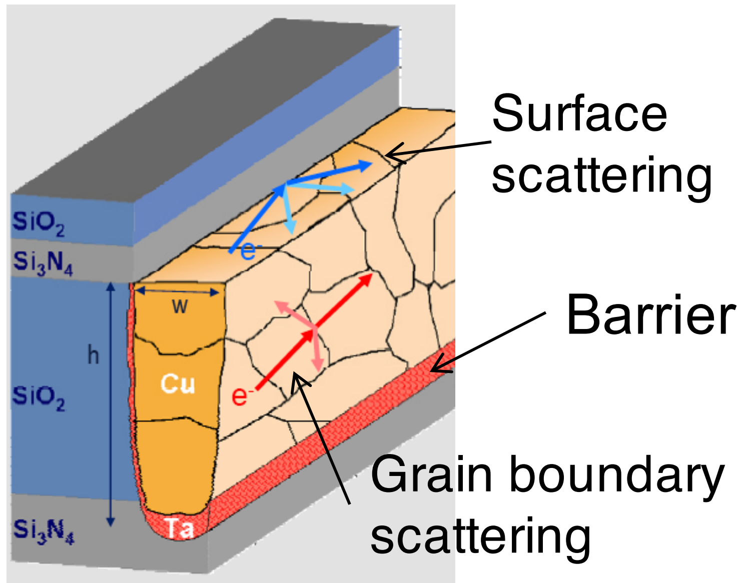
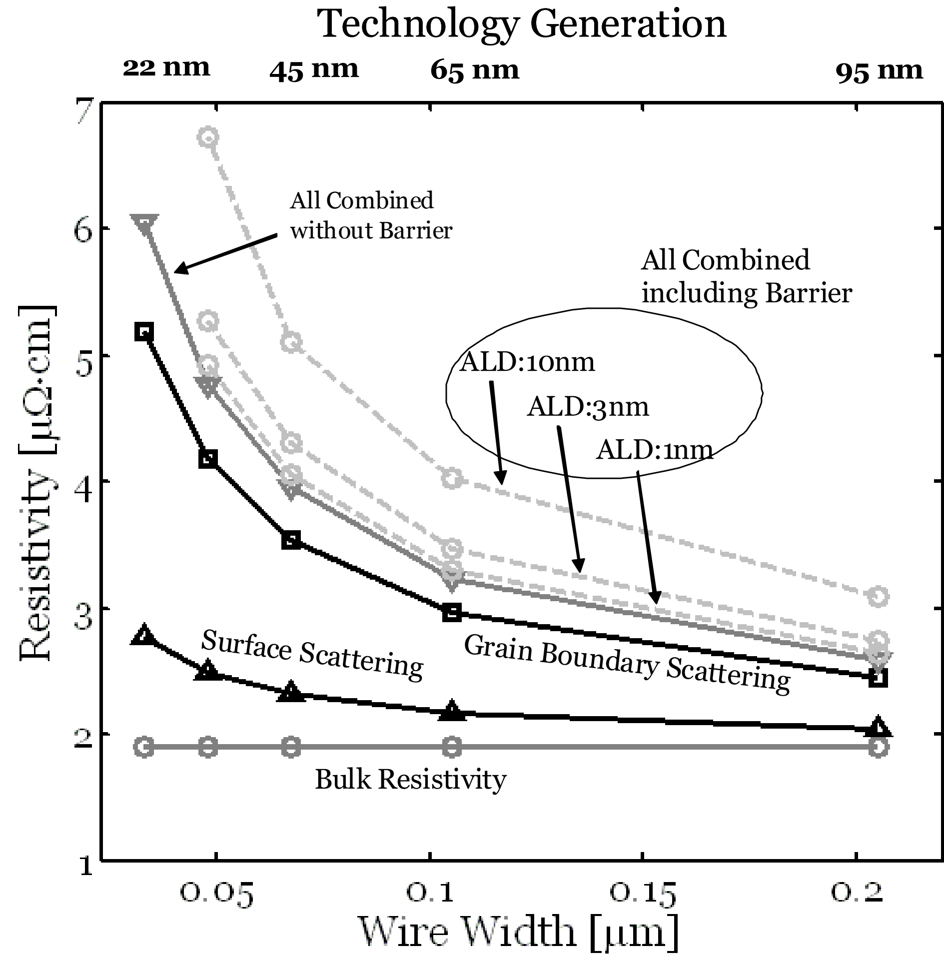
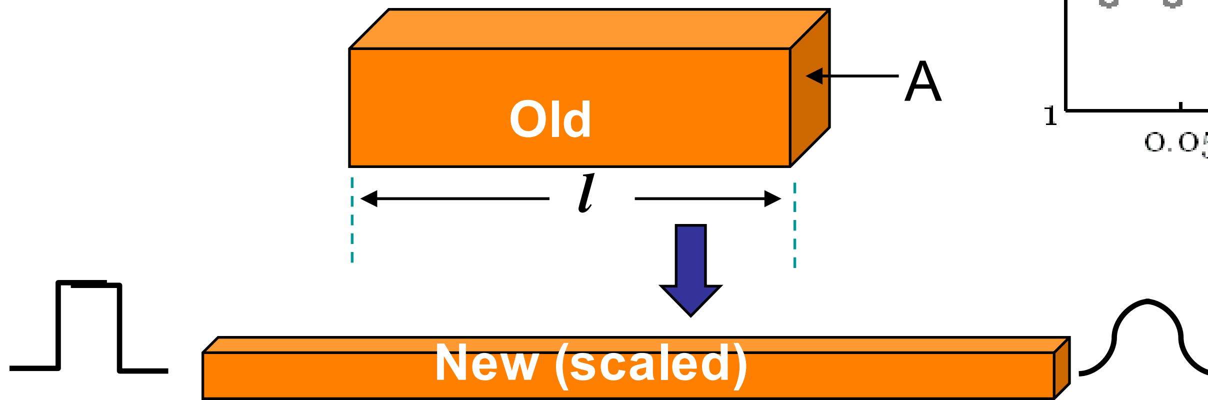
Outline

- Scaling limits of interconnects
  - ➢ Alternatives to Cu
- Performance simulations
  - Cu, CNT, optical interconnects
- Technology for novel optical interconnects
- 3-D integration
- Summary

Effect of Scaling on interconnect performance







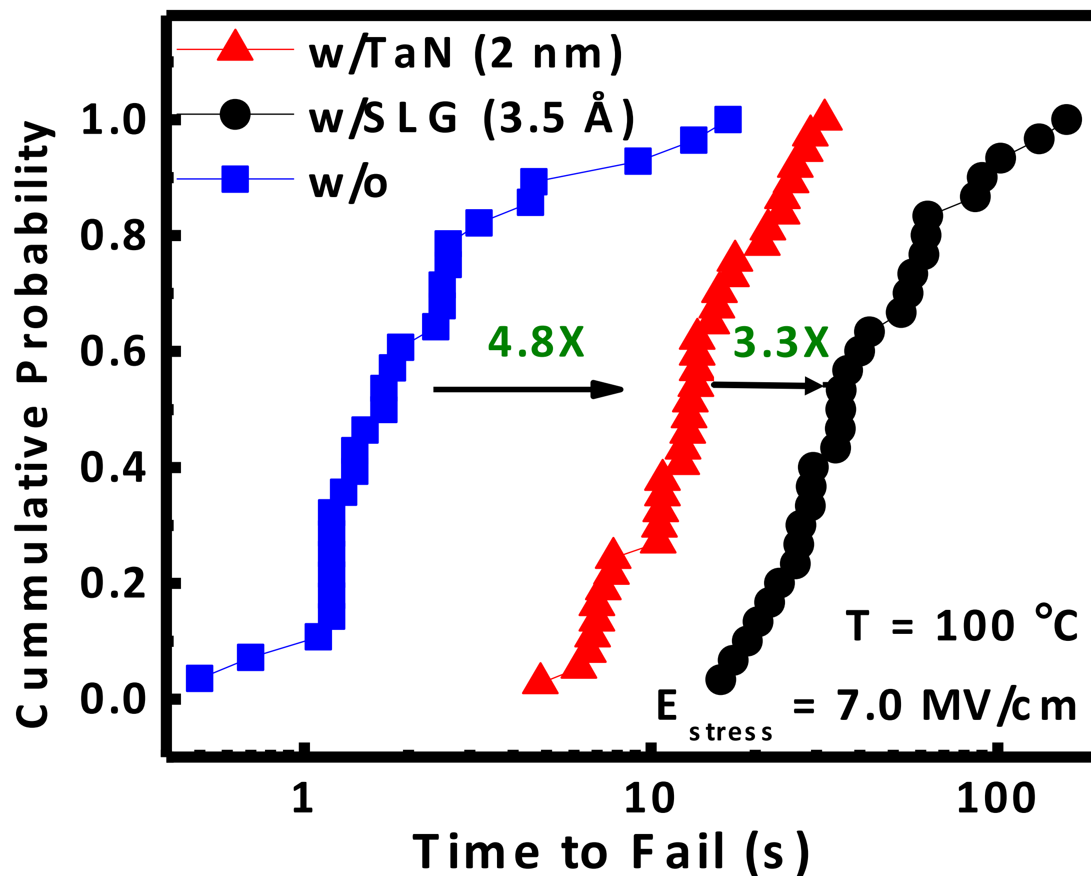
Bit rate $\propto A/l^2$

Delay $\propto l^2/A$

Power dissipation ~ CV^2f

K.-H. Koo and K. C. Saraswat, in Nanoelectronic Circuit Design, Springer, 2011, pp. 377-408

Graphene vs. TaN Barrier for Cu

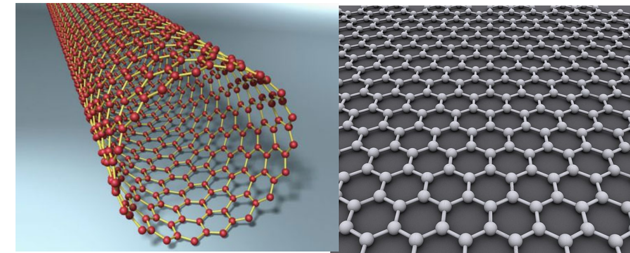


L. Li … H.-S. P. Wong, *Symp. VLSI Tech*. 2015
L. Li … H.-S. P. Wong, *ACS Nano* 2015

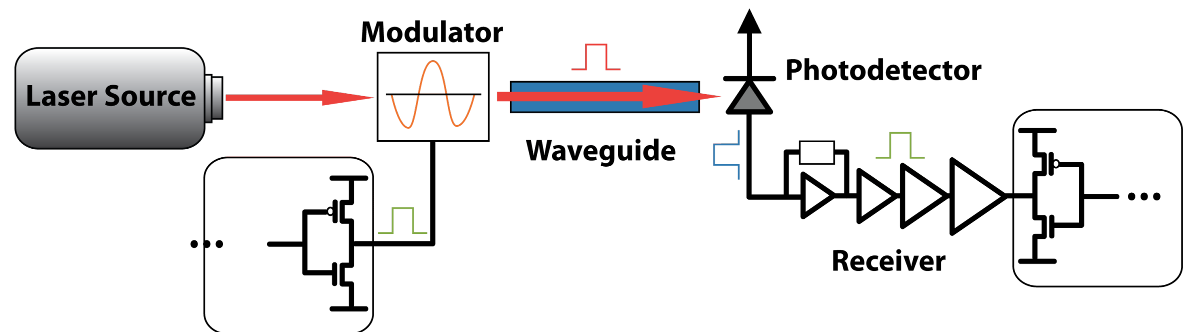
Thinner barrier: 3.5 Å single layer graphene is better than 2 nm TaN

How can we improve interconnect performance?

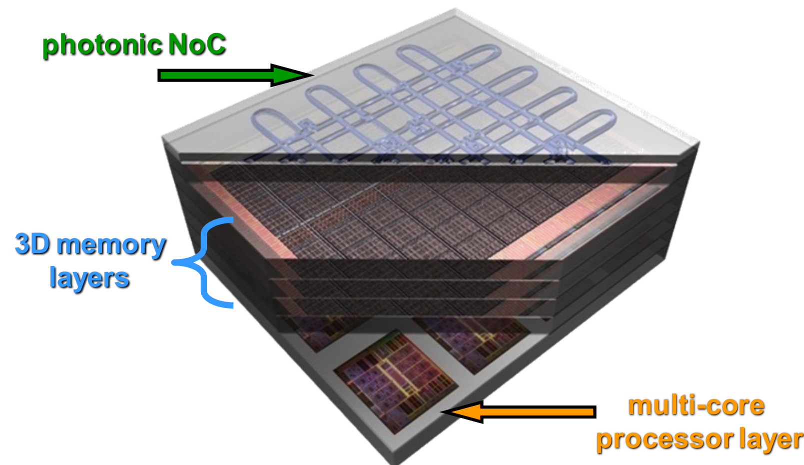
– Carbon nanotubes/ Graphene



– Optical interconnects

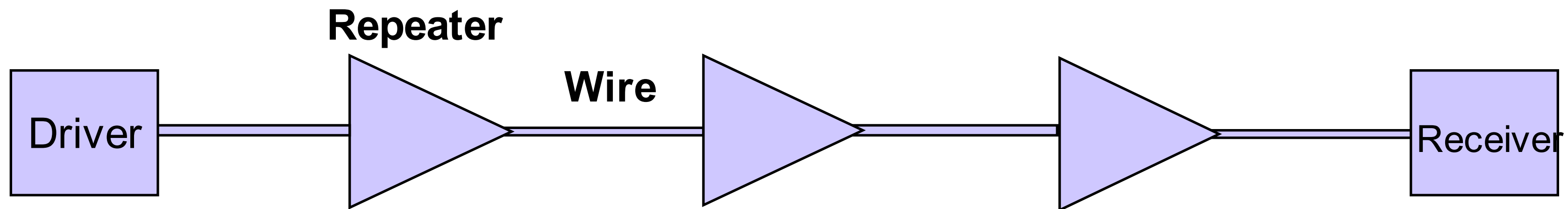


– 3D

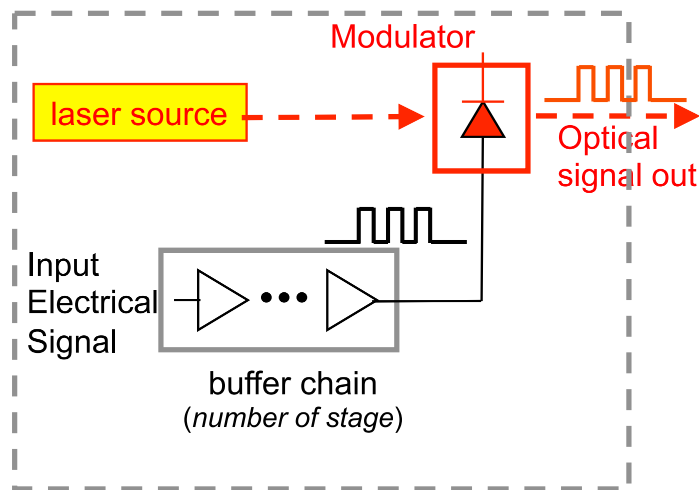


Optical & Electrical On-chip Wires: Schematic

Electrical Interconnect (Cu or CNT)

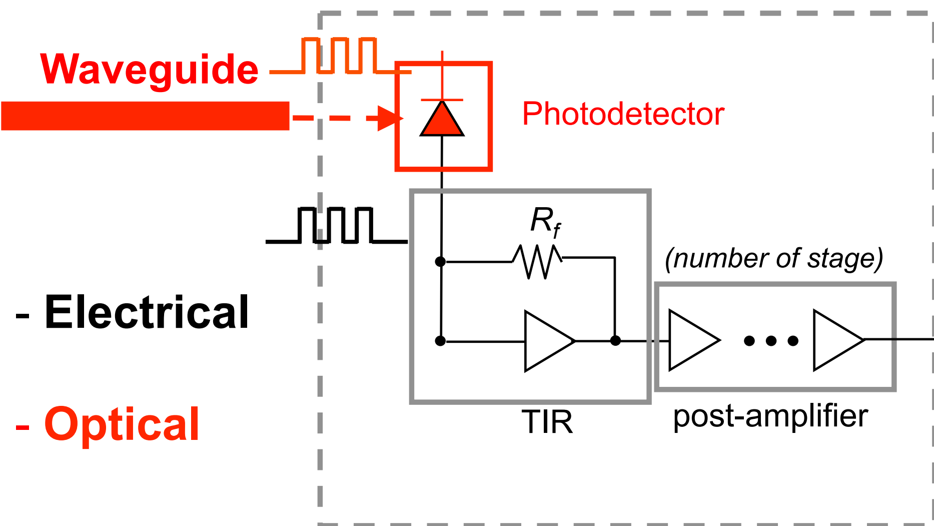


Optical Interconnect



Waveguide

- Electrical
- Optical

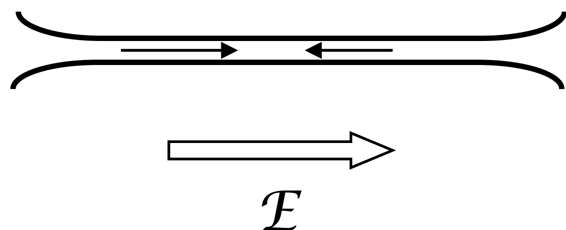


Laser/modulator converts electrical signal into optical signal

Photodector restores optical signal into electrical signal

Carbon Nanotubes

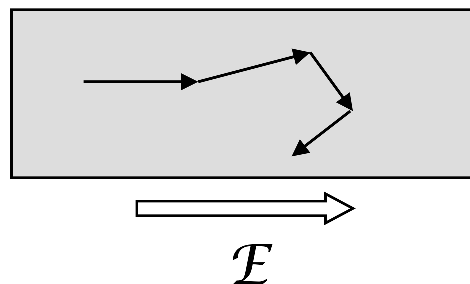
1-D conductors:



Quantum Wires:

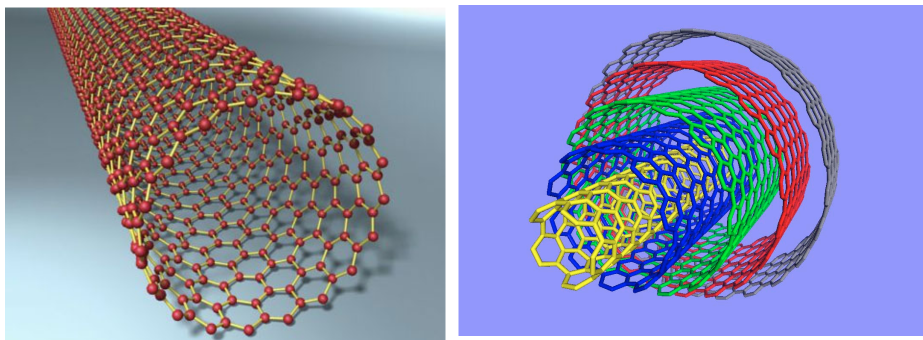
- 1D system with limited density of states. Hence quantum effects play an important role in determining the values of R, L and C
- Mean free paths as large as 1.6μm.

3-D conductors:



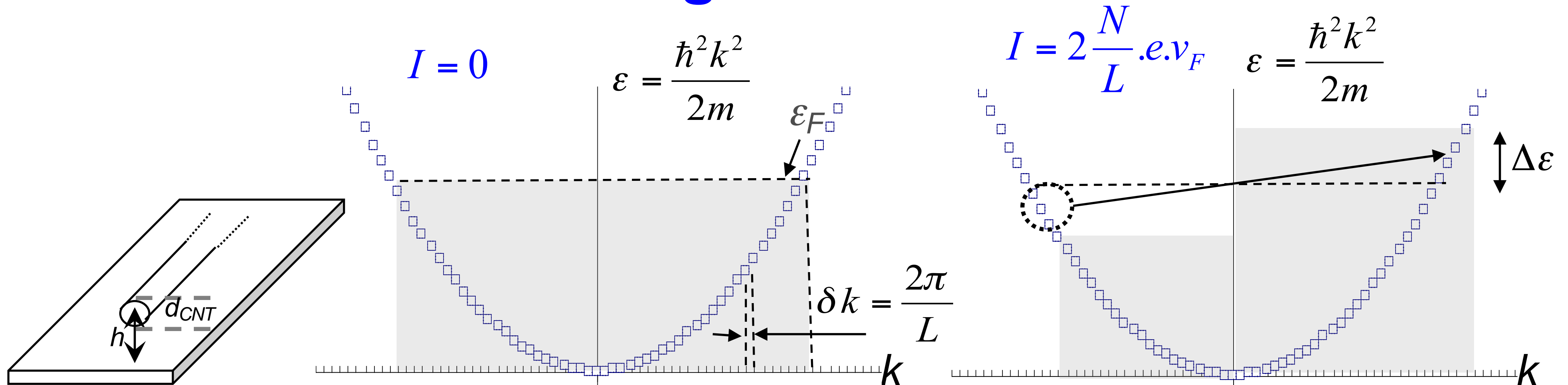
Conventional wires :

- Backscattering through a series of small angle scatterings.
- Mean free paths ~ 30nm.



Potential Candidates for GSI Interconnects.

RLC Model for Single-wall CNT: Inductance



- Nanotube is a 1D system with limited density of states $R_Q = h/4q^2 = 6.45\ K\Omega$
- With potential applied the carriers have to move to higher energy states resulting in increase in kinetic energy resulting in kinetic inductance L_K.
- To add electron into the wire, it requires additional potential energy, which is correspondent to quantum capacitance C_Q.

$$L_{wire} = L_M + L_K \qquad L_M = \frac{\mu}{2\pi}\ln\left(\frac{t}{d_{CNT}}\right) \sim 1.2nH/mm \qquad L_K = \frac{h}{2e^2 v_f} \sim 16\mu H/mm$$

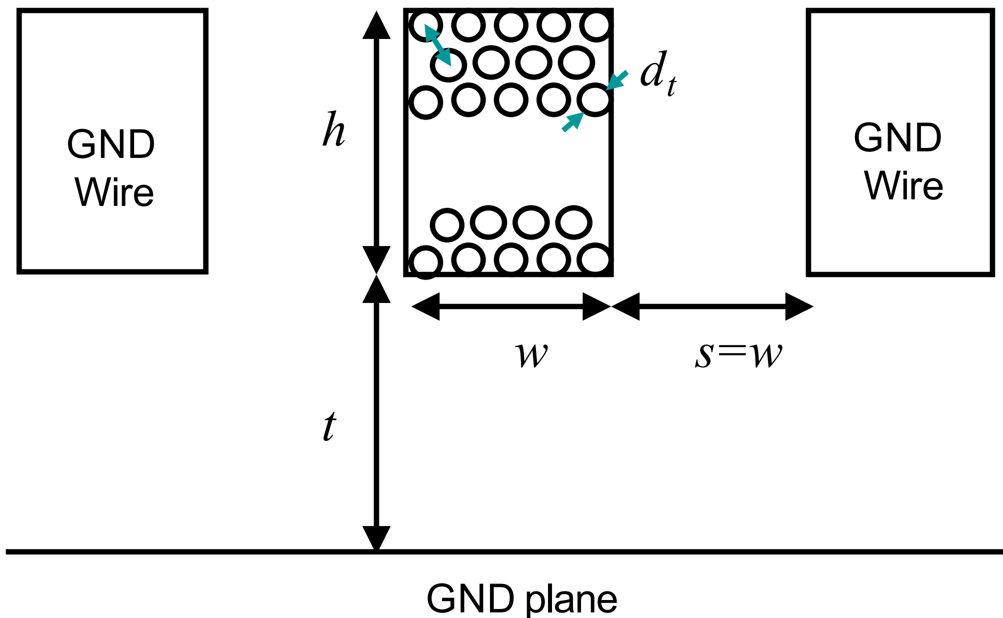
$$C_W = \frac{C_E.C_Q}{C_E + C_Q} \qquad C_E = \frac{2\pi\varepsilon}{\cosh^{-1}(2h/d_t)} \approx \frac{2\pi\varepsilon}{\ln(h/d_t)} \sim 190\text{fF/mm} \qquad C_Q = \frac{2e^2}{hv_f} \sim 100\text{fF/mm}$$

P. J. Burke, Trans. on Nanotechnology, 2002

SWNT to Bundled CNT

CNT bundle with n_{CNT} tubes

- Wire dimension is same as Cu/low-K
- Packing density: Fraction of metallic SWCNTs

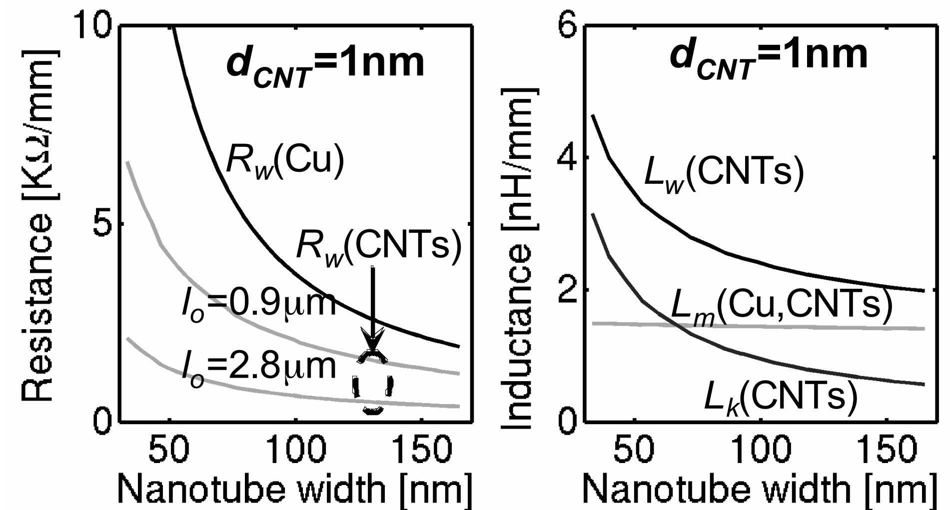


Bundle Parameters

$$R_w = \frac{R_Q}{n_{CNT}}\left(1 + \frac{l}{l_o}\right)$$

$$L_{tot} = \frac{L_k}{n_{CNT}} + L_m \approx L_m$$

$$C_w = \frac{C_E n_{CNT} C_Q}{C_E + n_{CNT} C_Q} \approx C_E$$

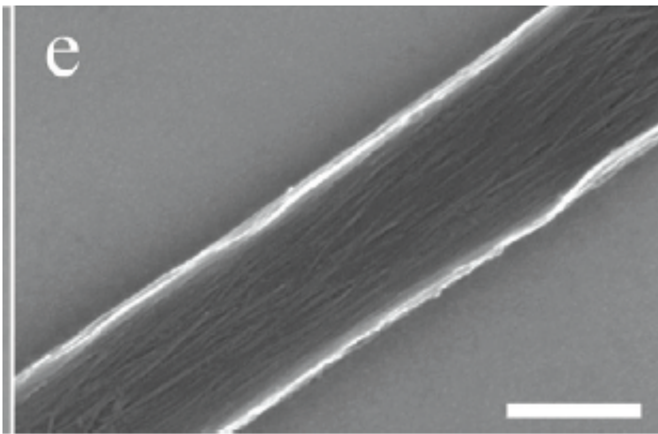


Values for 22nm technology node

Cho, Koo, Kapur and Saraswat, IEEE IITC 2007

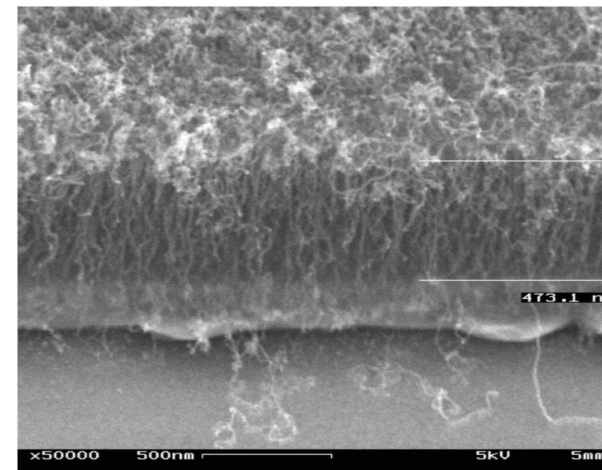
Formidable Task: Fabricating Dense Bundles of SWNTs

- Fabricating Bundles of Densely Packed SWNTs for interconnects has proven very challenging.
- Making contacts to horizontal bundles of SWNTs is very difficult.
- Promising progress in creating aligned isolated SWNTs by transferring SWNTs grown on sapphire to other substrates.
- Single SWNTs are too resistive for general purpose CMOS circuits.



Young Lae Kim et al.
(RPI, RICE & NorthEastern Univ)

Vertical Growth

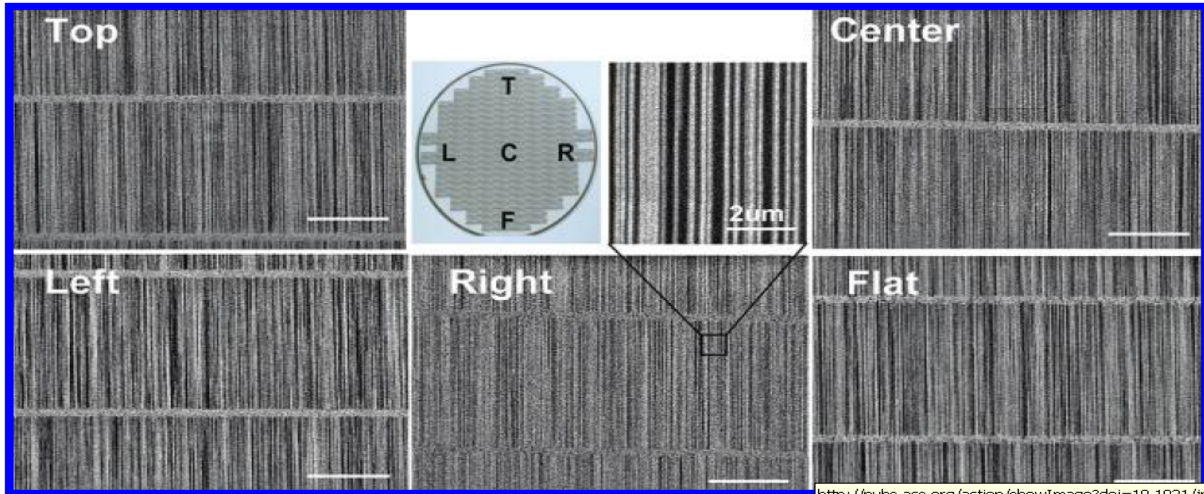


C.V. Thompson, MIT

Examples of Dense Bundles of SWNTs

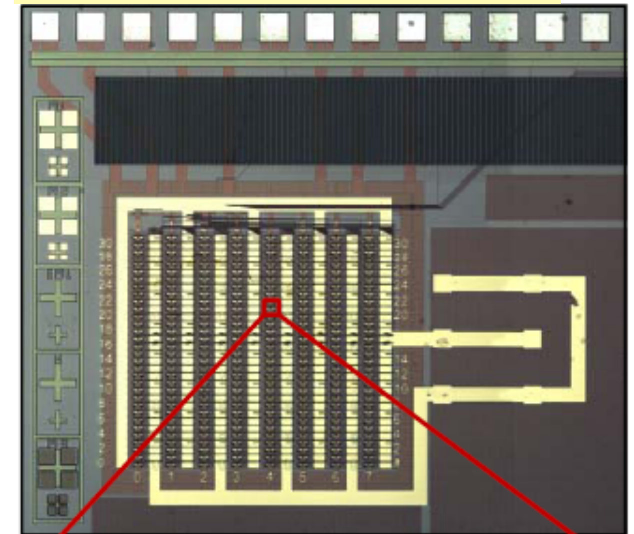
Growth for Interconnects

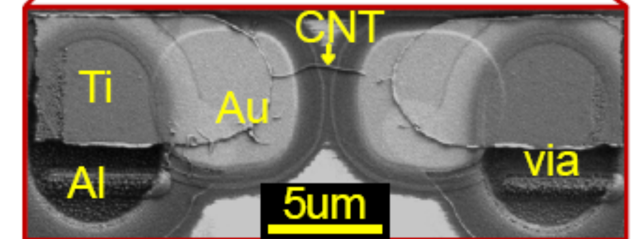
Y. Nishi and H.-S. Philip Wong (Stanford)



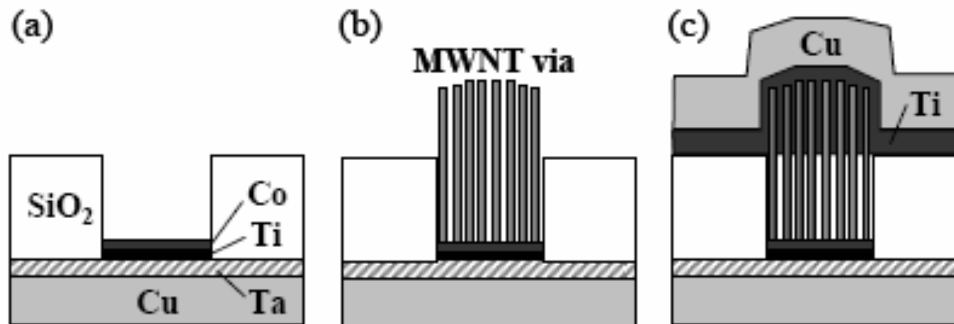
256-Element CNT Ring Oscillator

H.-S. Philip Wong (Stanford)





Growth in Vias



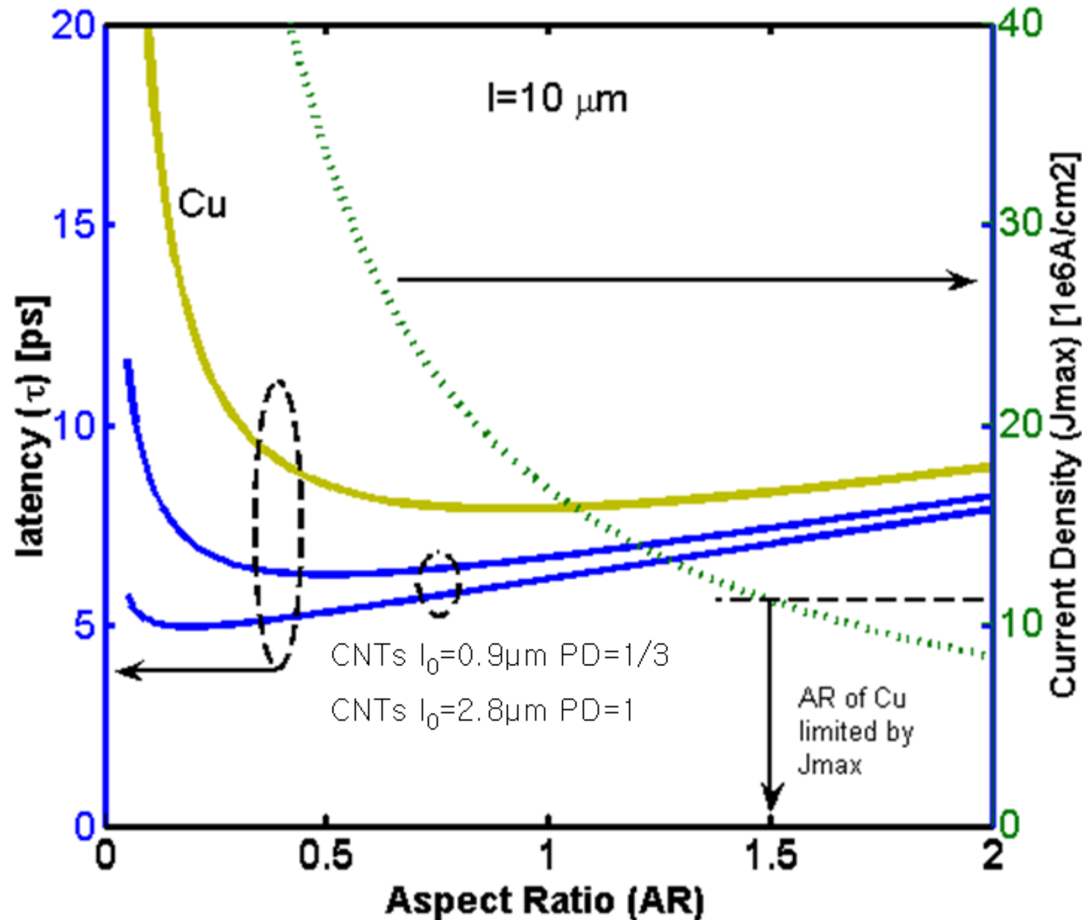
Awano et al. IITC 2005

Potential reliability performance comparison

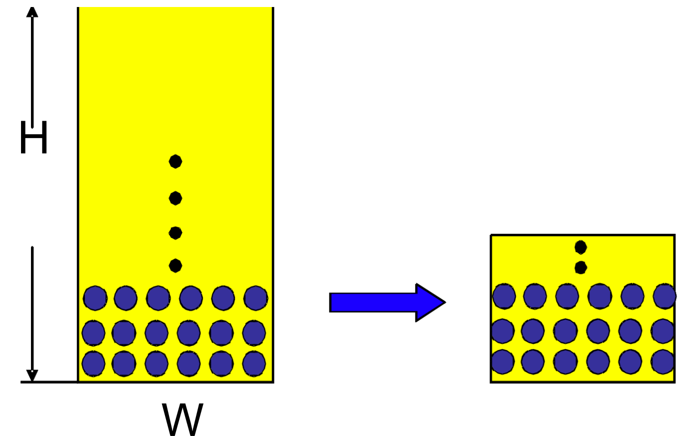
- **Good thermal conductivity**
  - Graphene: $4.84 \times 10^3 \sim 5.30 \times 10^3 W/mK$
  - CNT: $1.75 \times 10^3 \sim 5.80 \times 10^3 W/mK$
  - Copper: $385\ W/mK$

- **High breakdown current**
  - Graphene: $\sim 10^8\ A/cm^2$
  - CNT: $\sim 10^9\ A/cm^2$
  - Copper (EM threshold): $\sim 10^7\ A/cm^2$

Local Interconnect: Cu vs. CNT Bundle



Koo, Cho, Kapur and Saraswat, IEEE TED, December 2007.

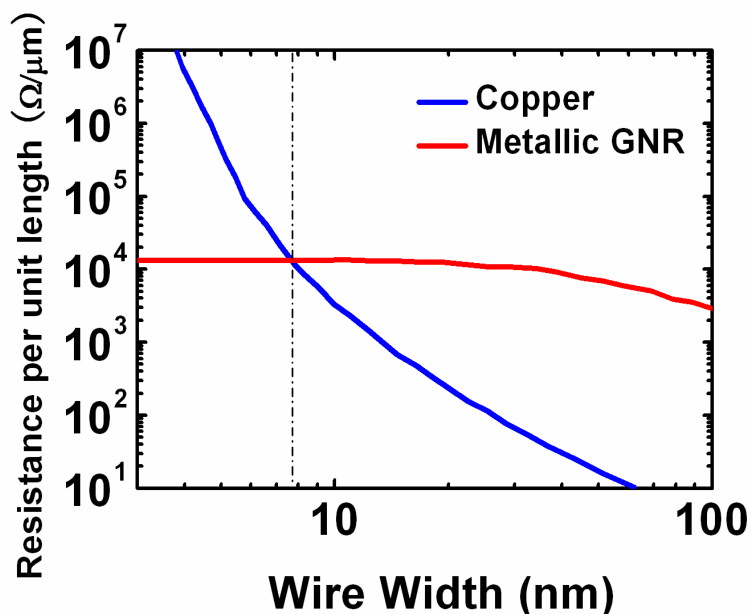


PD is packing density of metallic CNTs

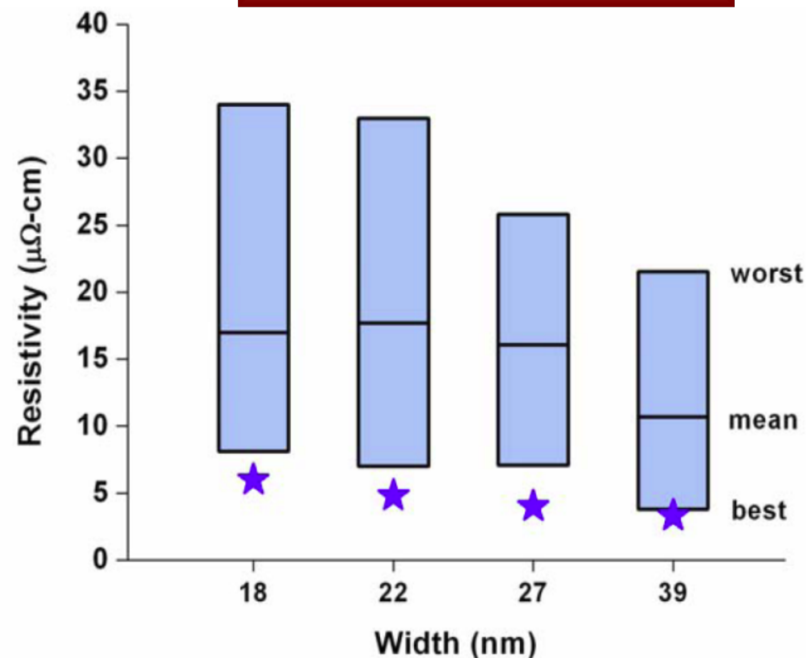
- CNT bundle doesn't suffer from electromigration (Cu wire does !! $J_{max} = 1.47x10^7$ A/cm^2 [ITRS])
- Aspect Ratio of CNT bundle can be tuned. Even a single nanowire can be used as an interconnect.

GNR interconnects conductivity

Theory



Experiment

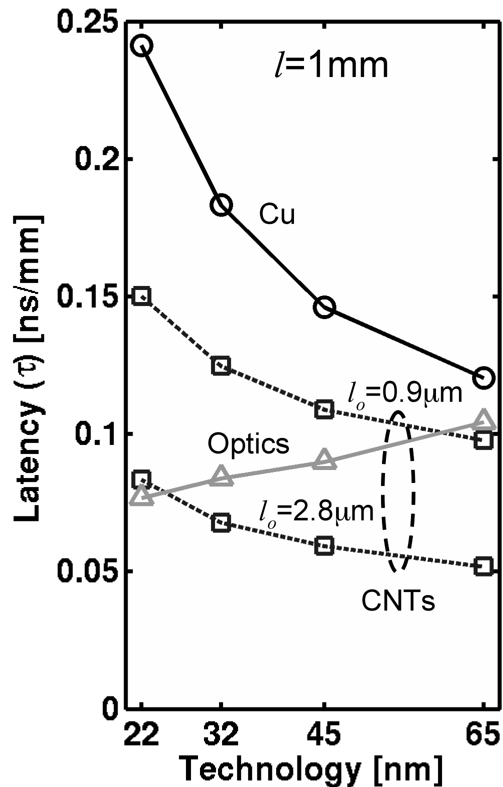


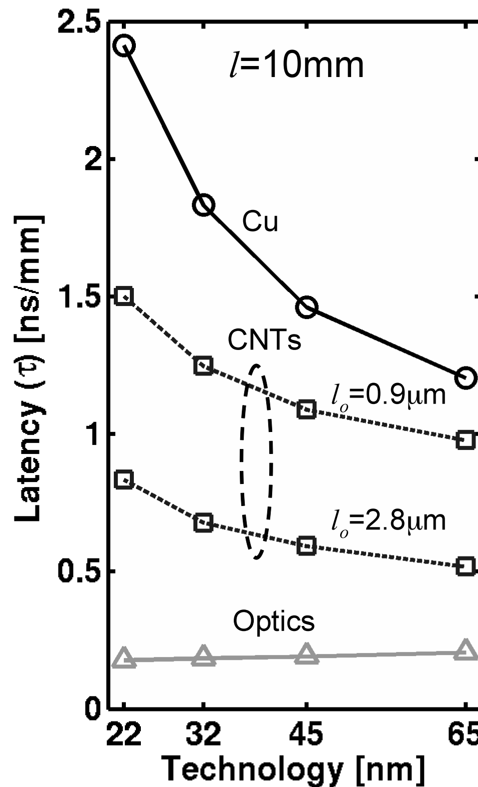
- Tight-binding model: GNR conductivity exceeds Cu at 8nm linewidth
- Best experimental GNR conductivity is comparable to Cu

A. Naeemi et al., EDL Vol.28, pp.428, 2007; R.Murali et al., EDL vol.30, pp.611 2009;

On-chip Interconnect Performance: Latency

Semi-global **Global**





W_{min} for Cu, CNT from ITRS
for optics = 0.6µm
$C_{det}=C_{mod}=10fF$

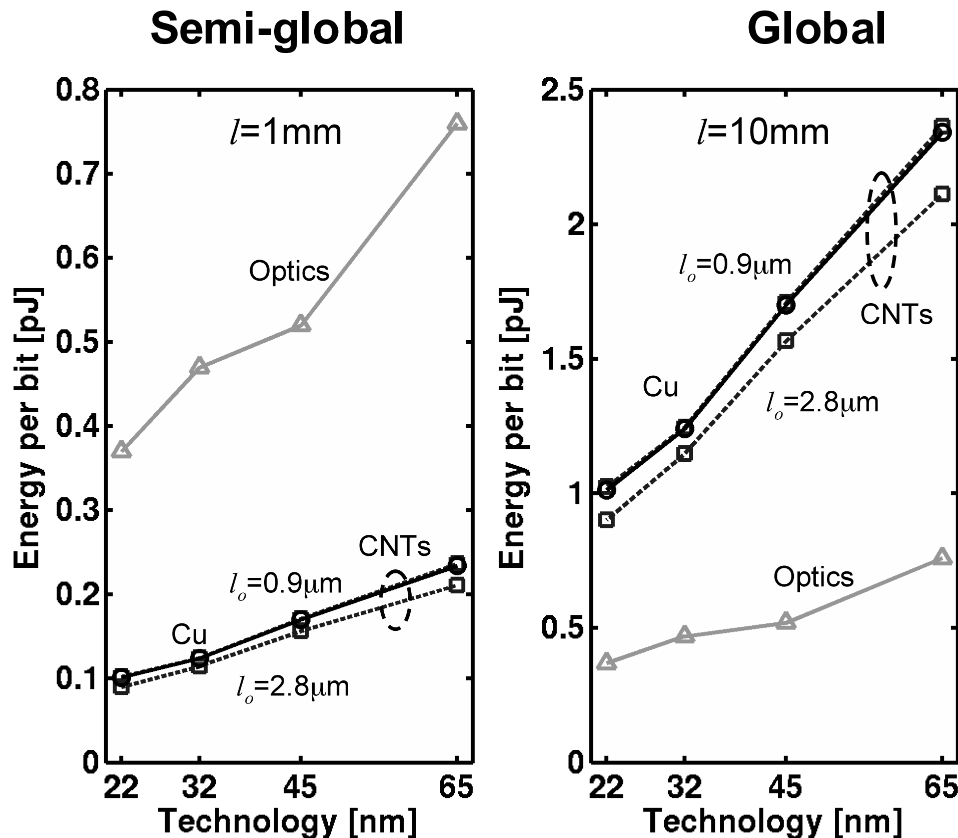
- **Electrical interconnects**
  latency by wire and repeaters

- **Optical interconnect (1 Channel)**
  latency by end devices

- **Cu, CNT: small wire width → more repeaters, wire capacitance → latency ↑**
- **CNTs and optics are favorable for shorter semi-global wires**
- **Optics: transmitter/receiver latency is the main component**
- **Optics favorable for longer wires**

Koo, Kapur and Saraswat, IEEE Trans. Electron Dev., Sept. 2009

On-chip Interconnect Performance: Energy/bit



W_{min} for Cu CNT from ITRS
for optics = 0.6µm
C_{det}=C_{mod}=10fF

- **Electrical interconnects**

power dissipated by wire and repeaters

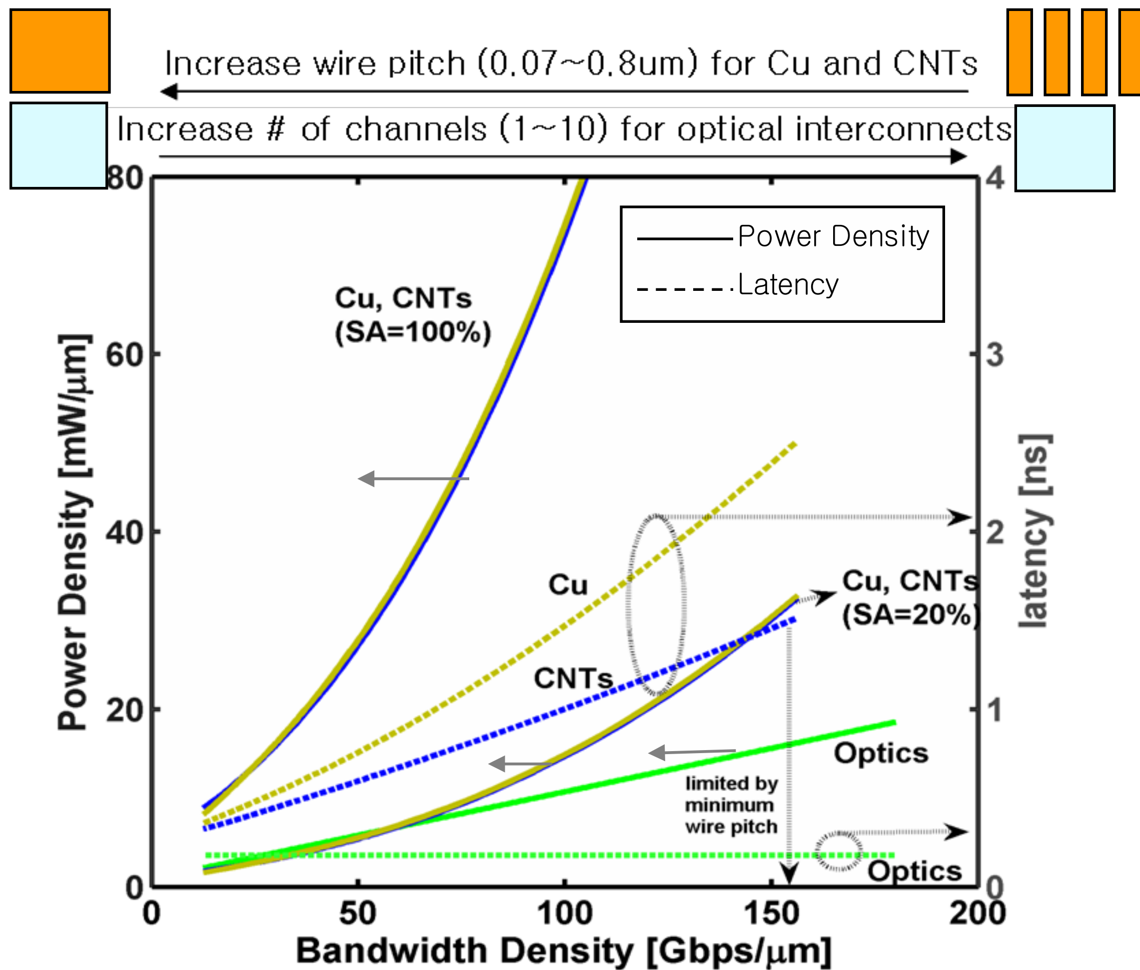
- **Optical interconnect (1 Channel)**

power dissipated by end devices

- **Cu, CNT: small wire width → Energy per bit decreases as wire pitch is scaled (CV^2)**
- **CNTs is favorable for shorter global wire**
- **Optics: transmitter/receiver power is the main component**
- **Optics favorable for longer wires**

Koo, Kapur and Saraswat, IEEE Trans. Electron Dev., Sept. 2009

Comparison Study: Global Interconnect CNTs, Cu, Optics



- **BW density**

  Cu and CNTs: f_{clk} / $pitch_{wire}$

  Optics: no. of wavelength of WDM

- **Power density**

  Cu & CNTs (non-linear):

  Cap and wire pitch

  Optics (linear):

  no. of wavelength

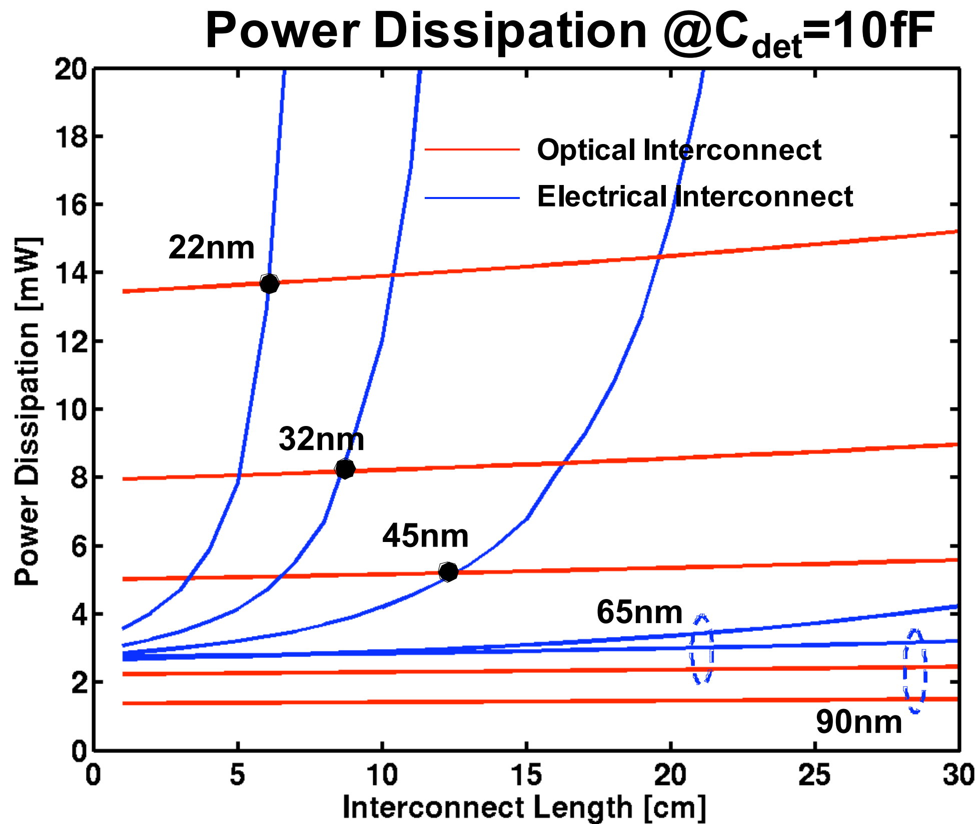
  channel

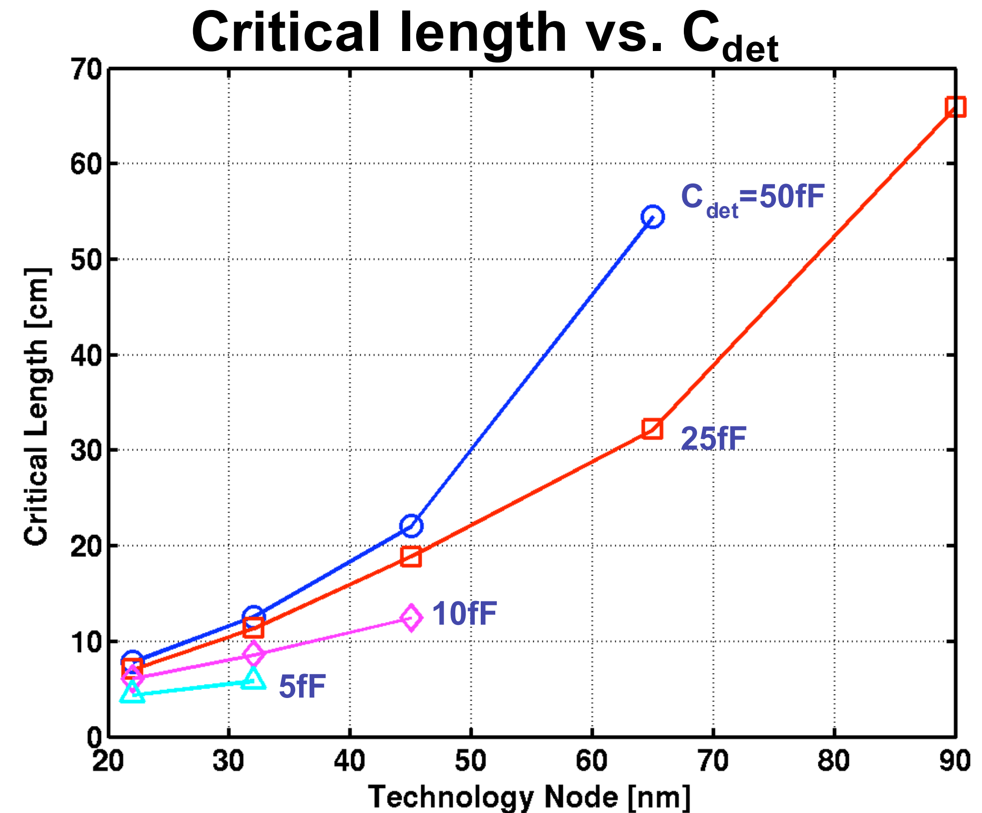
- **Latency**

  Optics < CNTs < Cu

Koo, Kapur and Saraswat, IEEE Trans. Electron Dev., Sept. 2009

Off-Chip Interconnect Performance: Electrical vs. Optical

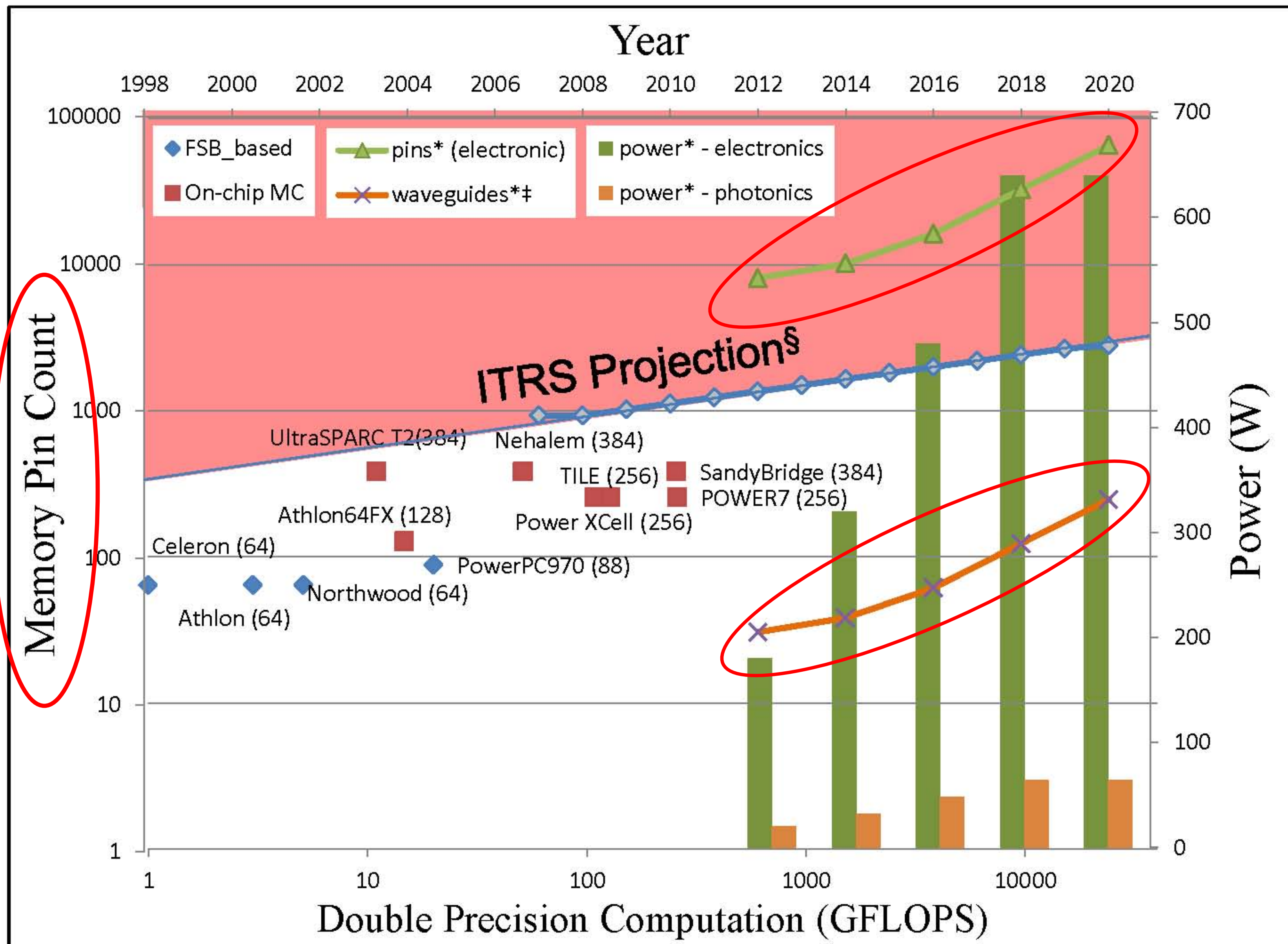




- **Beyond certain length optical I/O is more power efficient**
- **Critical length decreases at higher bit rate & lower detector capacitance**
- **Beyond 32nm Technology node critical length < 10cm**

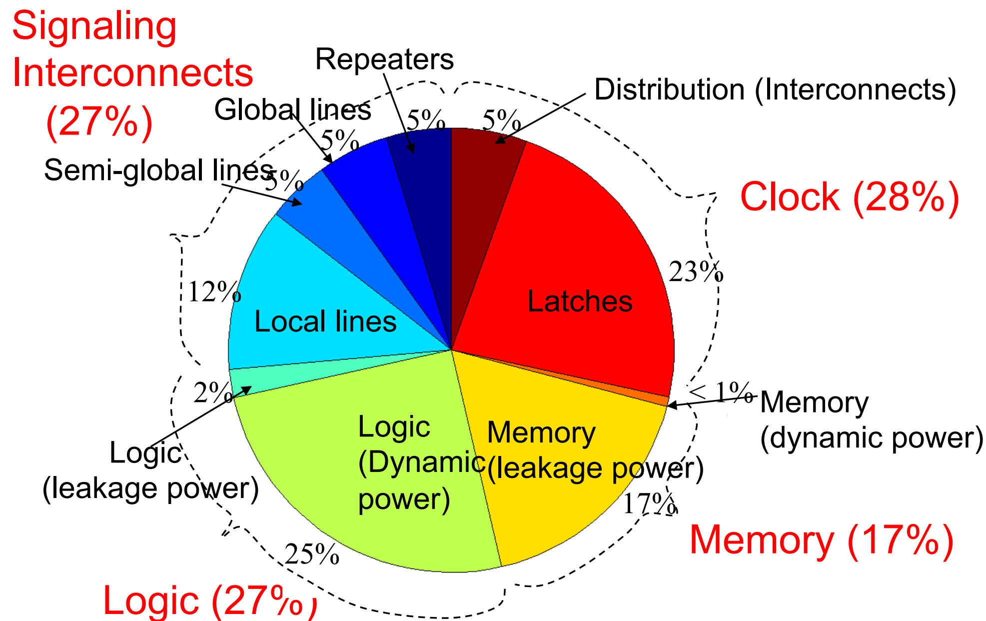
Cho, Kapur and Saraswat, IEEE IITC, June 2005

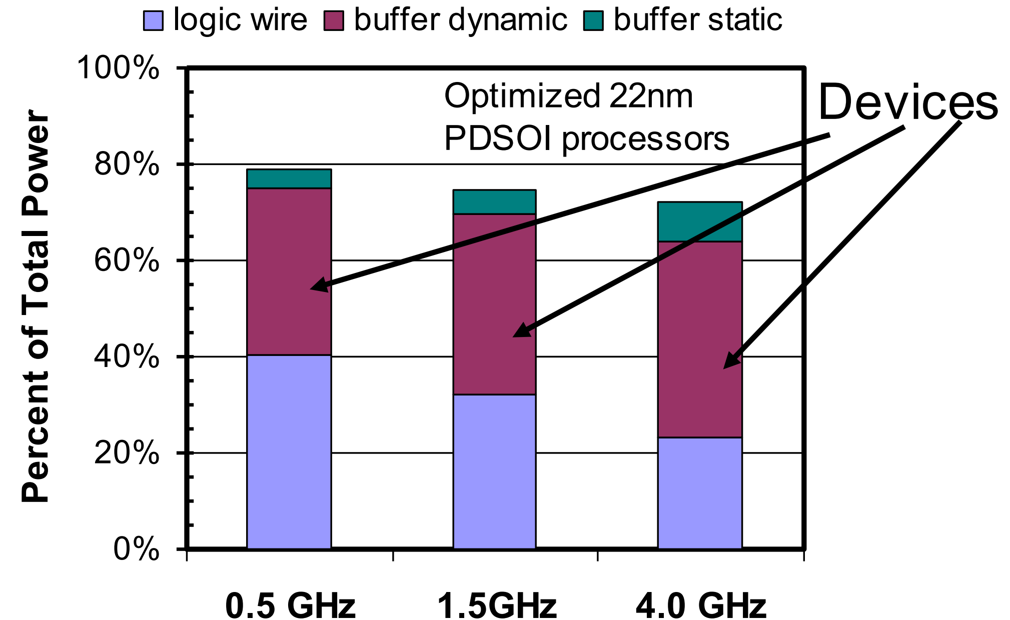
Why Really Photonics?



Source: Keren Bergman, Columbia University

Communication Dominates Power





More than half the power can be attributed to interconnects

70-80% of total logic power is for communication

– Need proper consideration of wires!!

Chandra, Kapur and Saraswat, IEEE IITC, June 2002

Wilfried Haensch, (IBM) Data Abundant Systems Workshop, Stanford Univ., April 2014

Why Off-chip Photonic Interconnects

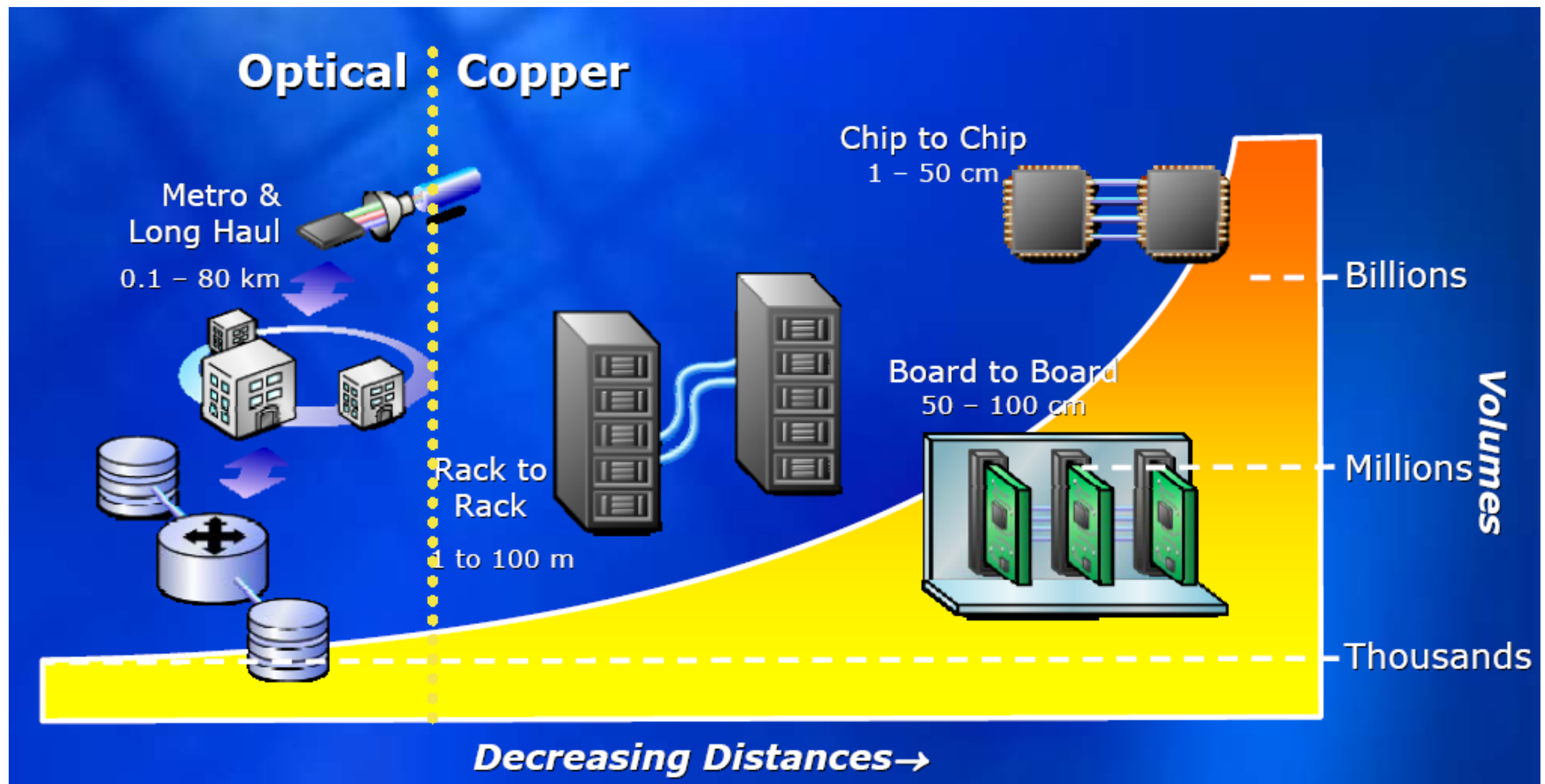
Copper wires

Optical Interconnects

- Copper wires are reaching physical limits
- Photonic interconnects offer the solution for the future

The Interconnect Problem

"For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, RF, or vertical integration … will deliver the solution" (ITRS)

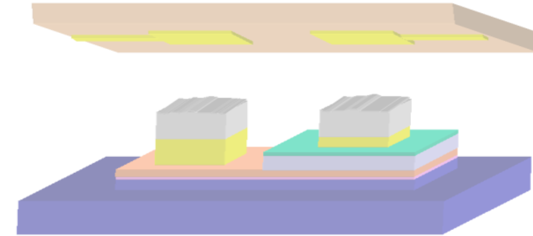


Source: Intel

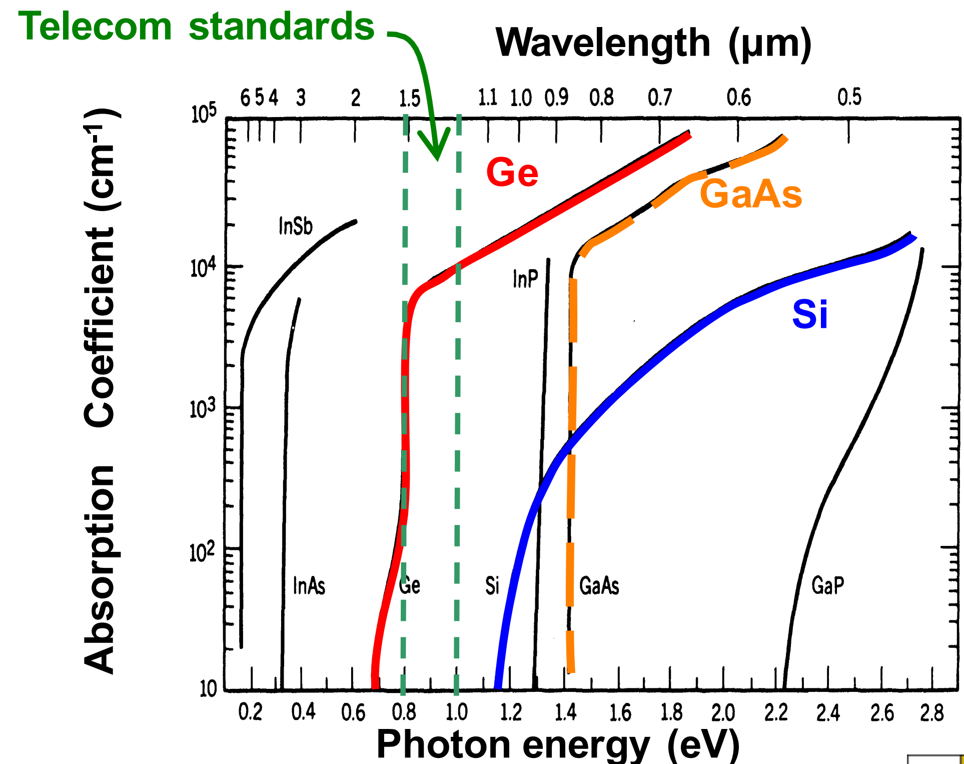
Material Options for Optical Interconnects

- **What are the right optical devices to use?**
  - Need to be cheap, available in large numbers
  - Compatible with CMOS
- **Silicon devices are a long shot**
  - Need 3D heterogeneous integration
- **Flip bond III-V to Si CMOS**
  - Current process
  - Cost, resources, yield?
- **How about germanium?**
  - Bandgap ideal for λ = 1.5 µm
  - Can be monolithically integrated on Si
  - Becomes direct bandgap material by straining or adding tin

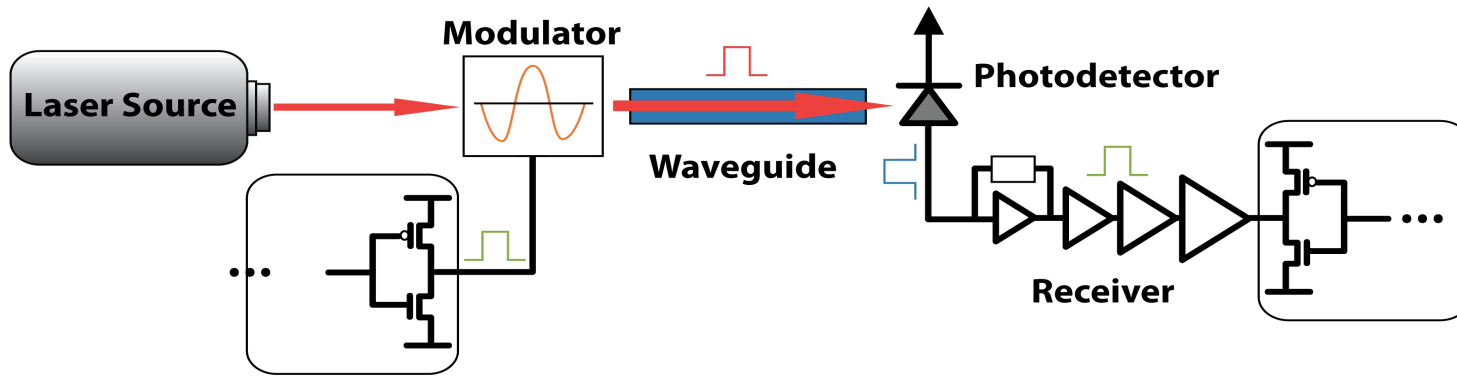
Si CMOS chip with gold bonding pads



GaAs optoelectronic chip with indium flip-chip bumps



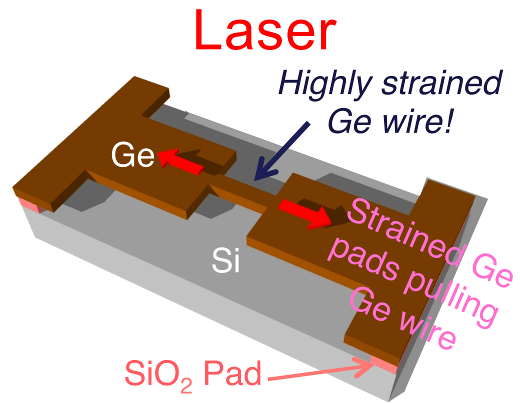
Si Compatible Photonic Interconnect



Laser/modulator converts electrical signal into optical signal

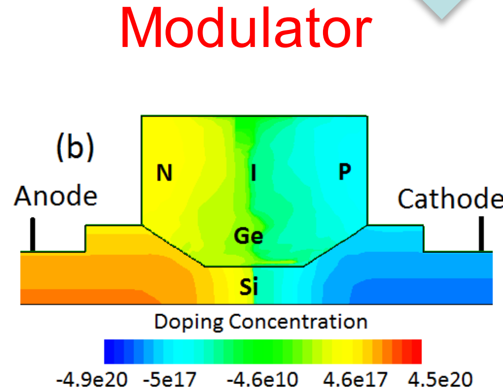
Photodector restores optical signal into electrical signal

Laser



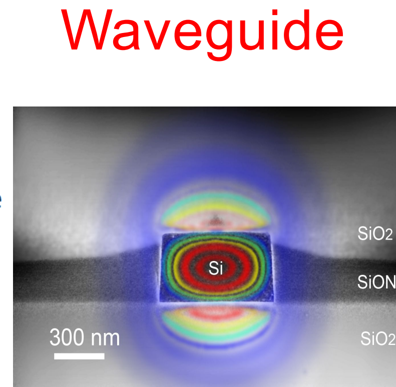
Nam…………Saraswat, Nano Letters, June 11, 2013.

Modulator

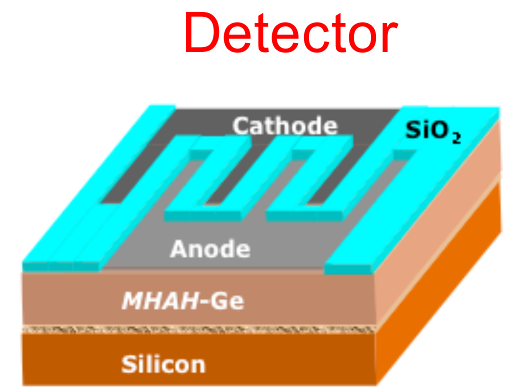


Gupta……….Saraswat, OFC, March 2015

Waveguide



Detector

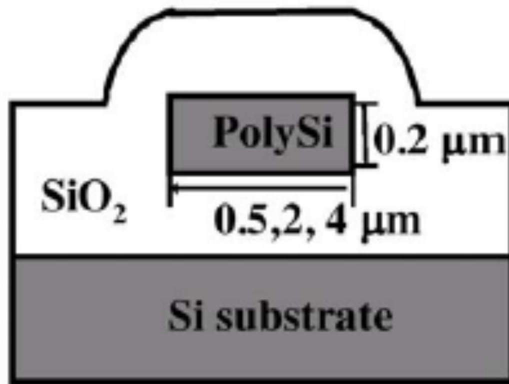


Okyay……… Saraswat, Optics Lett. 2006

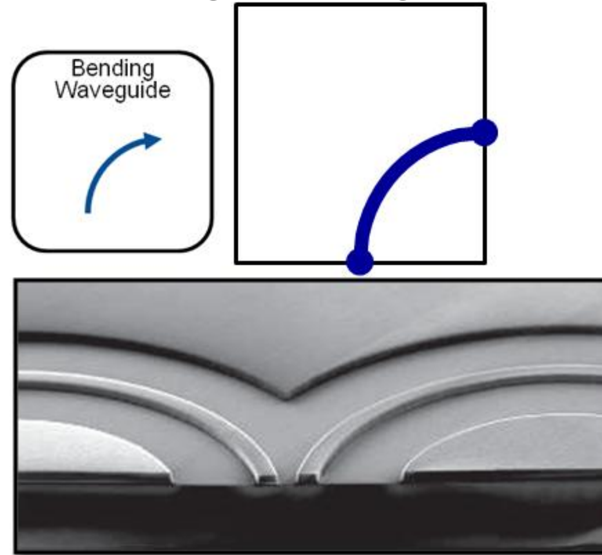
- Germanium devices can be monolithically integrated on silicon
- Laser is the only missing component

Technology for Optical Interconnects on Silicon: Optical Transmission Media

Waveguides

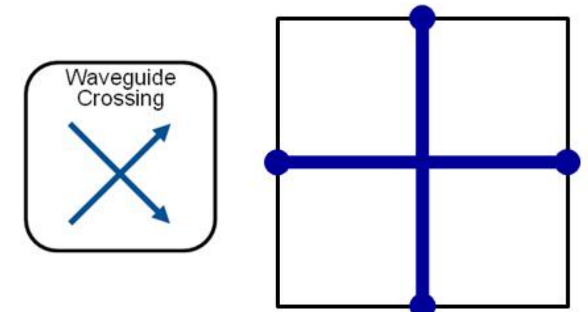


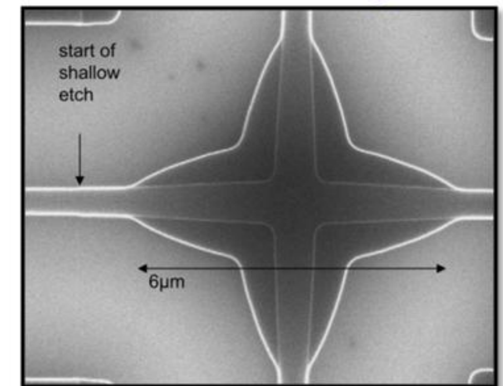
Bending Waveguides



[F. Xia *et al.*, Nature Photonics, 2006]

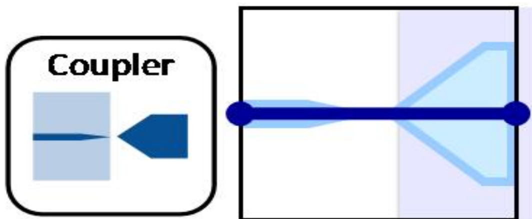
Waveguide Crossings

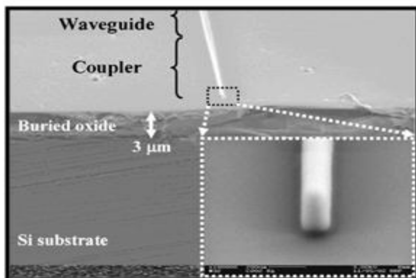




[W. Bogaerts *et al.*, Optics Letters, 2007]

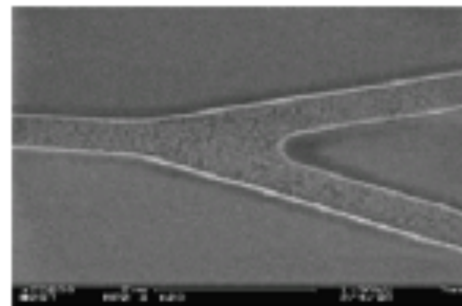
Couplers





[V. Almeida *et al.*, Optics Letters, 2003]

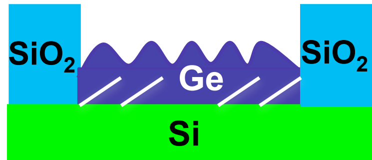
Splitter



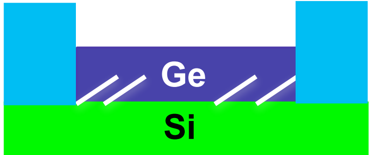
(Kimmerlingr, MIT)

Selective and Lateral Overgrowth of Ge on SiO_2

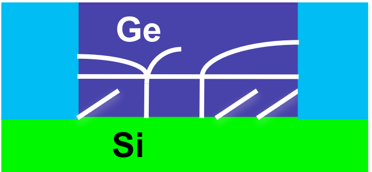
1st Ge epitaxial growth



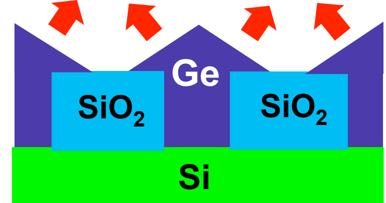
H_2 annealing 825°C



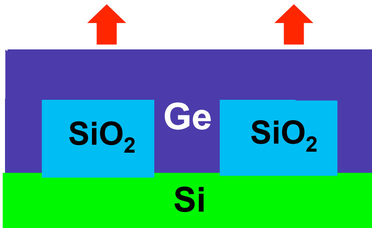
2nd Ge growth + H_2 anneal



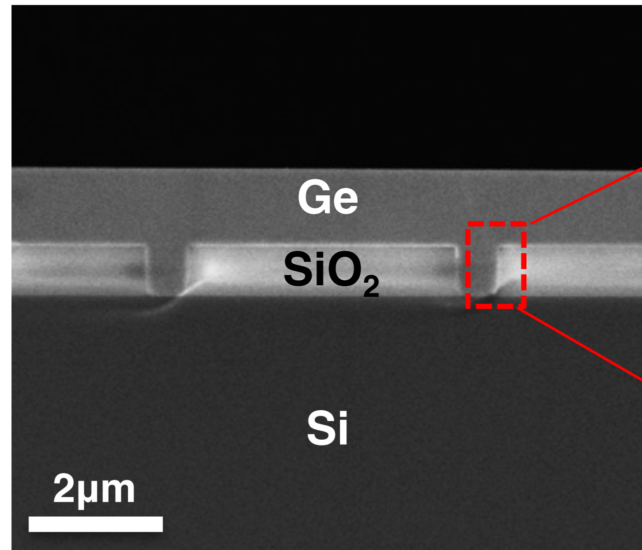
<311> Direction Growth



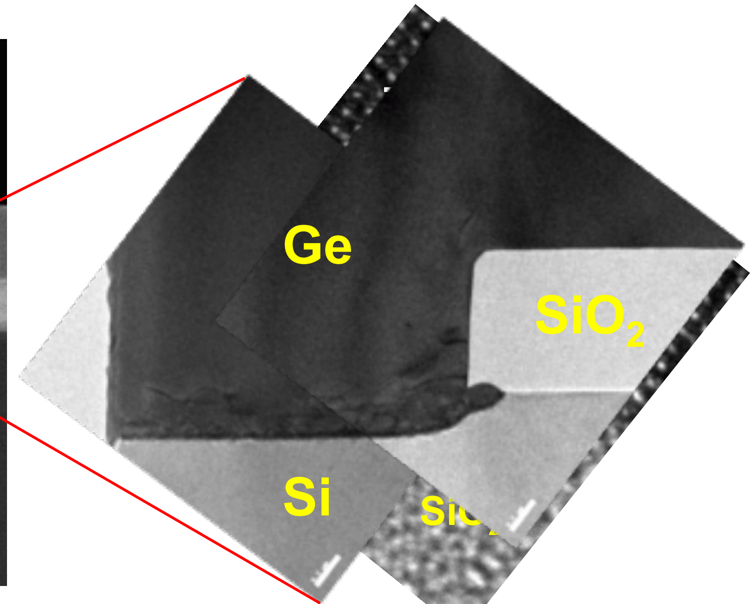
<100> Direction Growth



SEM



X-TEM



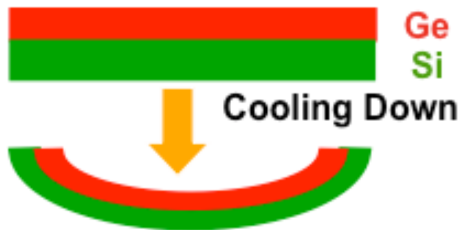
400°C deposition + 800°C H_2 anneal + 600°C deposition

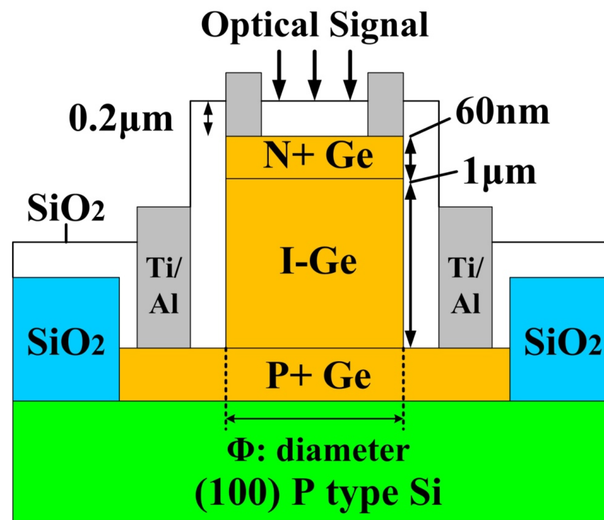
- Lateral Ge growth on SiO_2 window achieved
- Dislocation density of Ge on SiO_2 < 10^6 cm^{-2} (same thickness Ge on Si: 1×10^8 /cm^2)
- Surface RMS roughness ~0.4 nm after CMP
- Ge is ~0.2% strained due to thermal mismatch with Si

Ju Hyung Nam...........K. Saraswat, J. Crystal Growth, April 2015

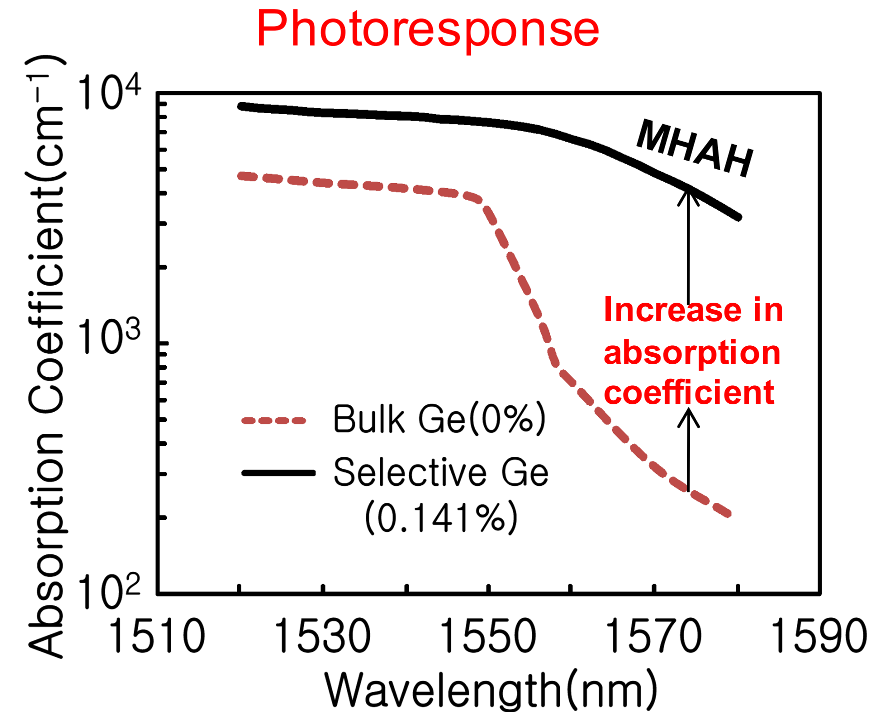
High Efficiency Ge p-i-n Photodetectors on Si

Biaxial Tensile Strain





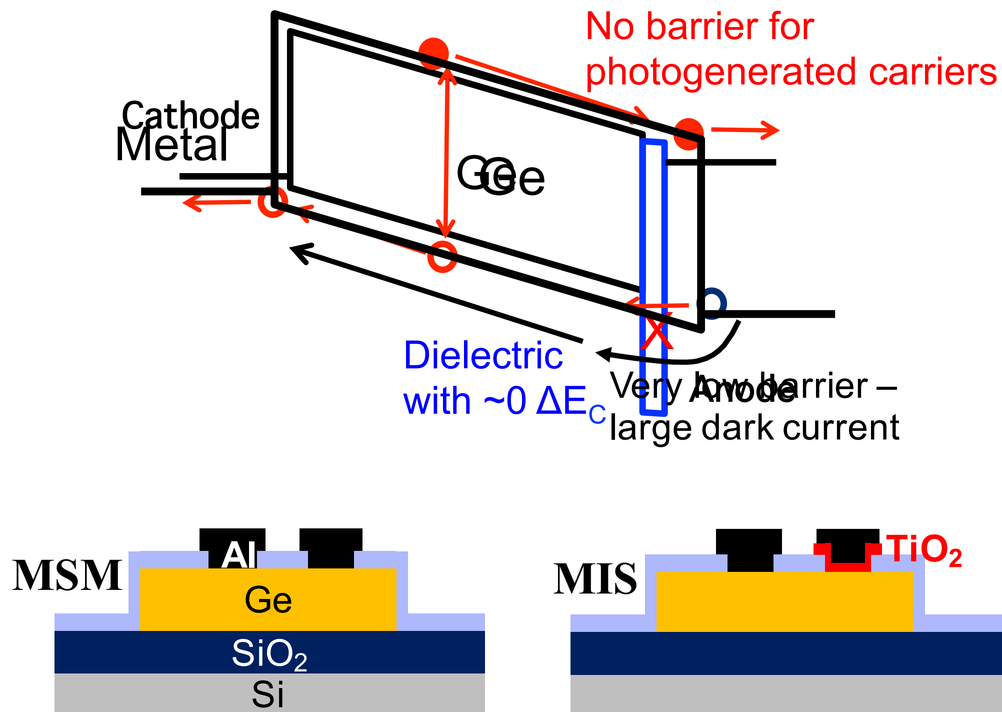
Photoresponse

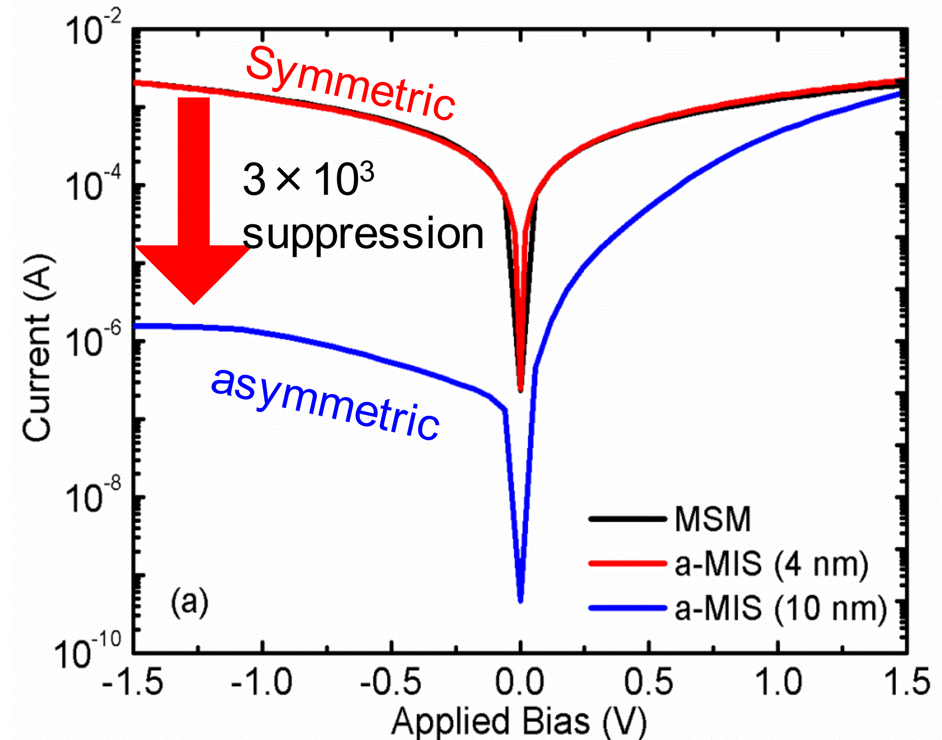


- Ge grown on Si by **M**ultiple **H**ydrogen **A**nneal and **H**eteroepitaxy (MHAH) Technique
- Ge film complies with Si substrate on cooling down resulting in tensile strain => bandgap reduces
- Detector efficiency improves at 1550nm due to tensile stress
- Dark Current high

Hyun-Yong Yu,……….. K. Saraswat, IEEE Electron Dev. Lett., Nov. 2009.

High Efficiency Ge MSM Photodetectors on Si



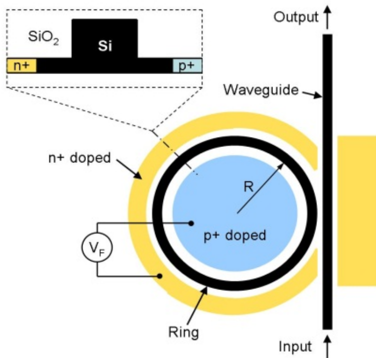


Ju Hyung Nam..........K. Saraswat, (To be published)

- Fermi level pins near valance band in Ge ⇒ high dark current
- At anode insert a dielectric to depin metal Fermi level
- Choose dielectric with ~0 ΔE_C to allow electron flow but large ΔE_V to block holes
- No barrier seen by photocarriers, thus large photocurrent
- Under the reverse bias (PD operation), large barrier between metal & Ge
  - Dark current is reduced by 3×10^3

Optical Modulator

Electro-optic Modulators

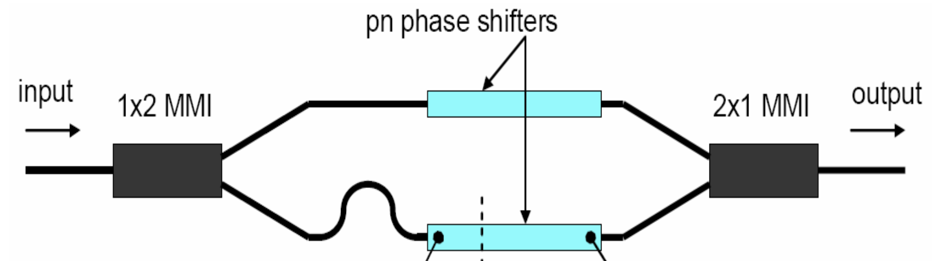


- Index change
- Weak mechanism
- High Q
- Temperature tuning

Lipson (Cornell)

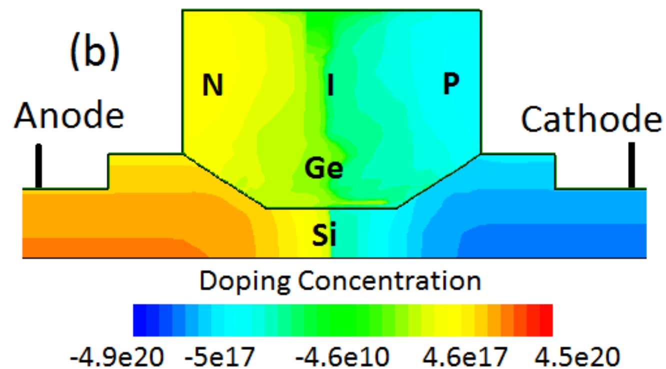
Mach-Zehnder Modulators

- Phase shift effect in waveguides
- Large size and power consumption



Electro-absorption Modulators

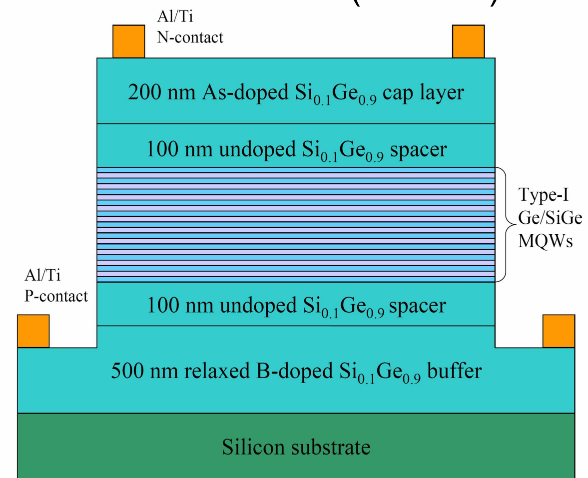
Saraswat (Stanford)



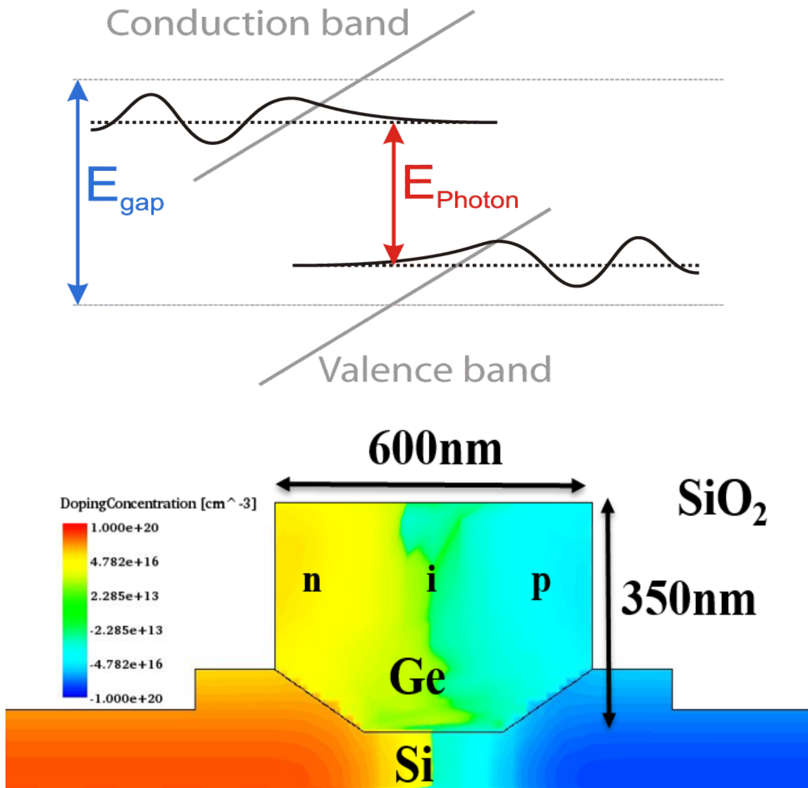
- Franz-Keldysh effect in bulk material

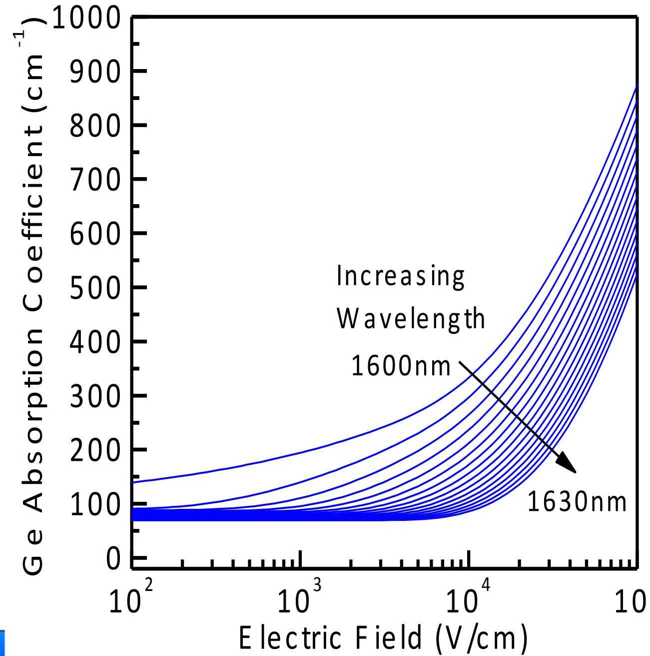
QCSE Ge/SiGe Modulator

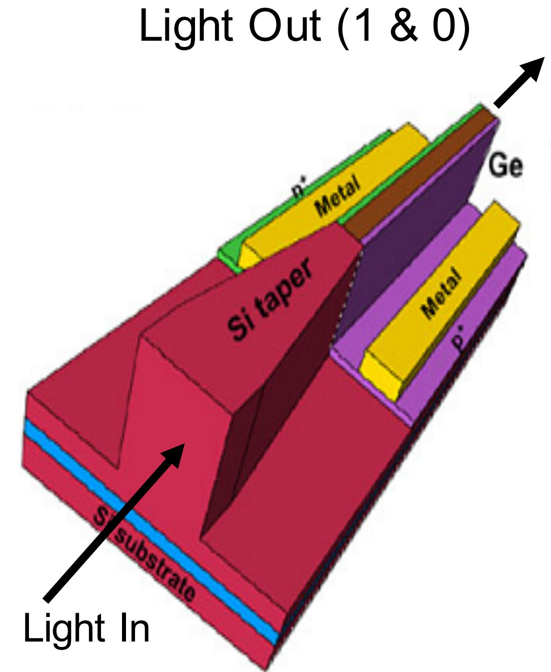
Harris and Miller (Stanford)

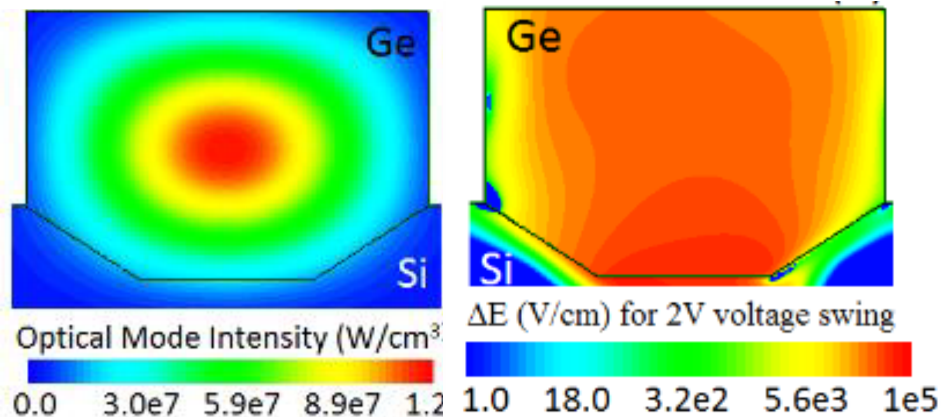


Ge/Si Electro-Absorption Franz-Keldysh Effect Modulator







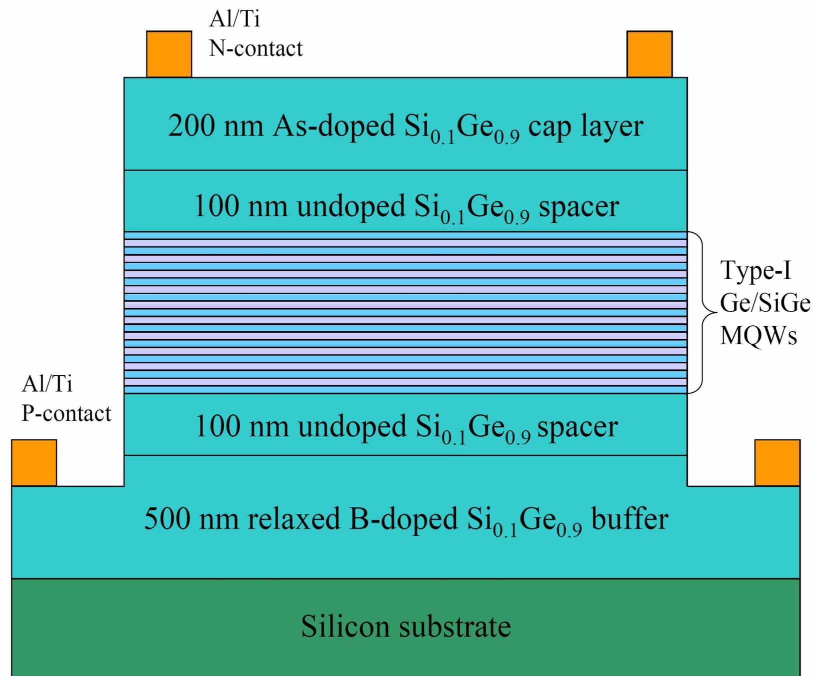


In the presence of an electric field, the conduction and valence bands of a semiconductor tilt. Application of an electric field leads to overlap in valence and conduction band wave functions, and hence optical absorption, at energies below the semiconductor bandgap.

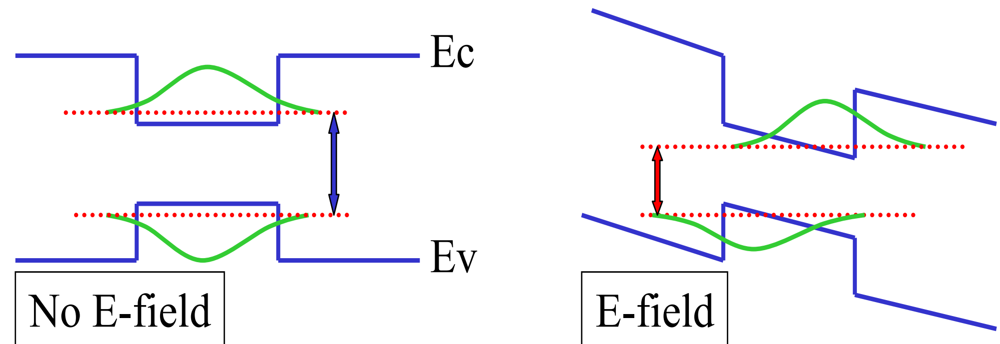
S. Gupta………………K. Saraswat, OFC, Los Angeles, Paper No. Tu2A.4, March 2015

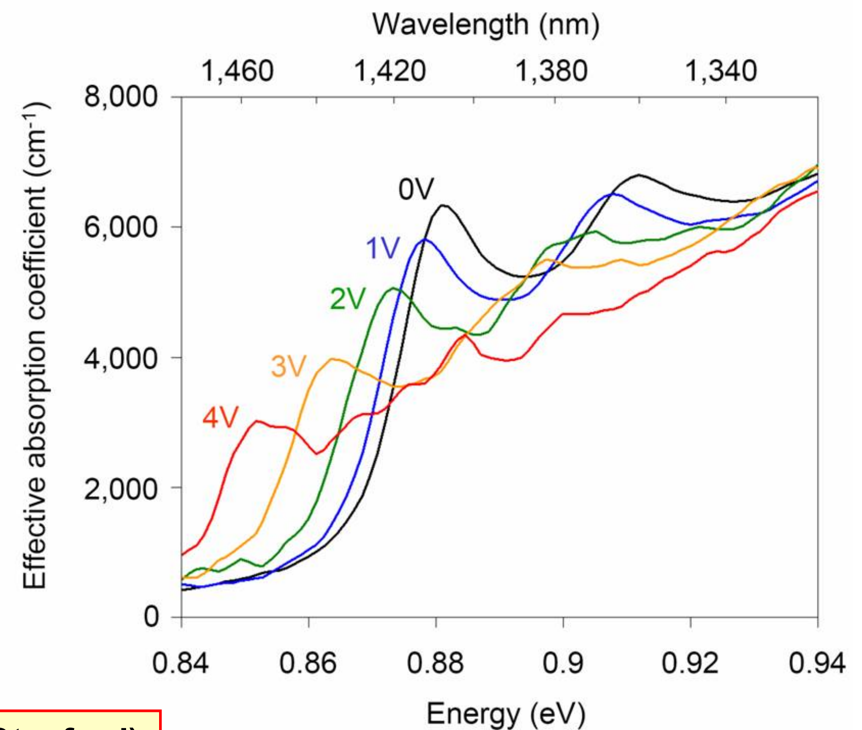
SiGe Optical Modulator

Ge/SiGe Quantum Well Modulator



Quantum Confined Stark Effect Ge/SiGe

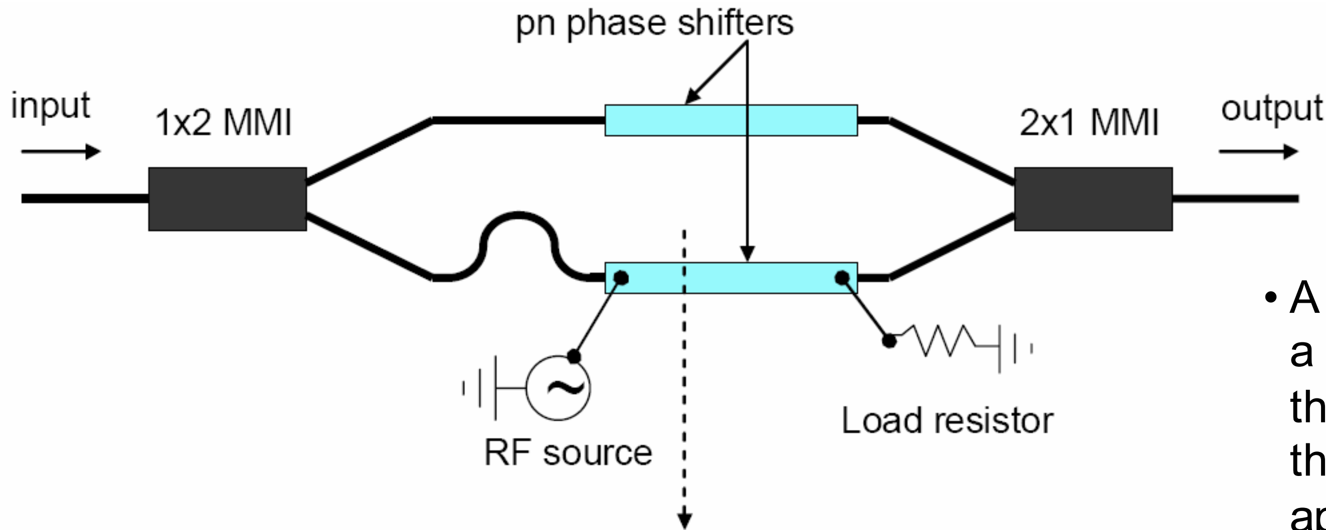


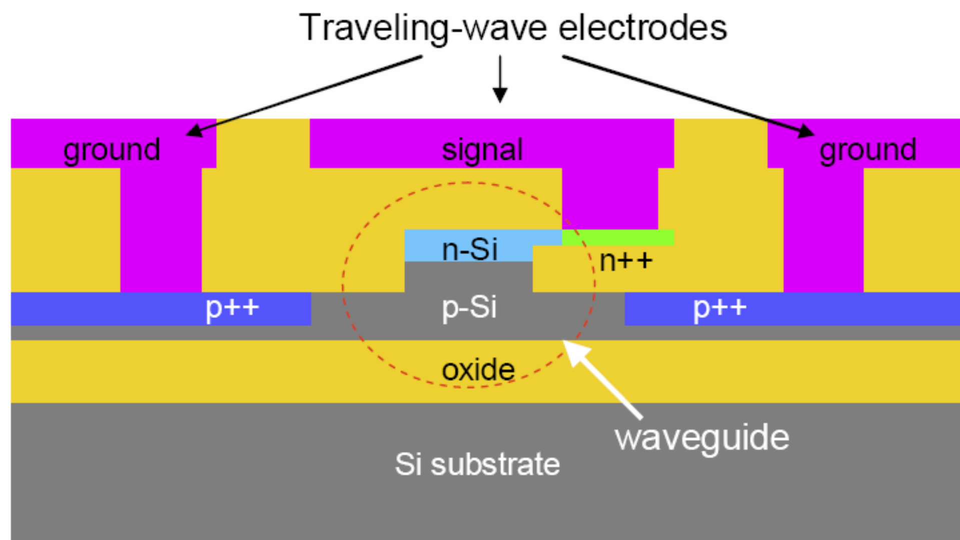


- **QCSE in Ge quantum wells on Si substrates**
  - With E-field, the potential wells get tilted.
  - This changes the energy levels and reduces wavefunction overlap
  - Reduced strength of light absorption
  - Absorb at longer wavelength
  - Fully compatible with CMOS fabrication

Harris and Miller Groups (Stanford)

Mach-Zehnder silicon waveguide modulator

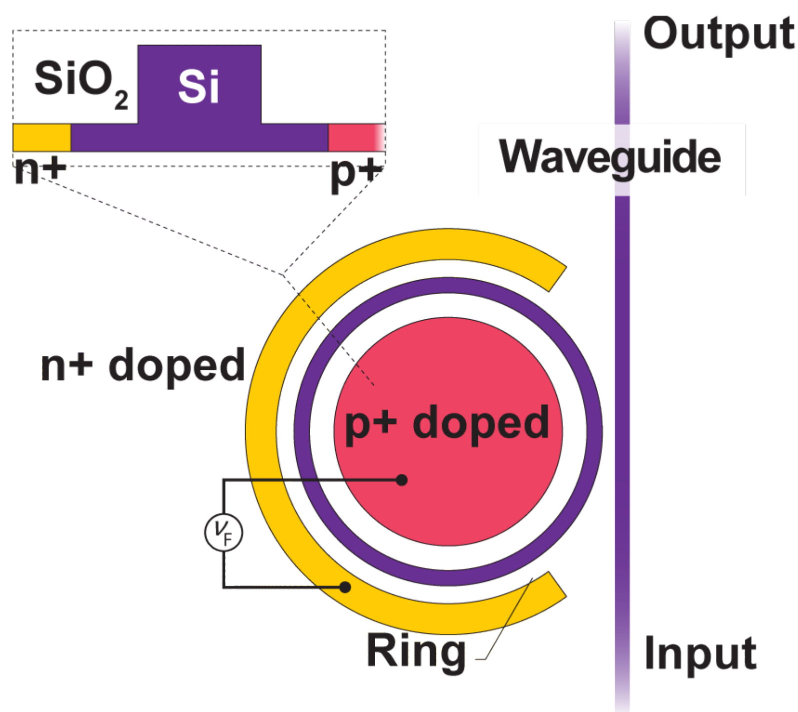


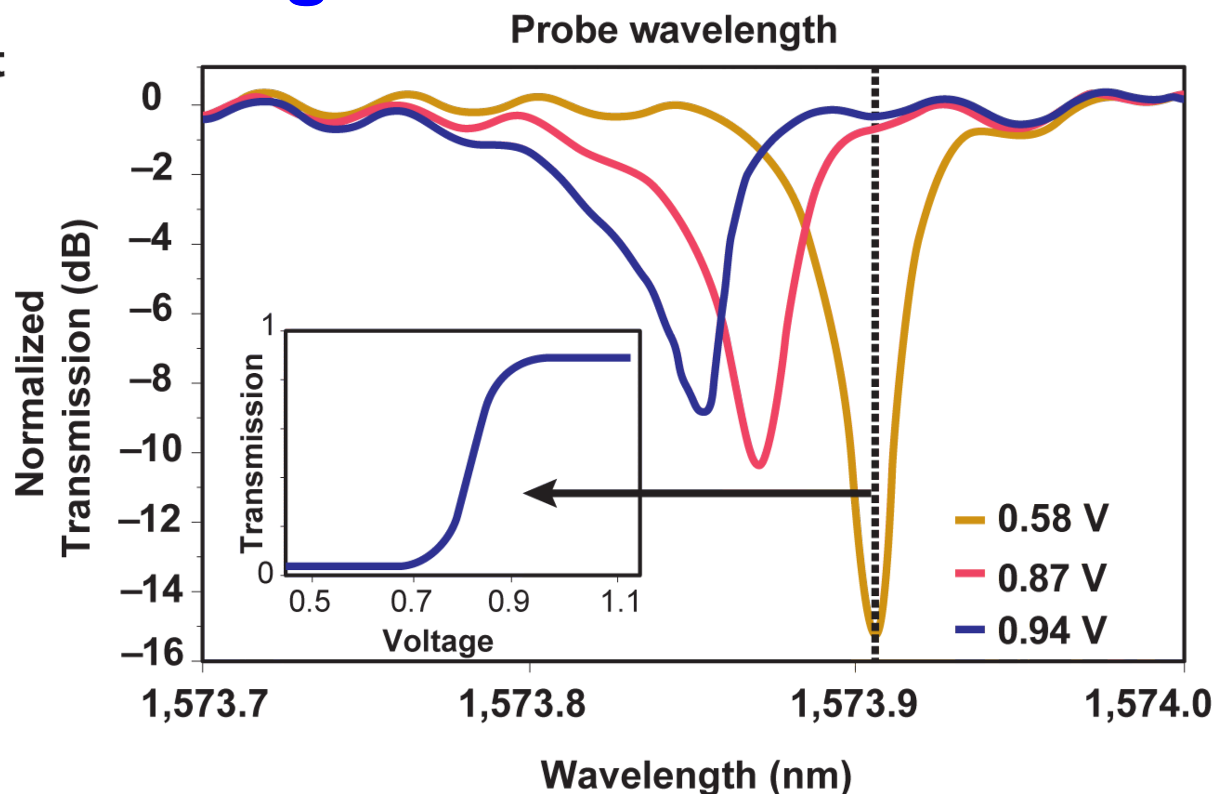


- A Mach-Zehnder interferometer is a waveguide-based device where the mode is split into two arms of the interferometer. An electric field applied to one of the arms changes the refractive index, which shifts the relative phase of the two propagating waves such that they constructively or destructively interfere at the output.
- Large size, several hundred μm
- High power consumption ~ 5 pJ/bit

A. Liu, et al., Opt. Express 15, 660 - 668 (2007).

Silicon micro-ring modulator





Light recirculates inside the micro-ring, where it acquires a phase that is dependent upon the refractive index, which is modulated by carrier depletion or other means inside a PN junction. A portion of the light is coupled back into the output waveguide on every pass. Destructive interference occurs at a specific wavelength that is dependent on the refractive index. Hence, modulation of the amplitude at the output waveguide can be achieved by moving the micro-ring resonance into or away from the laser wavelength.

- Weak mechanism
- High Q needed - difficult to fabricate the micro-rings with precise dimensions
- Temperature tuning takes too much power

G. T. Reed, et al., Nature Photon. **4**, 518 - 526 (2010)

Summary of the Modulator Work

- Silicon photonics - A key enabling technology for future CMOS systems
- Deployment Targets
  - Energy Consumption ~100fJ/bit for off chip and a few fJ/bit for global on-chip interconnects
  - High enough bandwidth to match the transistor speed and end user needs
  - Compact area
- This work
  - Ge electro-absorption modulators (EAMs) based on Franz-Keldysh Effect (FKE)
  - Demonstrated best energy-delay product for CMOS compatible modulators

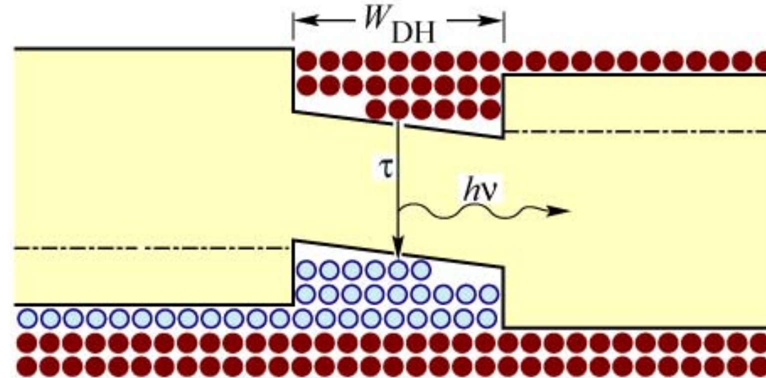
Modulator Type	3dB BW (GHz)	Modulator Capacitance (fF)	V Swing (V)	Active Footprint (μm^2)	ER (dB)	IL (dB)	Optical BW (nm)
This work	**50**	**10**	**2**	**24**	**4.6**	**4.1**	**>35**
GeSi FKE [2]	34	69.6	2	40	3.8	4.8	40
GeSi FKE [3]	1.2	11	3	30	8	3.7	14
GeSi QCSE* [4]	3.5	3	1	8	3.2	15	20
GeSi QCSE* [5]	6.3	200	3	400	4	3	20
Si MZI** [6]	30	~800	1.5	~1500	3.4	7.1	>80
Si Ring [7]	21	~17	0.5	20	6.4	1.2	<0.1

* QCSE – Quantum Confined Stark Effect **MZI – Mach-Zehnder Interferometer

S. Gupta,……..........K. Saraswat, OFC, Los Angeles, Paper No. Tu2A.4, March 2015

Structure Needs for Efficient Lasing

Heterojunction



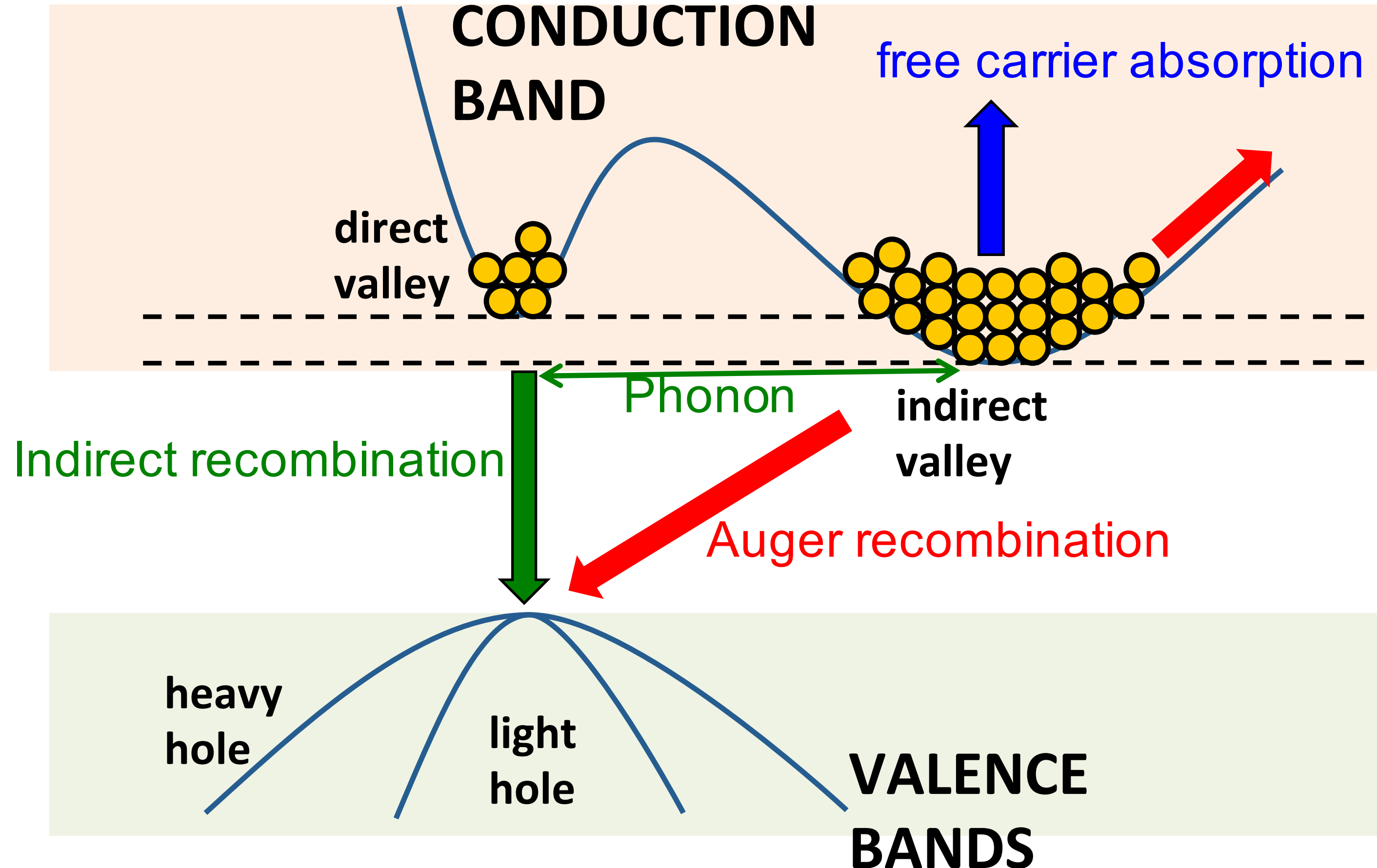
For efficient laser

- Direct bandgap cavity
- Hetrojunction quantum well for carrier confinement

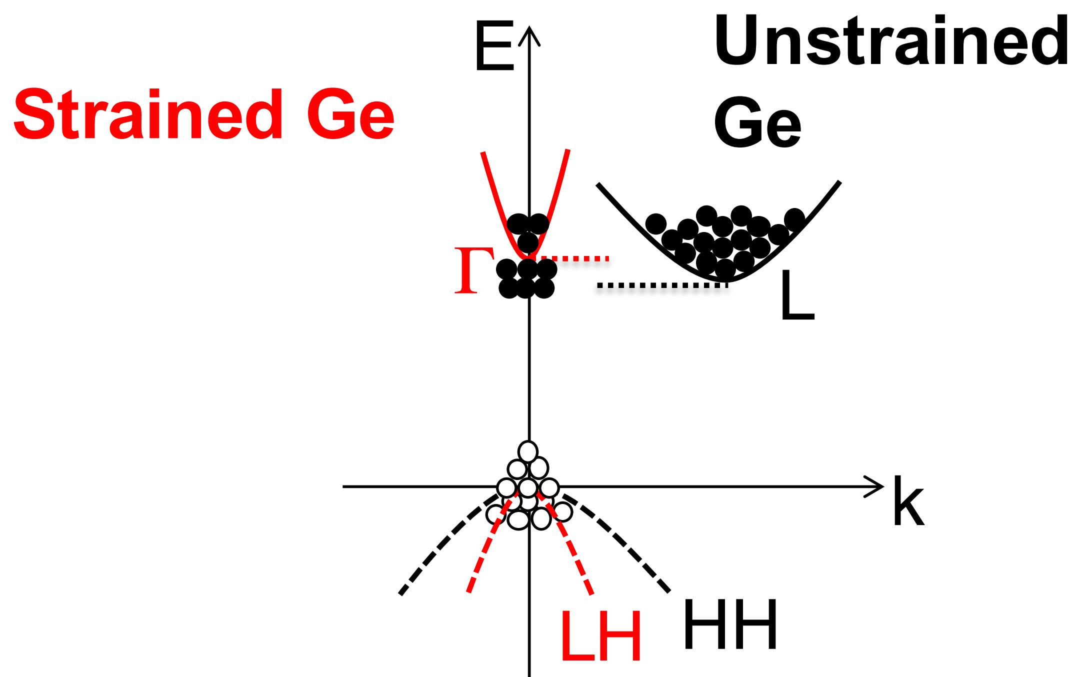
E. F. Schubert, Light Emitting Diodes (Cambridge Univ. Press)

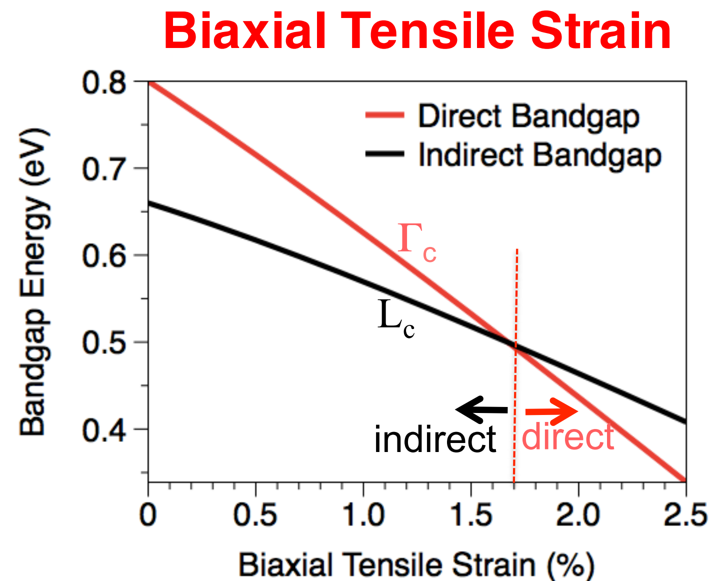
Engineering Ge for light emission- Doping

- N-type doping can be used to fill electrons into the L valley upto the level of Γ valley
- But it is difficult to heavily dope Ge n-type
- Increases free carrier absorption and auger recombination
- Inefficient light emission

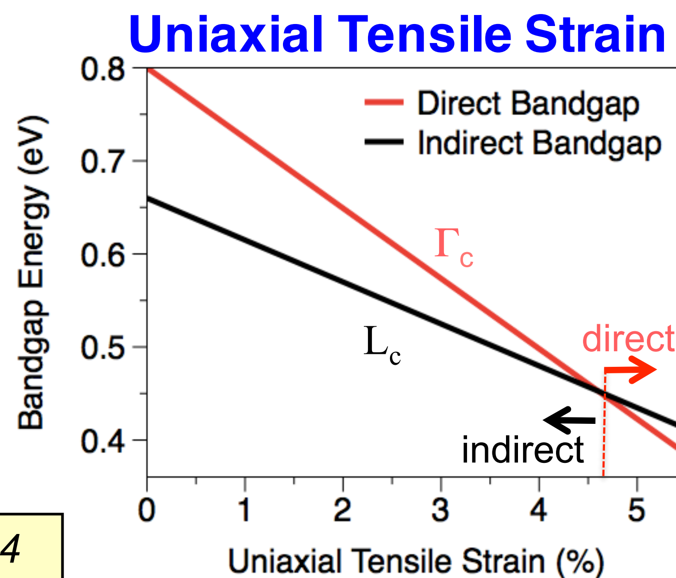


Engineering the Ge band structure for light emission: Strain



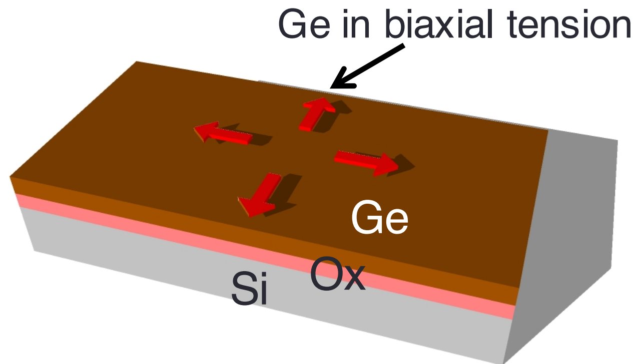


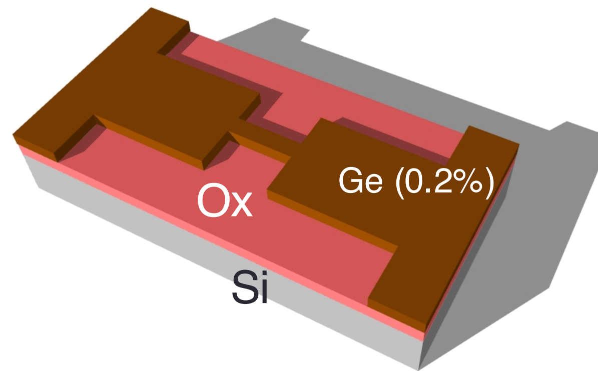
>1.7% biaxial tensile strain or
> 5% uniaxial tensile strain
turns Ge into a direct bandgap material, making light emission possible

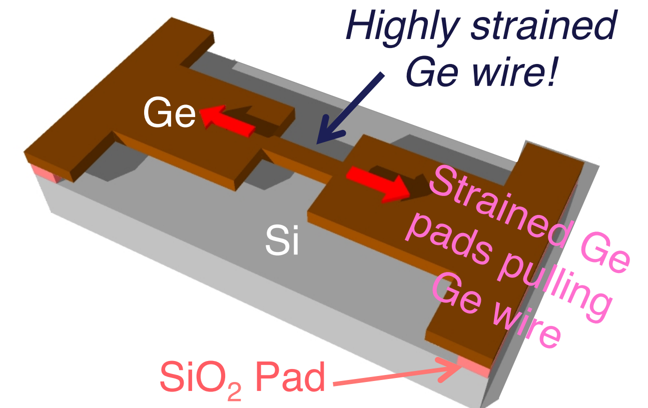


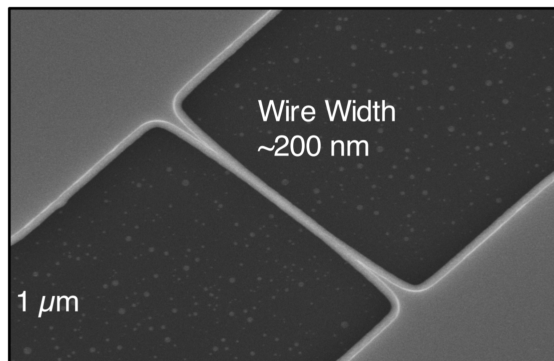
Sukhdeo,.......... Saraswat, Photonics Research, 2014

Geometrical Amplification of Strain

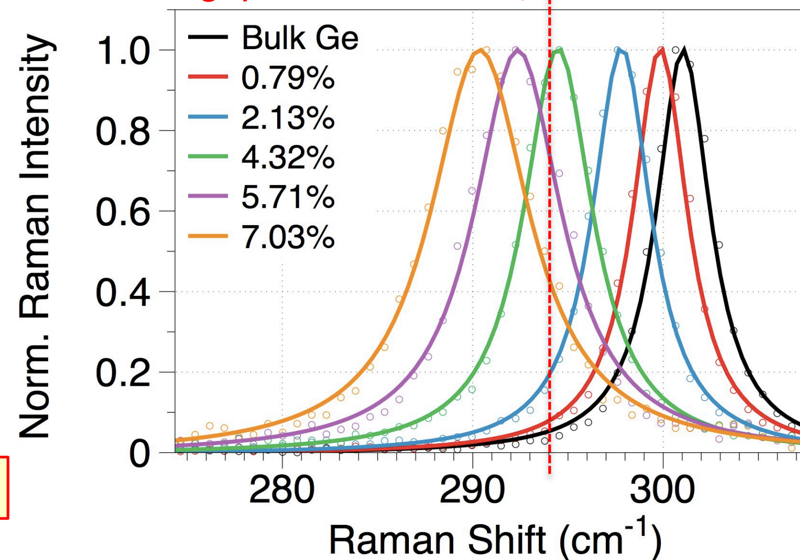








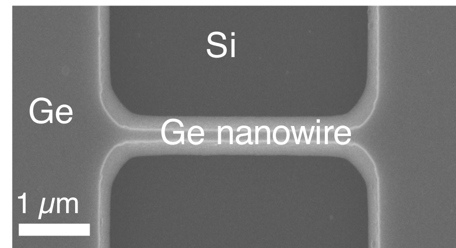
Raman measurements



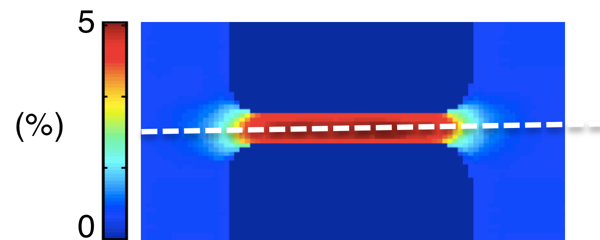
Nam, Saraswat, et al., Nano Letters, June 11, 2013.

Heterostructure in a Single Material: Strained Ge

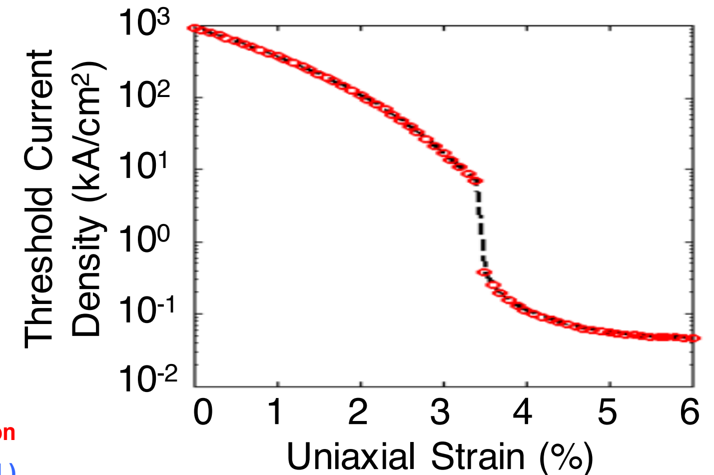
SEM



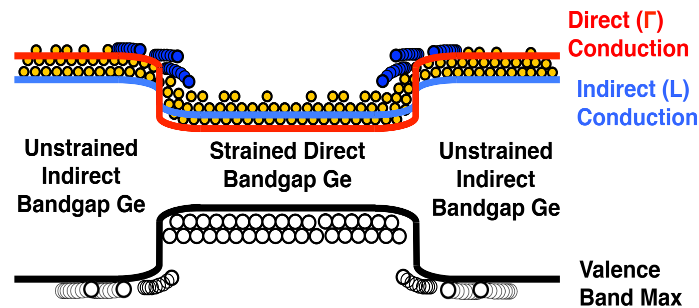
2D Strain Distribution



Threshold Current Simulations



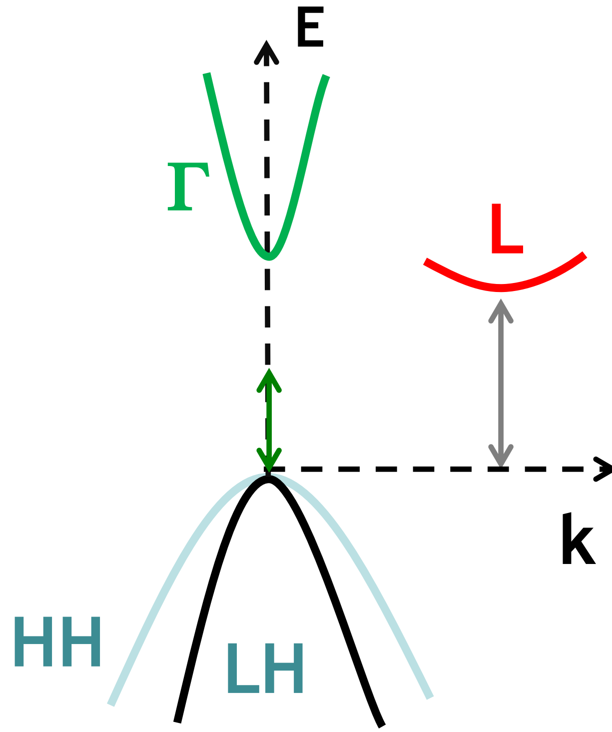
Band Diagram

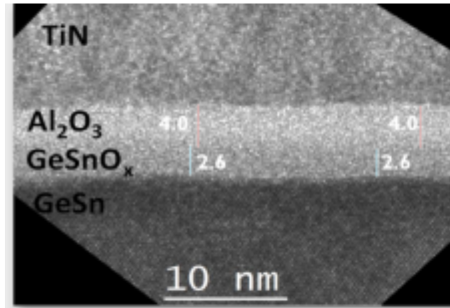


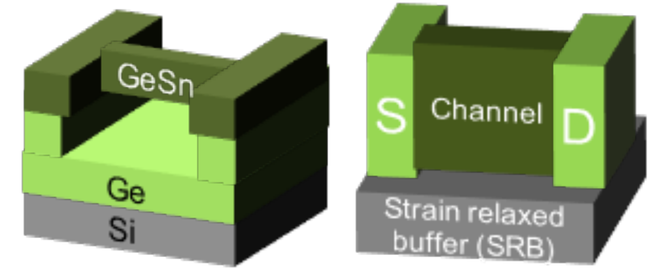
- Strain can be tunable with geometry
- Heterostructure created due to reduction in bandgap of strained Ge
- Direct bandgap cavity and hetrojunction quantum well in single material

Nam, Saraswat, et al., Nano Letters, June 11, 2013.

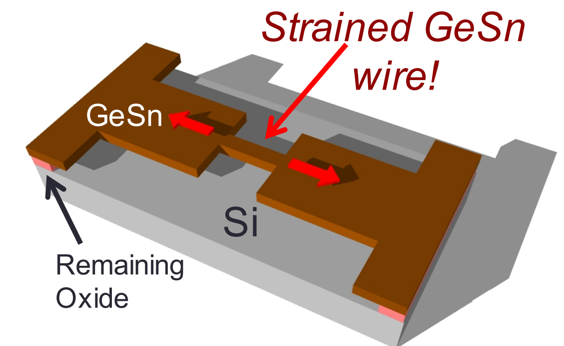
Engineering the Ge band structure by alloying with tin for GeSn CMOS and photonics



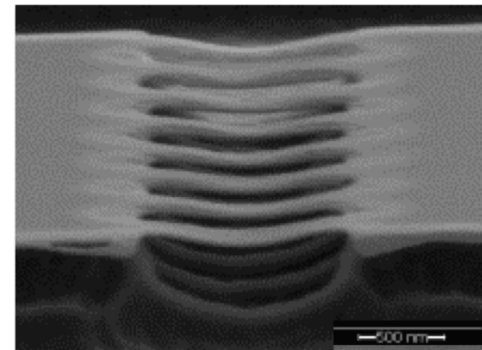


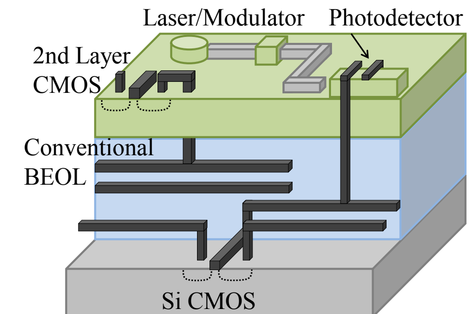


Strain engineering in FinFETs



Si-compatible Laser



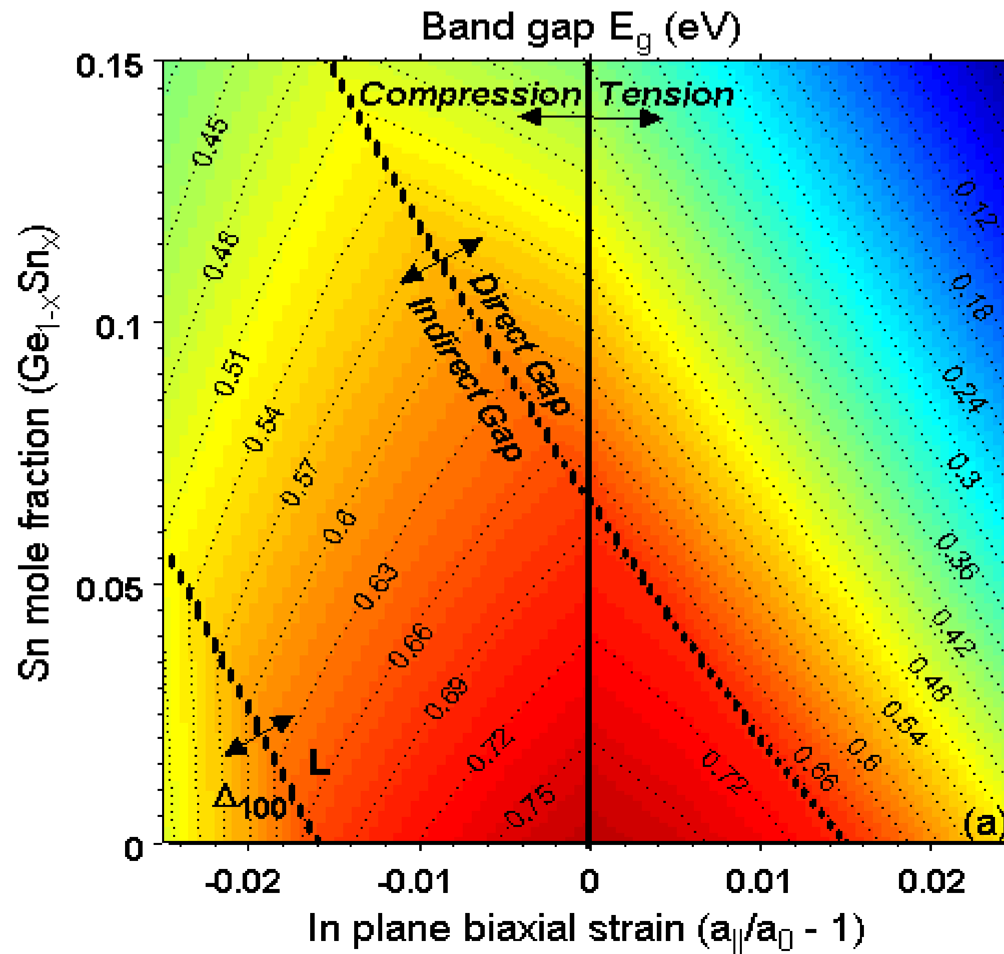


At ~ 7 Sn% $Ge_{1-x}Sn_x$ becomes direct band gap!

Gupta, Yeo, Takagi, Saraswat, et al., MRS Bulletin, Aug 2014

3-D IC: CMOS, Photonics co-integration

Multiple Knobs to Turn for Direct-Gap: Strained GeSn



- A combination of alloying Ge with Sn and strain can also give us a direct bandgap material
  - Efficiency would be comparable to present III-V lasers

Gupta, Magyari-Köpe, Nishi, Saraswat, J. Appl. Phys. **113**, 073707 (2013)

Direct Bandgap GeSn Microdisk Lasers at 2.5 µm for Monolithic Integration on Si-Platform

S. Wirths[1], R. Geiger[*,**], C. Schulte-Braucks, N. von den Driesch, D. Stange, T. Zabel[*], Z. Ikonic[***], J.-M. Hartmann[****], S. Mantl, H. Sigg[*], D. Grützmacher and D. Buca

PGI 9 and JARA-FIT, Forschungszentrum Juelich, Germany, [*]LMN, Paul Scherrer Institut, Villigen, Switzerland, [**]IQE, ETH Zürich, Switzerland, [***]IMP, Univ. of Leeds, UK, [****]Univ. Grenoble Alpes & CEA, LETI, MINATEC Campus, Grenoble, France
([1]E-Mail: s.wirths@fz-juelich.de, Phone: +49 2461 61 3149, Fax: +49 2461 61 2940)

Abstract

We report on the first experimental demonstration of direct bandgap group IV GeSn microdisk (MD) lasers (λ_{em}=2.5 µm) grown on Si(001). The evidence of lasing is supported by a detailed analysis of strain-dependent emission characteristics of GeSn alloys with $x_{Sn} \geq 12$ at.%. Residual compressive strain within the layer is relieved via under-etching of the MD enabling increased energy offsets up to E_L-E_Γ=80 meV. The lasing threshold and max. temperature amount to 220 kW/cm^2 and 135 K, respectively.

Introduction

The demonstration of optically pumped lasing in CMOS-compatible group IV GeSn alloys [1] along with

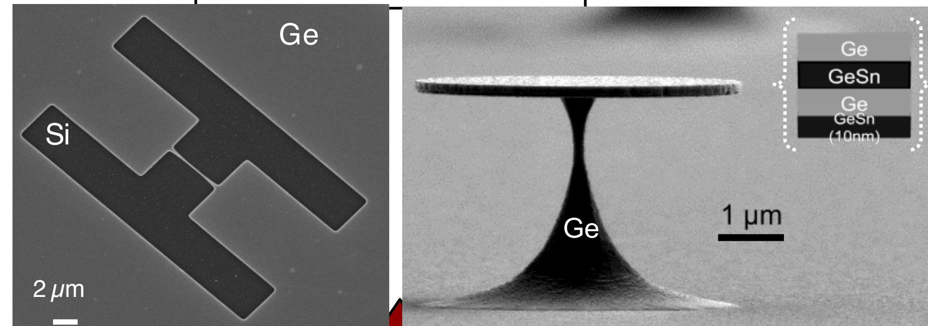
gap GeSn MD lasers are presented.

Layer Growth and Characterization

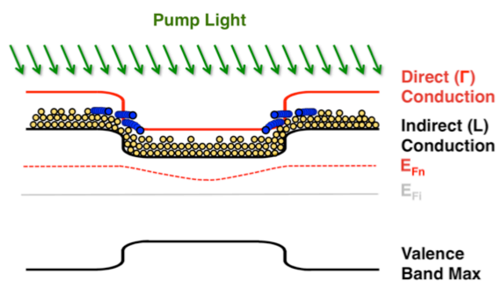
GeSn layers with x_{Sn} between 12 at.% and 12.5 at.% and varying thicknesses were grown on Ge-buffered Si(001) virtual substrates (Ge-VS) [5] using an industry-compatible 200 mm reduced pressure chemical vapor deposition (RP-CVD) tool with showerhead technology [6] at growth temperatures of 340-350°C [7] (Table 1). Although these direct bandgap GeSn layers are partially strain relaxed, they exhibit exceptionally high crystalline quality substantiated by transmission electron microscopy (TEM) imaging and ion channeling/Rutherford backscattering (RBS) measurements (Fig. 1 and Fig. 2). TEM analysis revealed a regular network

Towards a Ge Laser

Lasing Cavity

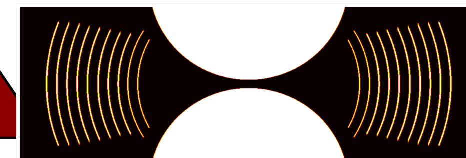


Heterostructure

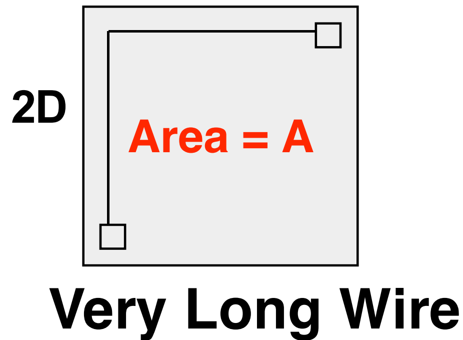


Germanium Laser

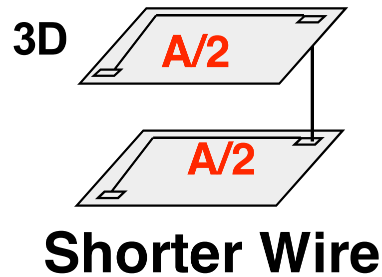
Optical Cavity



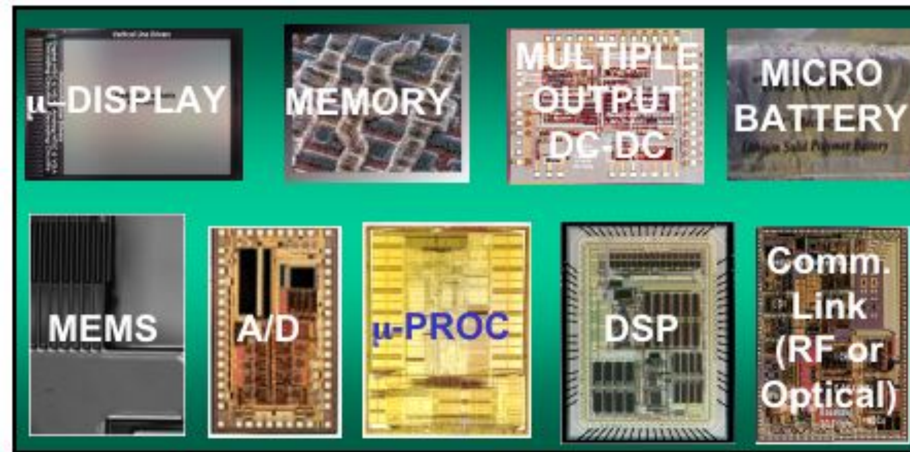
3-D Integration: Motivation



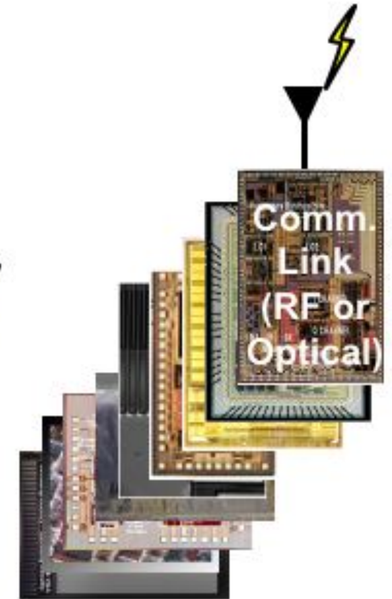
Very Long Wire



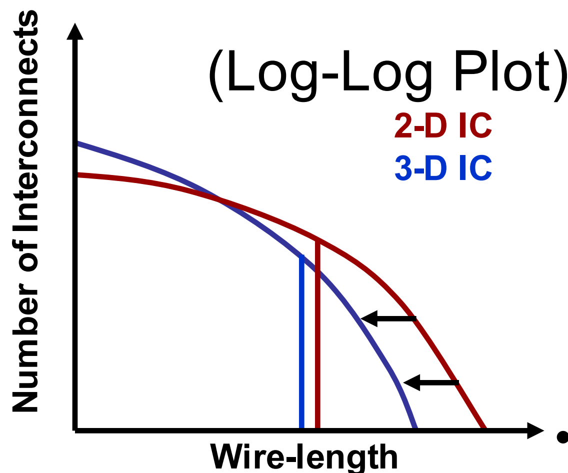
Shorter Wire



2-D System



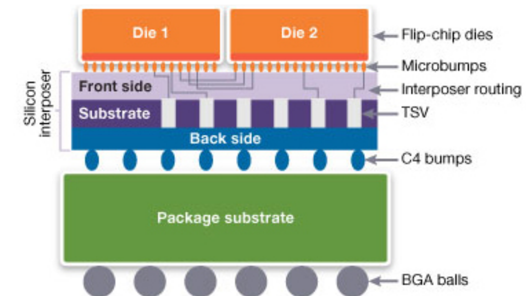
3-D System

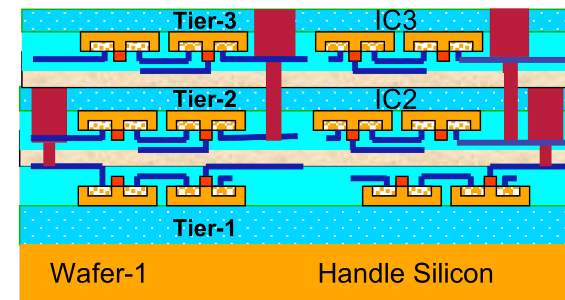


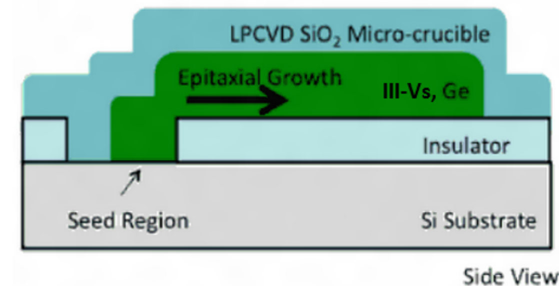
- Reduce Chip footprint
  - Improved form factor
  - Interconnect length ⇓ and therefore R, L, C ⇓
    - Delay reduction
    - Power reduction
    - Higher bandwidth
- Integration of heterogeneous technologies possible, e.g., memory & logic, sensors, optical I/O

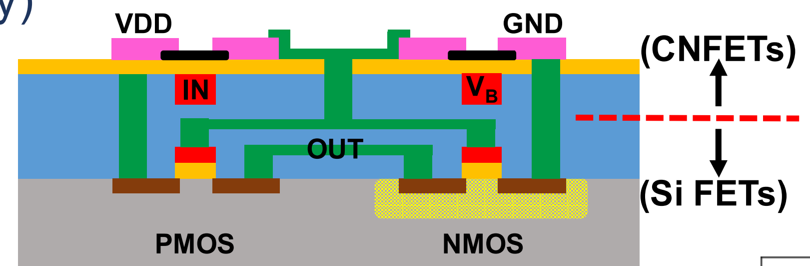
Technology to Fabricate 2.5D/3D ICs

- **2.5D packaging** (mature technology)
  - Wire bonded
  - Bump
  - vertical interconnect density < 20/mm or 400/mm²
- **3D bonding/TSV** (emerging technology)
  - Die stacking
  - wafer stacking
  - vertical interconnect density < 40,000/mm²
- **3D crystallization** (near future technology)
  - Epitaxial growth
  - Laser melting and crystallization
  - Seeded crystallization
  - Liquid phase crystallization
  - vertical interconnect density < 25M/mm²
- **3D self assembled devices** (future technology)
  - Si and Ge nanowires
  - Carbon nanotubes
  - Organic semiconductors



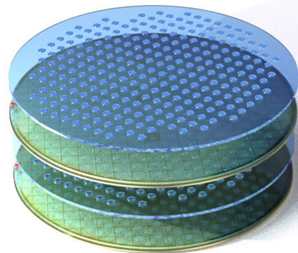




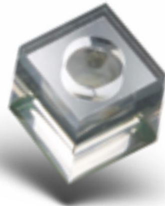


3D Wafer-level Camera Technology

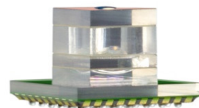
Manufacture of lenses at the wafer level

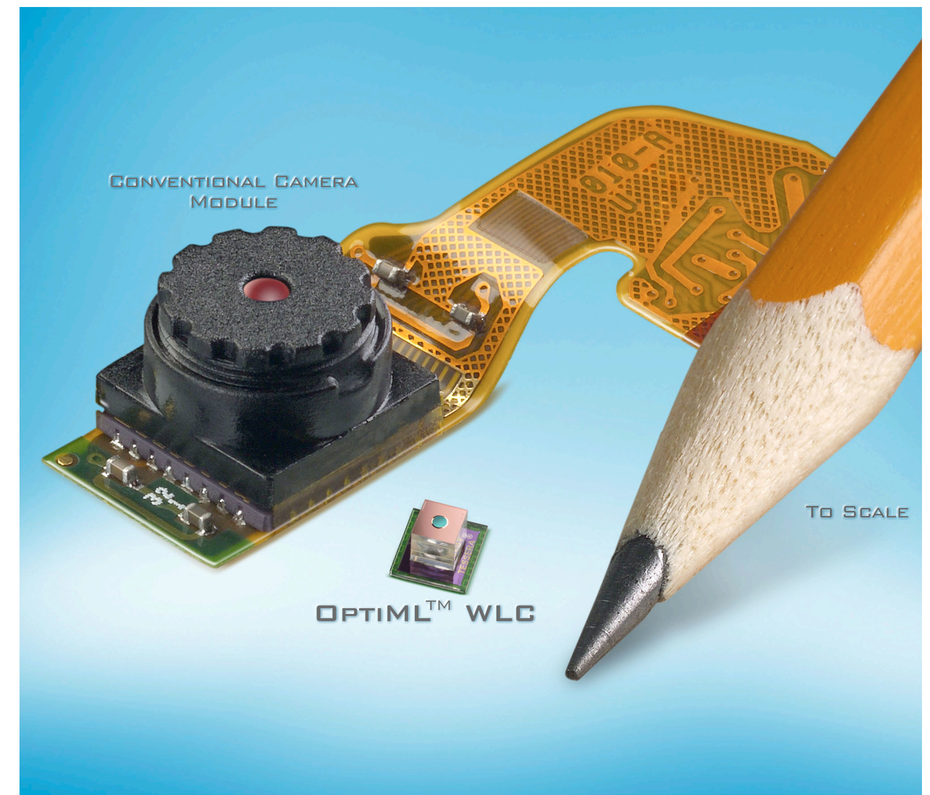


Wafer-to-wafer bonding and dicing of wafer stack



Bonding of wafer stack to the sensor

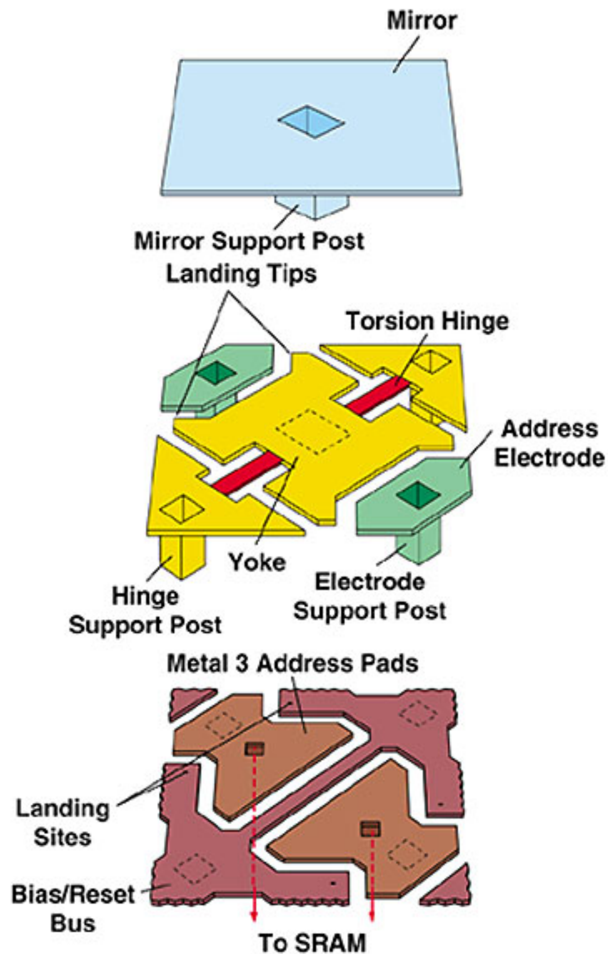




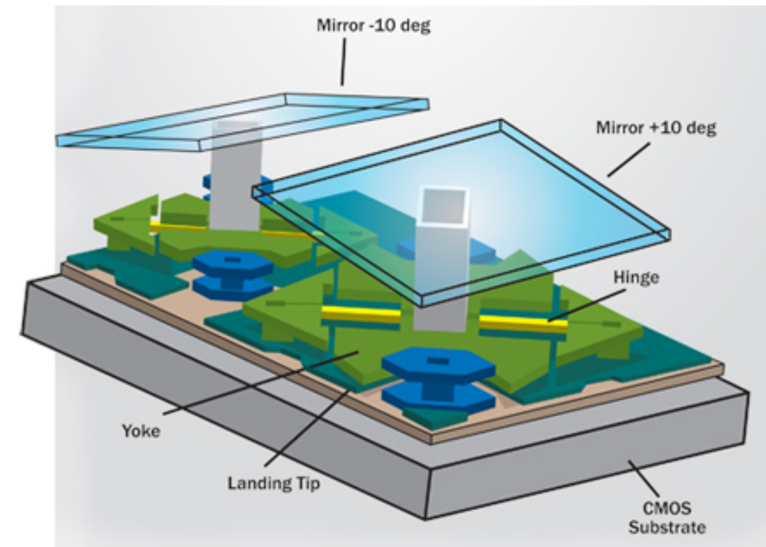
Courtesy: M. Feldman, (Tessera)

Digital Light Projection (DLP)

DLP MEMS Components



3D Integration



DLP Projector

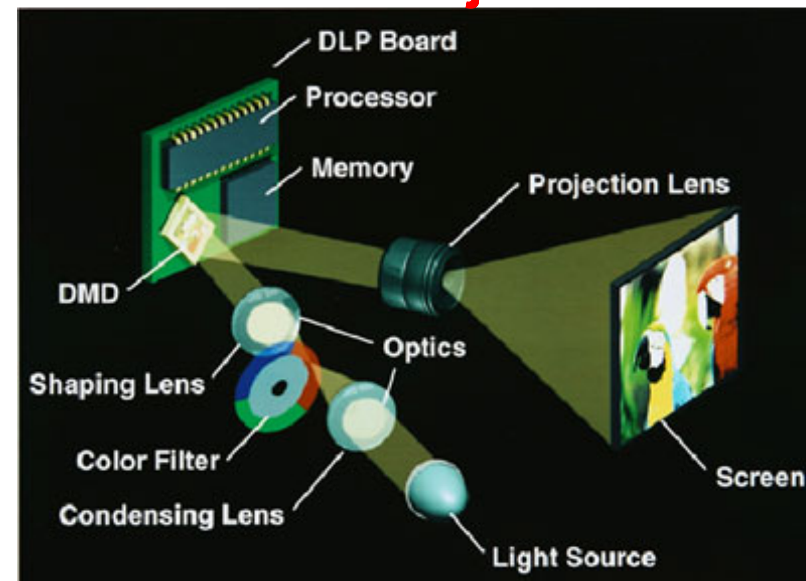
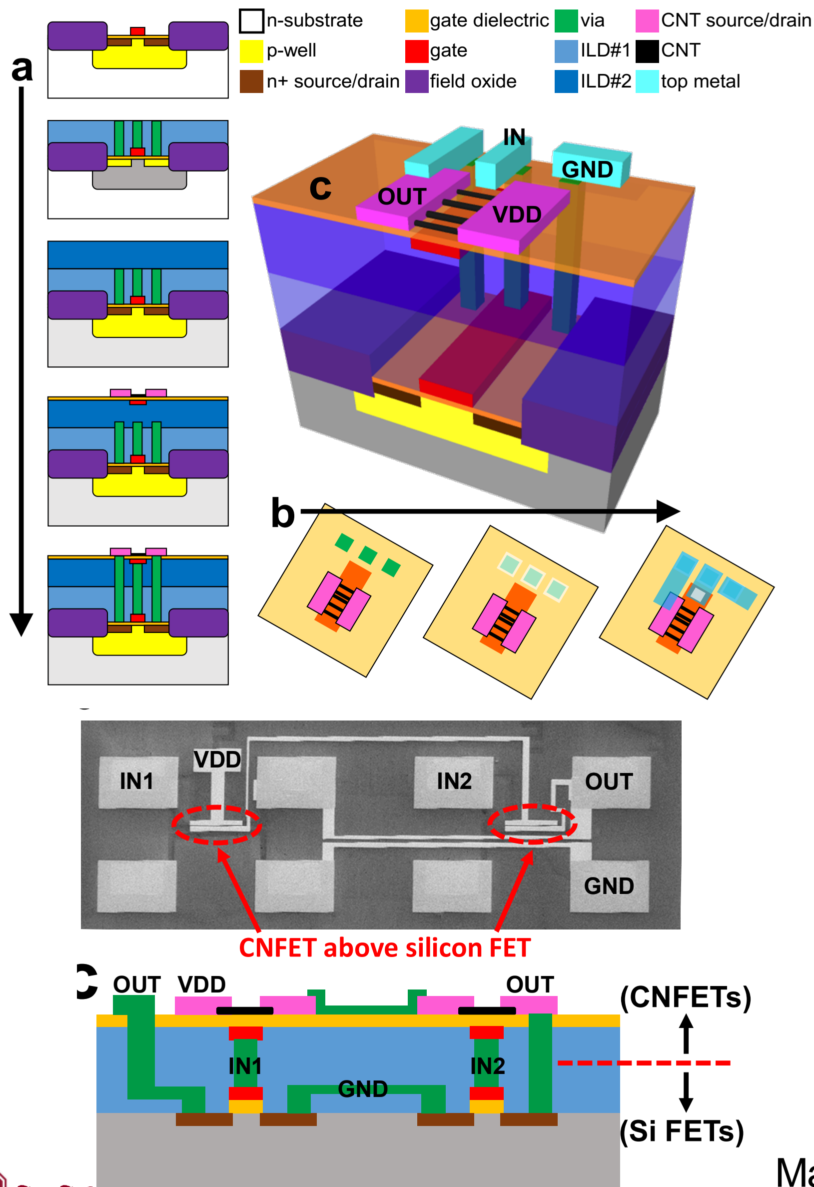
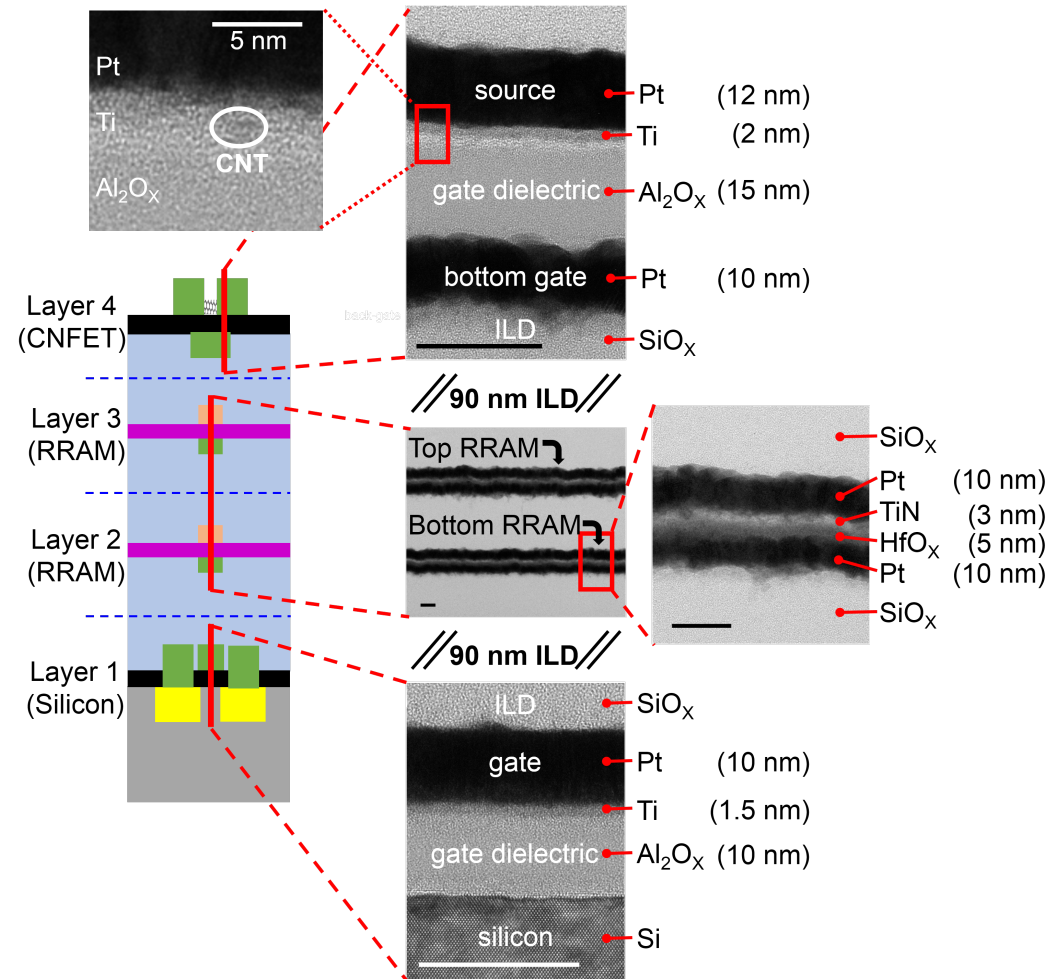


Photo courtesy of Texas Instruments

Monolithic 3D Integration of Si MOSFETs with RRAMs and CNTFETs

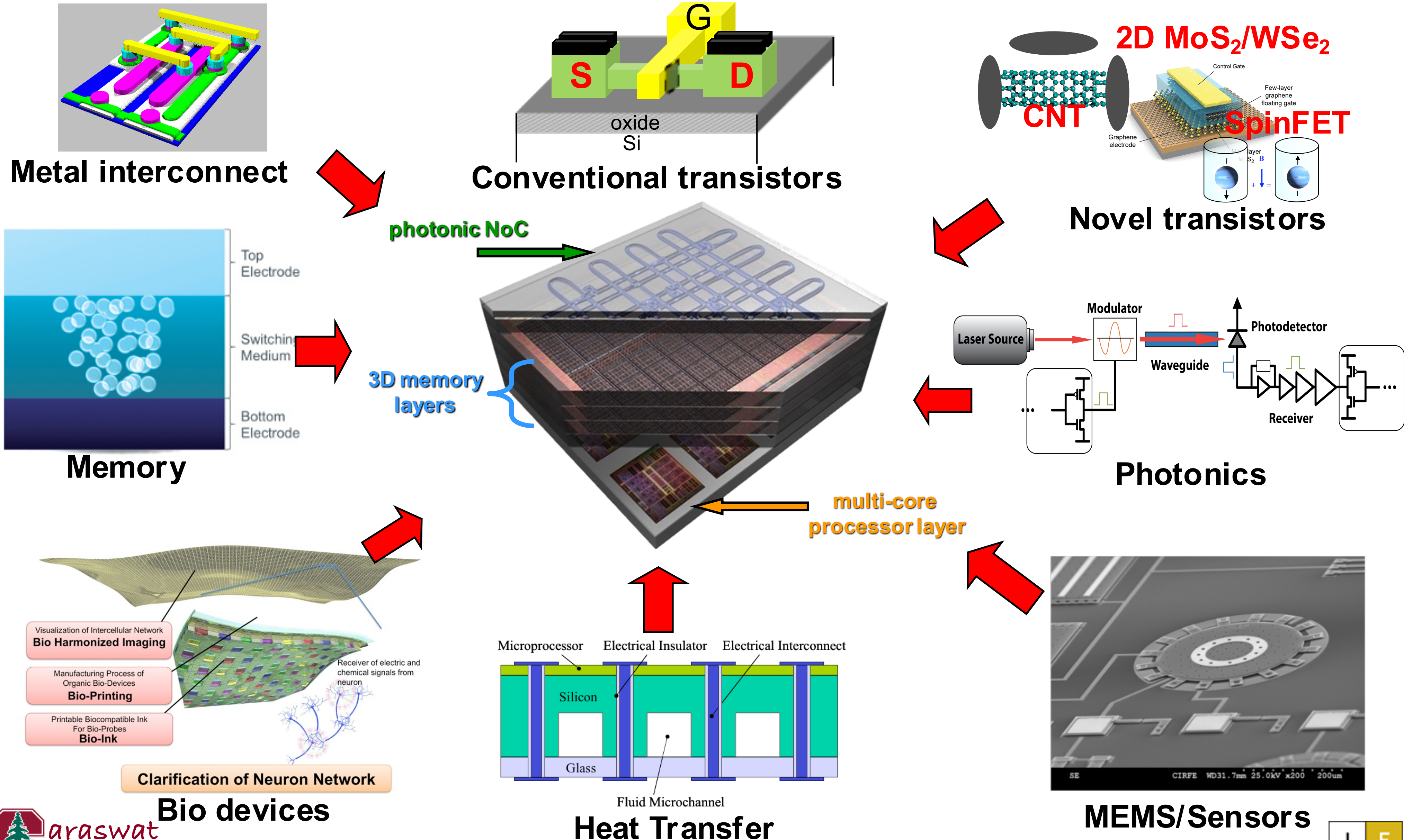




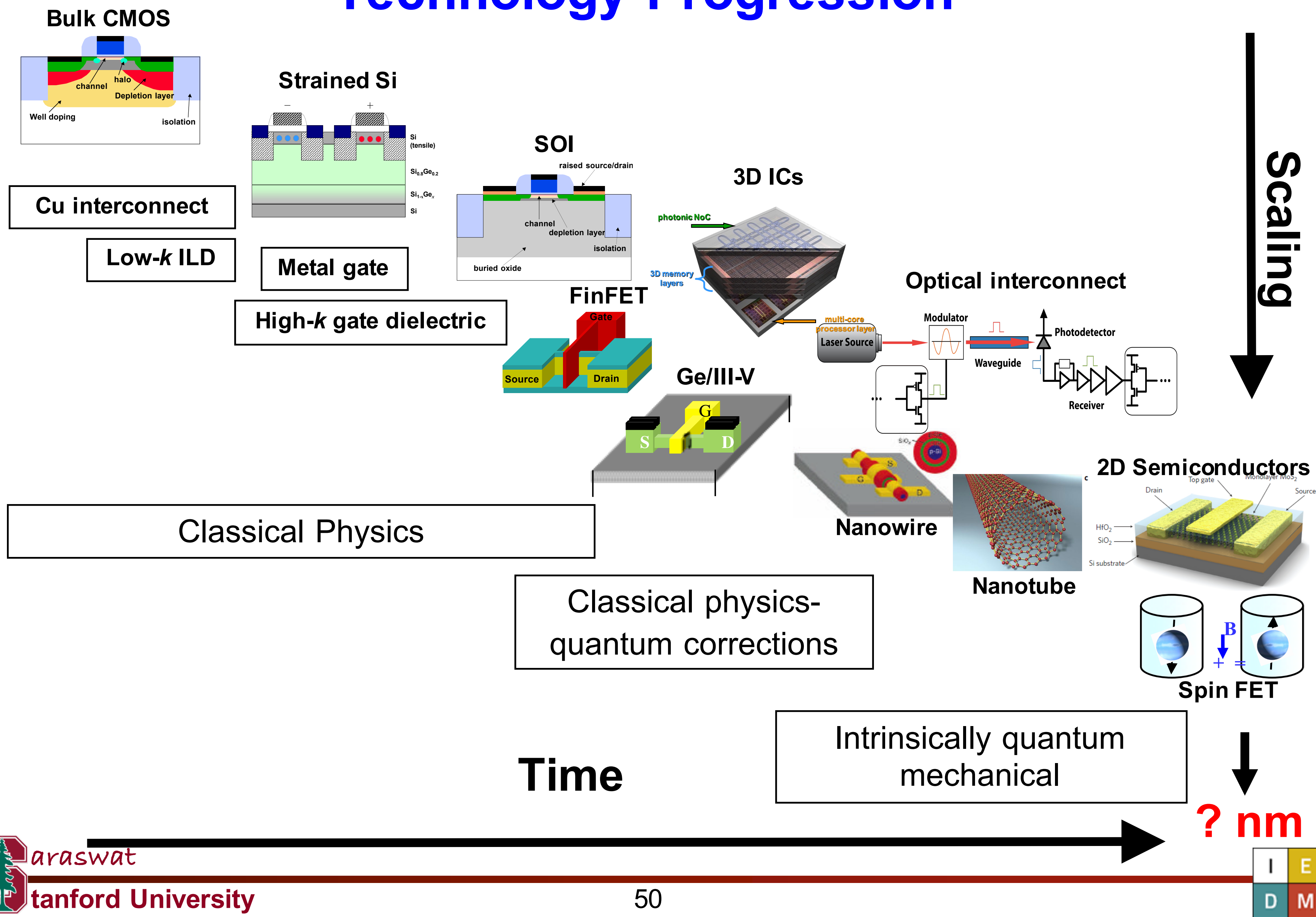
Max Shulaker, et al., IEDM, December 2014

Max Shulaker, et al., VLSI Symp. 2014

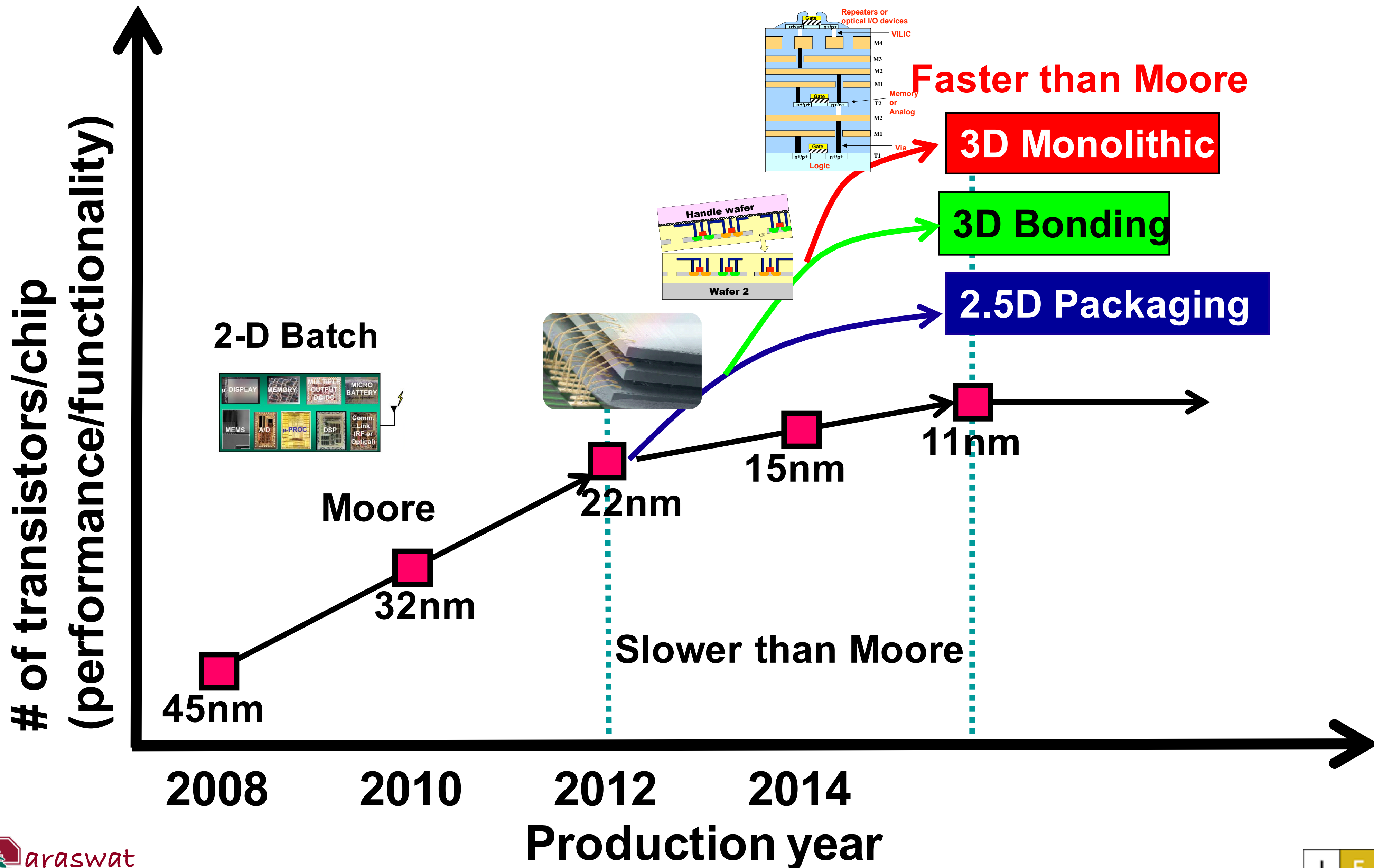
Future Systems will Require Heterogeneous Integration on a Si Platform



Technology Progression



Heterogeneous 3D Integration Faster than Moore



Conclusion

- ☹ Cu resistivity increases as technology scales down. This will be a bottleneck of future high-performance chip.
- ☺ CNTs have a significant advantage over Cu wires especially for local interconnects
- ☺ Optical links have smallest latency and energy per bit for longer global interconnects requiring higher band width
- ☺ 3D heterogeneous integration will keep the Moore's law going for awhile.

Contributors / Collaborators:

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