Tutorial IEDM 2015:
Advance Device Concepts for 7nm Node and Beyond

12/05/2015
Objective

- Understand key device advantages and limitations of the non-ideal bulk FinFETs adopted for 14/16/22nm nodes
  - $+I_{ON}$, DIBL, SS, $\sigma V_T$
  - $-$ minimal $L_G$ scaling

- Understand simple physical picture of nanoscale MOSFETs
  - Source-side injection MOSFET model
  - Mobility, velocity saturation, ballistic transport, quantum capacitance, quantum confinement
  - Key: Small conductivity $m^*$ channel direction, large confinement mass, large DOS mass are all key

- With simple picture of nanoscale MOSFET and advantage and limitations of non-ideal bulk FinFET, understand how future nodes 10, 7, 5nm might develop
  - Bulk Si FinFET for 10 and 7nm
  - Tall fins
  - Subfin Leakage fix
Outline

- State-of-the-art for logic devices
- FinFET device physics basics
- Metrics for advance logic devices
- Deeper look at some advanced device concepts
  - Essential Nanoscale Device Physics
    - mobility, ballistic transport, velocity saturation, thermal velocity, m* and density of states
  - Transistor variation / random doping effect
  - Strain I, Ge and III- channels
  - Quantum confinement
  - External resistance
  - Sub fin doping and gate all around devices
- Conclusion: How does the roadmap evolve?
Up until 130nm node, everything going according to plan (Dennard Scaling)

- $T_{OX}$ scaling slows/stopped at 90-65nm
- $T_{OX}$ replaced by mobility boost from stress – Moore’s Law continues
- $T_{OX}$ scaling continues with new materials but lasts maybe 2 generations

* $L_G$ scaling has slowed this past decade even with introduction of high K and FinFETs and must be addressed for 10 and 7nm.*
State-of-the-Art: 14nm FinFET

- 14 nm used for A9, Exynos 7420, Broadwell, and Snapdragon 820
- FinFET PLUS all the performance “boosters” of last 10 years
- Note: Bulk Finfet $L_{GATE} \sim 30$nm and will need to be scaled by 7nm

**Bulk Finfet $L_{GATE} \sim 30$nm and will need to be scaled by 10 and 7nm**
Non-uniformity in Fin etch and device architecture results in three distinct fin regions:

1. Ideal “Tri-Gate” at the top, thin width, good gate control
2. Wider FinFET in the middle, less gate control
3. Sub-fin “BJT”, an ungated device which contributes to leakage

- Sub-fin leakage needs to be addressed as Si FinFET scaled to 10 and 7nm
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Why FinFET: Scaling Requires Depleted Devices

Depleted devices improve SCE (both SS, DIBL, Ioff) and transistor matching.

Historically SCE addressed in Dennard classic scaling by increasing Cox (thinning Tox).

Limited $L_G$ scaling benefit due to drain to source sub-surface leakage path (non-gate controlled region) in FinFETs.

- Bulk FinFET is being designed for Electrical $W$, DIBL, SS, $\sigma VT$ benefit and this trend will continue for 10 and 7nm.
Depletion also improved performance

- Delay metric $\rightarrow$ Effective current: $I_{\text{eff}} = (I_H + I_L)/2$
- Undoped channels (FinFET, FD-SOI, DDC) have intrinsically low DIBL
  - This translates into higher $I_{\text{eff}}$, especially at low $V_{dd}$

\[ t_d \propto \frac{C_{\text{load}}V_{dd}}{2 \cdot I_{\text{eff}}} \]
Improved SS: Improved IOFF and/or Better Low V performance

- Fully depleted channel $C_{depl} \sim 0 \rightarrow SS \sim 60\text{mV/dec}$

\[
SS = \ln(10) \frac{kT}{q} \left( 1 + \frac{C_{depl}}{C_{ox}} \right) \approx 60 \frac{mV}{dec} \left( 1 + \frac{C_{depl}}{C_{ox}} \right)
\]

- Improved SS Allows for Lower $V_T$ for same $I_{OFF}$ (key for advanced node VDD scaling)
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Executive Summary: Metrics Advanced Nodes: 14 to 7nm

<table>
<thead>
<tr>
<th>Metric</th>
<th>Insight into Metric</th>
</tr>
</thead>
</table>
| Cost            | • Moore’s Law: Unlikely major adoption if not lower cost  
• 14,10,7nm patterning cost is slowing Moore’s Law                                                                                   |
| $I_D$           | • Large mA/μm being targeted  
• Requires large electrical width in planar area  
  • One of key FinFET strengths  
• Helped by tall fins on tight pitch (increase fin parameter)  
• Note Intel’s drive current is normalized by top down W not $W_{EFF}$  
• Large $I_D$ being targeted even at some degradation to CV/I                                                   |
| DIBL            | • Improved DIBL  
• Important for low voltage performance                                                                                               |
| SS              | • Improved SS allows for lower $V_T$ which enables lower $V_{DD}$                                                                                   |
| N/P ratio       | • Close to 1  
• **Allow pFET width to be similar to nFET (vs historical 2:1)**  
• Requires large uniaxial $<110>$ stress on pFET  
• One of key reason FinFET on Bulk is adopted for 16 through 7nm                                                                |
| Transistor      | • Key for low voltage SRAM operation  
• Many sources of transistor variation  
• Fins are still doped at 14nm so RDF still a factor                                                                                       |
| Matching        |                                                                                                                                                   |
| $L_{GATE}$      | • Smaller/ better BUT to date FinFET has only provided modest scaling                                                                                  |
Cost per transistor decreased until 28nm node then starts increasing
- Mainly driven by lithography cost
- 20nm and below will be more expensive than 28nm for level of functionality
How to Think About FinFET: \((\text{Large } W_{\text{ELECTRICAL}})\)

- Top down planar transistor
- X-section planar transistor

\[ W_{\text{ELECTRICAL}} = W + 2 \Delta W \]
FinFET: Key Advantage is Large $W_{ELECTRICAL}$

- Recessed STI to set Fin Height
- Cut Diffusion into strips

![Diagram of FinFET structure]

Mathematical expressions:

$$W_{ELECTRICAL} = FIN_{PERIMETER} = \# FINS \left( 2FIN_H + FIN_W \right)$$

$$W_{ELECTRICAL} = \frac{PLANAR_{WIDTH}}{FIN_{PITCH}} \left( 2FIN_H + FIN_W \right)$$
22/14nm Design Point: Little Volume Inversion

- NO Significant bulk inversion in the fin bodies for 22/16/14 designs
- Will be issue as move to 10/7nm
Normalize Currents by Planar W or Fin Perimeter?

For Intel 14nm: \[(\text{Fin perimeter} / \text{Planar W}) = \frac{2\text{Fin}_H - \text{Fin}_W}{\text{pitch}} \approx 2.2\]
State-of-the-art for logic devices

FinFET Basics

Metrics for advance logic devices

Deeper look at some advanced device concepts
  - Drive current and relation to mobility, velocity saturation, and density of states
    - Transistor variation / random doping effect
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    - Sub fin doping and gate all around devices

Conclusion: How does the roadmap evolve?
Drift Velocity and Velocity Saturation

Electric field = 0  |  Electric field | > 0

Drift velocity versus electric field for different semiconductors. The red arrows show how drift velocity, i.e., mobility, can be improved at even lower electric fields by replacing silicon by other high-mobility semiconductors.

Intel 45 nm

after M. Fischetti, 2001
Velocity Saturates: Nanoscale Device Over Most of the Channel

Intel 14 nm
Source: Intel

\[ L_{GATE} \approx 30\text{nm} \rightarrow L_{ELECTRICAL} \approx 20\text{nm} \]

\[ \frac{V_{DS}}{L_E} \approx \frac{0.9V}{20\text{nm}} \approx 4.5 \times 10^5 \text{V/cm} \]

Drift velocity versus electric field for different semiconductors. The red arrows show how drift velocity, i.e., mobility, can be improved at even lower electric fields by replacing silicon by other high-mobility semiconductors.

\[ \approx 2 \times 10^4 \text{V/cm} \]

after M. Fischetti, 2001
Key Concepts: Ballistic Transport

\[ \langle KE \rangle = \frac{1}{2} m v^2 \]

- Source to drain transport “without” scattering
- \( L \ll \lambda \) — Not right metric to near ballistic transport
- Scattering in high field region and velocity in high field does NOT matter
Essential Physics of Nanoscale MOSFET

\[ I_D = \frac{v \cdot Q_{inv}}{W} = v_T \cdot C_{OX} (V_{GS} - V_T) \]

\[ < v(\omega) > \approx \frac{1 - r}{1 + r} v_T \]

\[ v_T \propto \sqrt{\frac{2k_B T_L}{\pi n_i^*}} \]

- Carries injected into channel from “the source” / Gate largely controls source barrier
- Some fraction of carriers injected into channel backscatter and return to source
- Current increases as \( m^*_t \) decrease (why uniaxial stress)
Quantum Capacitance

- Parallel-plate capacitor and low density of states in the semiconductor
- Capacitance is *not* given by the normal formula $\varepsilon_0\varepsilon_r/t_{ox}$ for parallel-plate capacitors
- Capacitance lowered due to another capacitor in series.
- Second capacitance (quantum capacitance) is important for low-density-of-states systems

\[ I_D/W = ν \cdot Q_{inv} = νT \cdot C_{OX} (V_{GS} - V_T) \]

- Lowers inversion charge for low density of state conduction band III-V semiconductors and 2D 2-dimensional electronic system (graphene et. al.)
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FinFET: Many Additional Sources of Variation

- Multiple sources of variation (WID, WIW, WTW)
  - Fin height
    - Variation from: STI dep, STI CMP, wet etch
  - Fin width
  - Fin shape
  - Fin doping
  - Fin line edge roughness
  - Fin side wall plane
  - Gate LER (gate etch over fin topography)
  - Etched fin plane interface traps
  - Additional Epi variation (growth on etched plan)
  - SDE doping along fin height

Additional variation will be one of biggest challenges for SOC
Fin Height & Width Variation Large in Bulk FinFETs

- Additional sources of variation not present in bulk planar structures

![Diagram of FinFET structure with variations](image)

### Table 2: Sources of variability for junction-isolated bulk FinFETs.

<table>
<thead>
<tr>
<th>Sources of variability</th>
<th>Nominal (nm)</th>
<th>3-sigma tolerance (current)</th>
<th>3-sigma tolerance (future)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HM oxide</td>
<td>8</td>
<td>0.4</td>
<td>0.2</td>
</tr>
<tr>
<td>HM nitride</td>
<td>70</td>
<td>7</td>
<td>3.5</td>
</tr>
<tr>
<td>Trench etch</td>
<td>170</td>
<td>8.5</td>
<td>4.25</td>
</tr>
<tr>
<td>Oxide recess</td>
<td>100</td>
<td>5</td>
<td>2.5</td>
</tr>
<tr>
<td>Pad oxide</td>
<td>2</td>
<td>0.1</td>
<td>0.05</td>
</tr>
<tr>
<td>Well anneal</td>
<td>0</td>
<td>3</td>
<td>1.5</td>
</tr>
<tr>
<td>Total fin height</td>
<td>12.5</td>
<td>6.2</td>
<td></td>
</tr>
<tr>
<td>variability (nm)</td>
<td>Total fin width</td>
<td></td>
<td></td>
</tr>
<tr>
<td>variability (nm)</td>
<td>2.5</td>
<td>1.2</td>
<td></td>
</tr>
</tbody>
</table>

- 35% W variation
- 18% W variation

Fin Scaling from 22nm to 14nm

Transistor Fin Improvement

22 nm 1st Generation Tri-gate Transistor

14 nm 2nd Generation Tri-gate Transistor
22/16/14nm FinFET Still Use Channel Dopants

\[ N_{DOPANTS} = N_A W L W_{dep} \]

\[ \sigma_{N_{DOPANTS}} = \sqrt{N_A W L W_{dep}} \]

\[ \sigma_{Vt} = \frac{q T_{ox}}{\varepsilon_{ox}} \sqrt{\frac{N_{sub} W_{dep}}{3 L W}} \]

- Doped glass used to dope sub-fin.
- Some will diffuse into bottom of FIN

Source: Intel/Bohr
Note data is not normalized to W as for Planar.

Large finFET W is a REAL advantage for SRAM and is responsible for significant part of $\sigma_{VT}$.
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What is the Desired Band Structure

\[ \mu = \frac{q\tau}{m^*} \]

Out of Plane: Large \( m^* \) for quantum confinement to be additive with strain

Channel Direction: Small \( m^* \) for high mobility

In-plane \( \perp \) to Channel: Large \( m^* \) for high density-of-states
What “Velocity” Sets $I_{ON}$ and Why is N/P Ratio ~1

$N/P$ ratio $= I_{ON}^{N} / I_{ON}^{P} \approx 1.1$

SiGe Stress $m^*_t \sim m^*_lh \sim 0.15m_o$

$$I_D/W = v \cdot Q_{inv} = v \cdot C_{OX} (V_{GS} - V_T)$$

$v = \mu E$ ?

$v = v_{SAT}$ ?

$v = v_T$ ?

$v_T \propto \sqrt{\frac{2k_B T_L}{\pi m^*_t}}$

Figure 5: Transistor I-V Curves

Intel 14nm Transistor
Layout of Real Chips with SiGe Stressors

- SiGe stress allows for N/P ~1
- SiGe stress reduced pmos W by factor of 2
- Improves layout density and lowers $C_{\text{GATE}}$
Same Physics for IV, V Materials

Si

Ge

GaAs

Unstressed  1GPa Biaxial  1GPa Uniaxial
Strain Enhancement: Simple Estimate

\[ \propto \frac{m_{hh}}{m_{lh}} \]

Conductivity mass ratio

Unstrained

(a)

Uniaxial Strained

(b)
III-V Channel: Inversion Mode Device

TABLE III. Band and transport parameters for Si, Ge, and some III–V semiconductors.

<table>
<thead>
<tr>
<th></th>
<th>$E_g$ (eV)</th>
<th>$m_n$ (cm$^2$/V s)</th>
<th>$\mu_n$ (cm$^2$/V s)</th>
<th>$m_{hh}/m_{hl}$</th>
<th>$\mu_h$ (cm$^2$/V s)</th>
<th>$g_{mn}$ (Norm.)</th>
<th>$\Delta E_{FL}$ (eV)</th>
<th>$m_l/m_l(L)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>0.92/0.19</td>
<td>1450</td>
<td>0.53/0.15</td>
<td>500</td>
<td>1</td>
<td>…</td>
<td>…</td>
</tr>
<tr>
<td>Ge</td>
<td>0.67</td>
<td>1.59/0.082</td>
<td>3900</td>
<td>0.33/0.043</td>
<td>2270</td>
<td>0.92</td>
<td>…</td>
<td>…</td>
</tr>
<tr>
<td>InSb</td>
<td>0.17</td>
<td>0.014</td>
<td>$7.7 \times 10^4$</td>
<td>0.45/0.016</td>
<td>850</td>
<td>1.9</td>
<td>0.51</td>
<td>1.56/0.094</td>
</tr>
<tr>
<td>InAs</td>
<td>0.35</td>
<td>0.024</td>
<td>$2-3.3 \times 10^4$</td>
<td>0.41/0.026</td>
<td>$100-450$</td>
<td>1.29</td>
<td>0.72</td>
<td>1.56/0.094</td>
</tr>
<tr>
<td>GaSb</td>
<td>0.73</td>
<td>0.041</td>
<td>3750</td>
<td>0.40/0.05</td>
<td>680</td>
<td>0.28</td>
<td>0.084</td>
<td>0.95/0.11</td>
</tr>
<tr>
<td>InP</td>
<td>1.34</td>
<td>0.08</td>
<td>5370</td>
<td>0.6/0.089</td>
<td>150</td>
<td>0.77</td>
<td>0.59</td>
<td>1.9/0.15</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.42</td>
<td>0.063</td>
<td>9200</td>
<td>0.5/0.076</td>
<td>400</td>
<td>1.03</td>
<td>0.29</td>
<td>1.9/0.075</td>
</tr>
<tr>
<td>Strained Si</td>
<td>1.08</td>
<td>…</td>
<td>2900$^a$</td>
<td>…</td>
<td>2200$^b$</td>
<td>2</td>
<td>…</td>
<td>…</td>
</tr>
</tbody>
</table>

$^a$See Ref. 26.
$^b$See Ref. 99.
$^c$These two columns list the $L$ valley data for selected III–V semiconductors. The other data in the table are taken from Refs. 134 and 135.

Ge and III-V channel pFET will benefit greatly by strain and will be needed for performance over Si.
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MOSFET inversion layer Confinement

- Conduction band forms a potential well and quantum confinement occurs
- Carriers in bound states cannot propagate to infinity
- Bulk confinement potential

Fundamentals of Modern VLSI Devices: Taur, Ning
Location of Inversion Charge (NFET)

For Lighter confinement mass, inversion charge centroid further into semiconductor
Case Study of GaAs

\[ \Delta E = 0.3 \text{ eV} \]

\[ \Gamma_6 : \text{spherical, } m^* = 0.067 m_0 \]

\[ L_6 : \text{ellipsoidal, } m_z = 0.27 m_0 \]

GaAs under (001) electric confinement

\[ F = 1 \text{ MV/cm} \]
Quantum Confinement FinFET

Source J.G. Fossum and V. P. Trivedi
Real Issue for 10/7nm node

Fig. 6 Sub-band distributions for (a) (100), and (b) (110) DG nMOSFETs with $T_{Si} = 6$ nm when $N_{inv} \approx 10^{13}$ cm$^{-2}$.

Fig. 7 The charge distributions for (a) (100), and (b) (110) DG nMOSFETs with $T_{Si} = 20$ (black line) and 6 (blue line) nm. All charge distributions are plotted for $N_{inv} \approx 10^{13}$ cm$^{-2}$.

Source: Anson C-C Wang, Edward Chen, Tzer-Min Shen, Jeff Wu, and Carlos H. Diaz. TSMC
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Real Limiter: Parasitic Resistance

Channel Resistance

Parasitic Resistance

ITRS Roadmap “Goal”

Parasitics Dominate!
Real Fin Shape: Why?

- Self aligned to gate Fin thinning / straighten after gate removal?
- Helps with mechanical support, SiGe Stress, and spacer removal
- Negative is higher parasitic capacitance
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Scaling $L_G$ for 10 and 7nm Nodes

- $\lambda$ derived from Poisson’s equation and relates to SCE and control of drain over the channel
- For strong gate control of barrier $L_G > (5-10)\lambda$

For strong gate control of barrier $L_G > (5-10)\lambda$
Current Double Gate Scalable to 7nm Node With 6nm Fin Thickness

<table>
<thead>
<tr>
<th>Node</th>
<th>22nm</th>
<th>14nm</th>
<th>10nm</th>
<th>7nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Pitch</td>
<td>90nm</td>
<td>70nm</td>
<td>~55nm</td>
<td>~45nm</td>
</tr>
<tr>
<td>$L_G$</td>
<td>35nm</td>
<td>30nm</td>
<td>25nm</td>
<td>20nm</td>
</tr>
<tr>
<td>$\sim L_E$</td>
<td>25nm</td>
<td>20nm</td>
<td>15nm</td>
<td>15nm</td>
</tr>
<tr>
<td>$t_{Si}$ Single Gate</td>
<td>9 nm</td>
<td>6 nm</td>
<td>3 nm</td>
<td>3 nm</td>
</tr>
<tr>
<td>$t_{Si}$ Double Gate</td>
<td>18 nm</td>
<td>12 nm</td>
<td>6 nm</td>
<td>6 nm</td>
</tr>
</tbody>
</table>

- Strong gate control of barrier $L_E = 5\lambda$
- $\text{Tox} \approx 0.9\text{nm}$
- Will require improvements to sub-fin Leakage
Few Ways to Address SubFin Leakage

FinFET on SOI

Source: Synopsys

Bulk Sub Leakage solution

- Industry likely to continue with bulk FinFET for 10 and 7nm
- Key reason: Maintaining SiGe pFET effective mass improvement

Source: Intel / US20130320455
Gate All Arround - SiGe Stress – Larger W

- No technical barrier
- Could support 5nm node
- Possible with SOI wafer technology
- Compatible with SiGe pFET effective mass improvement
- Cost is the issue (both transistor and interconnect cost with EUV required for 5nm node)

Source: Intel / US 20120138886

BACKGROUND

[0001] Maintaining mobility improvement and short channel control as microelectronic device dimensions scale past the 15 nm node provides a challenge in device fabrication. Nanowires used to fabricate devices provide improved short channel control. For example, silicon germanium (Si$_x$Ge$_{1-x}$) nanowire channel structures (where x<0.5) provide mobility enhancement at respectable Eg, which is suitable for use in many conventional products which utilize higher voltage operation. Furthermore, silicon germanium (Si$_x$Ge$_{1-x}$) nanowire channels (where x>0.5) provide mobility enhanced at lower Eg which is suitable for low voltage products in the mobile/handheld domain, for example.
Conclusion

- FinFETs adopted for 14/16/22nm nodes
  - $+I_{\text{ON}}$, DIBL, SS, $\sigma V_T$
  - - minimal $L_G$ scaling
  - $I_{\text{ON}}$ is from large fin perimeter

- Simple physical picture of nanoscale MOSFETs
  - Source-side injection and inversion charge sets $I_{\text{ON}}$
  - Mobility, scattering, velocity saturation NOT important
  - Light in-plane and heavy out-of-plane conductivity mass key
  - Strained Si still provided large improvement and enables n/p ratio ~ 1

- How future nodes 10, 7, 5 nm might develop?
  - Bulk Si FinFET for 10 and 7nm
  - Tall fins
  - Subfin Leakage fix (gate all around?)
  - Semiconductors with light confinement mass and high dielectric constants (i.e. 3-5 materials) might not provide much advantage in a system with electrical and physical confinement (i.e. FinFET)