Multi-Scale Modeling of Self-Heating Effects in Nano-Devices

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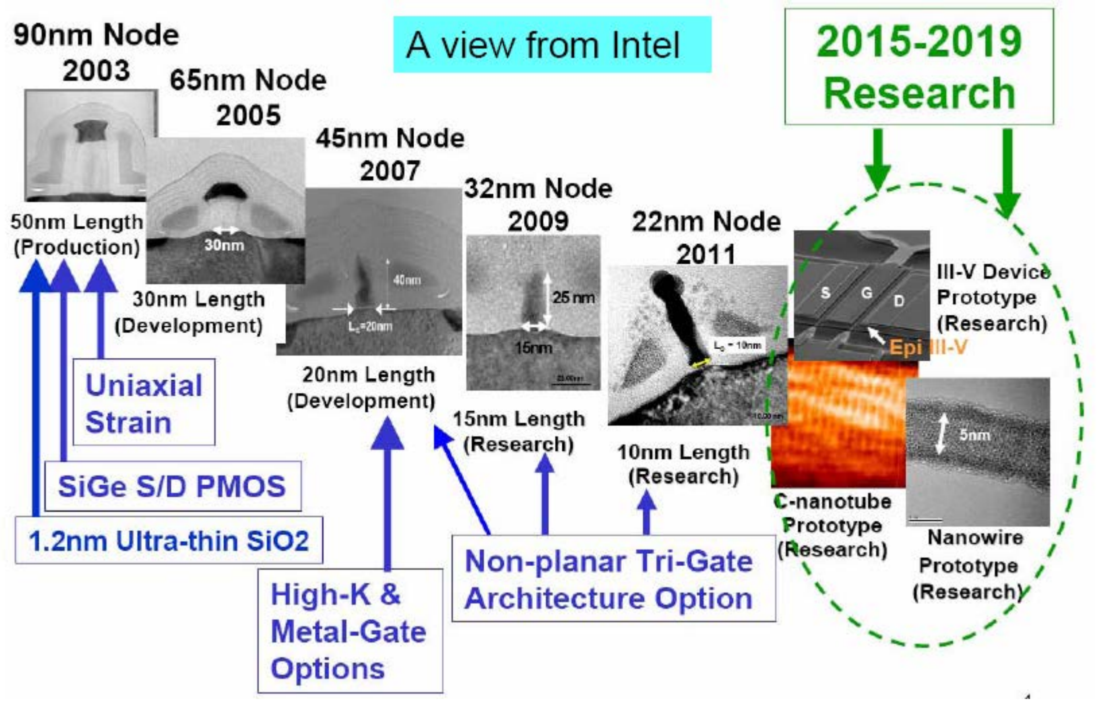
Outline

- Motivation
- Device Level Modeling
- Circuit/Interconnect Level Modeling
- Sample Simulation Results
- Conclusions

Transistor Scaling



Two avenues for reducing transistor size:

1. Alternative Materials

Strained Si, strained SiGe

High-K dielectrics

2. Alternative Transistor Designs

FD SOI Devices

Dual-Gate Devices

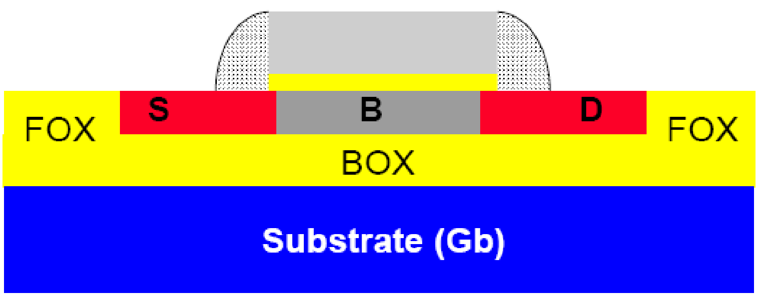
FinFETs

MugFETs

22nm and 14nm technology nodes from Intel are FinFET devices

Why Electro-Thermal Modeling?

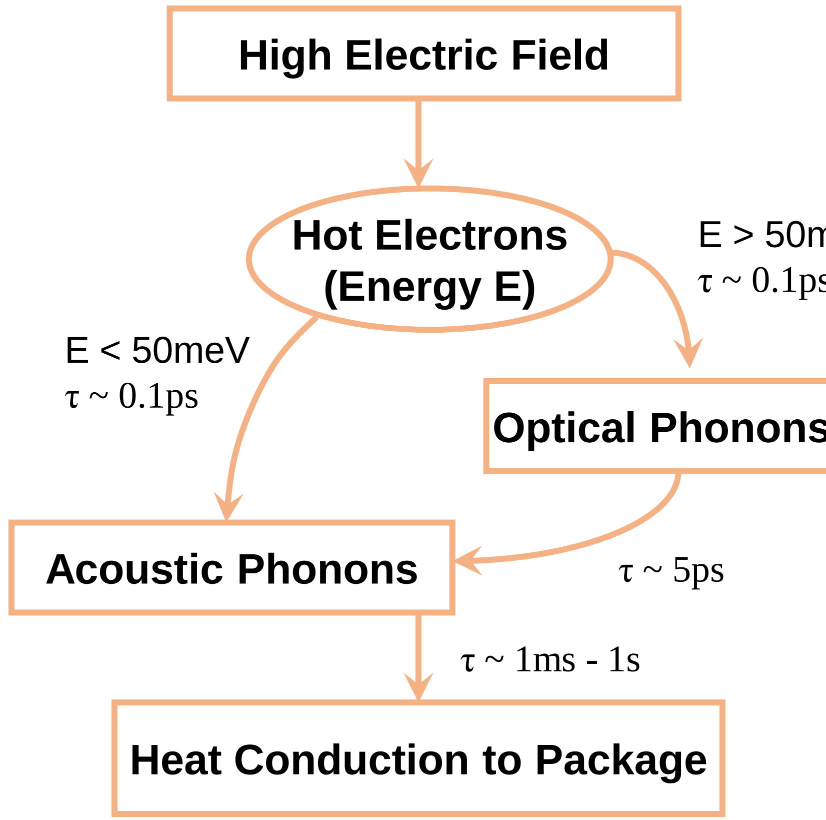
Reason for Observation of Self-Heating



Fully depleted (FD) body

Material	k_{th} (W/mK)
Si	148
Ge	60
Silicides	40
Si (10 nm)	13
SiO_2	1.4

Theoretical Model for Thermal Transport through Phonons



Modeling of Electro-Thermal Effects

We solve self-consistently the:

- Boltzmann Transport Equation for the Electrons (using the Monte Carlo method) self-consistently coupled to 2D/3D Poisson Equation Solvers
- Energy Balance Equations for the Acoustic and Optical Phonons

J. Lai and A. Majumdar, "Concurrent thermal and electrical modeling of submicrometer silicon devices", J. Appl. Phys. , Vol. 79, 7353 (1996).

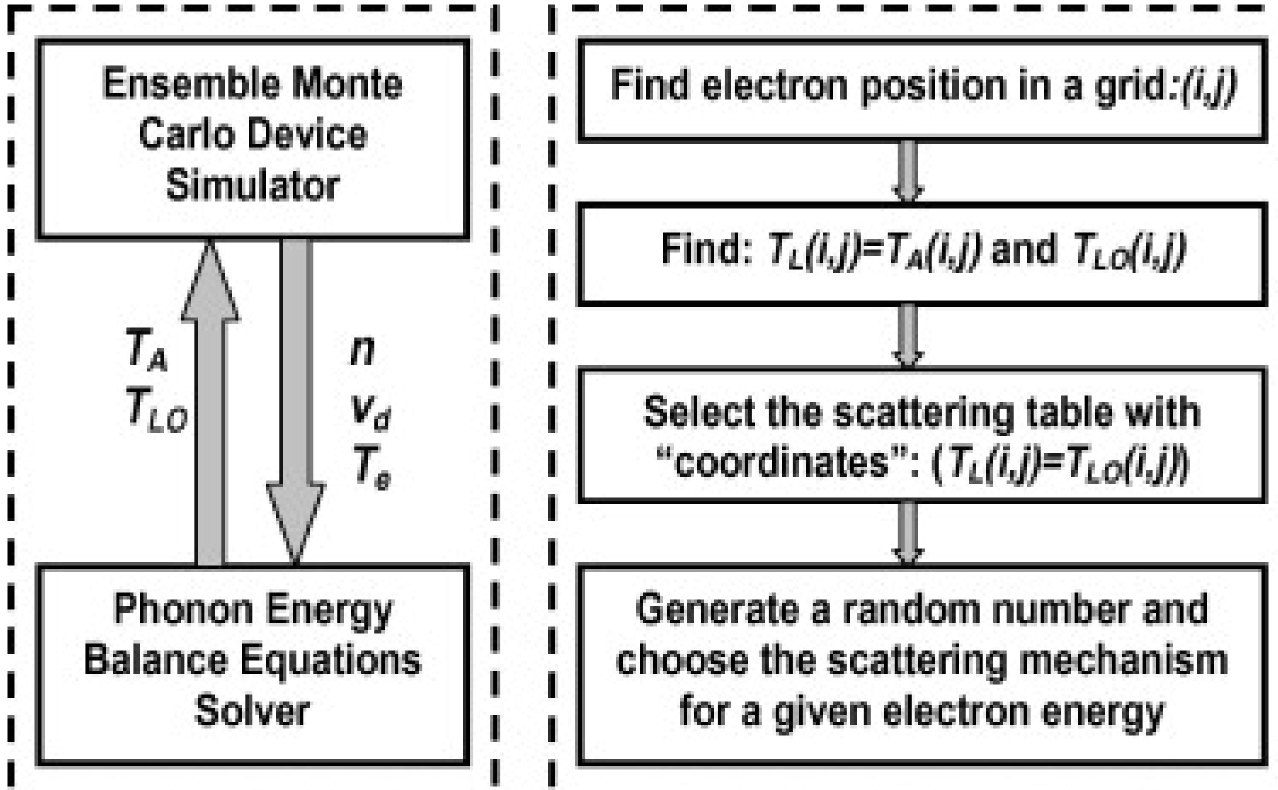
$$C_{LO}\frac{\partial T_{LO}}{\partial t}=\frac{3nk_B}{2}\left(\frac{T_e-T_{LO}}{\tau_{e-LO}}\right)+\frac{nm^* v_d^2}{2\tau_{e-LO}}-C_{LO}\left(\frac{T_{LO}-T_A}{\tau_{LO-A}}\right)$$

$$C_A\frac{\partial T_A}{\partial t}=\nabla(k_A\nabla T_A)+C_{LO}\left(\frac{T_{LO}-T_A}{\tau_{LO-A}}\right)+\frac{3nk_B}{2}\left(\frac{T_e-T_L}{\tau_{e-L}}\right)$$

Monte Carlo – Energy Balance Coupling

Particle Model

Fluid Model

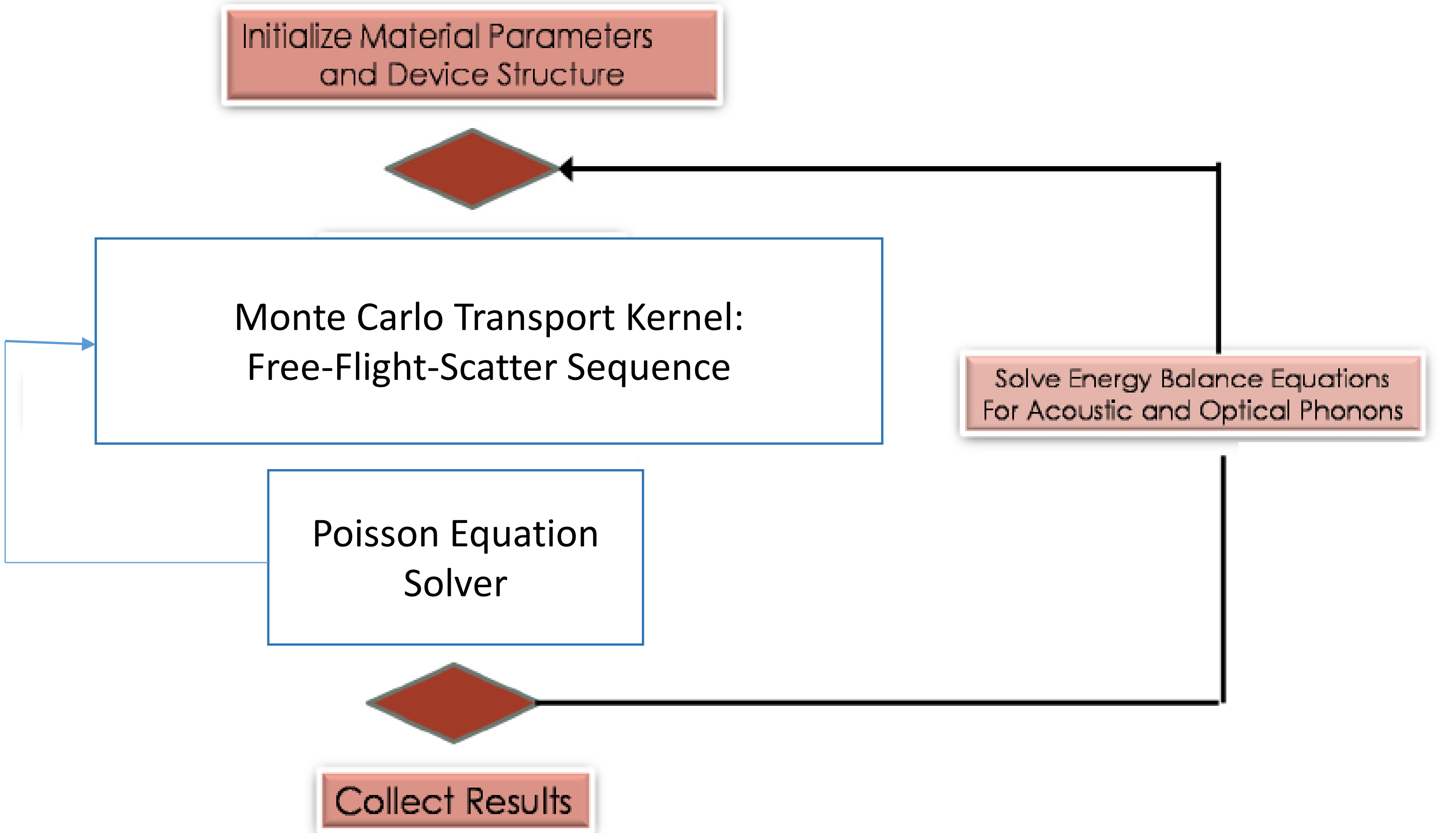


Exchange of variables

Scattering Mechanisms Selection

K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, Modeling Thermal Effects in Nanodevices, IEEE Transactions on Electron Devices, vol. 55, issue 6, pp. 1306-1316, June 2008

Flow-chart of Electro-Thermal Solver



Experimental methods for measuring the temperature of hotspot

1. Thermoreflectance Method[1,2]

Emphasis has been on how to measure average temperature but not the peak hotspot temperature.

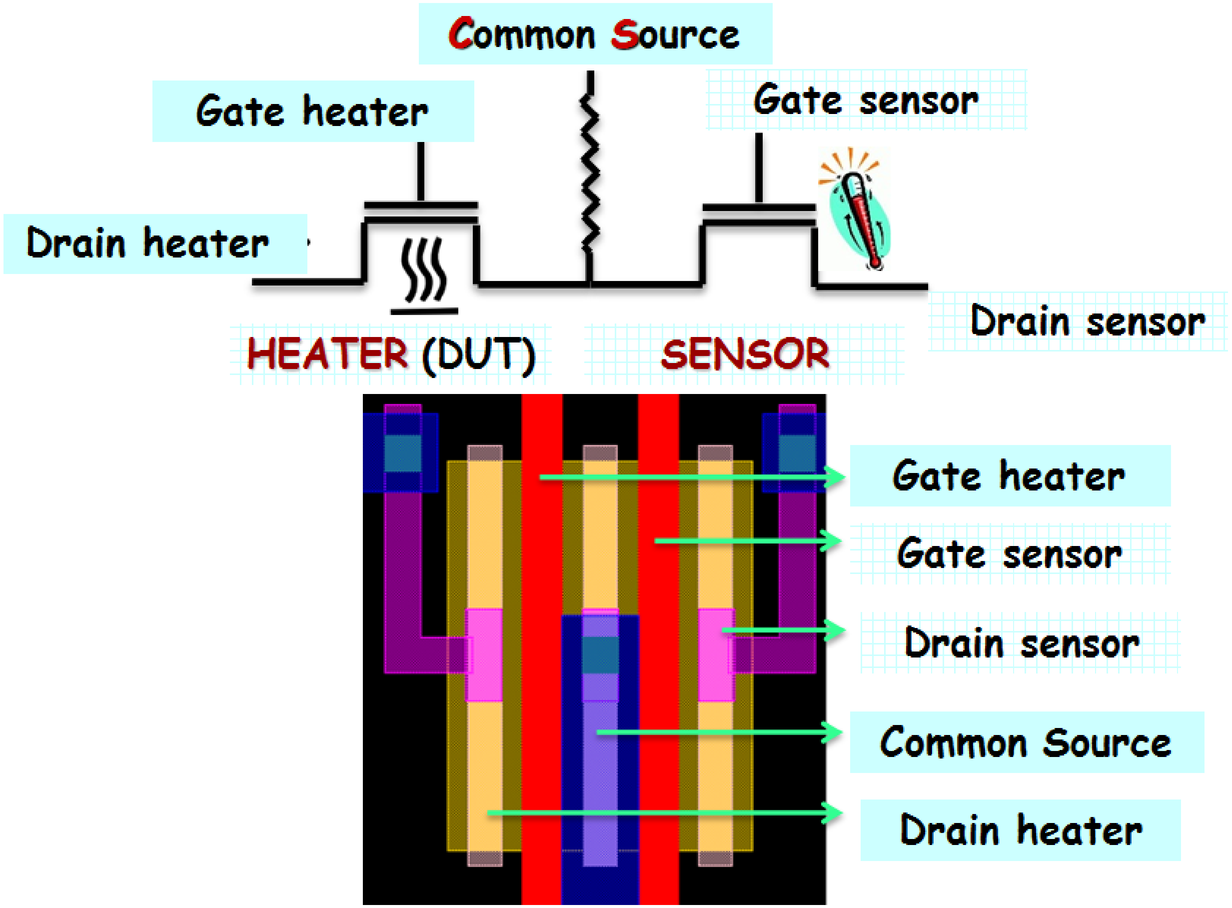
2. IMEC Heater Sensor Approach[3]

1. Nanoscale thermal transport. II. 2003–2012, David G. Cahill, Paul V. Braun, Gang Chen, David R. Clarke, Shanhui Fan, Kenneth E. Goodson, Pawel Keblinski, William P. King, Gerald D. Mahan, Arun Majumdar, Humphrey J. Maris, Simon R. Phillpot, Eric Pop, and Li Shi, Applied Physics Reviews 1, 011305 (2014)

2. Bias-dependent MOS transistor thermal resistance and non-uniform self-heating temperature, Xi Wang, Younes Ezzahri, James Christofferson and Ali Shakouri, J. Phys. D: Appl. Phys. 42 (2009)

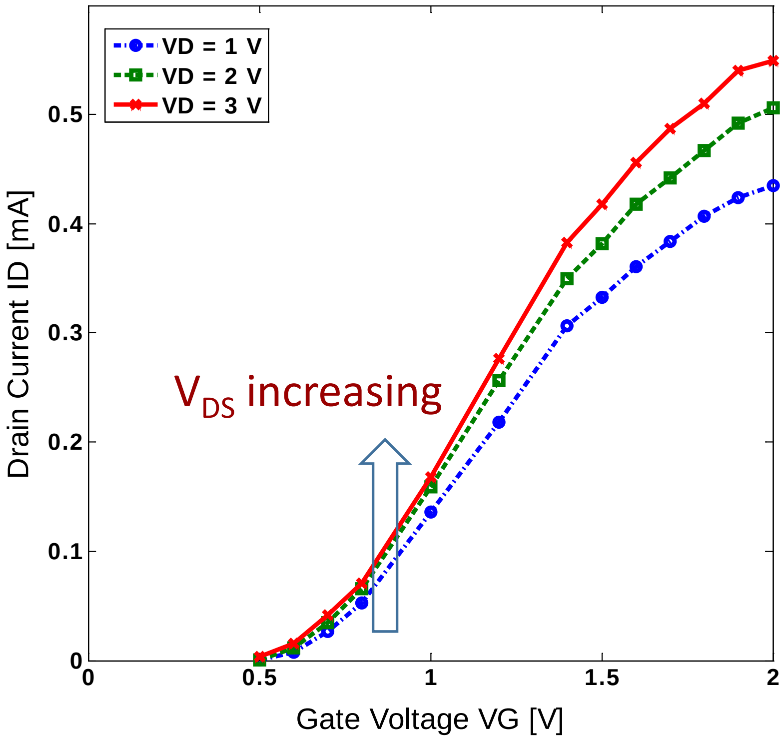
3. Uncovering the temperature of the hotspot in nanoscale devices, Katerina Raleva, Erik Bury, Ben Kaczer and Dragica Vasileska, Computational Electronics (IWCE), 2014 International Workshop on , vol., no., pp.1-3, 3-6 June 2014

IMEC Scheme for Hot-Spot Temperature Measurements (Modeling of a Circuit)

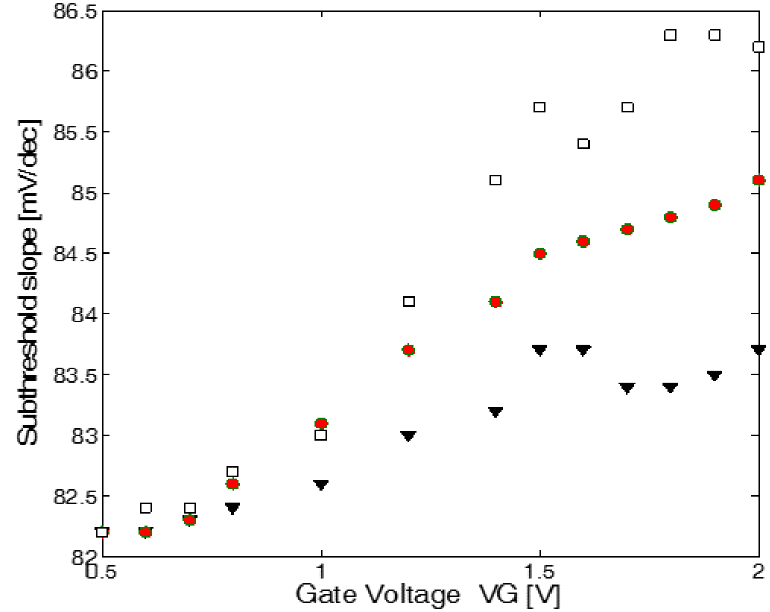


E. Bury, B. Kaczer, P. J. Roussel, R. Ritzenthaler, K. Raleva, D. Vasileska, G. Groeseneken, “Experimental validation of self-heating simulations and projections for transistors in deeply scaled nodes”, in Proceedings of IEEE, Reliability Physics Symposium, 2014 IEEE International, pp. XT. 8.1-XT. 8.6.

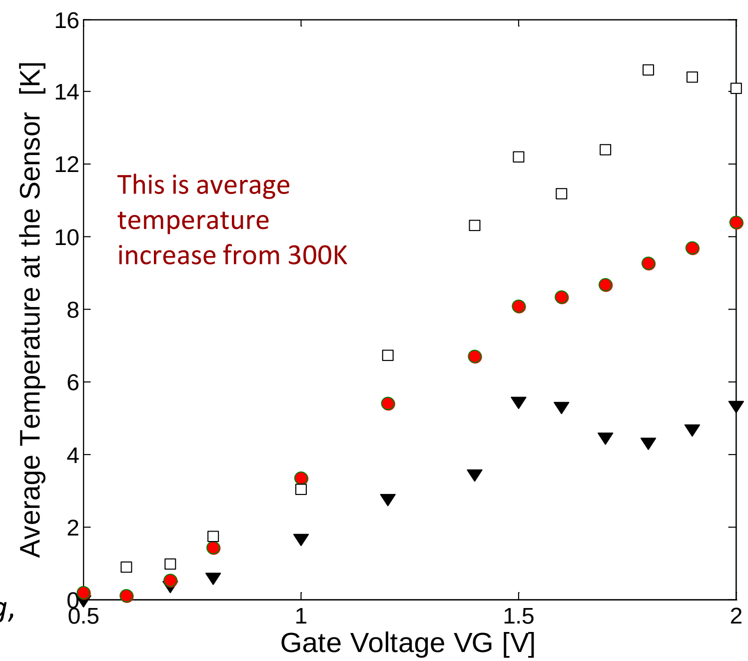
Measured Data



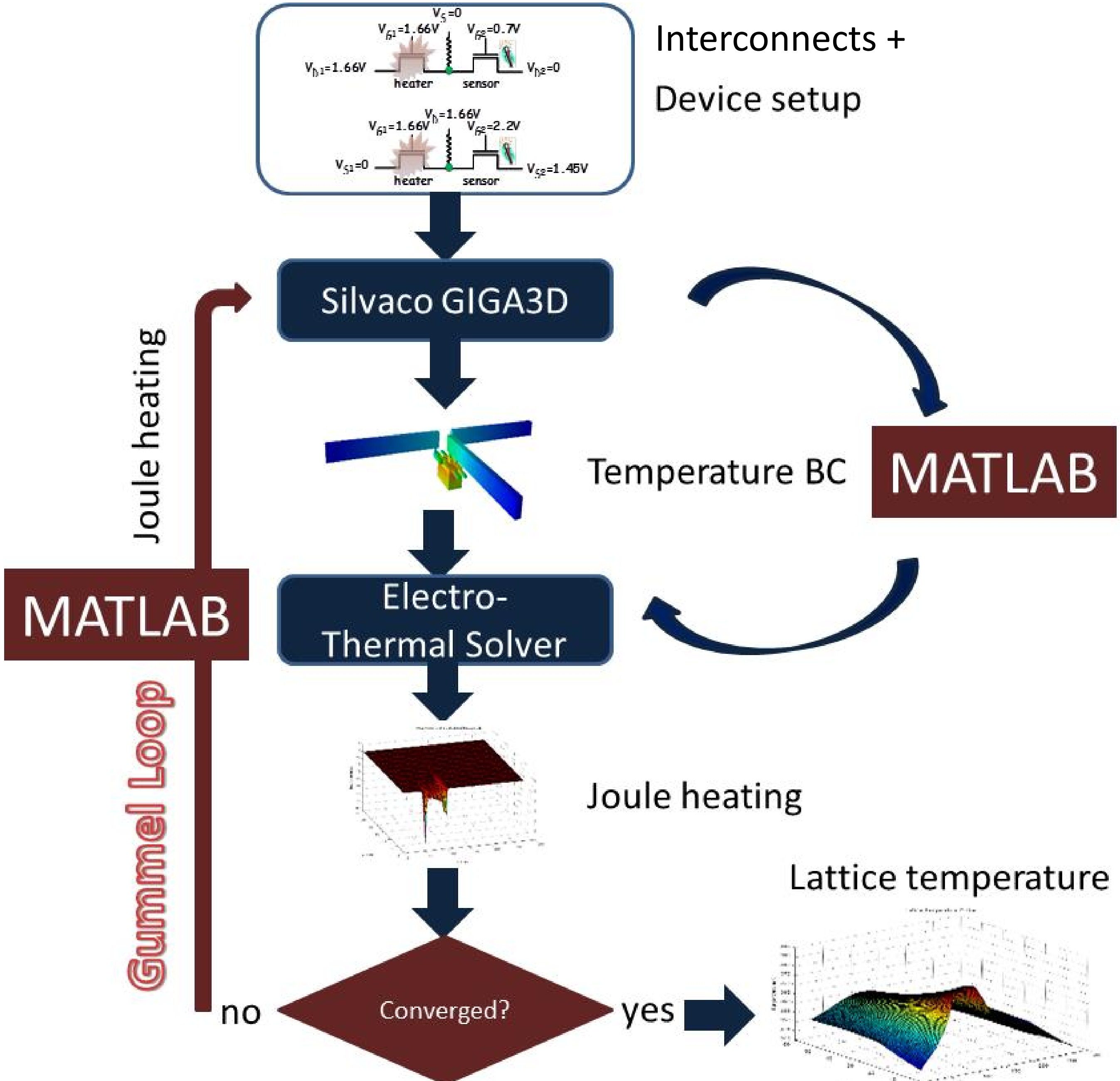
Sensor Transfer Characteristics



EKV Model

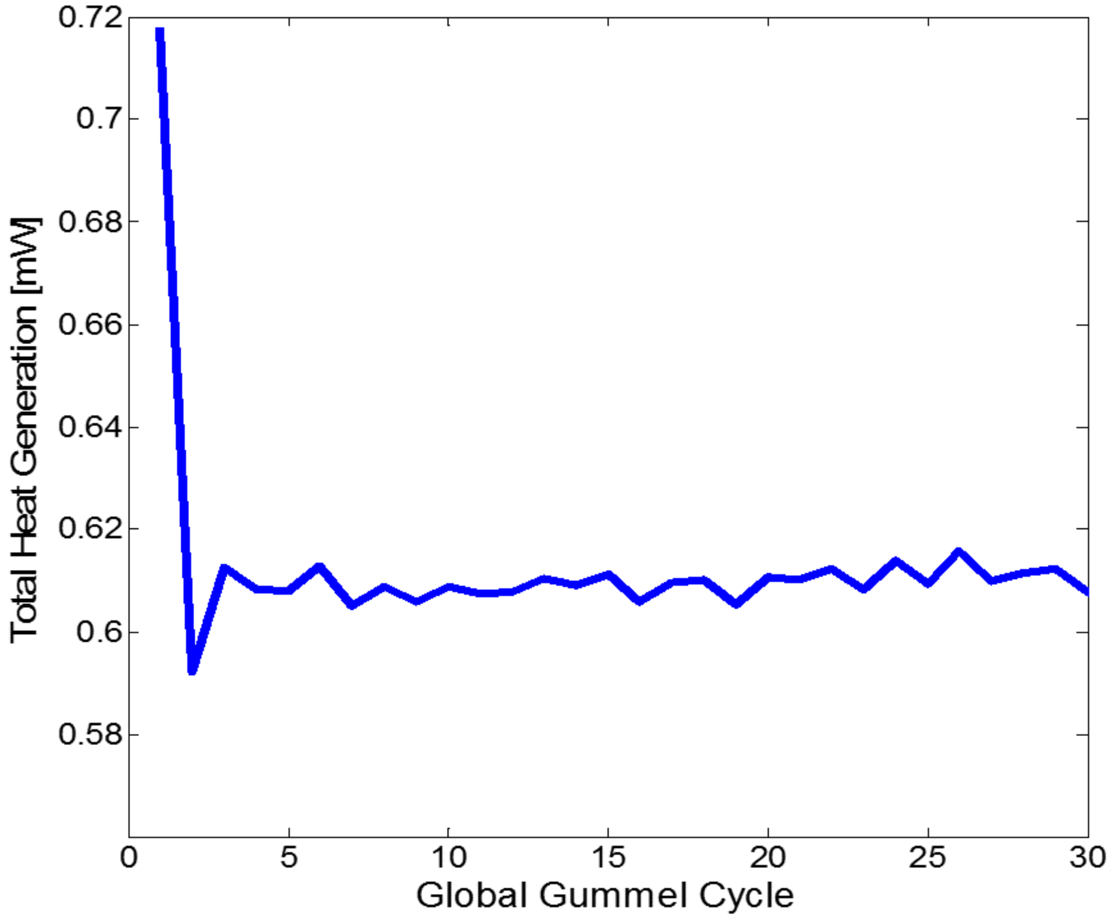


C. C. Enz, F. Krummenacher and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", *Analog Integrated Circuits and Signal Processing*, **8**, pp.83-114 (1995)

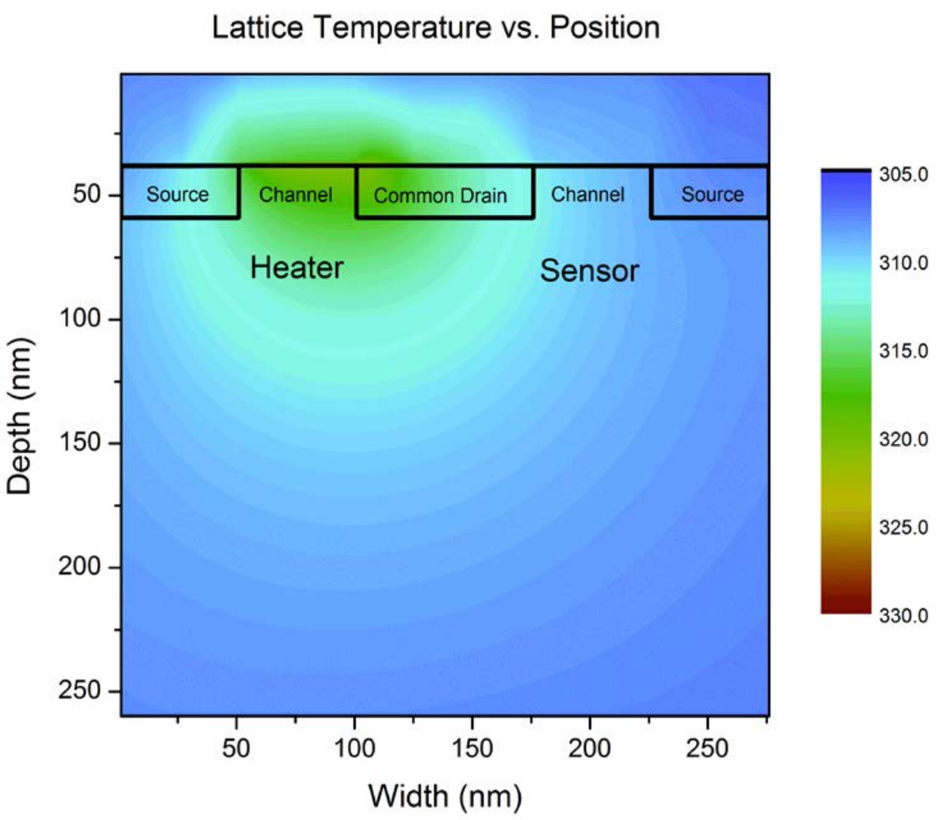


Katerina Raleva, Erik Bury, Ben Kaczer, Dragica Vasileska, "Uncovering the temperature of the hotspot in nanoscale devices", in *Proceedings of IEEE, Computational Electronics (IWCE), 2014 International Workshop on*, pp. 104-106.

Convergence in Multi-Scale Analysis

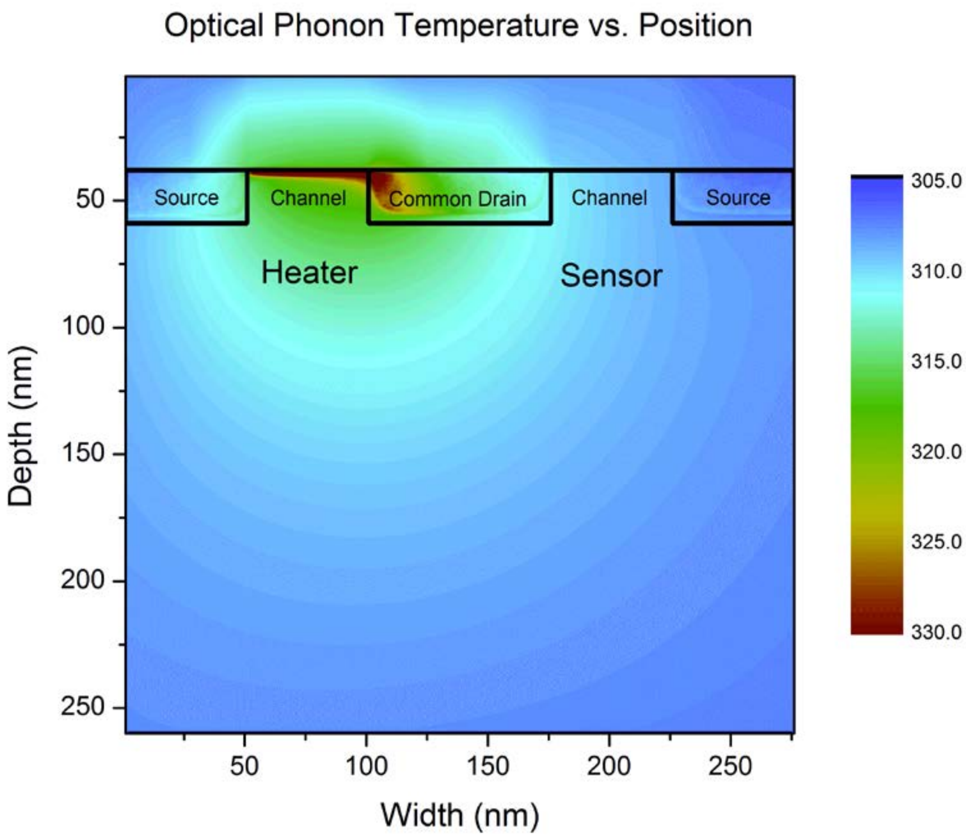


Results from Multiscale Electro-Thermal Simulation



Global Lattice Temperature Profile

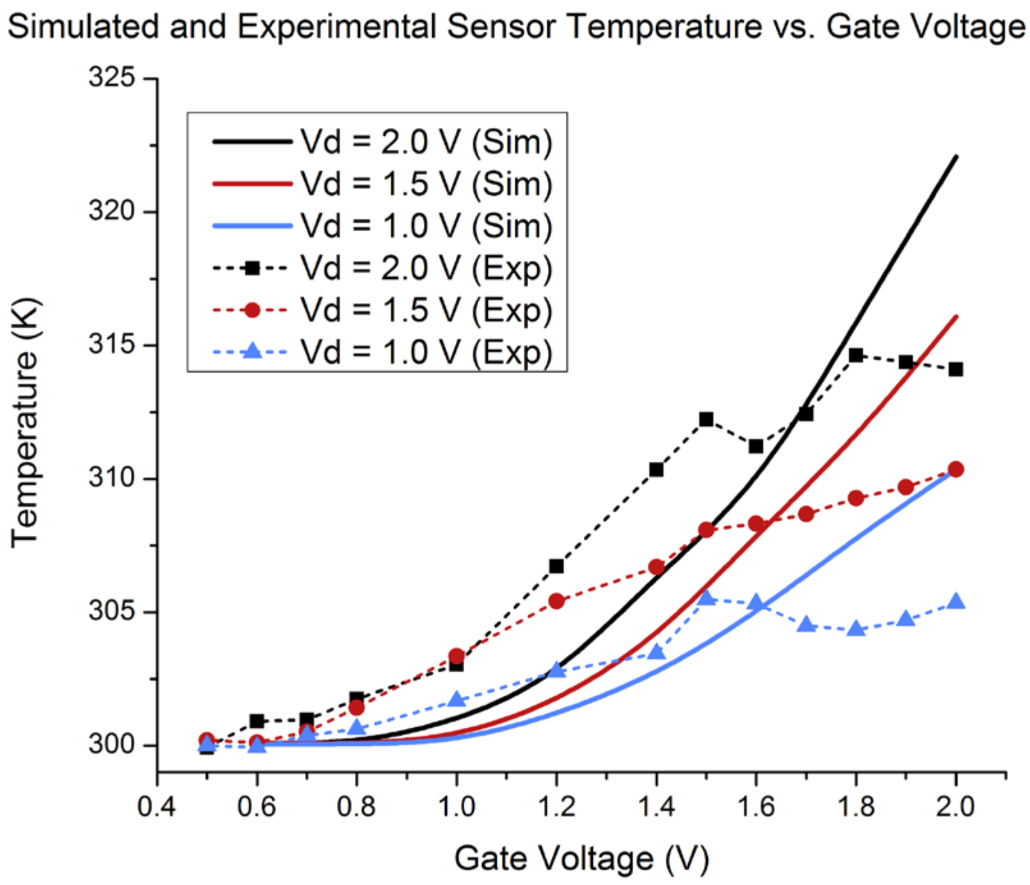
Max Temperature = 320.49K



Global Optical Phonon Temperature Profile

Max Temperature = 356.42K

Global Simulation Results: Proof of Concept



Conclusions

- A Multi-Scale simulator has been developed to model the heater-sensor combination + interconnects.
- The Electro-Thermal device simulator is a multi-scale solver that self-consistently solves the BTE for the electrons with the energy balance equations for the optical and acoustic phonon bath.
- At the circuit level, GIGA3D module from Silvaco was used to solve for the lattice temperature and hence obtain the boundary conditions for the Electro-Thermal Device simulator.
- Simulation results for the average sensor temperature are in agreement with experimental measurements.

Thank You

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