Nanometer Scale Patterning and Processing

Spring 2016

Lecture 1 - Introduction

Nanometer Scale Patterning and Processing

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- Background:
  - 1995 BS, University of Science and Technology of China
  - 1998 MS, 2005 PhD, MIT
  - 2005-12, Assistant Professor, Purdue University
  - 2012-presnt, Associate Professor, Purdue University
- Website for this course to be setup

About the course

- This is a graduate course, so we take it for knowledge, not for grades.
- My goal: you become a general consultant on top-down nanofabrication, e.g. answering questions from your groupmates; and an expert in one or a few special techniques, e.g. e-beam lithography, nanoimprint, etc.
- Small class size means more interaction with instructor and fellow students
  - Know your classmates!
- Questions and in-class discussions are welcome.
- Office hours: open-door or by appointment.
- Meeting time and location:
  EE 226, MWF 1:30 – 2:20 pm
- Lectures will be video taped.

Major References

- Xiao, Hong, "*Introduction to semiconductor technology*"– 2nd ed. SPIE, 2012, ISBN 978-0-8194-9092-6 (Abbreviated as Xiao 2012)
- Frey, Hartmut, Khan, Hamid R, Editors, "*Handbook of Thin-Film Technology*", Springer, 2015, ISBN 978-3-642-05429-7 (Abbreviated as Frey, 2015)
- Both books available in electronic format through Purdue Library.

Assignments, Expectations and Grading

- Midterm: 30%
  - Closed book with notes or take home. Questions from recent literature.
- Homework: 10% (+ bonus points)
  - Literature reading and some technical calculations
- Key technical paper search (individual) 30%
  - This is an important component of the course.
  - I need your initial input early in the semester.
  - Treat it as if you are preparing your prelim, though the stuff would be someone else's.
  - You can reuse your previous literature studies from your thesis proposal, prelim, etc.
  - Spend time on how to best present it if you have previous materials ready.
- Technology Intelligence Case Study (group) 30%
  - I will prepare a few topics and you will vote to select.
  - More detail will come.

Tentative Schedule

Date	Topic
Week 1	Introduction to nanometer-structures technology and applications; top-down approach and bottom-up approach; Contamination control (classes of cleanrooms, etc.), Substrate cleaning
Week 2	Adding materials for nanofabrication: spin-coating, evaporation (including lift-off), Chemical Vapor Deposition (CVD); Resist technology.
Week 3	Fourier optics and optical microscopy; Optical resolution. Spatial filtering and contrast in optical microscopy;
Week 4	Optical systems for lithography: contact and near-field optical lithography, projection optical lithography; Laser interferometer technology.
Week 5	Resolution enhancement techniques; Negative refraction and superlens effect.
Week 6	Laser interference lithography and its application to periodic nanostructures, including negative index metamaterials and photonic crystals. Surface profilometer and Atomic Force Microscopy (AFM); Ellipsometry.
Week 7	Electro-optical systems for microscopy and lithography; Signals and noise in scanning-electron-beam systems.

Tentative Schedule (Continued)

Week 8	Electron-beam lithography systems; Electron scattering and proximity effects
Week 9	Introduction to the Vector Beam system in Birck Nanotechnology Center.
Week 10	Focused ion-beam lithography; Mask making; Maskless lithography.
Week 11	Proximity x-ray lithography, electron and ion projection lithography, focused ion-beam lithography, proximal-probe lithography; embossing; Resolution, throughput and cost of future lithography tools.
Week 12	Nanoimprint Lithography: thermal and step-and-flash. Soft-lithography. Registration and overlay techniques in lithography.
Week 13	Removing materials: plasma basics, (deep) reactive-ion etch, sputter etch, ion-milling; Wet etch; polishing and planarization.
Week 14	More ways of adding materials: sputter deposition, electroplating, Atomic Layer Deposition (ALD) and epitaxy (lattice mismatch, critical thickness).
Week 15	Technology Intelligence Case Study Presentations

Nanotechnology/Nanostructures: the various elements

- Nano-scale entities:
  - Macromoecules
  - Nanoparticles, quatum dots, and buckyballs (0D nanostructures)
  - Nanotubes, nanowires (1D nanostructures)
  - Planar nanofilms and nanostructures (2D nanostructures)
  - 3D nanostructures (fixed, such as IC circuits)
  - Movable 3D nanostructures (NEMS)
  - Subcellular biological entities

Nanofabrication: Two Fundamental Approaches

Top Down: Implementation of various techniques to remove, add or redistribute atoms or molecules in a bulk material to create a final structure. Miniaturizing existing processes at the macro/micro-scale

- Lithography and planar processing
- Direct manipulation (e.g. scanning probes)

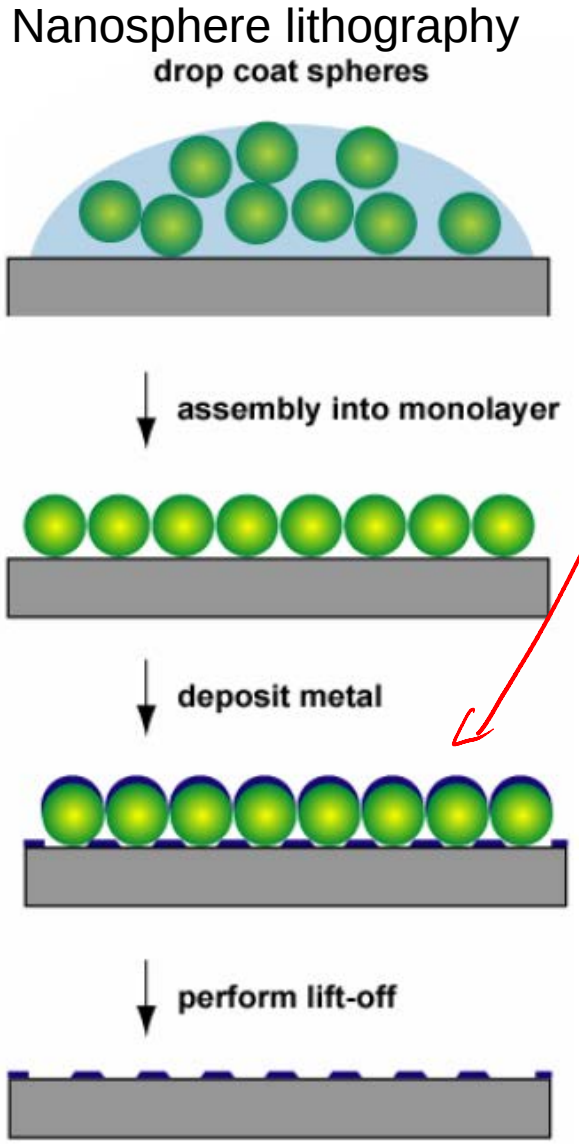
Machined

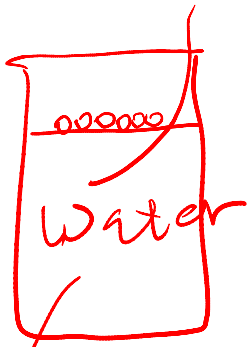
Bottom up: Atomic and molecular scale directed assembly to create larger scale structures with engineered properties

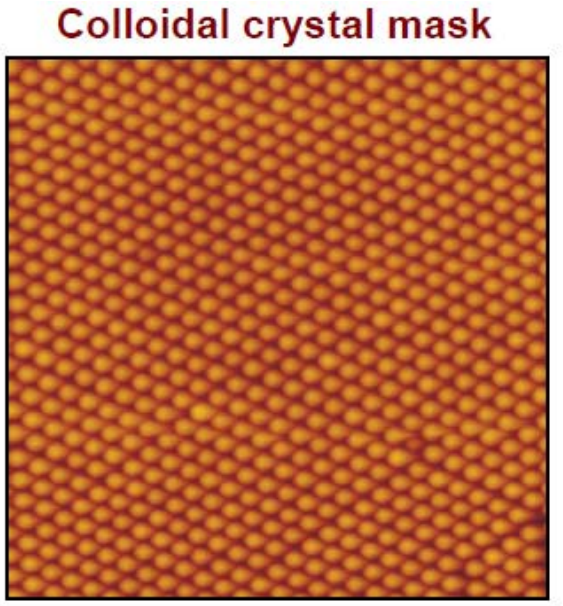
- Chemical synthesis
- Self assembly
- Biology (guided synthesis and assembly)
- 3D printing (macroscopic at this moment, though)

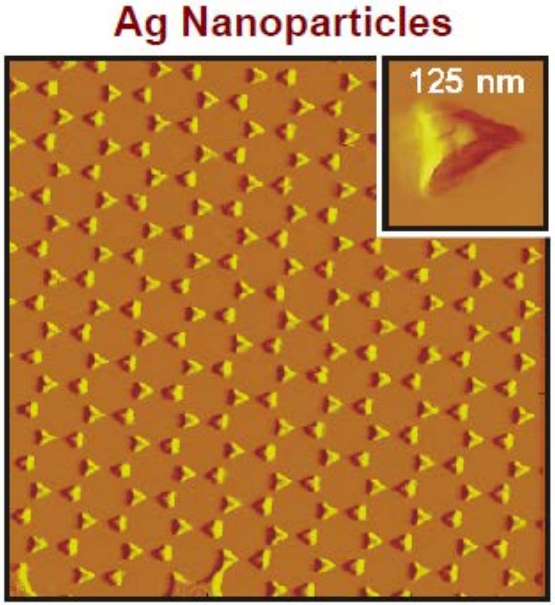
Assembled

Example of a Bottom-Up Fabrication Process



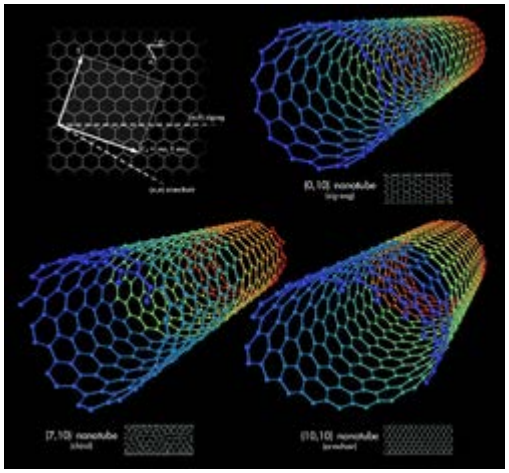






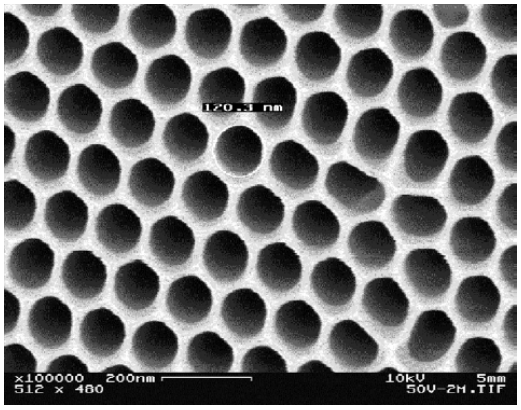
Bottom-up Nanofabrication

Chemical synthesis
- Nanotubes and nanowires
- Quantum dots and nanoparticles
- Polymers
- Proteins
- Nanofibers produced by proteins



Carbon nanotube

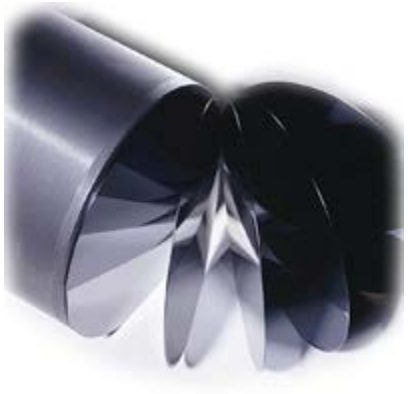
Functional arrangement
- Self assembly
  - Mono-layers, e.g. nano-sphere lithography
  - Block copolymers
  - Functionalized nanoscale structures
- Fluidic or field assisted assembly
- Surface tension directed assembly
- Templated growth
  - Step edges and defect or strain fields
  - Porous materials, e.g. anodized aluminum oxide
- Scanning probe manipulation
  - AFM, STM with atomic resolution



Anodized aluminum oxide

Contents courtesy of Prof. Bo Cui

Top-Down Nanofab: Semiconductor Industry

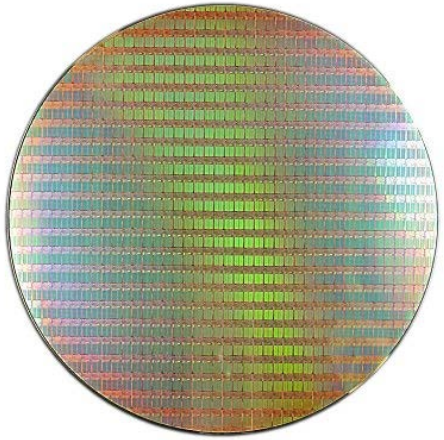


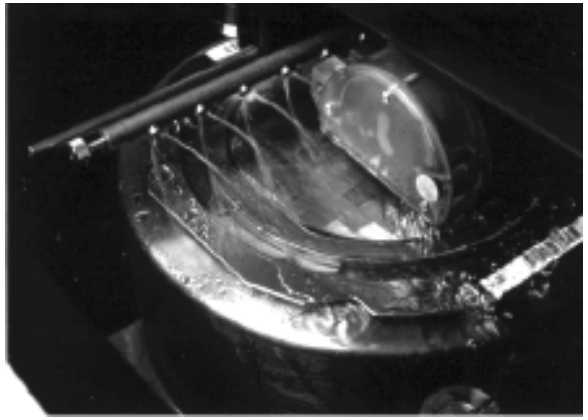
ECE 695

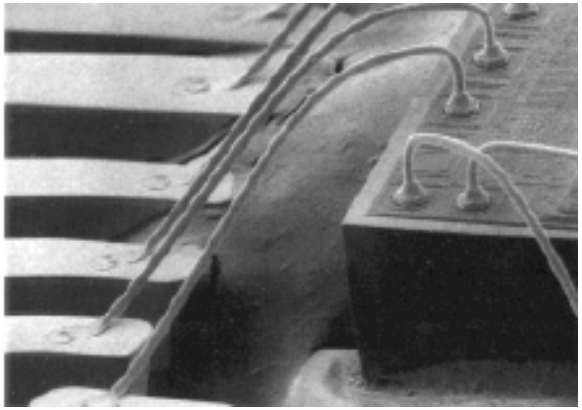
ECE 556

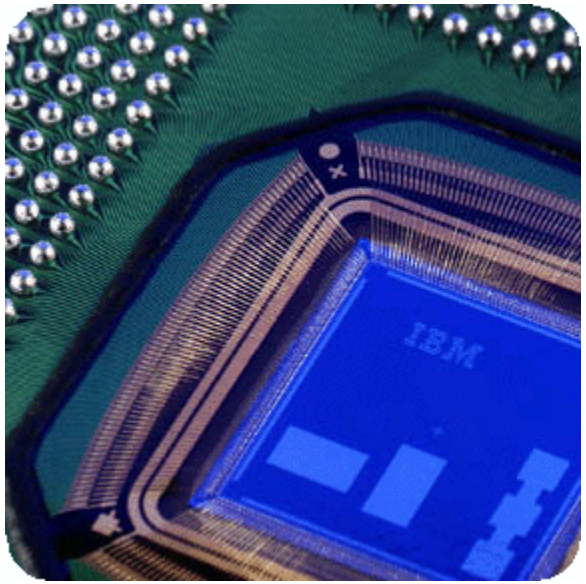
ECE 557

+ $10 billion

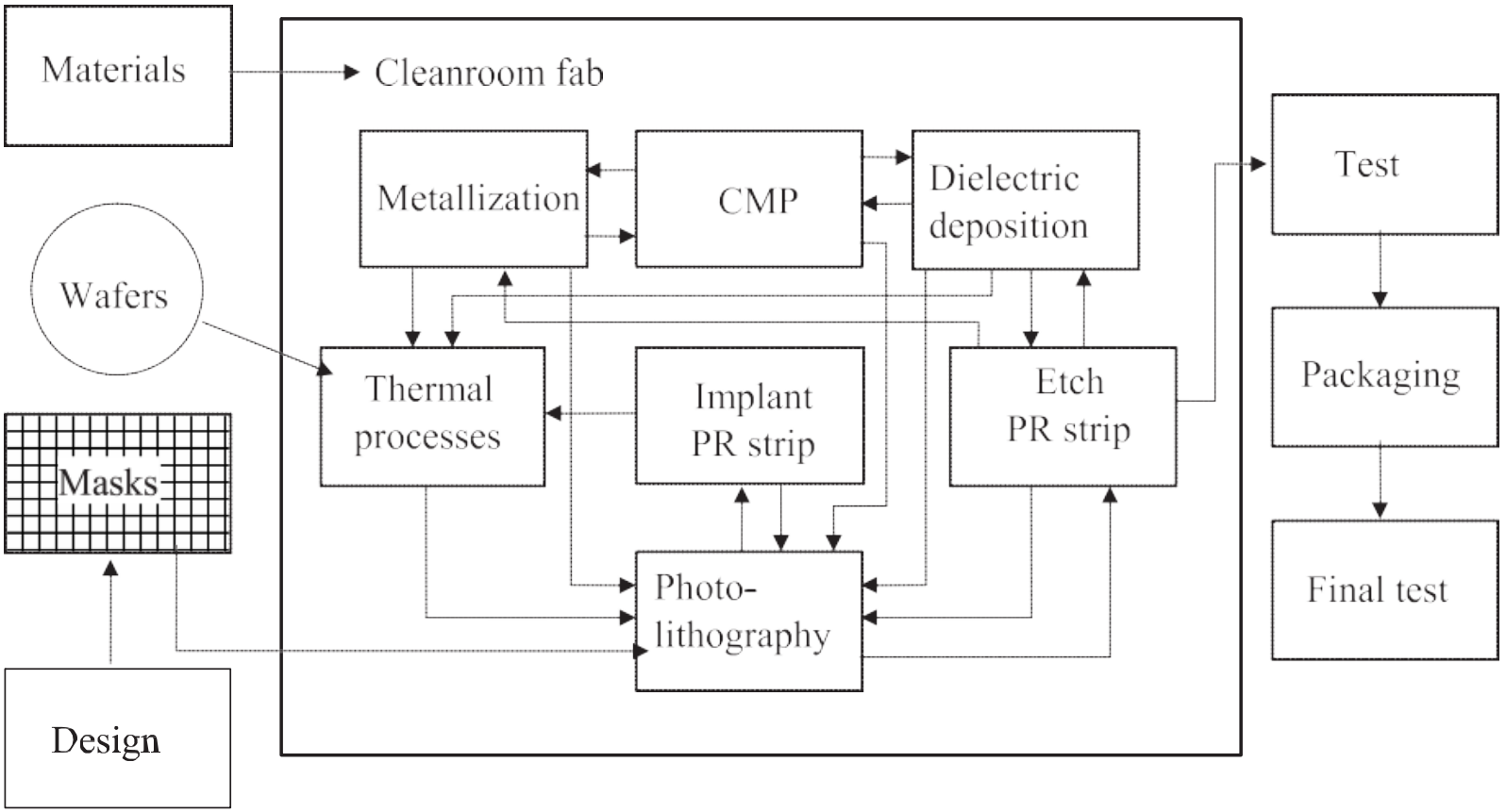






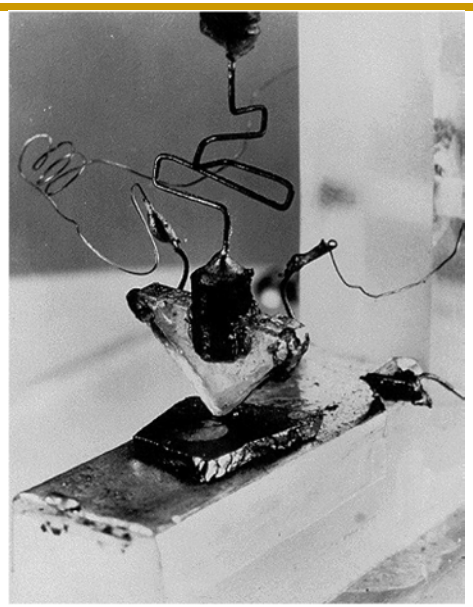


How are Chips made?

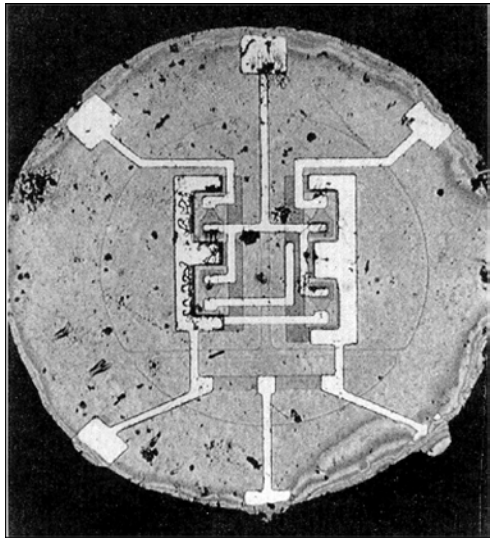


- Unit Processes for CMOS manufacturing

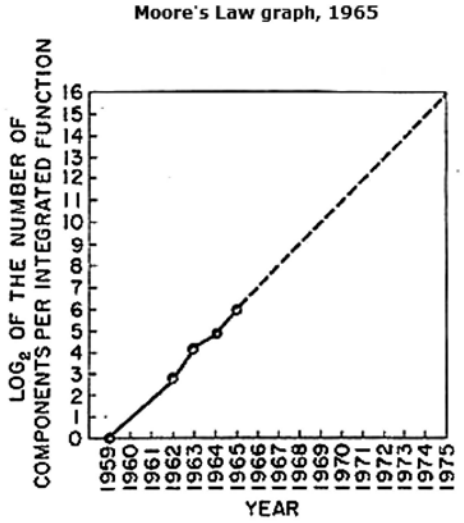
Brief History of Semiconductors and Integrated Circuits



(Xiao 2012) Figure 1.1 The first transistor made in AT&T Bell Laboratories (AT&T Archives).



(Xiao 2012) Figure 1.4 The first IC made on a silicon wafer by Fairchild Semiconductor (Fairchild Semiconductor International).



(Xiao 2012) Figure 1.7 Moore's observation and prediction in 1965 (source: http://www.intel.com/technology/mooreslaw/).

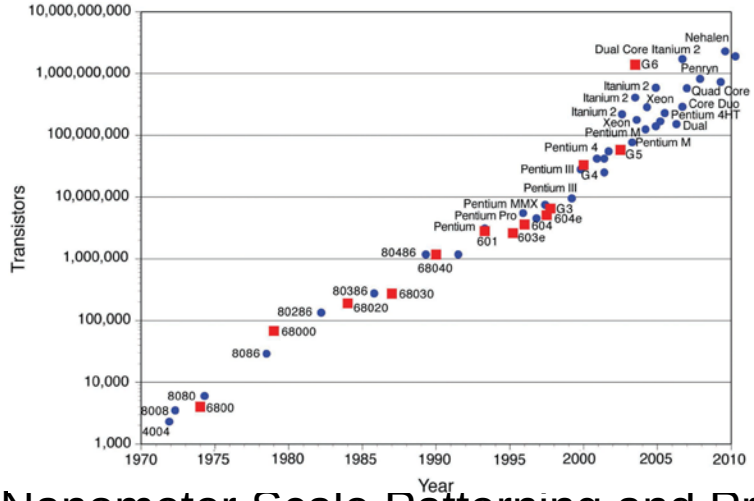
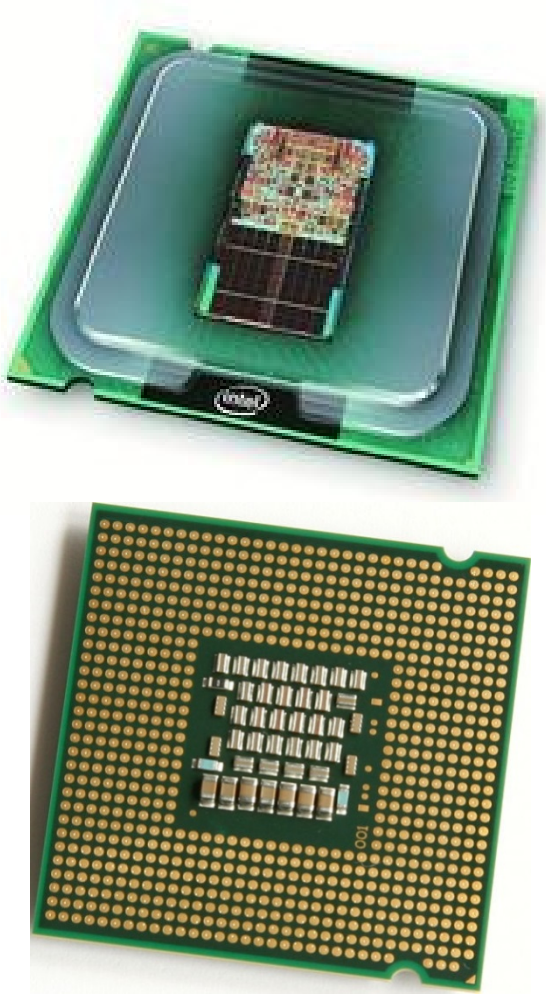
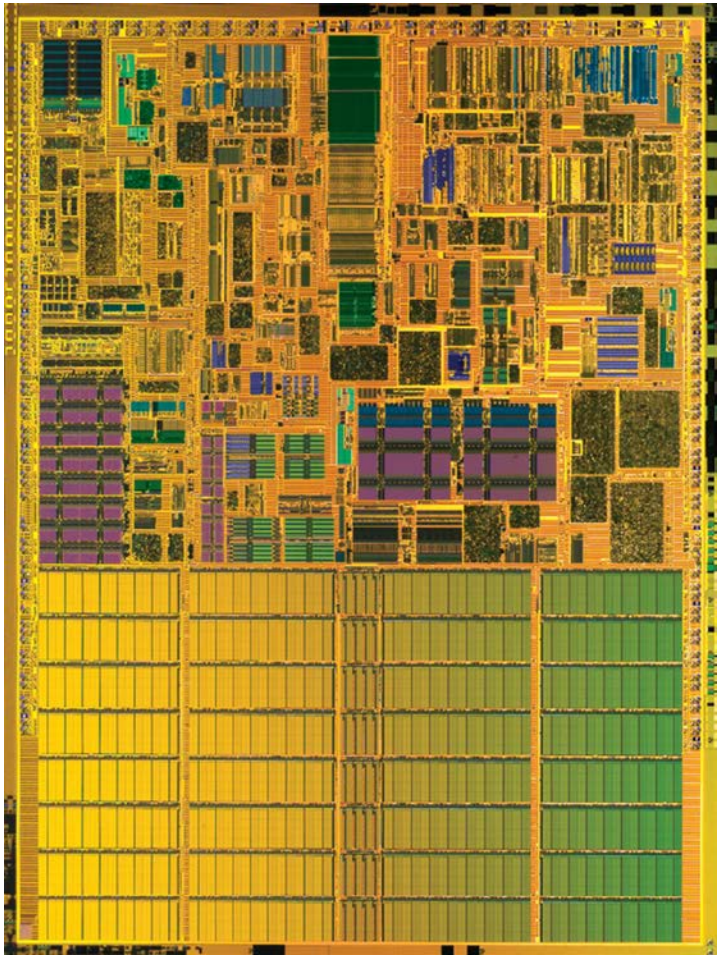


Figure 1.8 Moore's law of microprocessors (source: http://www.is.umk.pl/~duch/Wyklady/komput/w03/Moores_Law.jpg).

Integrated Circuits

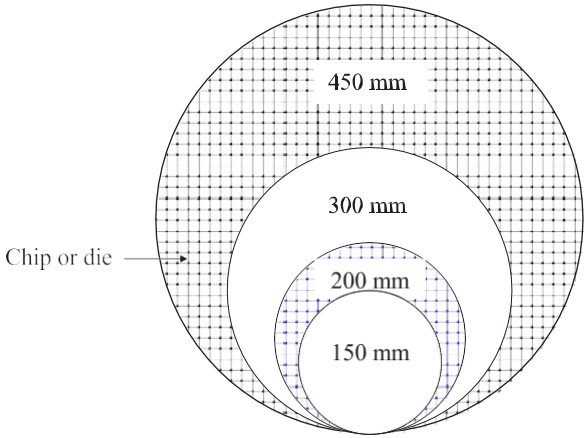


Intel core 2 duo
©Intel

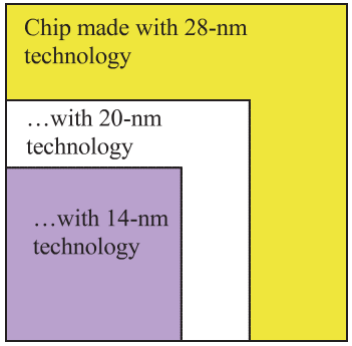


Intel Centrino die photo
©Intel

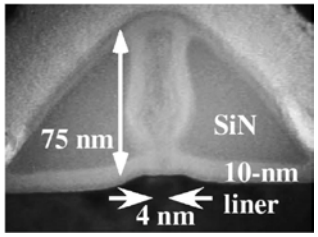
Wafer Sizes and Technology Nodes



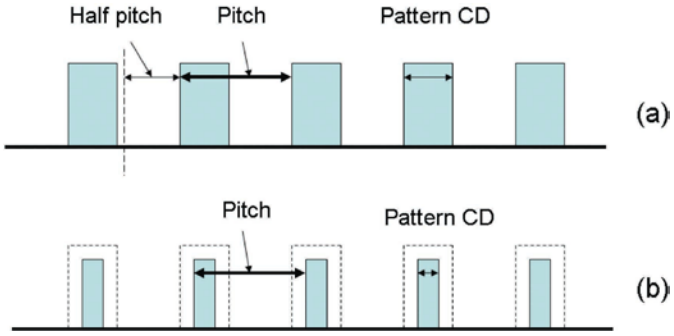
(Xiao 2012) Figure 1.11 Relative wafer sizes.



(Xiao 2012) Figure 1.9 Relative chip size with different technology nodes.



(Xiao 2012) Figure 1.10 The world's smallest known metal-oxide-semiconductor transistor (H. Wak- abayashi, et al., *IEEE Proc. IEDM*, 2003).



(Xiao 2012) Figure 1.12 Relationship of pattern CD and pattern pitch. (a) Initial photoresist pattern and (b) photoresist pattern after trimming. Although pattern CD is reduced by the trimming process, pattern pitch remains the same.

Inside transistor and silicon

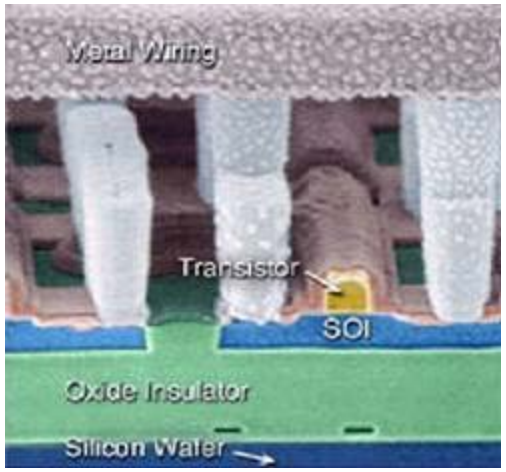
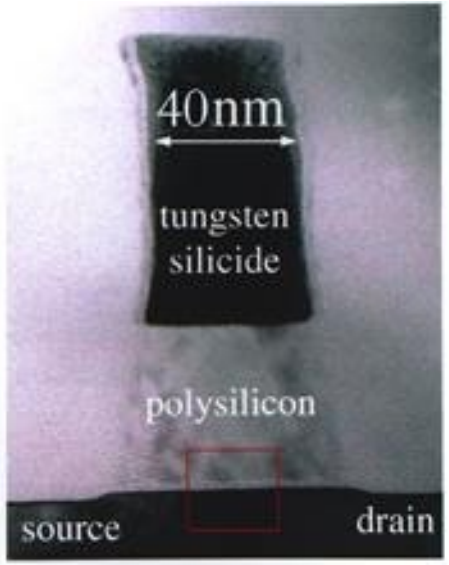
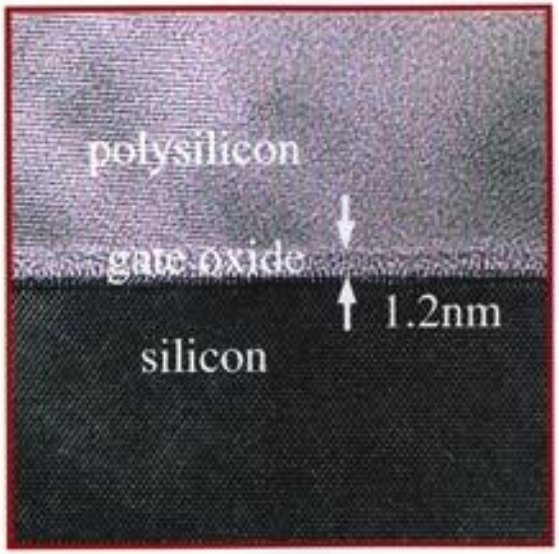
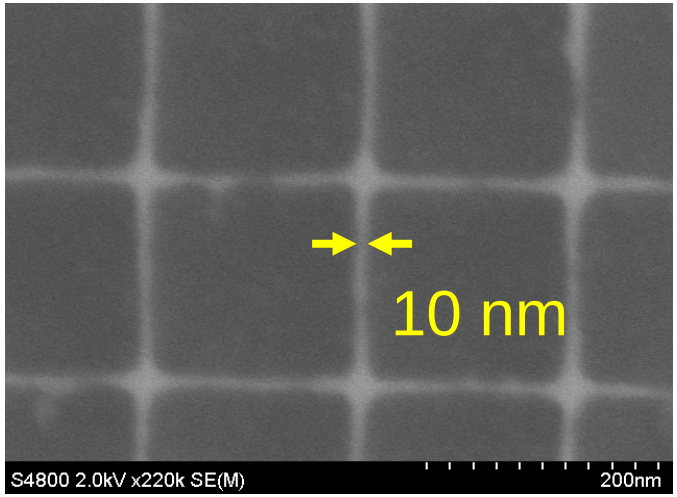


Illustration of a transistor ©IBM





Silicon-oxide interface ©Bell-Labs



10 nm lines of SiO_2 on Si

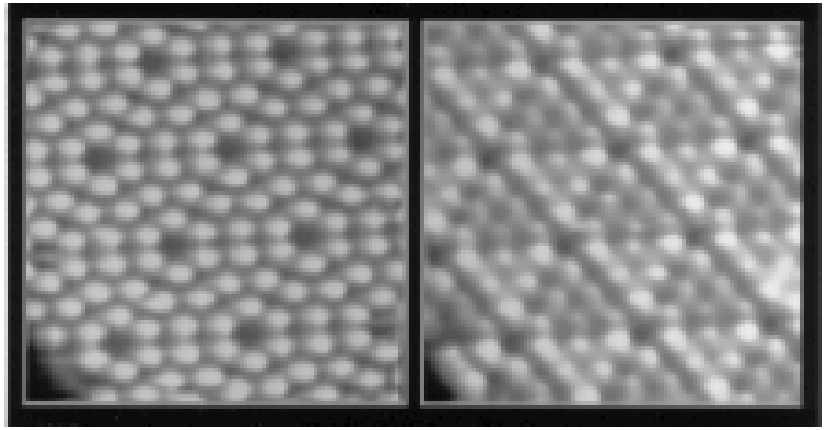
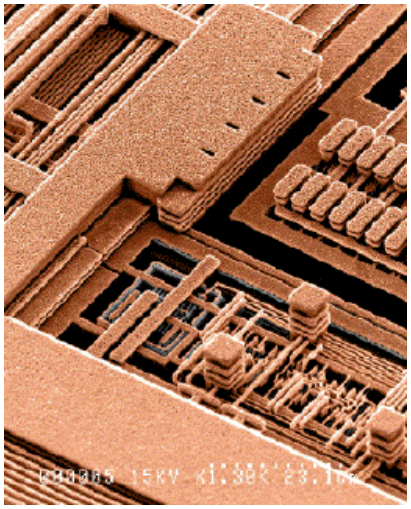
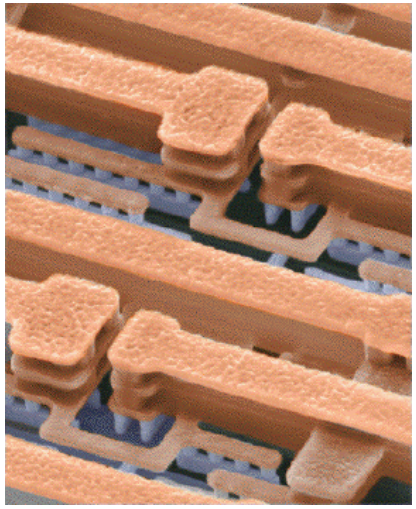


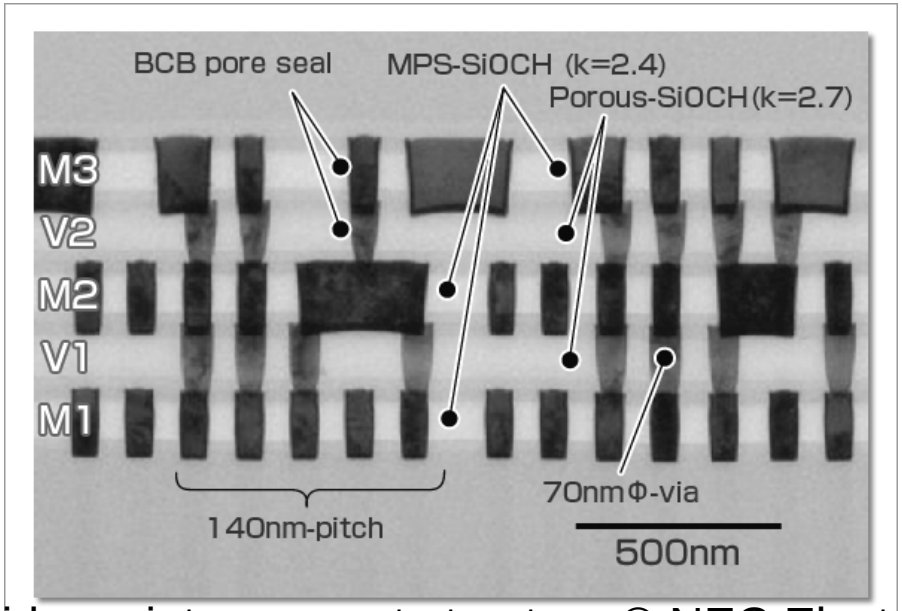
Image of atoms via STM on the {111} surface of silic

Inside an integrated circuit chip





IBM copper interconnects ©IBM



Multi-layer interconnect structure © NEC Electronics Corp.

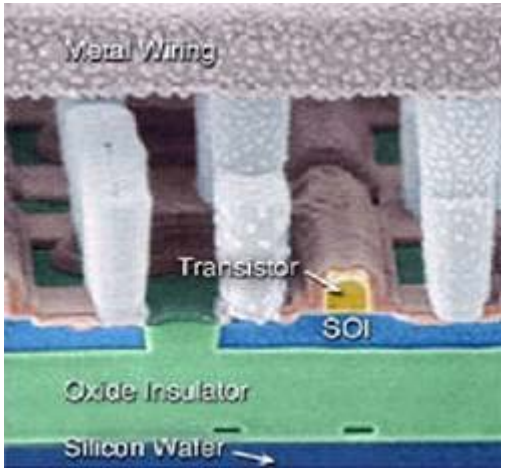
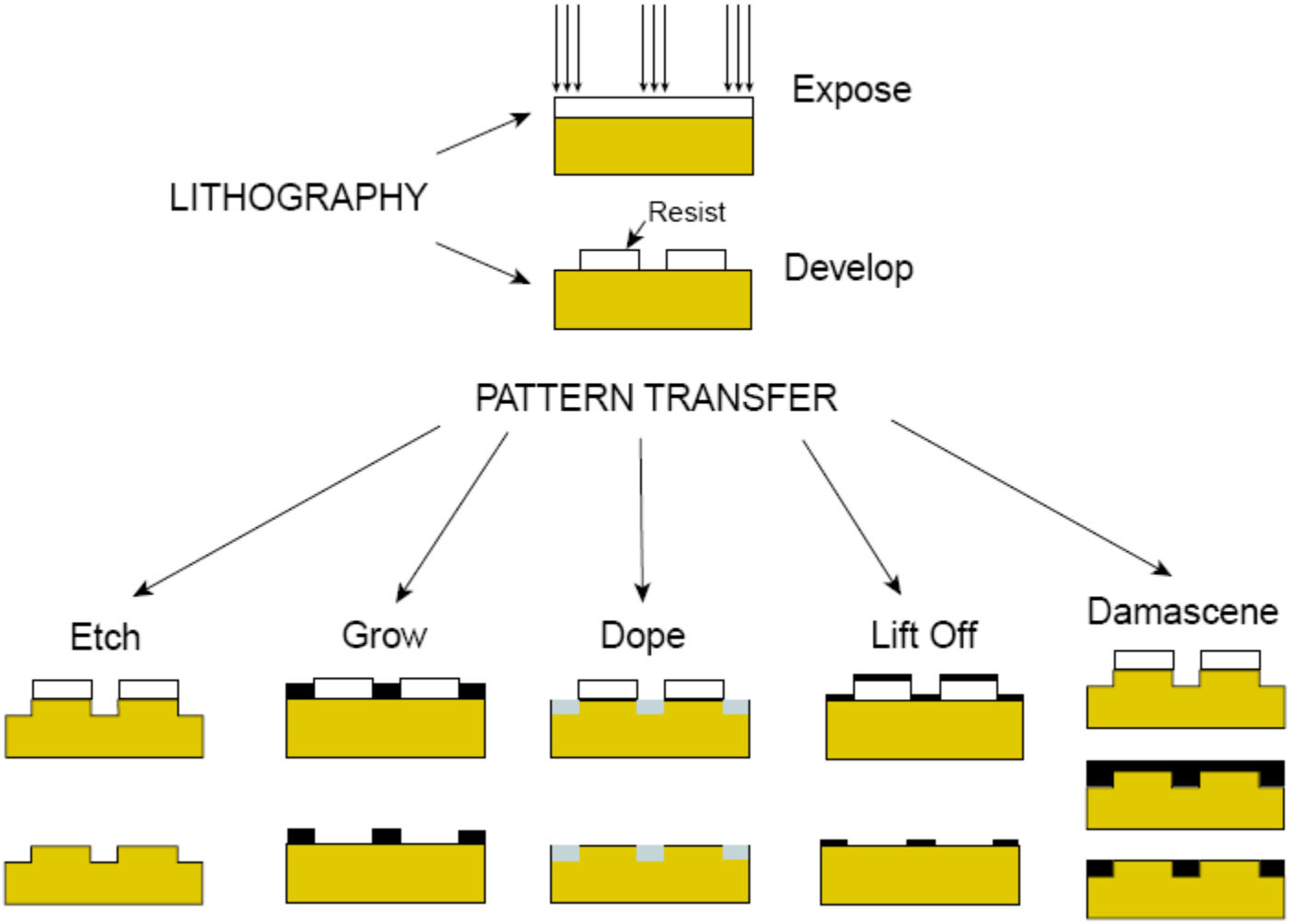


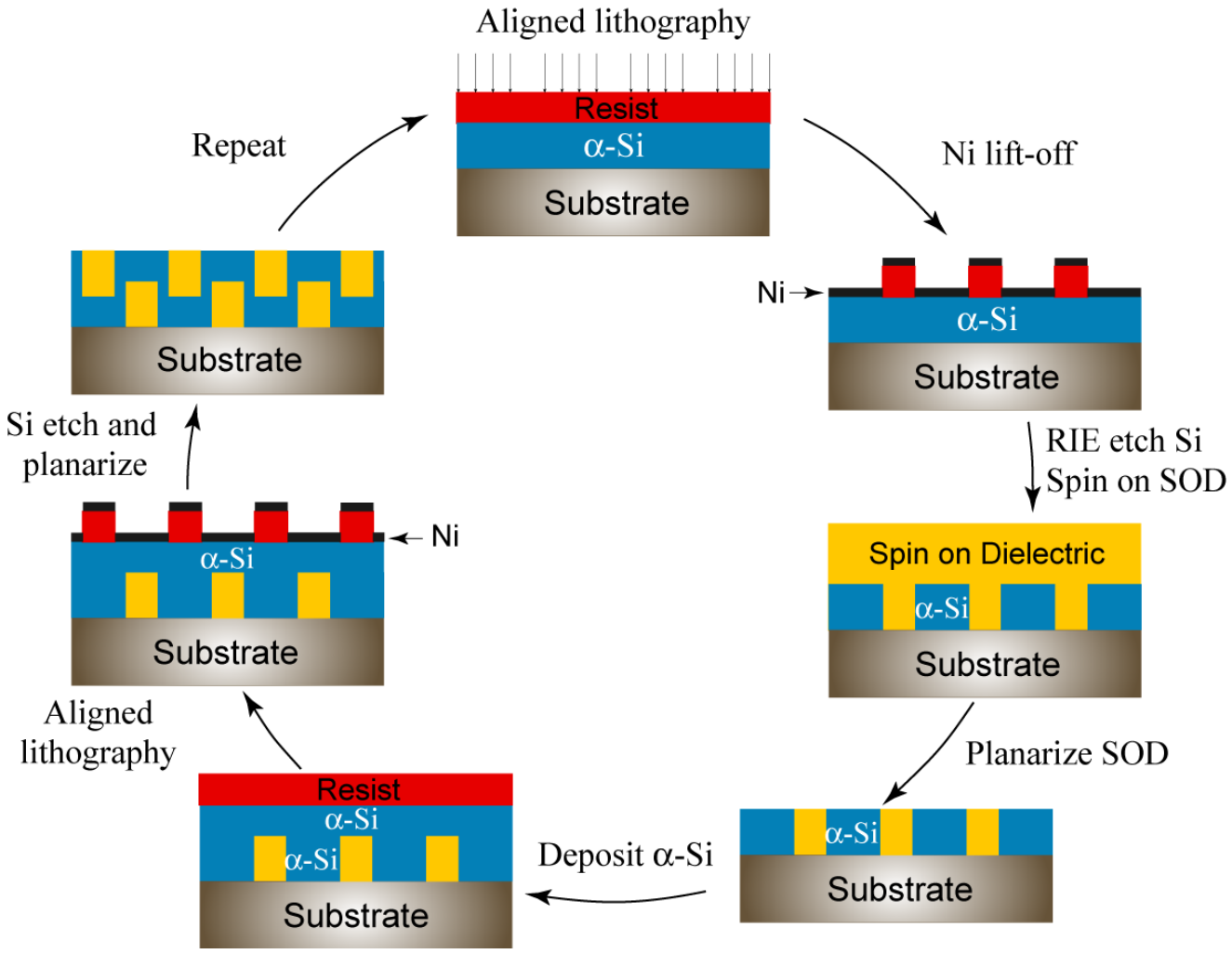
Illustration of a transistor ©IBM

The Planar Fabrication Process



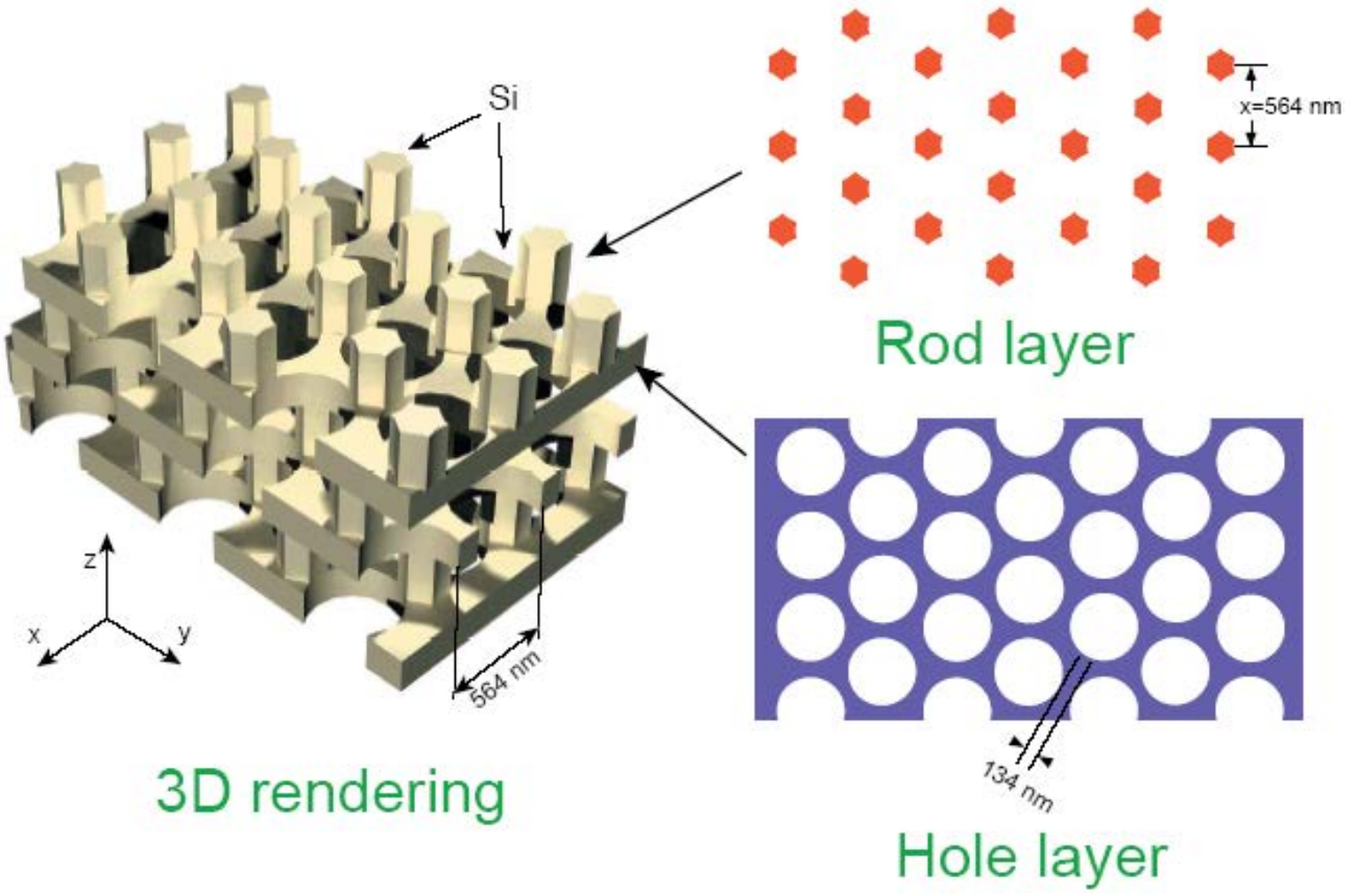
Contents courtesy of Prof. Henry I. Smith

Layer-by-layer approach to 3D Nanostructures



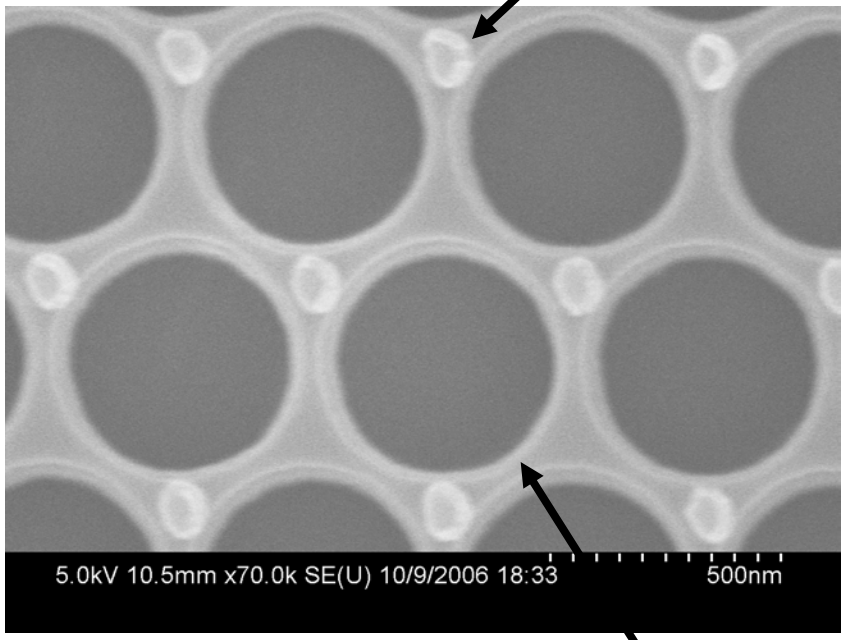
Can fabricate any 3D structures (in principle).

A Layered 3D Photonic Crystal



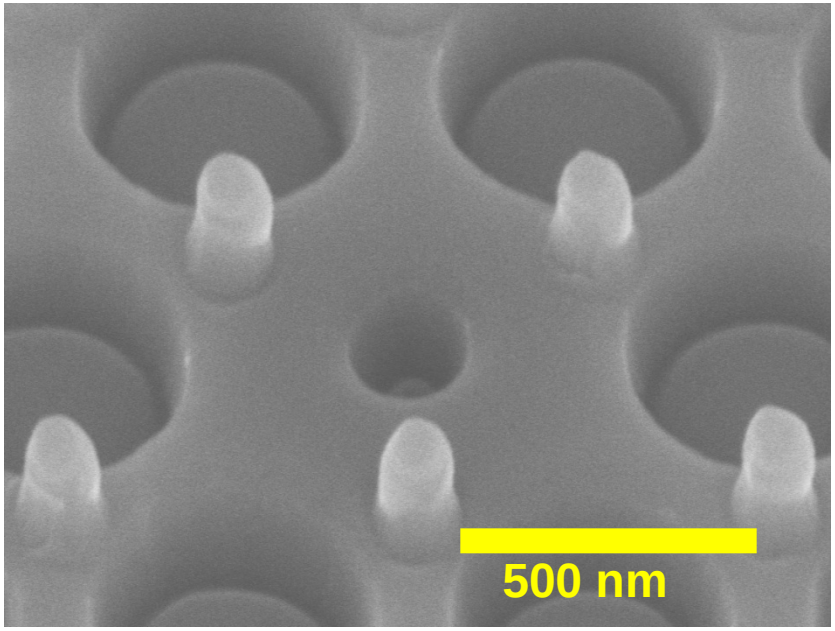
Aligned Nanostructures

2nd layer rods



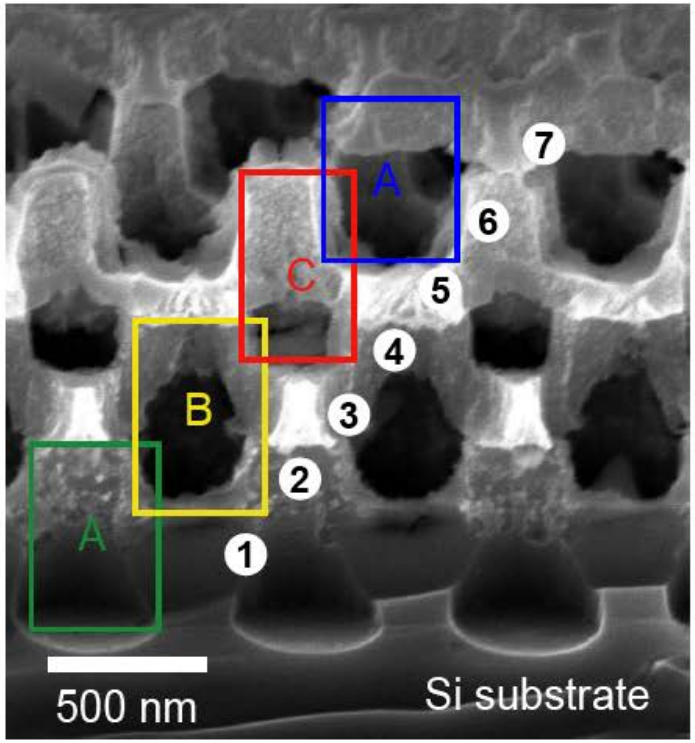
1st layer holes

Top view

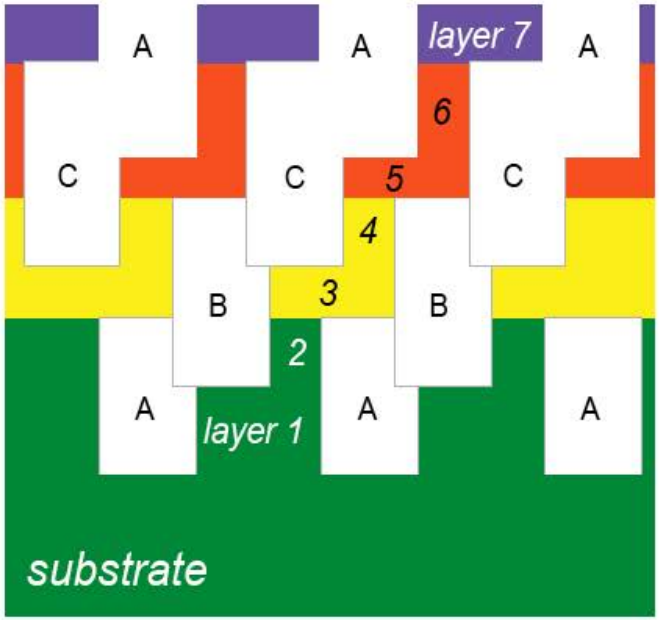


Tilted view

Cross-Sectional View

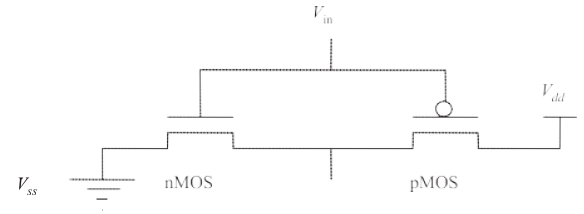


SEM micrograph

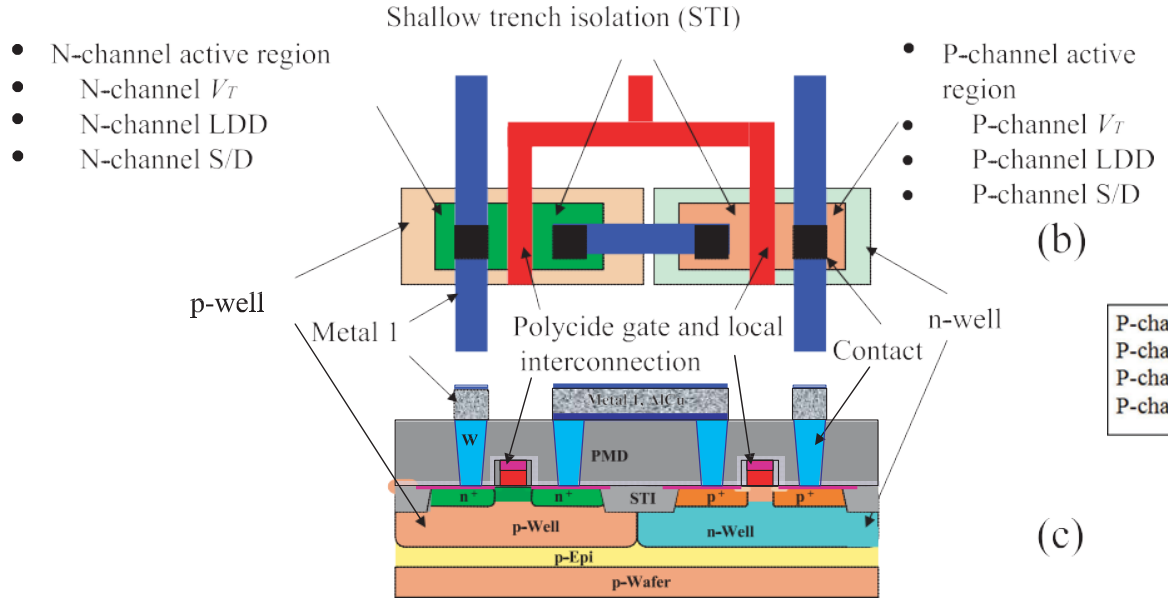


Schematic

Anatomy of a CMOS Transistor

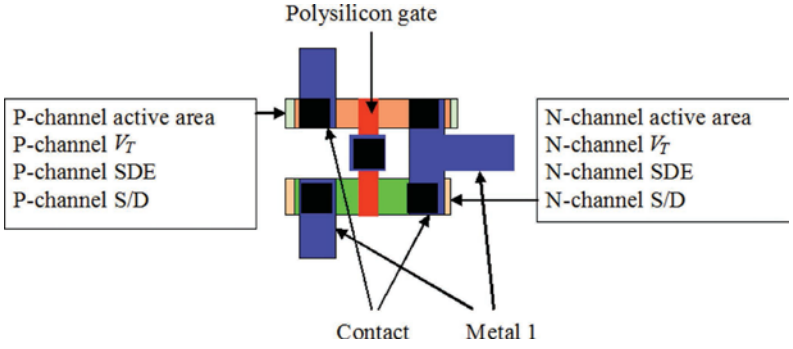


(a)



(b)

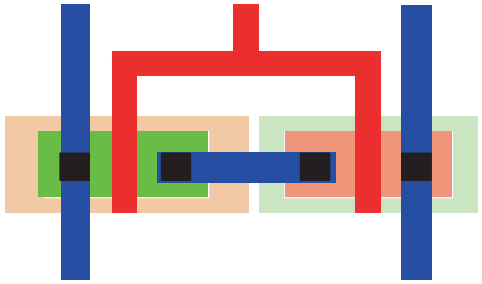
(c)



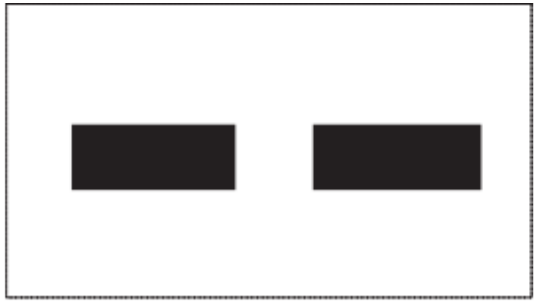
(Xiao 2012) Figure 1.14 (a) The circuit of a CMOS inverter, (b) an example of a textbook-style design layout of a CMOS inverter, and (c) the cross section of the textbook layout.

(Xiao 2012) Figure 1.15 CMOS inverter in a real-life IC layout.

Example: Layout and Binary Masks for a CMOS Inverter (Xiao 2012) Figure 1.17



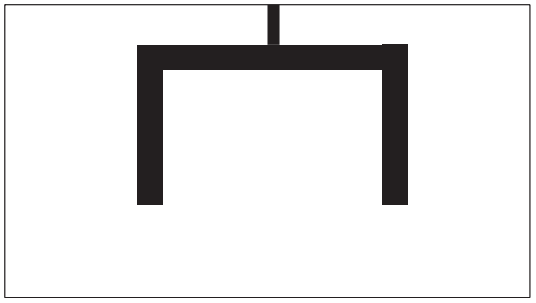
CMOS inverter layout



Mask 1, shallow trench isolation

Mask 2, N-well and P-Vt

Mask 3, P-well and N-Vt

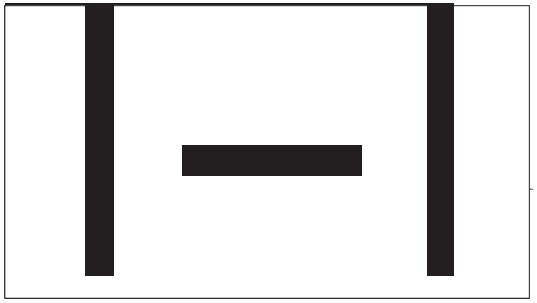


Mask 4, gate/local interconnection

Mask 5 and 7, N-SDE and N-S/D

Mask 6 and 8, P-SDE and P-S/D

Mask 9 contact



Mask 10, metal 1