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Connecting Devices to Systems
32-Bit Micro-processor at 5-nm Technology Node

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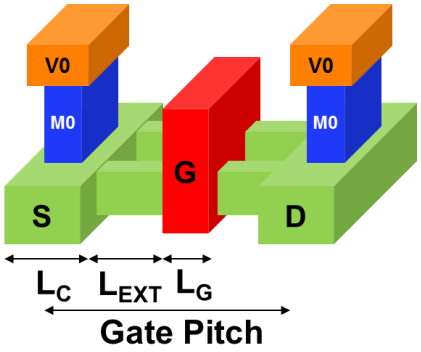
Outline

- Motivation and goal
- Examples for demonstration
- Goal for Year 5

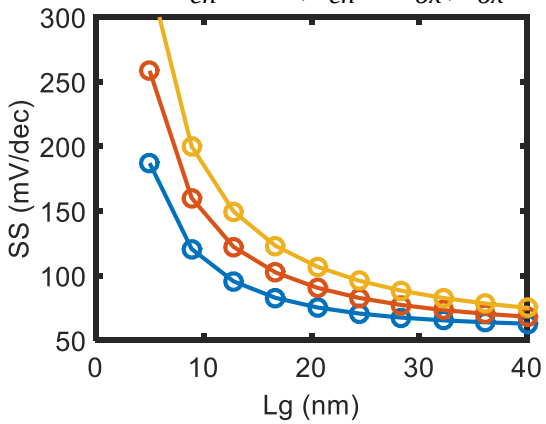
Dimensional Scaling Makes Parasitics Worse



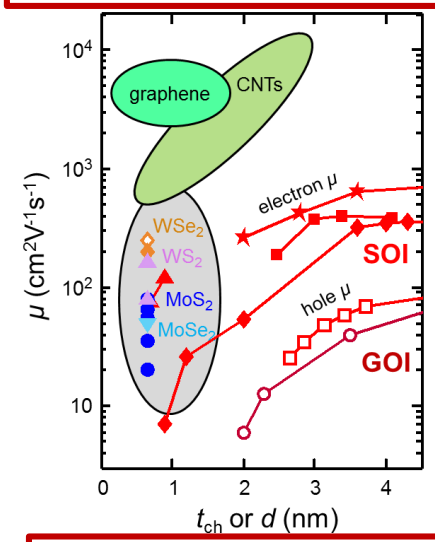
Constrained Multivariable Optimization!

Short-Channel Effect

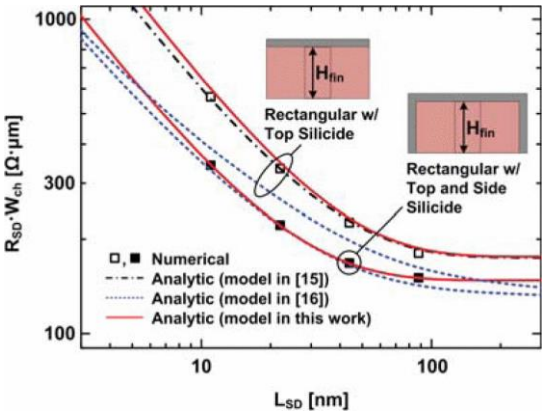
$$\lambda = t_{ch} + 2(\varepsilon_{ch} / \varepsilon_{ox})t_{ox}$$



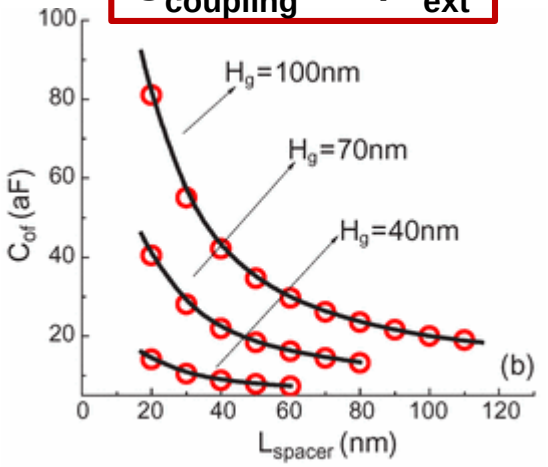
Scatterting ↑ as t_{ch} ↓



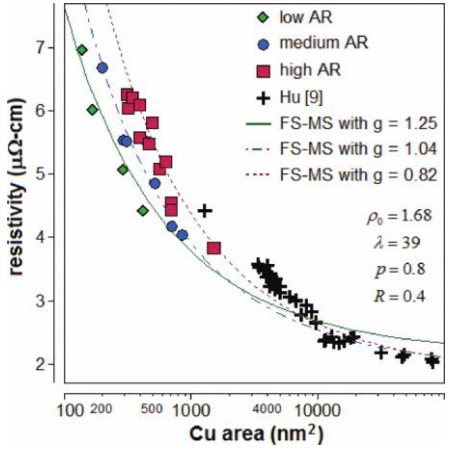
R_{con} ~ $1/L_c$



$C_{coupling}$ ~ $1/L_{ext}$



R_{wire} ↑ as W_{wire} ↓

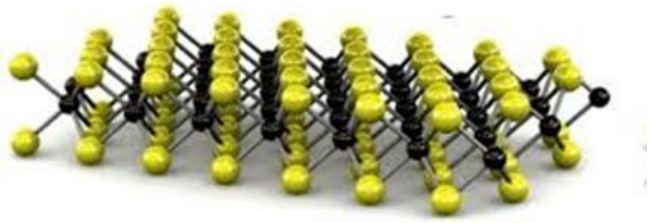


[Sources: E. Pop (Stanford); A. Pyzyna, VLSI-T '15; C.-W. Sohn, TED '13; J. Zou, TED '11]

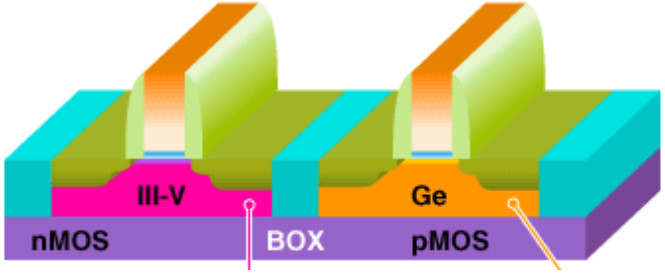
Opportunity and Challenge

- New materials/technologies to continue scaling
- **Which one is the best when integrated into a SYSTEM?**

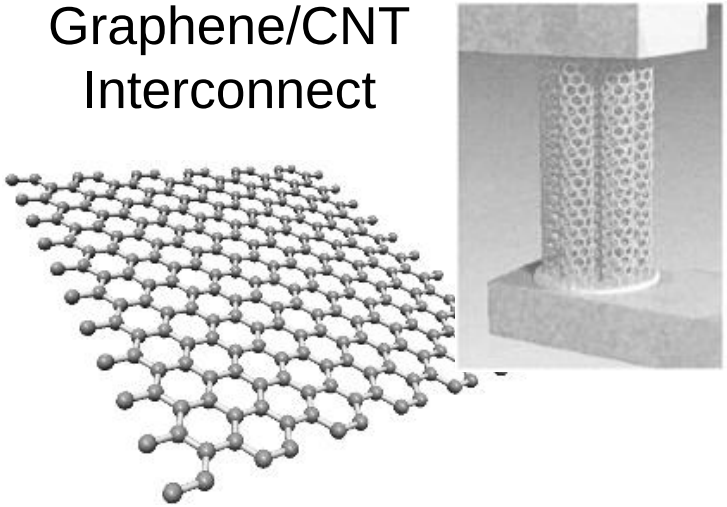
2D-Material FETs
(MoS2, WS2, MoSe2, BP, …)



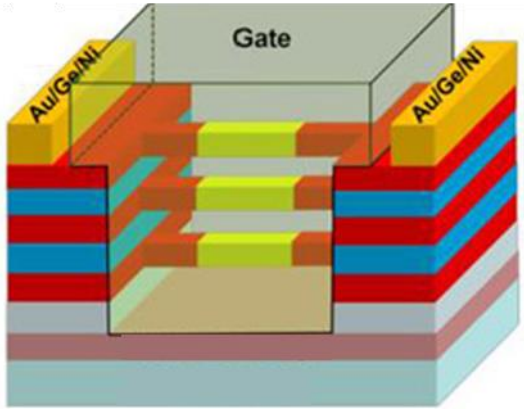
Ge/III-V Channel



Graphene/CNT
Interconnect

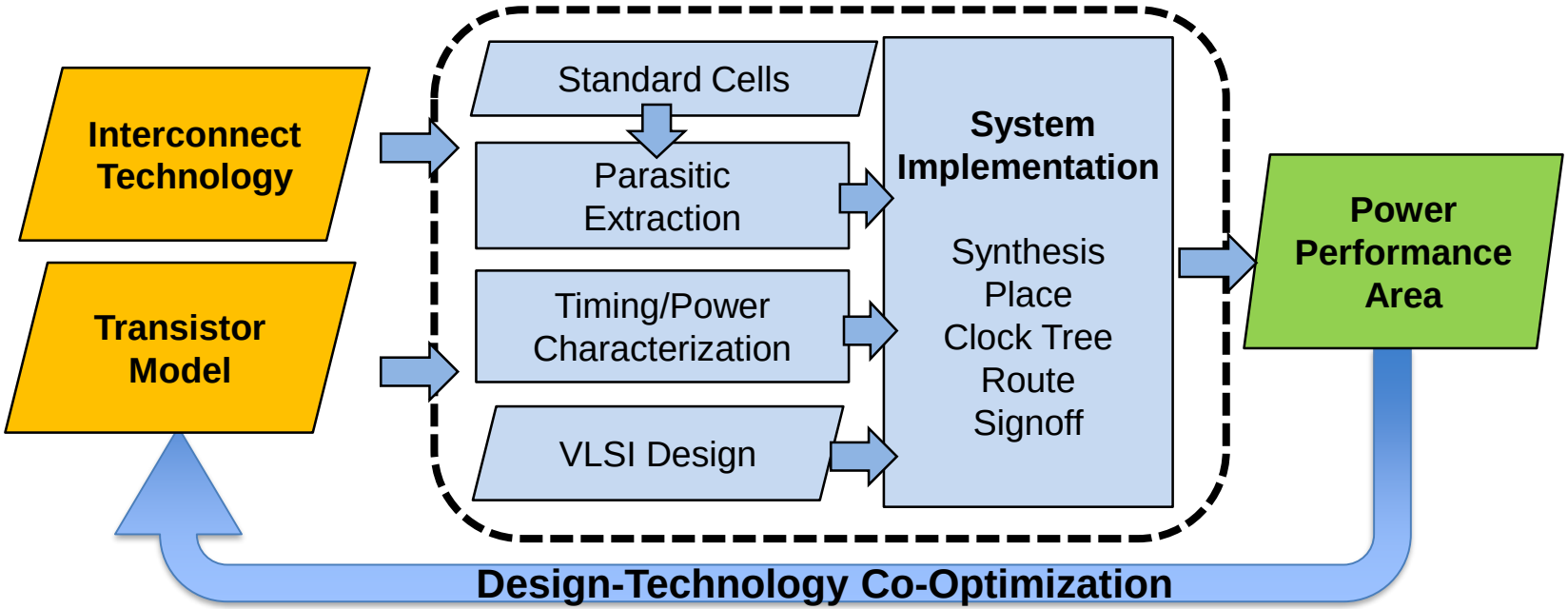


Nanowire FET



Full System Design for Technology Assessment

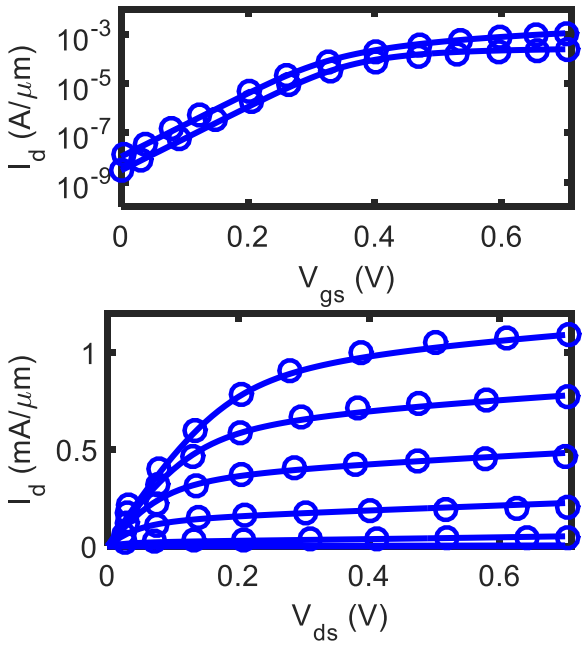
- Implement a full system for early assessment of emerging technologies in presence of parasitic and interconnect RC.



5-nm Si FinFET as Example

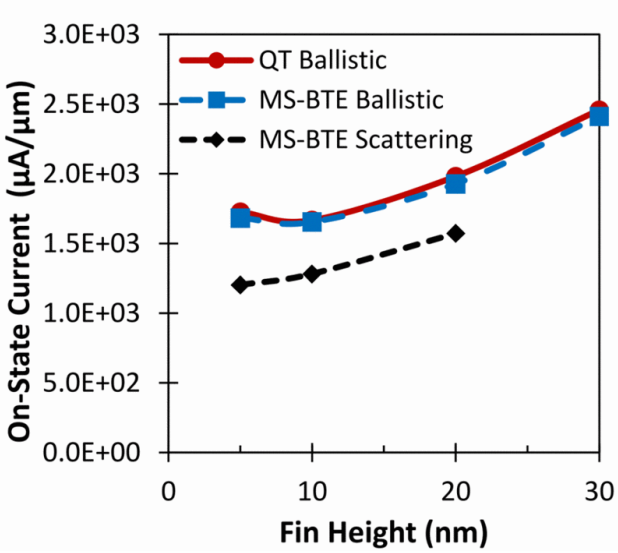
- Model based on experimental data + TCAD simulations

MVS Model Fitting
Intel 14-nm FinFET



5-nm FET Design	
Fin width	5 nm
Fin height	30 nm
Fin pitch	21 nm
Gate length	16 nm
EOT	0.7 nm
Vdd	0.6 V

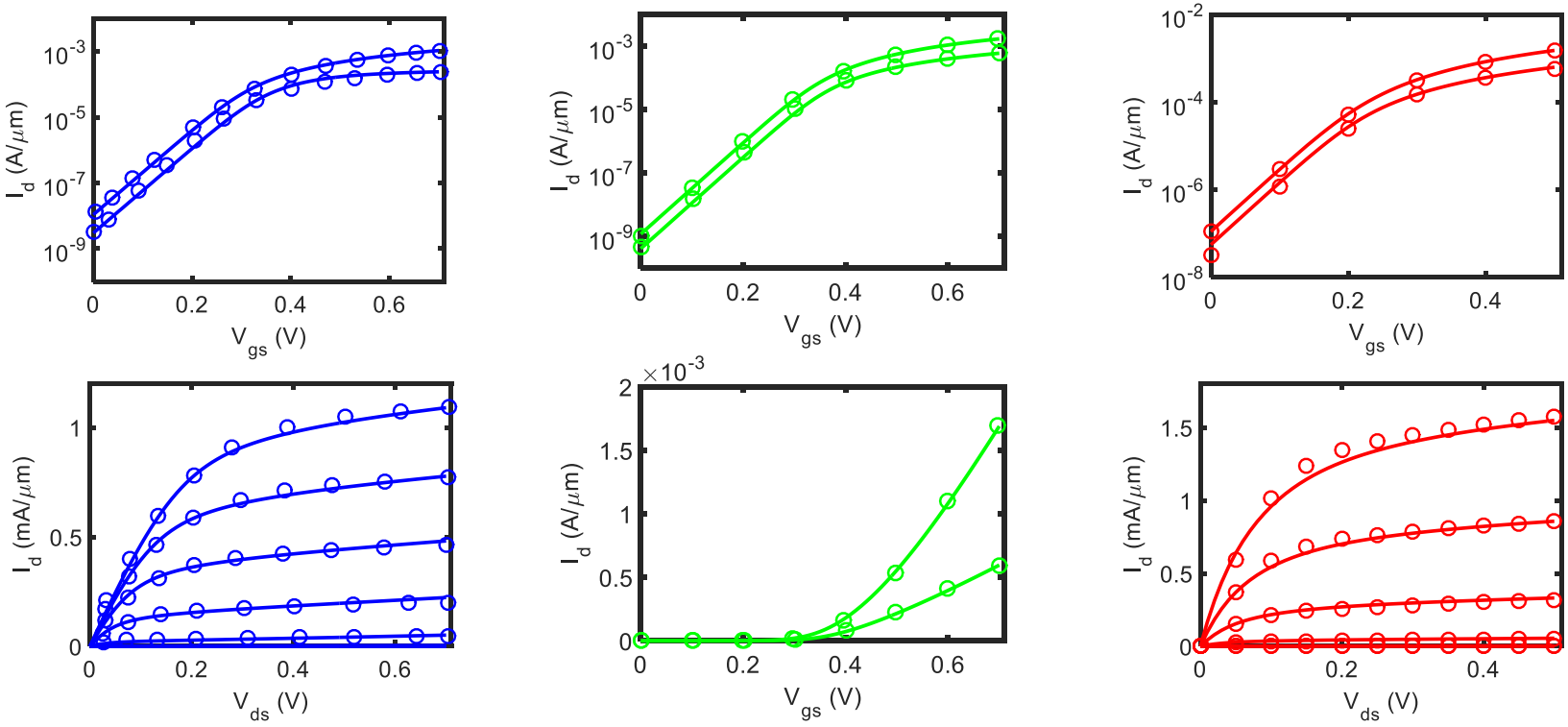
Synopsys 5-nm Projection



[S. Natarajan (Intel), IEDM '14; L. Smith (Synopsys), SISPAD '15]

Compact Models Are the Key

- Bridge between devices and systems
- Example: MVS model + experiment/simulation data



Si FinFET

[S. Natarajan (Intel), IEDM '14]

Si NWFET

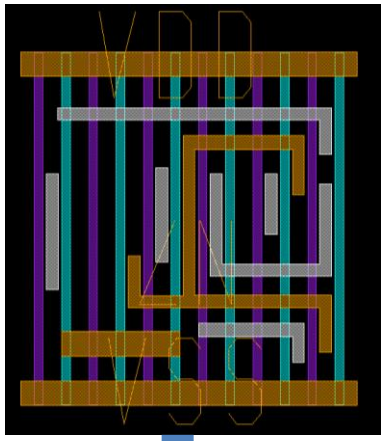
[M. Choi (Synopsys), SISPAD '15]

MoS_2-FET (Simulation)

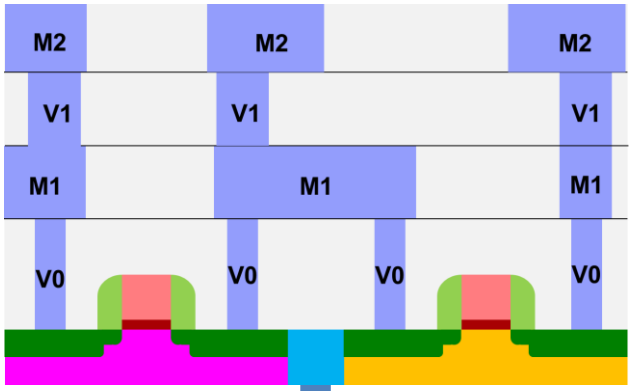
[L. Liu, J. Guo, TED '13]

Parasitic Extraction and Interconnect

Standard Cell Layouts

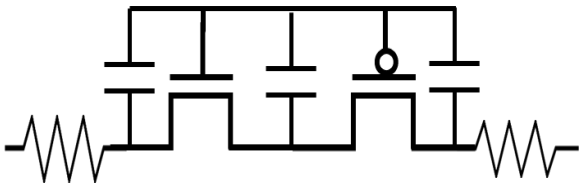


Interconnect Definition
(Thickness, dielectric, resistivity)

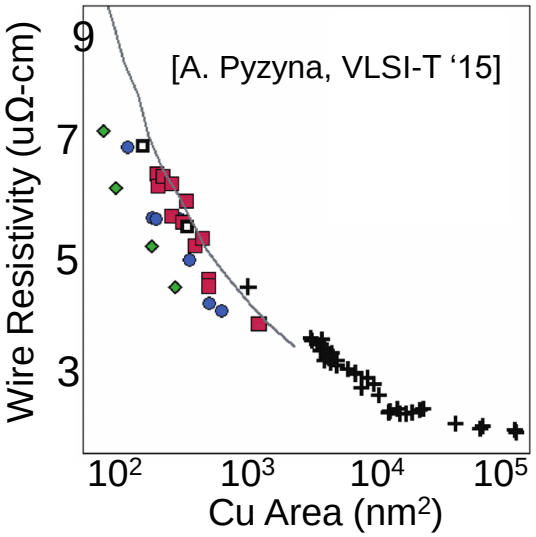


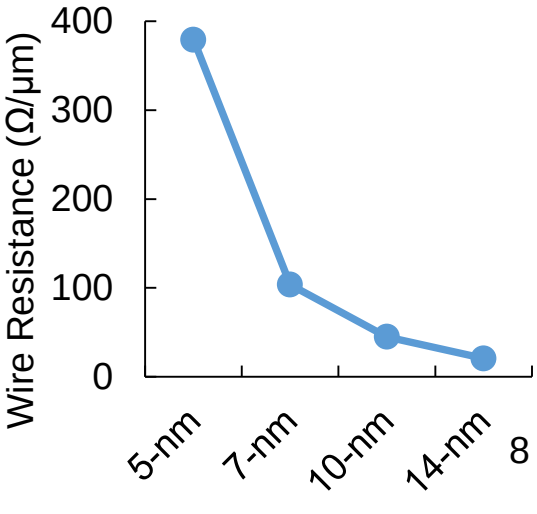
Synopsys
StarRC

Extracted Netlist



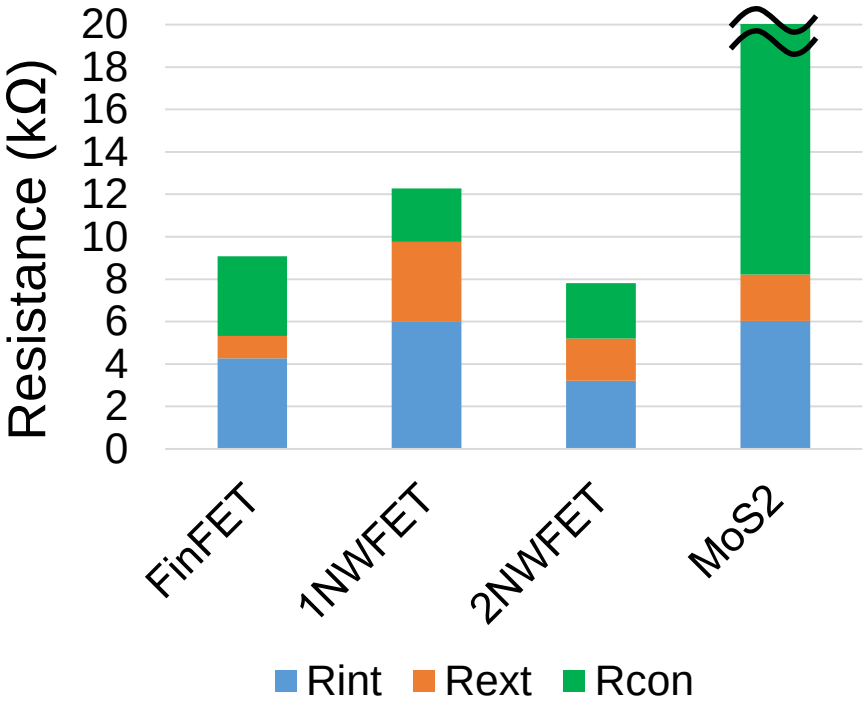
Area-Dependent Cu Resistivity

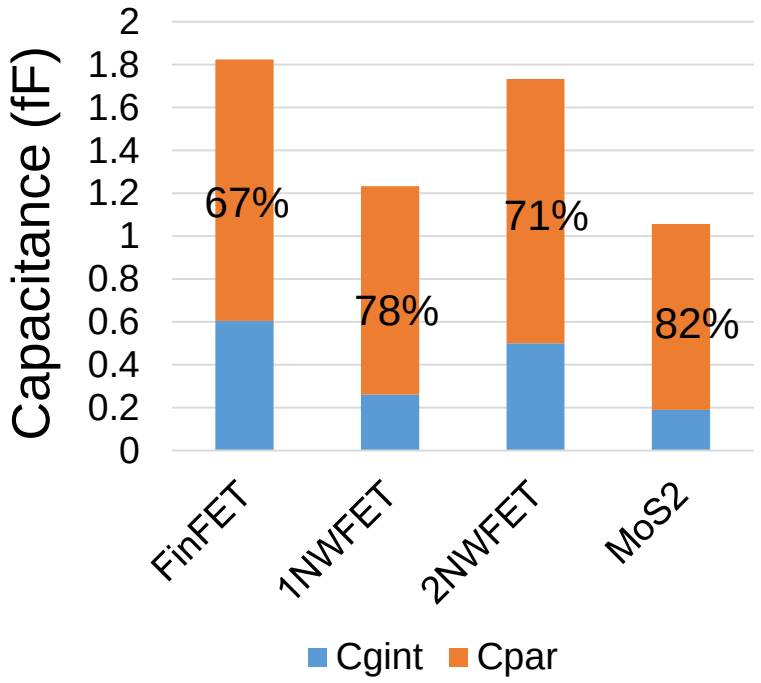




RC Breakdown of INV_X1 Cell

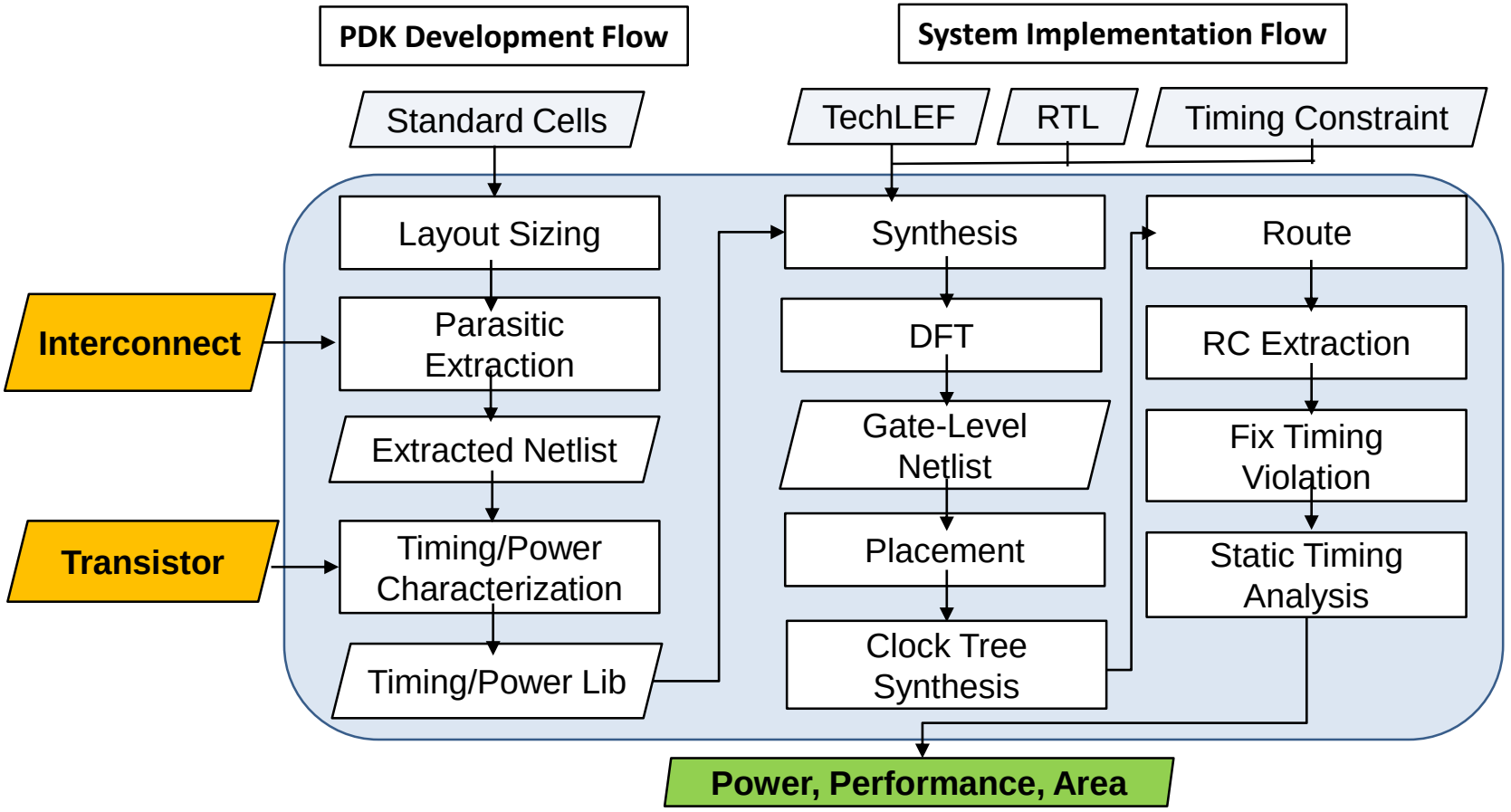
- Parasitic RC dominates over device intrinsic RC, especially the capacitance





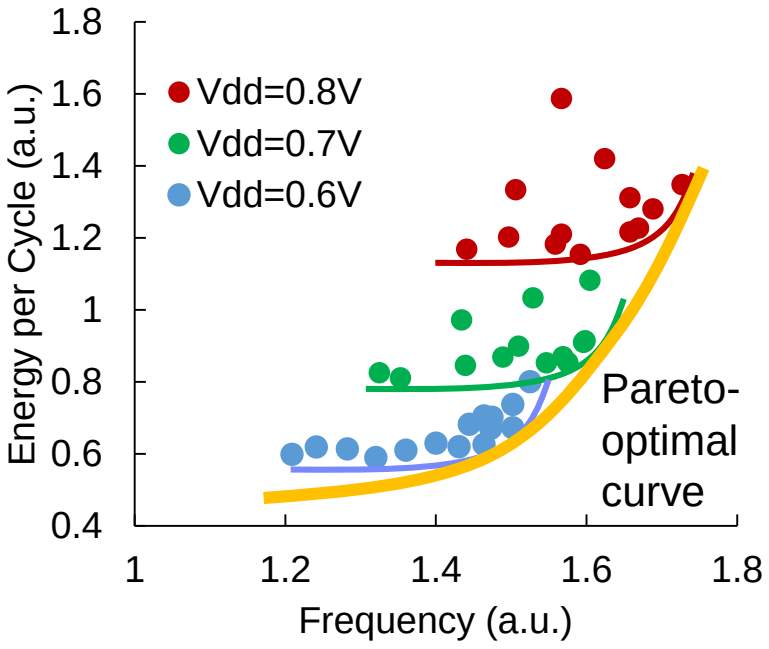
VLSI System Implementation Flow

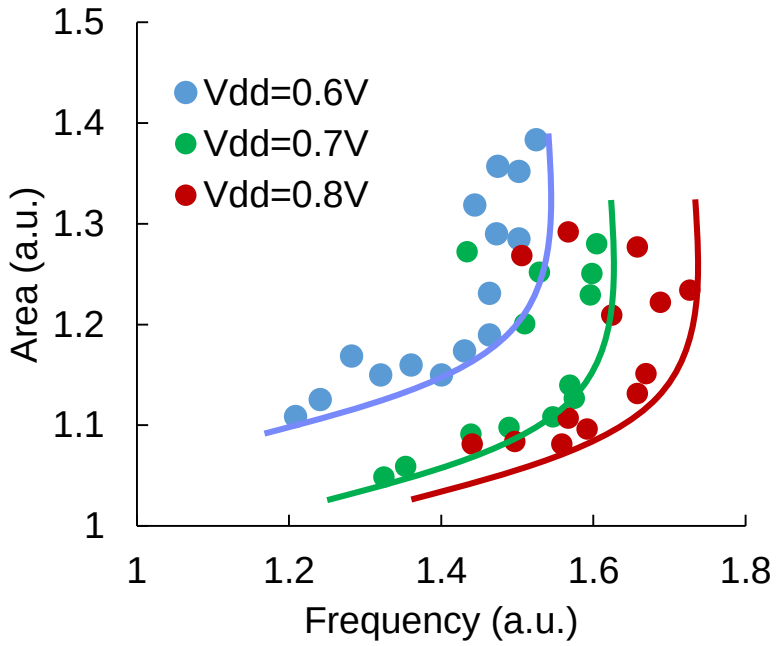
- Details in the poster session…



ARM Processor on 5-nm Tech as Example

- Place-and-route is a stochastic process
  - Gate placement and routing are optimized stochastically
- Depends on choice of Power, Performance, Area

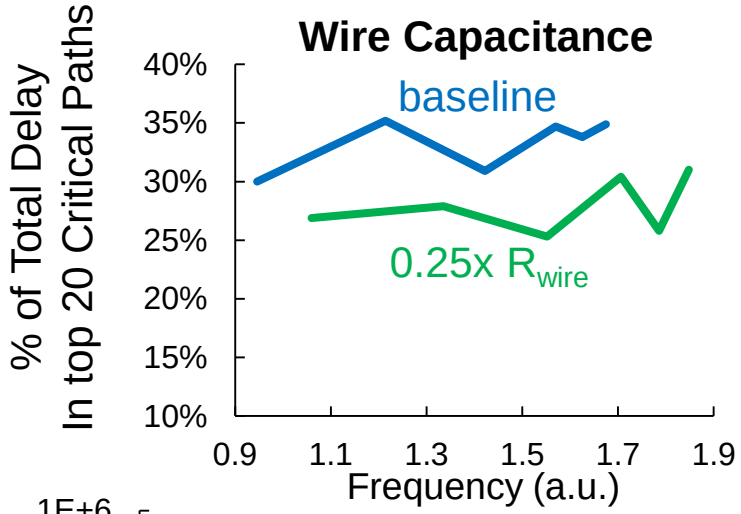


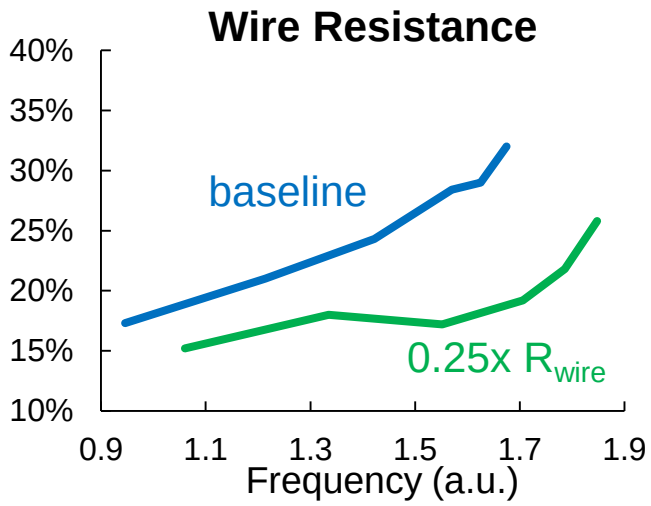


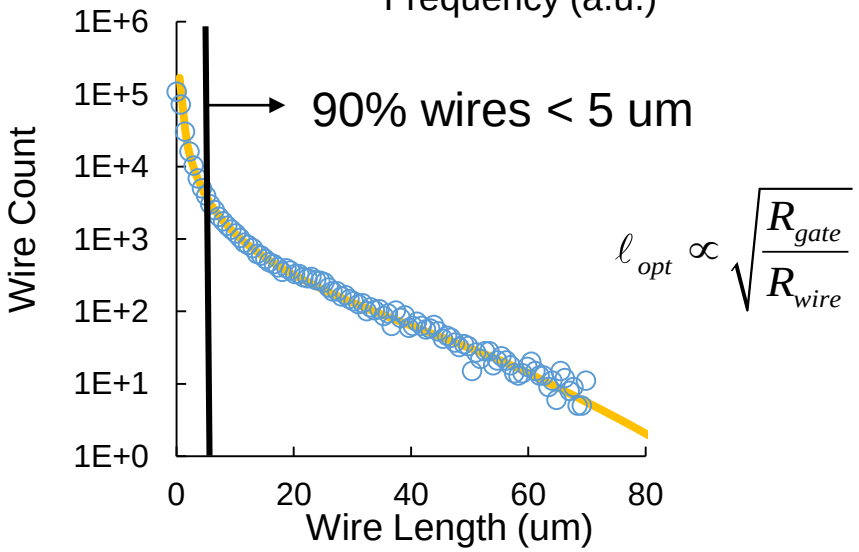
Each dot on the plot represents a target clock frequency.

Why Need A Full System?

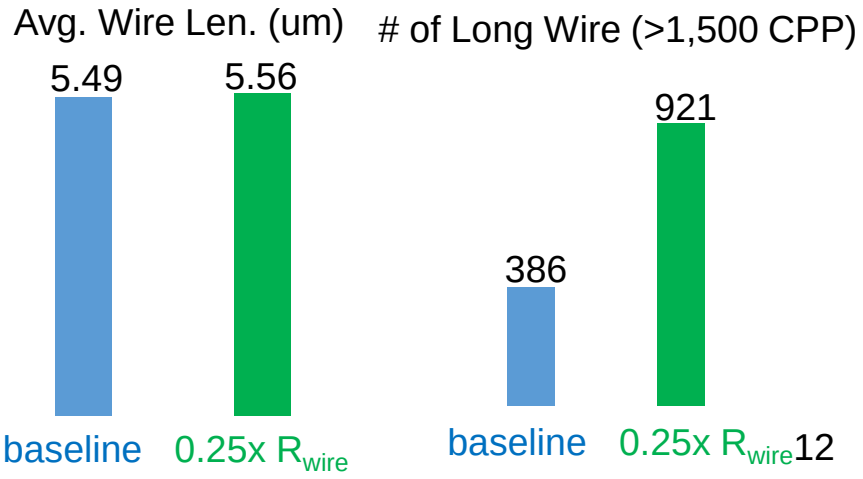
- Because it is hard to predict the wires





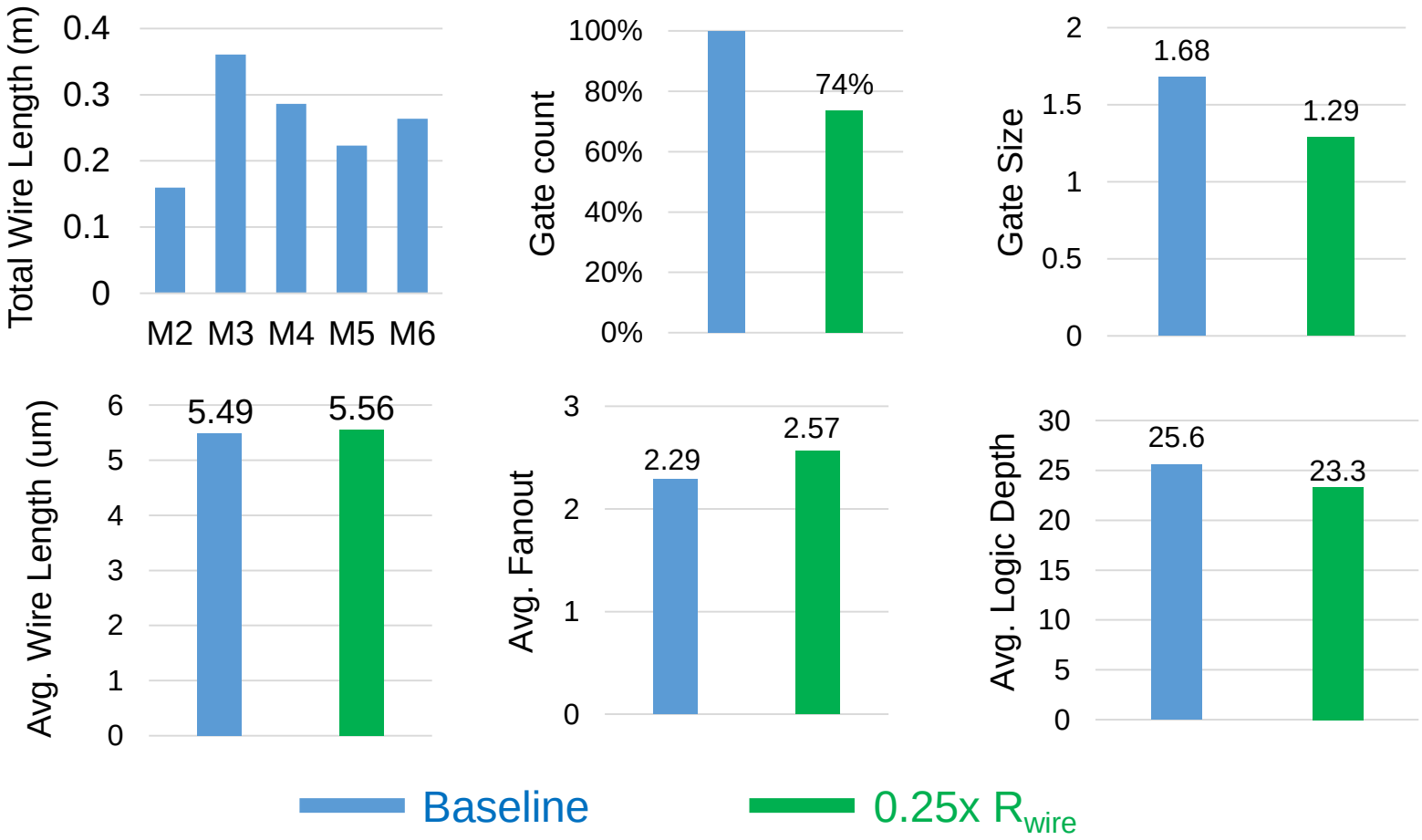


$$\ell_{opt} \propto \sqrt{\frac{R_{gate}}{R_{wire}}}$$



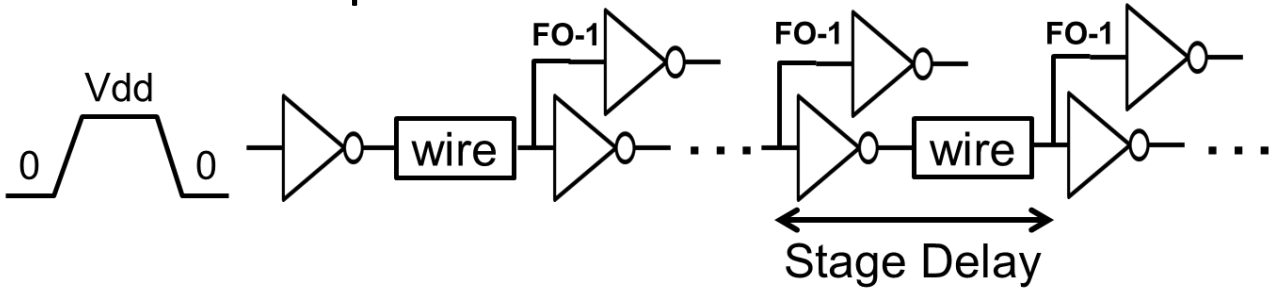
Complex Gate-Wire Balancing

- Many knobs to balance wires and gates:
  - wire length, fanout, logic depth, gate size, metal layers

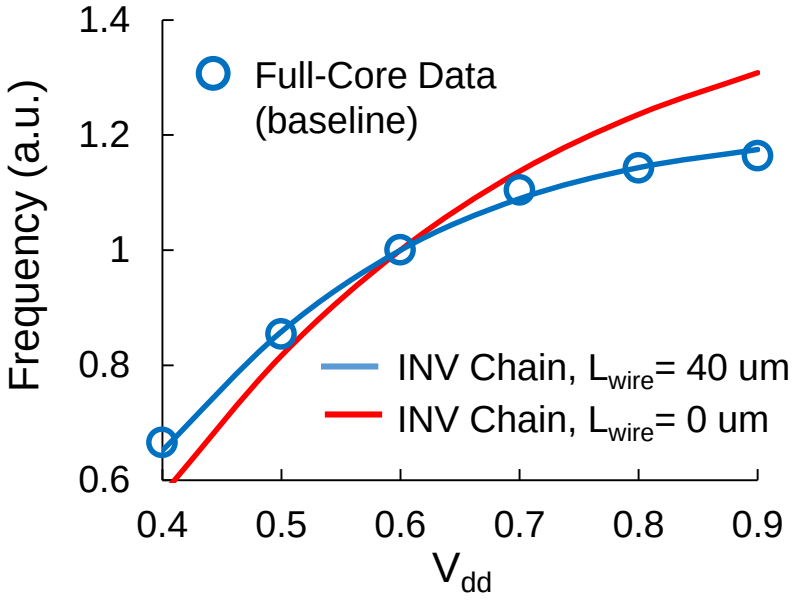


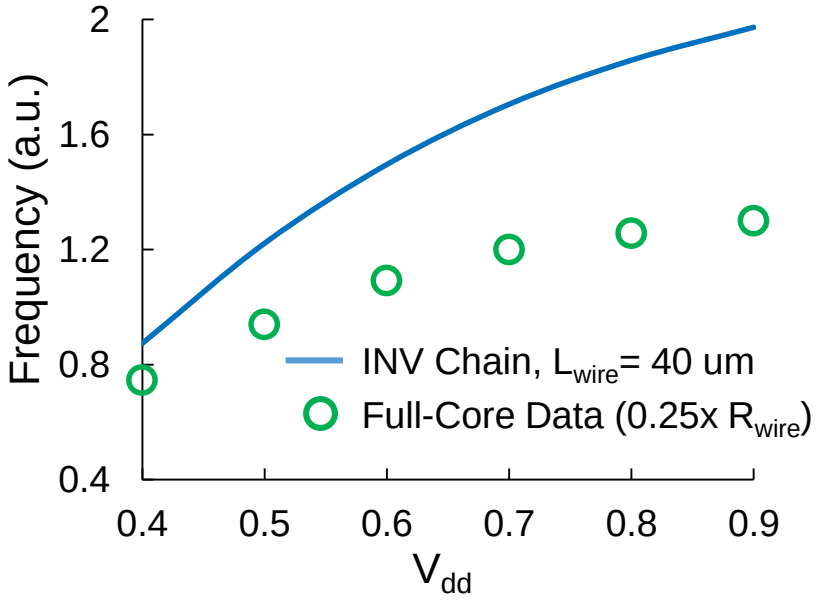
Correlation Between Inverter Chain and Full-Core Data

- Inverter chain as performance benchmark circuit



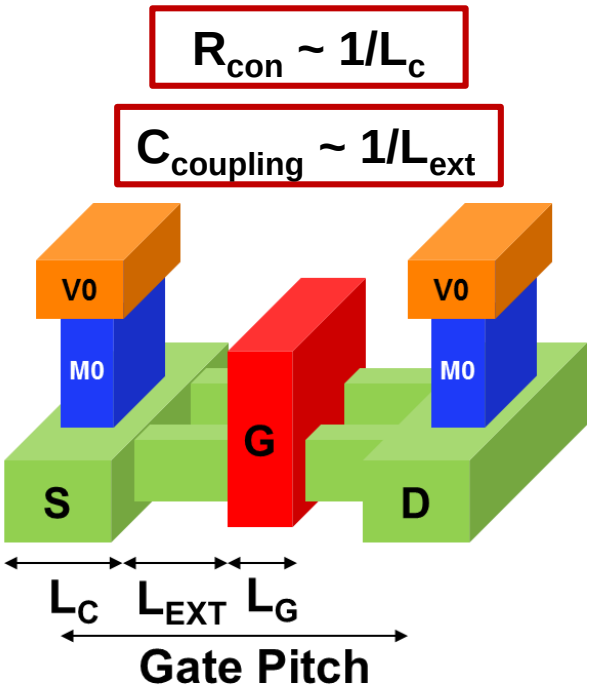
- Hard to estimate wires across technologies with simple circuits

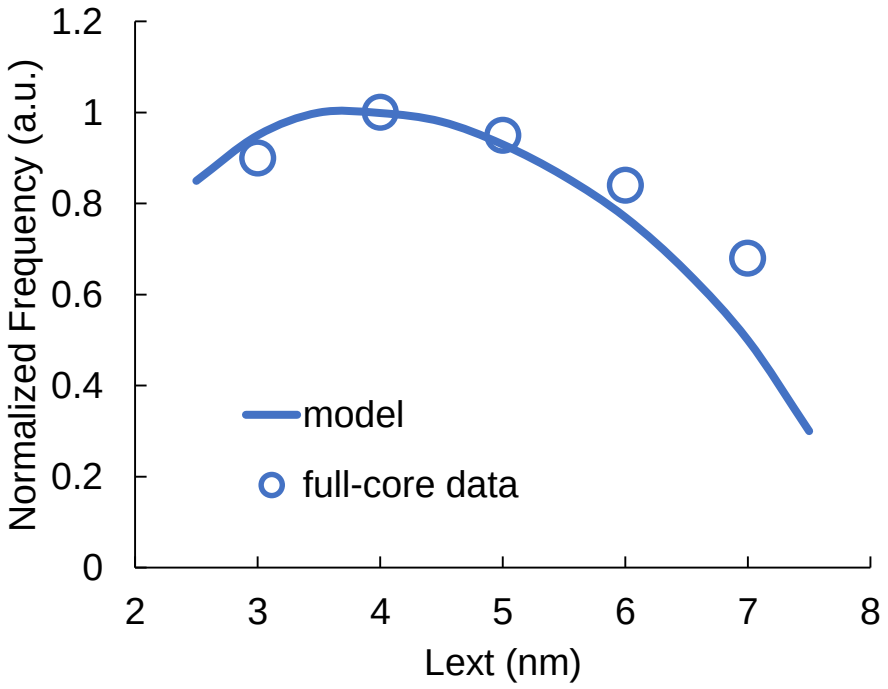




Technology Optimization Using Analytical Model

- Full-core implementation is time-consuming
  - Hours ~ days to build PDK and perform synthesis, place and route
- With the analytical model calibrated to full-core data, optimization can be done more efficiently
- Example: Optimize the extension length (Lext) of FET

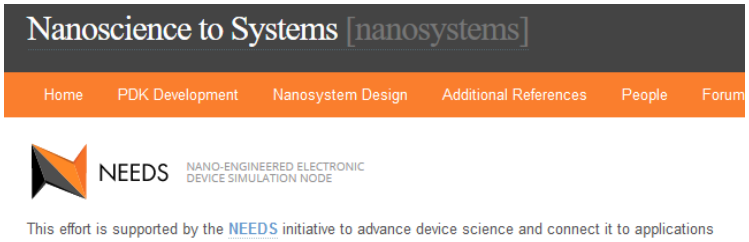




Deliverable in Year 5

- Package including scripts **for nanotech researchers** to design digital systems for emerging FETs and interconnect
  - Standard tools exist
  - Complete physical design too complex to learn quickly

- https://nanohub.org/groups/nanosystems by G. Hills (Stanford)



- 2.0 will focus on **parasitic** extraction and **interconnect**.