New thermoelectric materials and structures are being developed toward higher ZT.

In this work, we use electrical interface resistance 0.006 Km.

All parameters are taken from experiment and have temperature dependence.

Device level performance, however, can be significantly lower than that predicted from intrinsic material.

With both electrical and thermal interface resistances

Therefore, the 3D flow of current due to current crowding is insignificant.

Physics-based, SPICE-compatible compact circuit model for TE device.

Device characterization and circuit simulation applications.

Parasitic Rth Thermal interface resistance

TIM Thermal insulating material

No interface resistance

Interface resistance

DC performance

Status and Plans

Summary:

• Capability for full, numerical simulation of realistic 3D TE devices is ready.
• Physics-based SPICE model produces essentially identical results.
• Sentaurus informed by first principles + SPICE informed by Sentaurus provide the tools needed.

Plan:

• Benchmark with experimental device performance
• Coupling to characterization techniques