Physics-based compact model of thermoelectric devices

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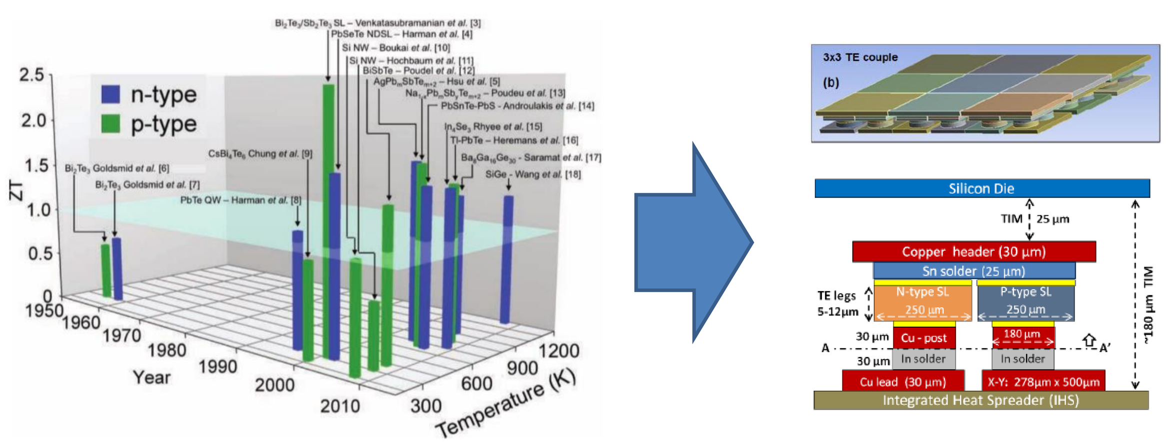
NEEDS

Objectives



- New thermoelectric materials and structures are being developed toward higher ZT.
- Device level performance, however, can be significantly lower than that predicted from intrinsic material.
- A TE design simulation must capture correctly all the physics in a full 3D device

Vineis, C. J., Shakouri, A., Majumdar, A. and Kanatzidis, M. G. (2010), Nanostructured Thermoelectrics: Big Efficiency Gains from Small Features. Adv. Mater., 22: 3970–3980. doi:10.1002/adma.201000839

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Background / Motivation

1) PDE-based simulation

$$\nabla\cdot(\epsilon\nabla f) = -e\left(p - n + N_D^+ - N_A^-\right)$$

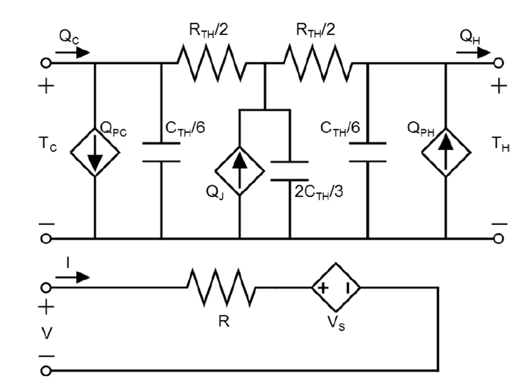
$$\frac{\partial p}{\partial t} = -\nabla\cdot\left(\vec{J}_p/e\right) \qquad \frac{\partial n}{\partial t} = \nabla\cdot\left(\vec{J}_n/e\right)$$

$$\frac{\partial\left(c_{tot}T\right)}{\partial t} = \nabla\left(k_{tot}\nabla T\right) + H$$

Sentaurus™: 1D/2D/3D PDE-based simulator for electrothermal transport.

Contact design, device design, and SPICE model benchmarking.

2) Spice modeling



Physics-based, SPICE-compatible compact circuit model for TE device.

Device characterization and circuit simulation applications.

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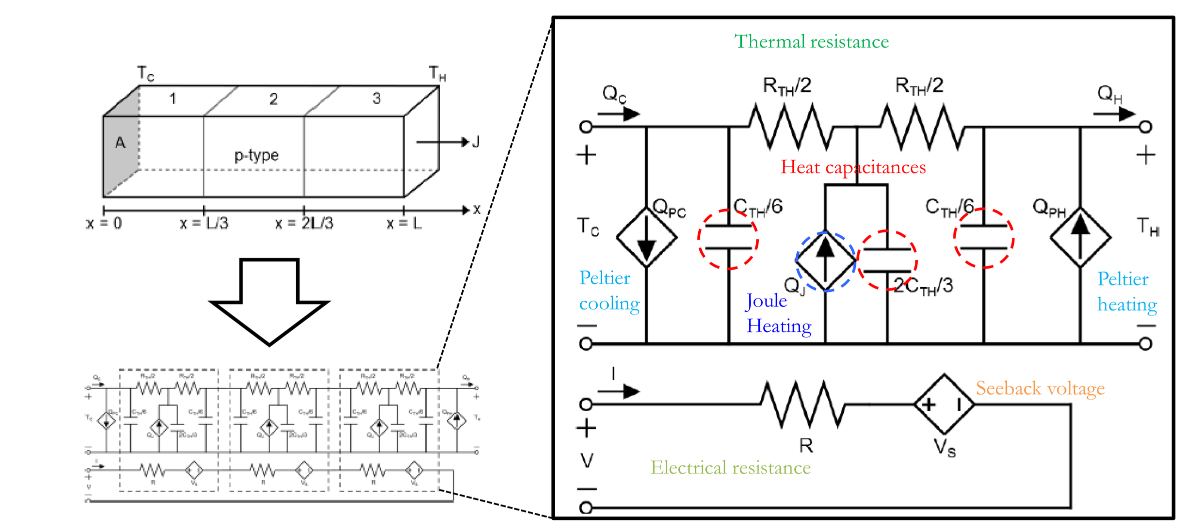
TE compact model



Thermoelectric device compact model (Available at https://nanohub.org/publications/80)

Conrad, K. (2015). A physics-based compact model for thermoelectric devices. Purdue University. M.S. Thesis

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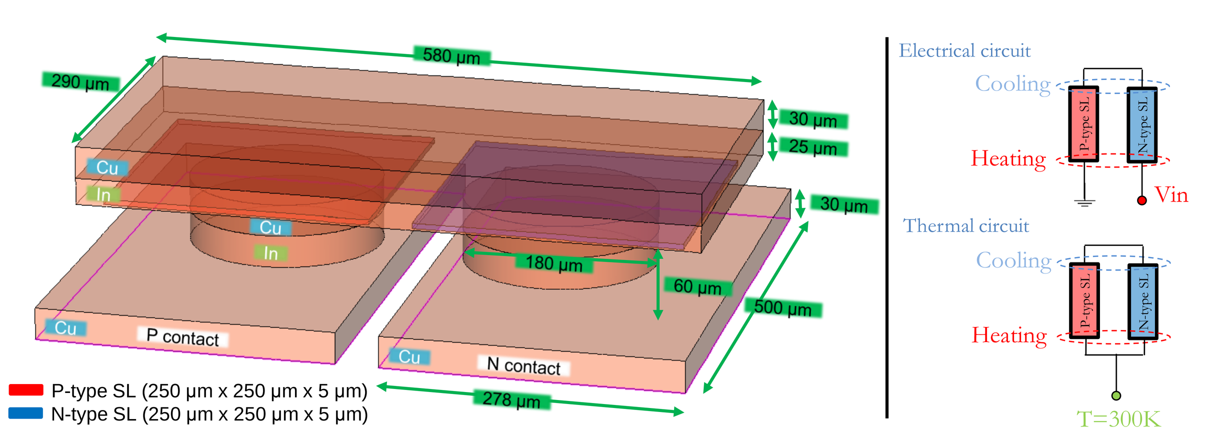
3D PDE device simulation



- In this work, we use Sentaurus™ to solve the 3D TE device and benchmark with SPICE model.
- All parameters are taken from experiment and have temperature dependence.

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3D effects on current flow

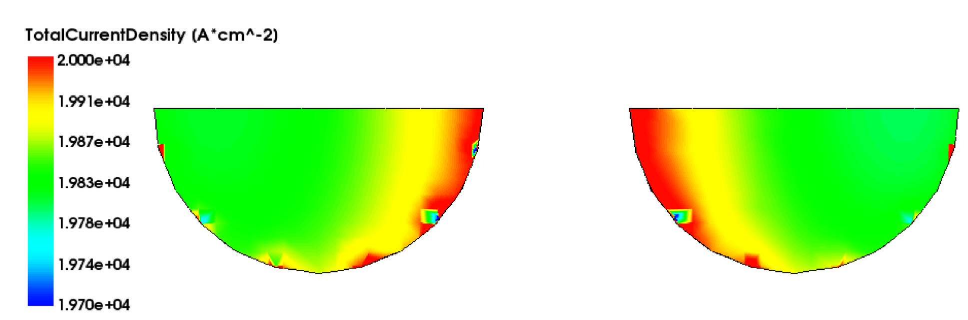
The transfer length of the metal/SL interface is

$$L_T = \sqrt{\rho_C / R_s} = \sqrt{7\times10^{-11}\Omega m^2 / 1.56\times10^{-8}\Omega m} = 6.7\times10^4\ \mu m$$

With diameter of 180 um, maximum variation factor across the surface is

$$\exp(-180\mu m / 6.7\times10^4\ \mu m) = 0.997$$

Therefore, the 3D flow of current due to current crowding is insignificant.



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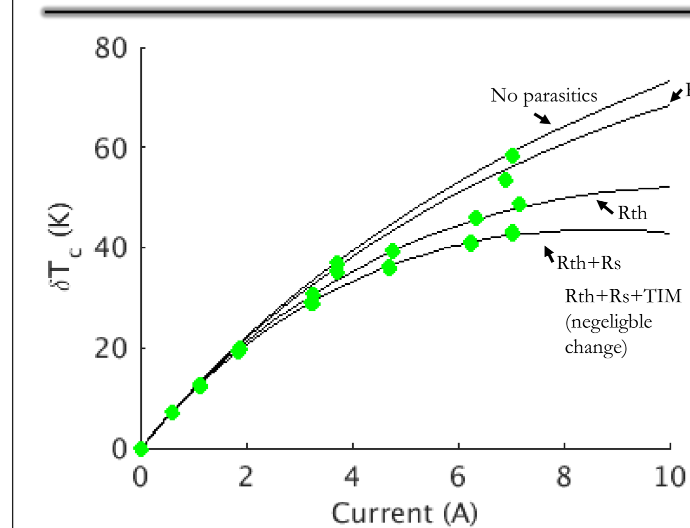
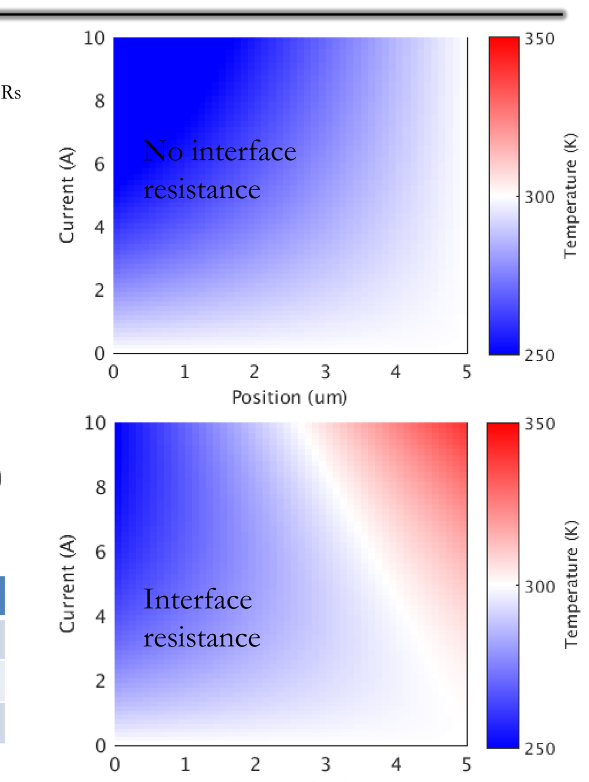
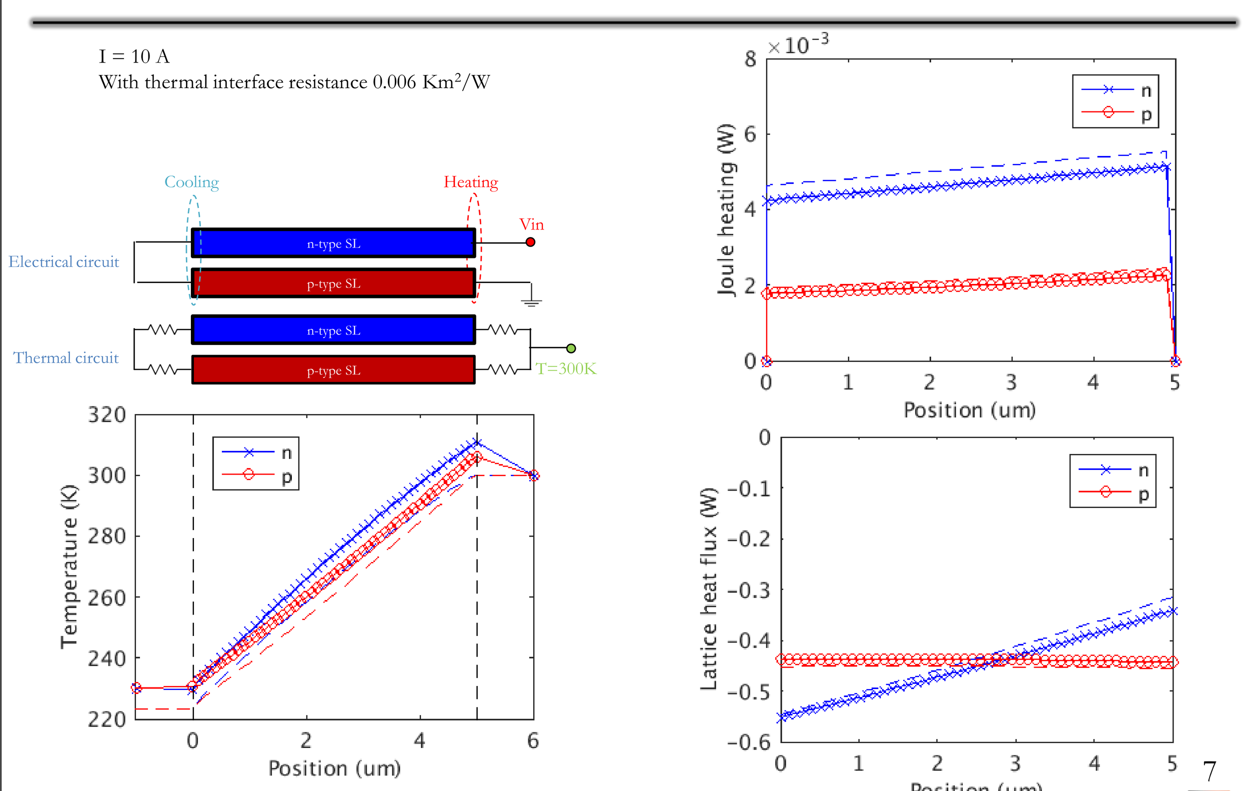
DC performance



Parasitic		
Rth	Thermal interface resistance	0.006 Km^2/W
Rs	Electrical interface resistance	$5x10^{-7}$ Ohm-cm^2
TIM	Thermal insulating material	0.023 W/K-m



With thermal interface R



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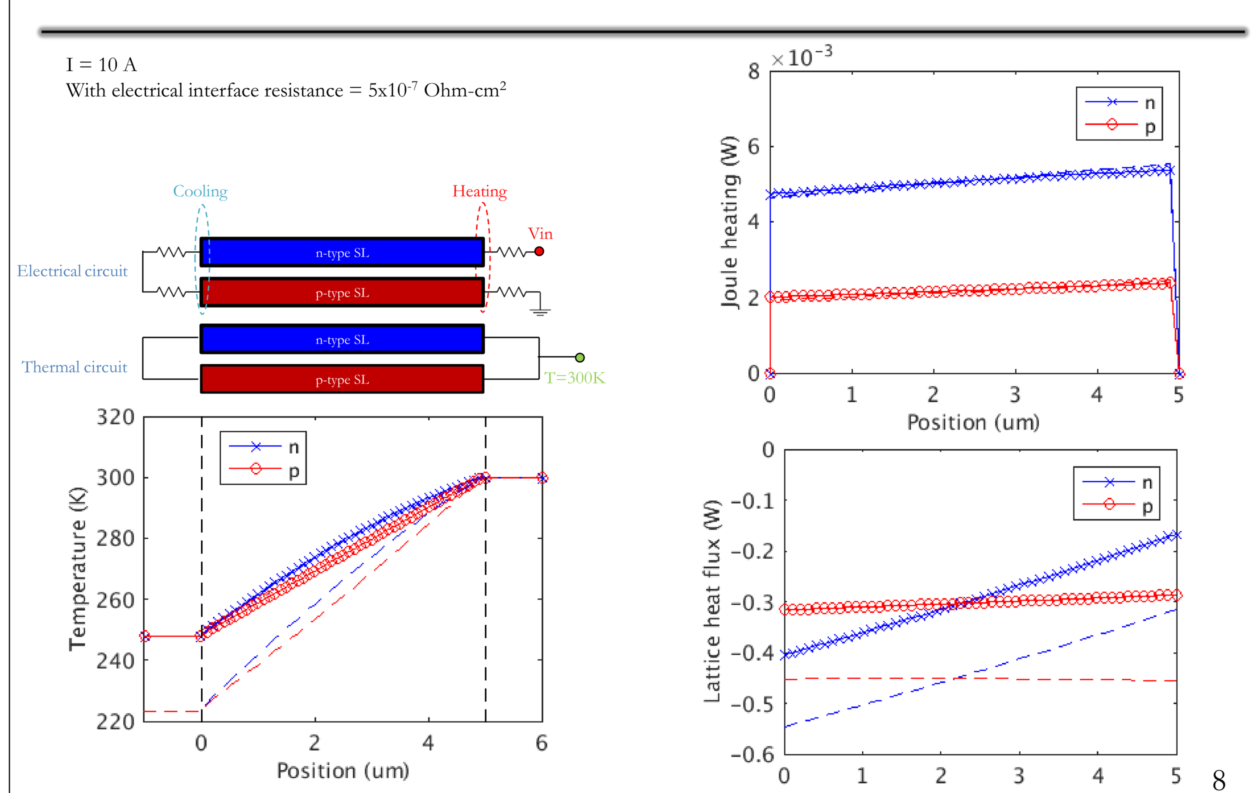
With electrical interface R



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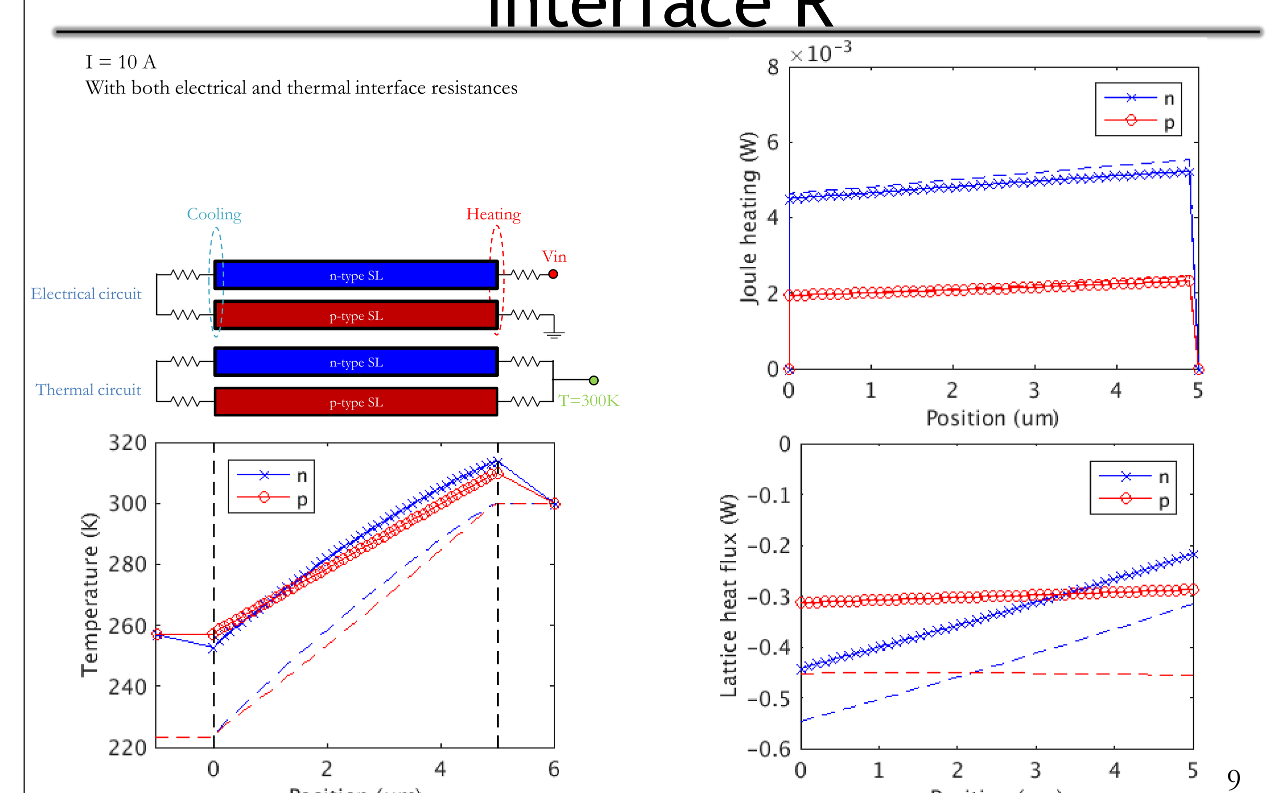
With both thermal and electrical interface R



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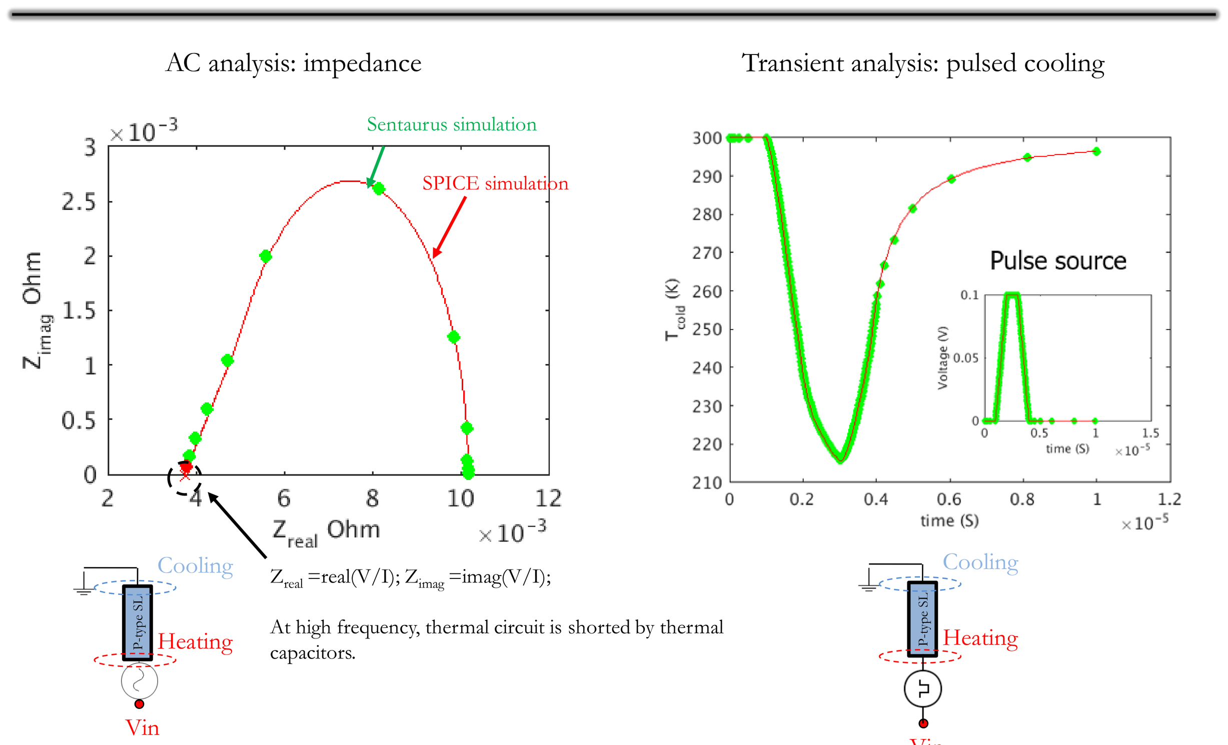
AC and transient analysis



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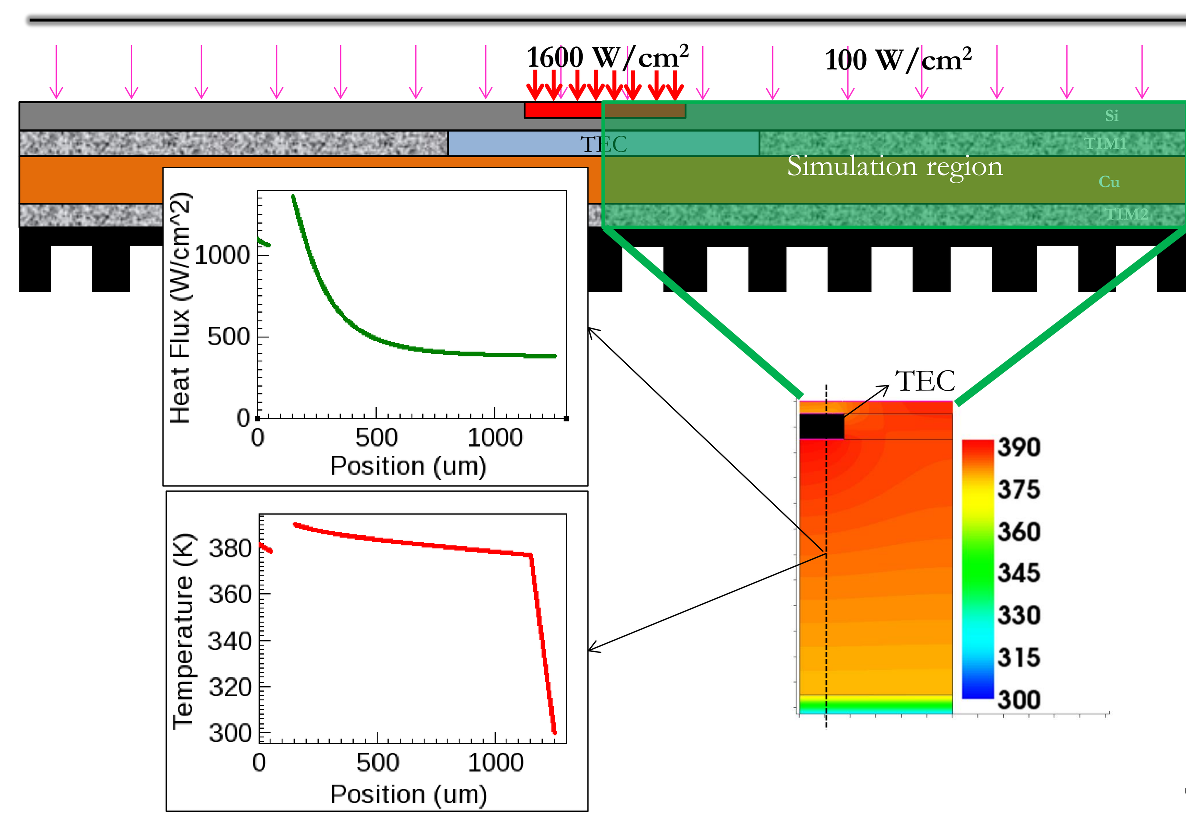
Coupling to application environment



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Status and Plans

Summary:

- Capability for full, numerical simulation of realistic 3D TE devices is ready.
- Physics-based SPICE model produces essentially identical results.
- Sentaurus informed by first principles + SPICE informed by Sentaurus provide the tools needed.

Plan:

- Benchmark with experimental device performance
- Coupling to characterization techniques

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