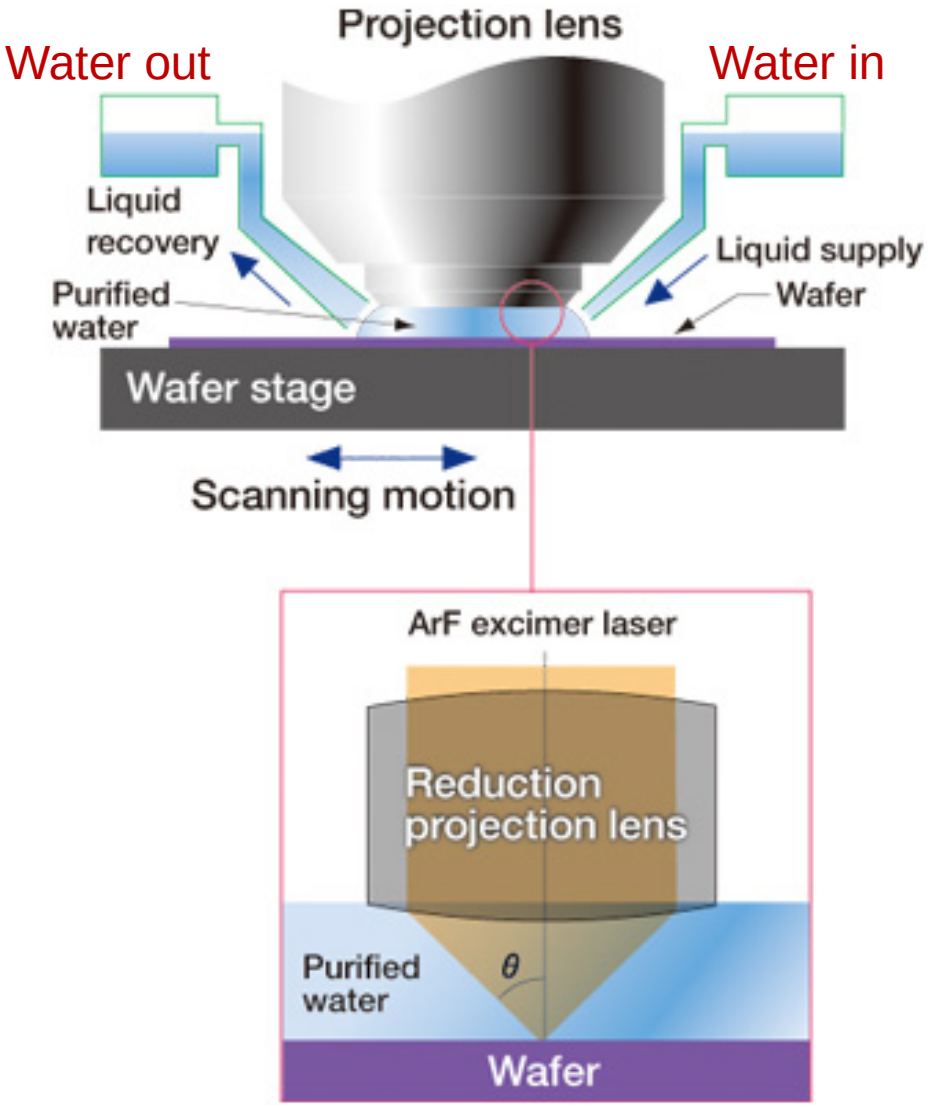
Nanometer Scale Patterning and Processing

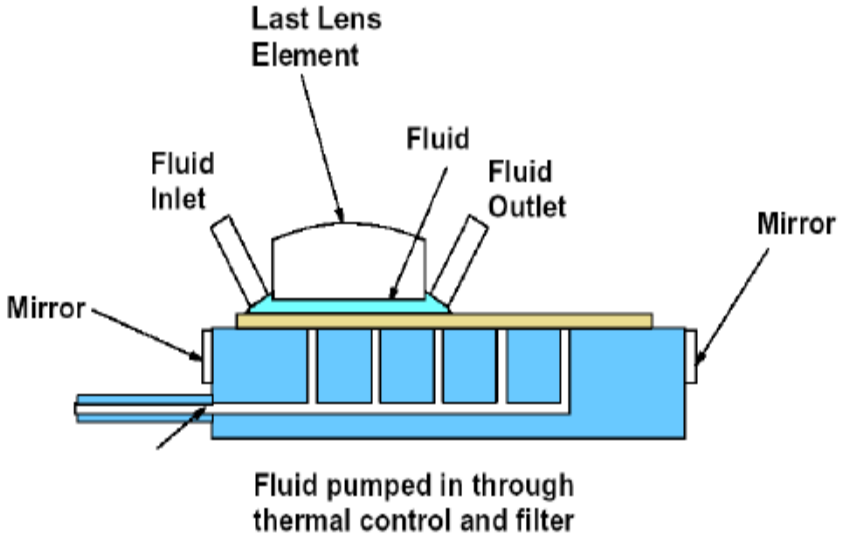
Spring 2016

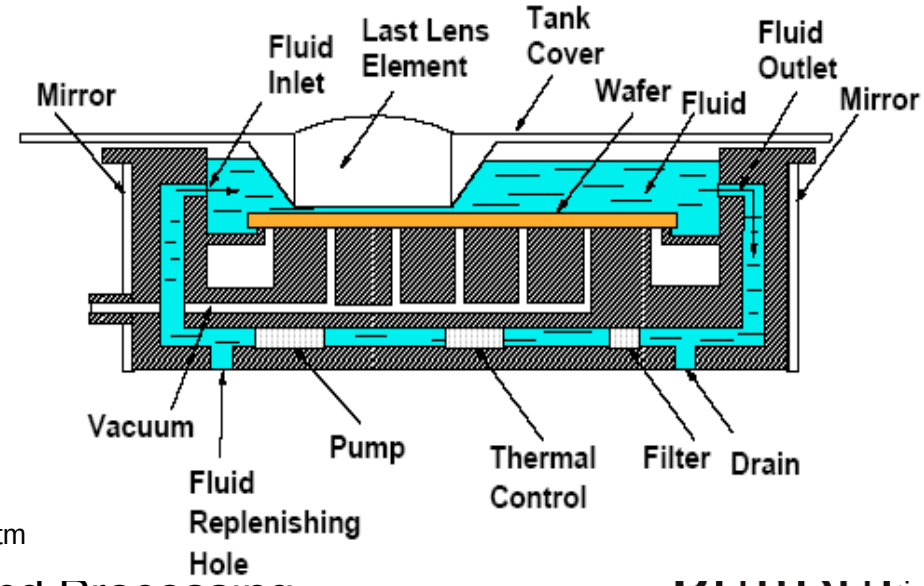
Lecture 11

Optical Lithography - Resolution Enhancement Techniques (RETs) in Optical Project Lithography (continued)

Immersion lithography system: >$50M

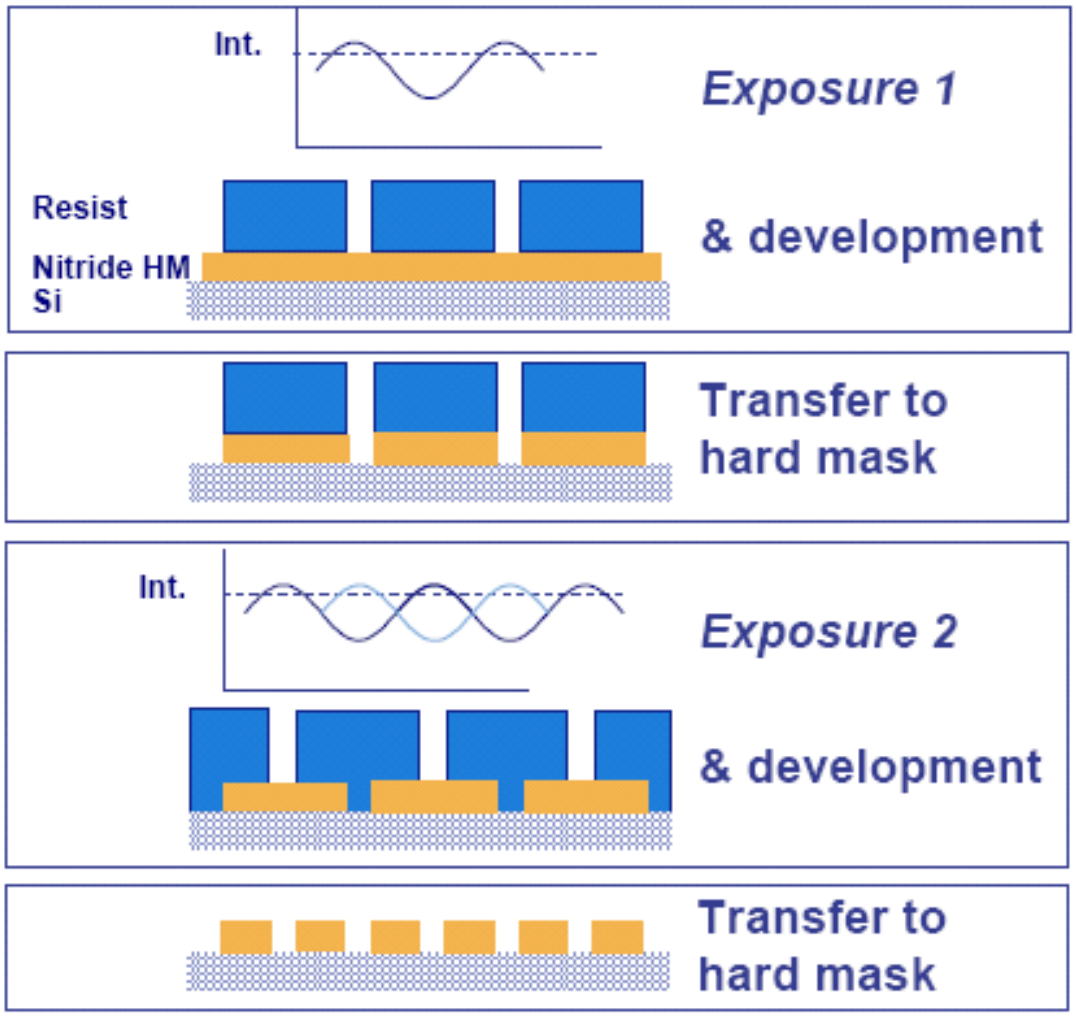


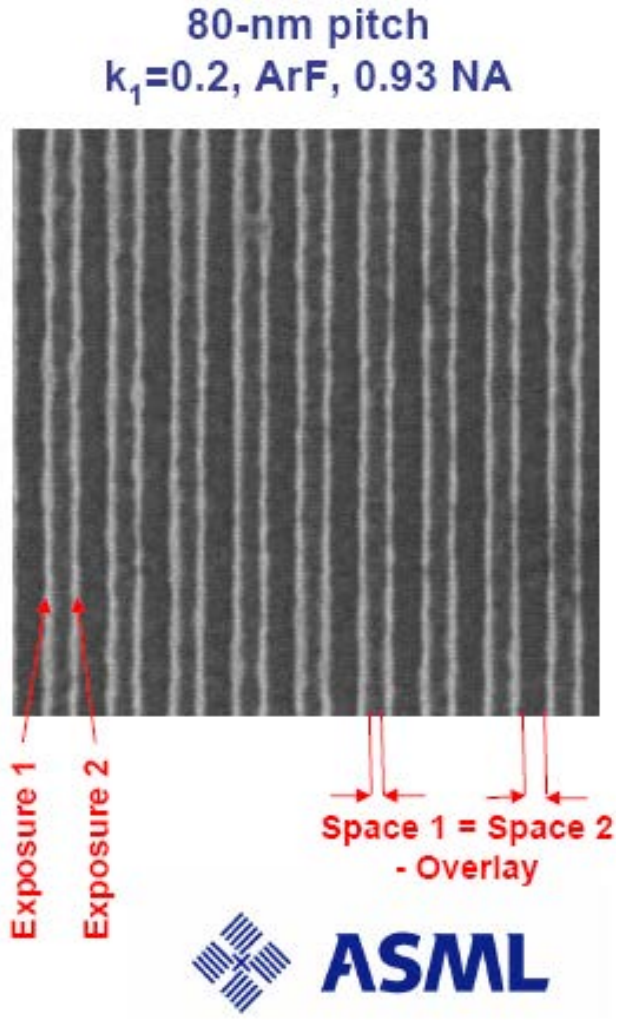




http://www.nikon.com/about/technology/rd/core/optics/immersion_e/index.htm

RET 5: Double Patterning Technology (DPT)





Single exposure, Double exposures, Double patterning

Single exposure

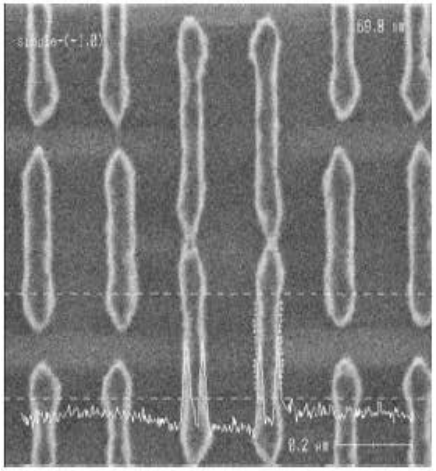
Double exposures in resist

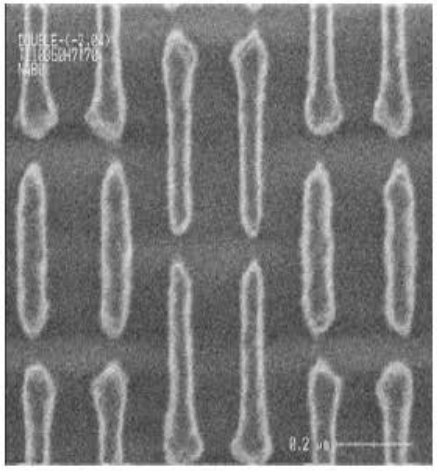
Double exposures through etch.

Resist

After resist development

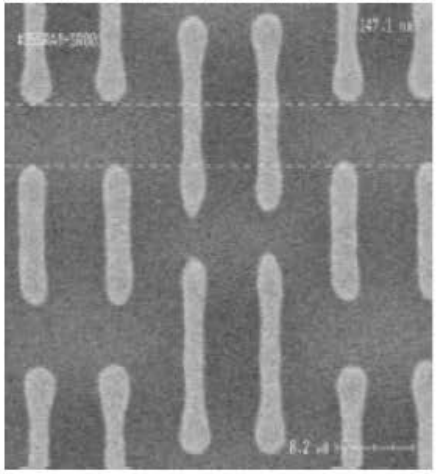
After etch into sub-layer

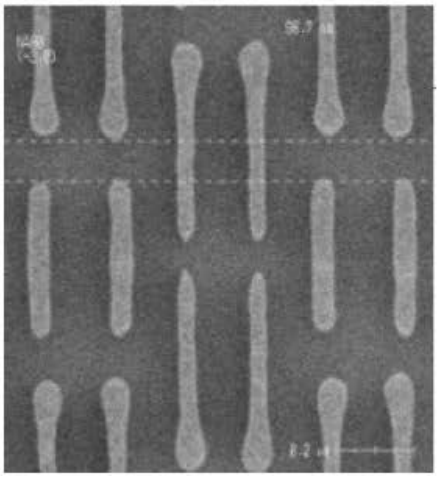


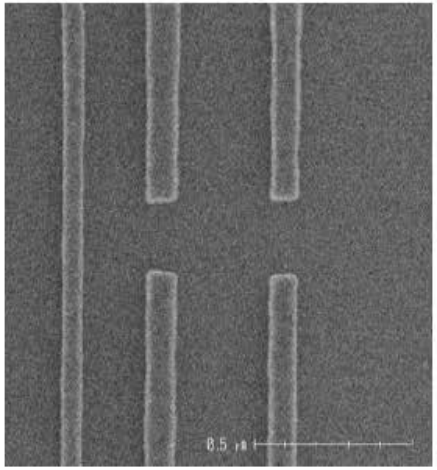


2 coatings
2 exposures
2 developments
2 etches

Double patterning







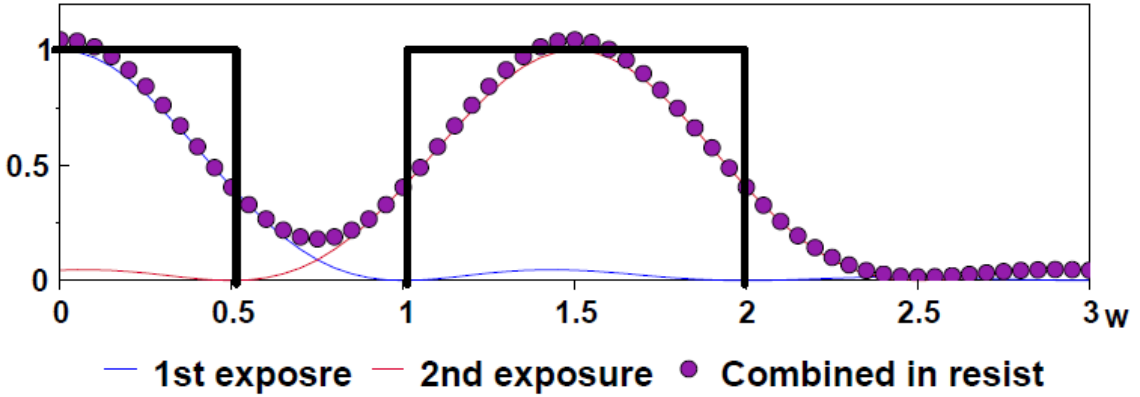
Slight Difference between Single and Double Exposures

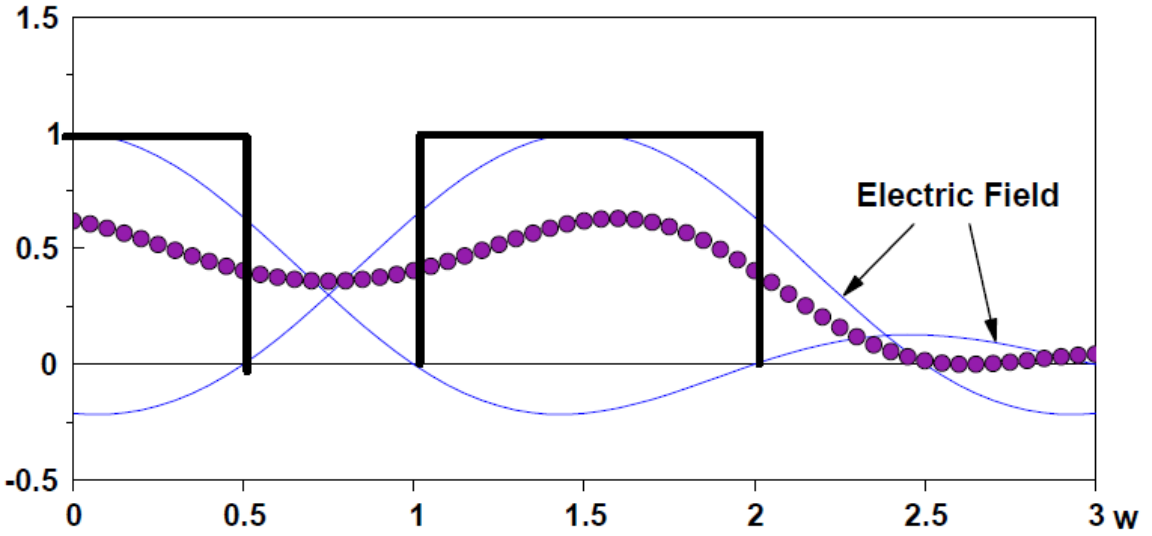
Incoherent combination of light with double exposure.
(Intensity=$E_1^2+E_2^2$)

Coherent combination with single exposure.
(Intensity in gap=$(\vec{E}_1+\vec{E}_2)^2>E_1^2+E_2^2$
Intensity ↓ in the pattern area)

In IC industry partial coherence is used that is better than coherence for high resolution, but still worse than incoherence.

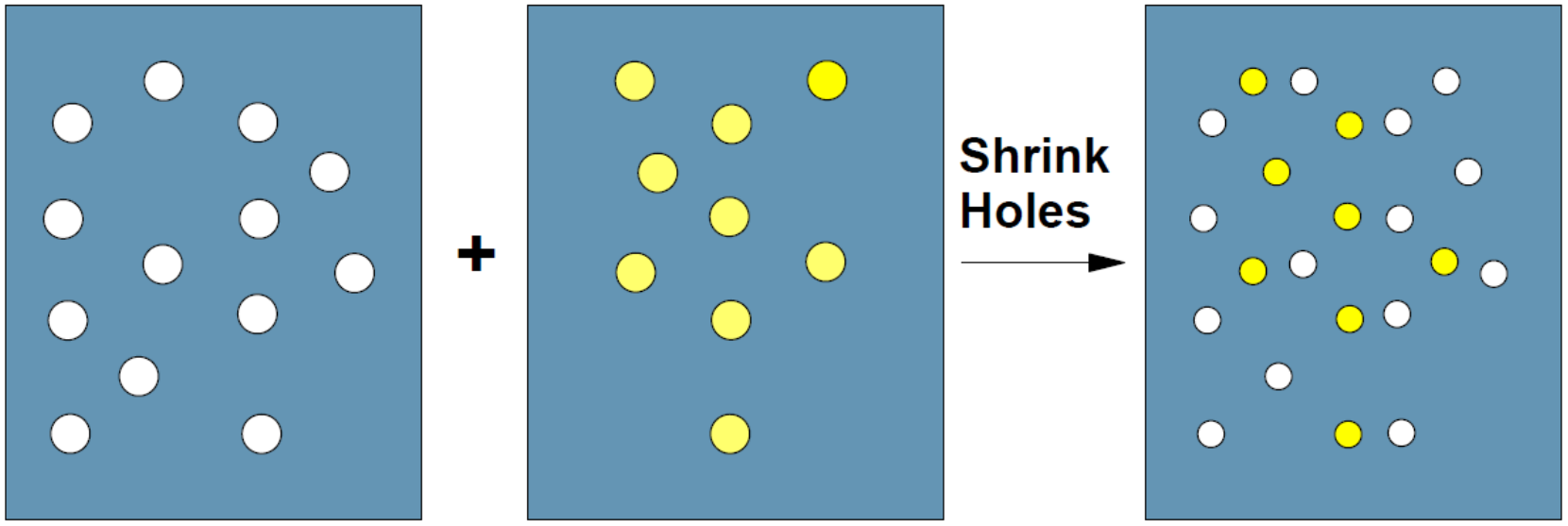
Combined intensity in resist



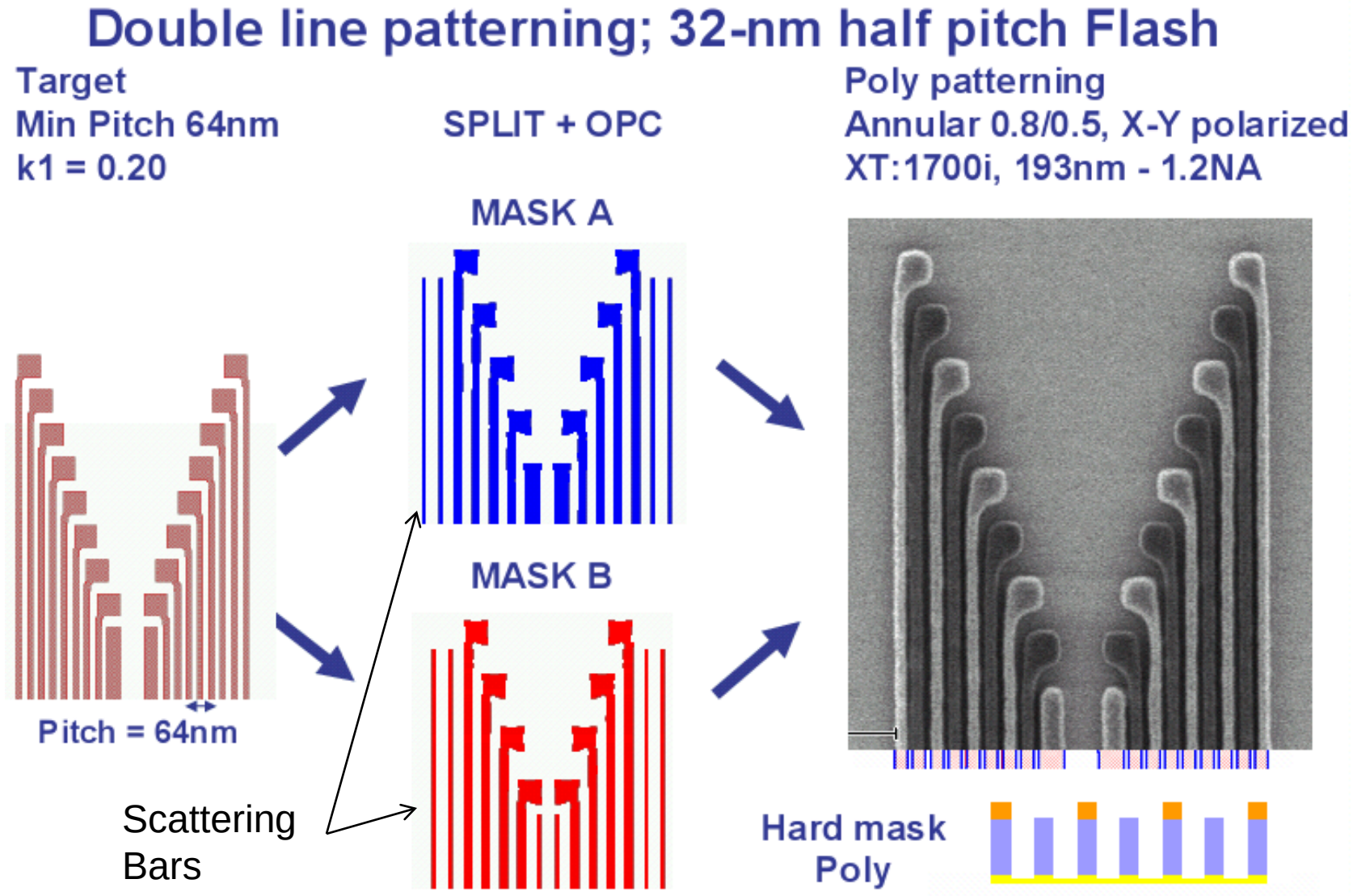


Pitch splitting to improve resolution (half pitch)

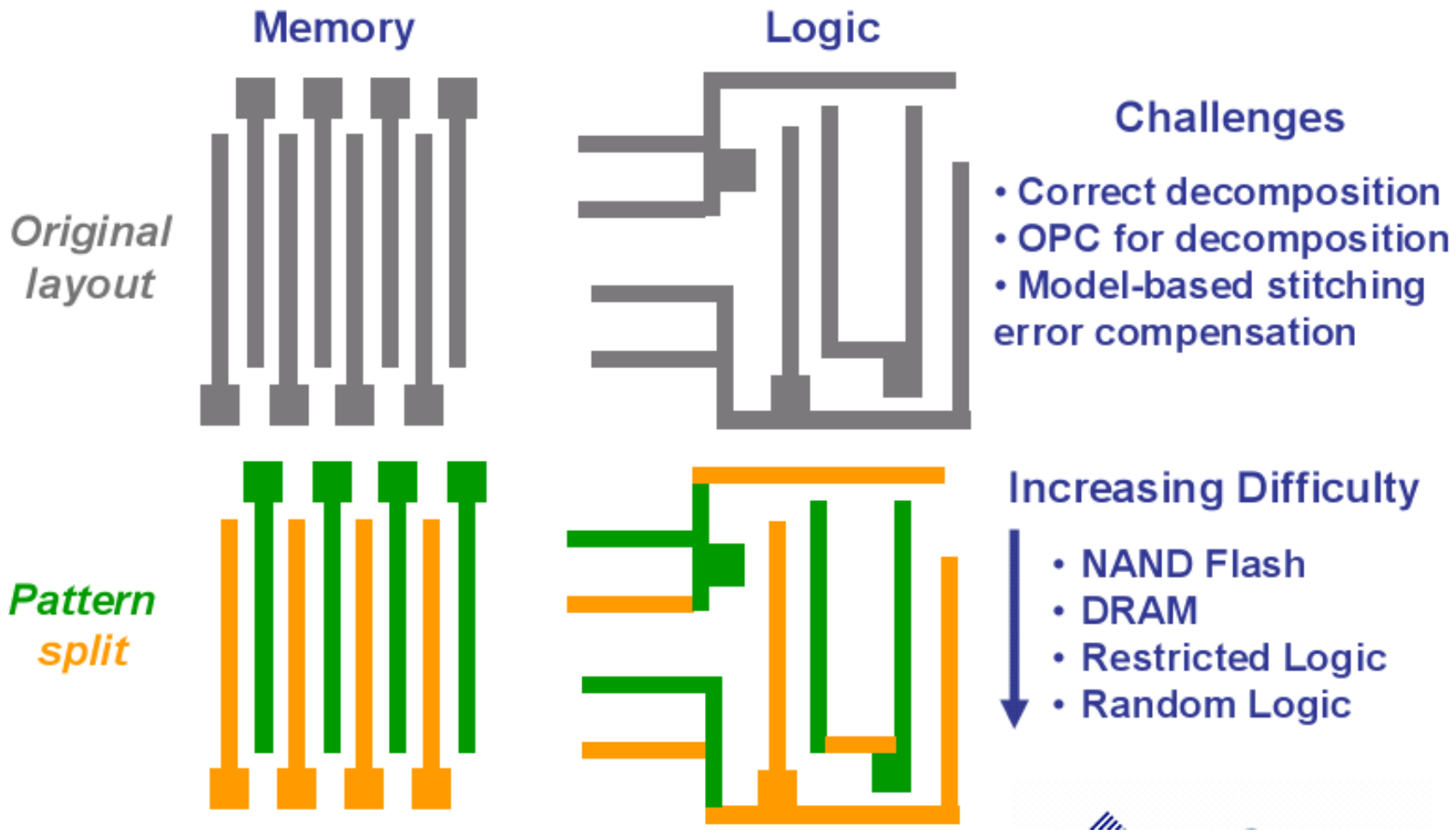
- Divide patterns on a mask into two masks, resulting in larger separation between features.
- Expose the resist twice using the two masks. (double exposure)
- For complete separation of cross talk, two exposures and two pattern transfers by etching is carried out. (double patterning)
- Finally, feature sizes are trimmed back (optional).



An Example of Double Patterning

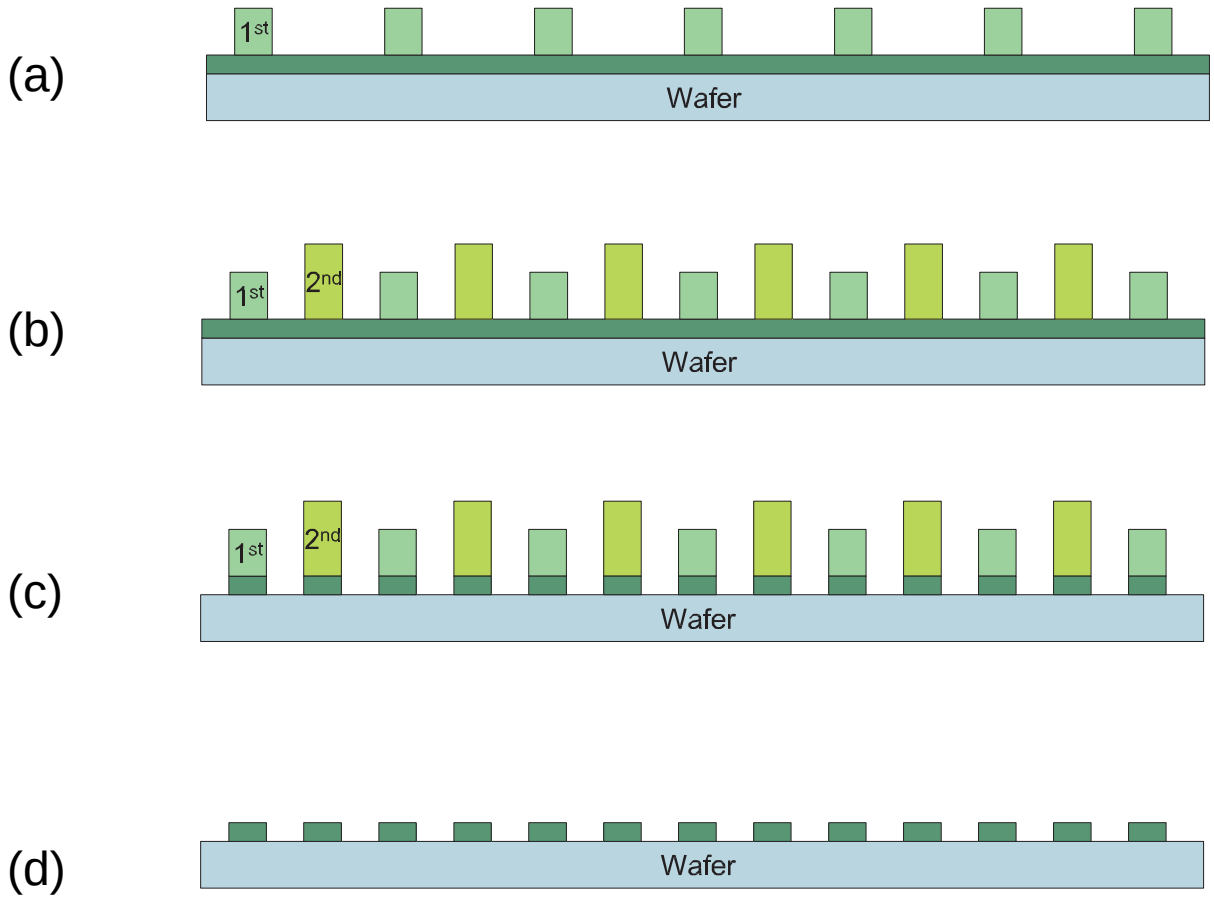


New software & algorithms required to split & optimize OPC and stitching for Double Patterning



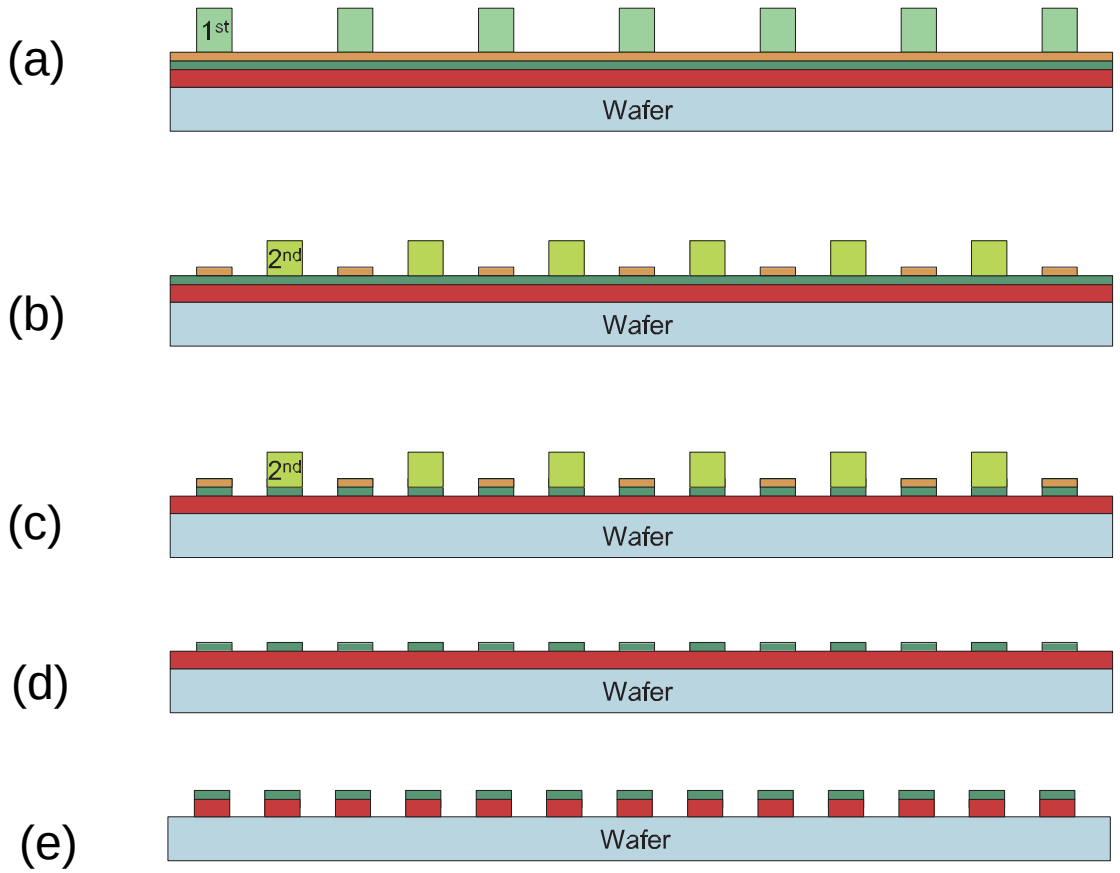
Circuit designs need to accommodate misalignment
Usually reduce the packing density slightly

DPT: Litho-Freeze-Litho-Etch (LFLE)



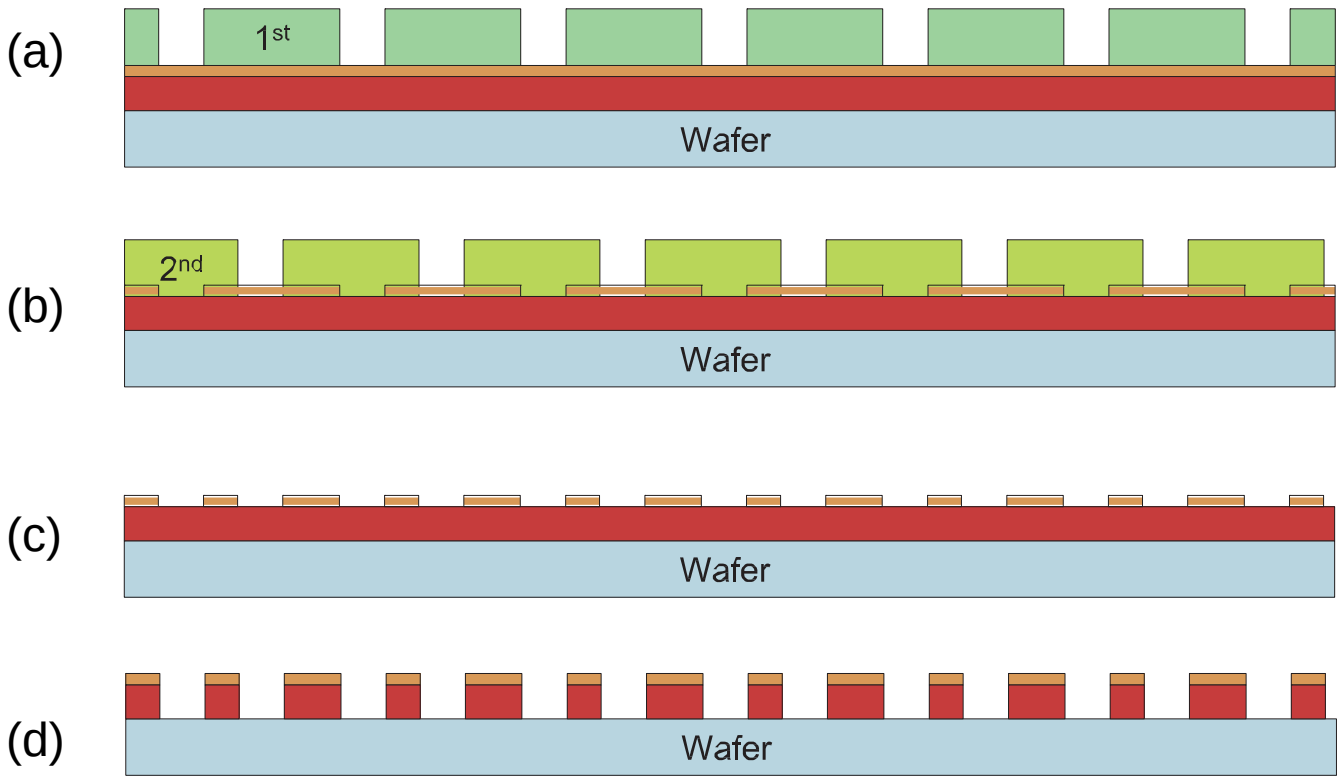
Xiao **Figure 6.59** Illustrations of the LFLE process: (a) the first photoresist pattern and pattern freeze, (b) the second photoresist pattern, (c) the etch pattern, and (d) the strip photoresist.

DPT: Litho-Etch-Litho-Etch (LELE)



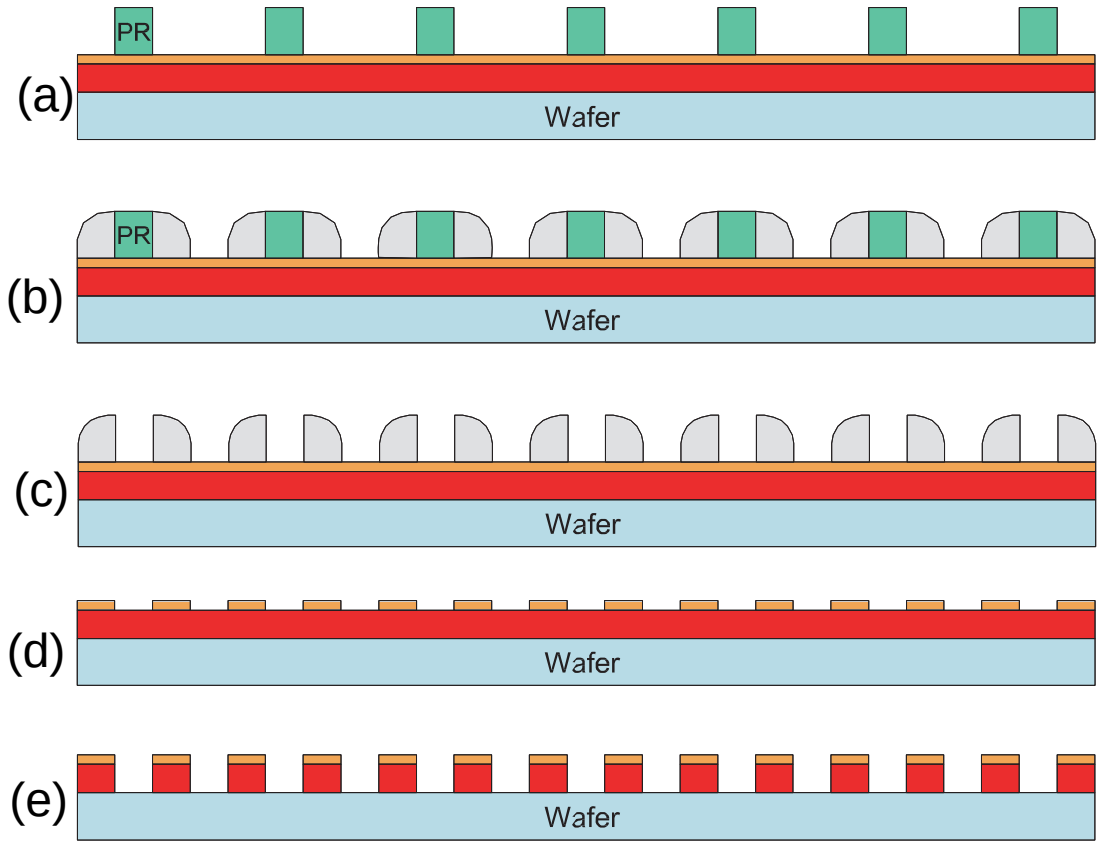
***Xiao* Figure 6.60** Illustrations of the LELE process: (a) first litho, (b) second litho after etch of the first hard mask layer, (c) etch of the second hard mask layer, (d) stripping of the second photoresist and the first hard mask, and (e) etch of the pattern on the wafer.

LELE using one hard mask layer



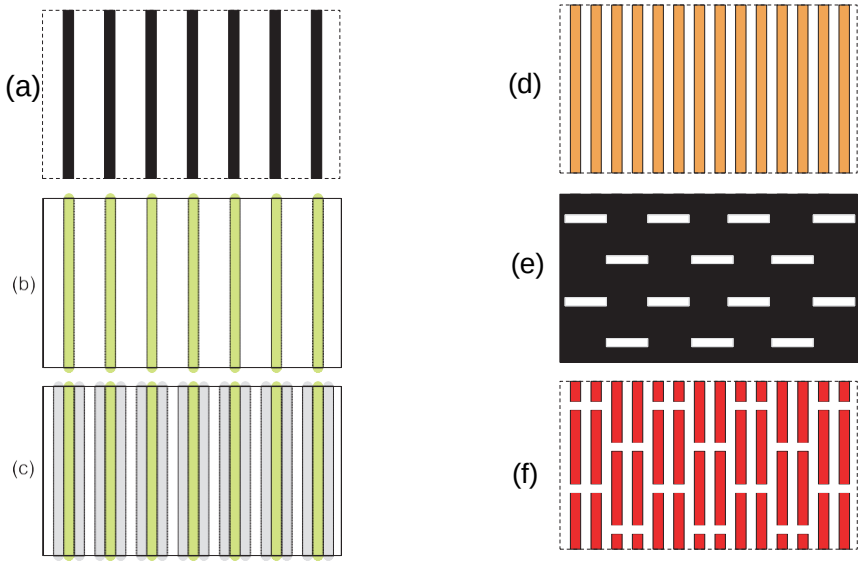
***Xiao* Figure 6.61** Illustrations of the LELE process using only one hard mask. Note the CD variation of the final pattern induced by an overlay error of the first and second masks.

Spacer (Self-) Aligned Double Patterning (SADP)



***Xiao* Figure 6.62** Illustrations of the SADP process: (a) first mask photoresist patterning; (b) low-temperature oxide CVD and spacer etch; (c) photoresist strip; (d) hard mask etch, spacer oxide strip, second mask pattern, and hard mask etch; and (e) final pattern etch.

Defining the Gate Pattern with SADP



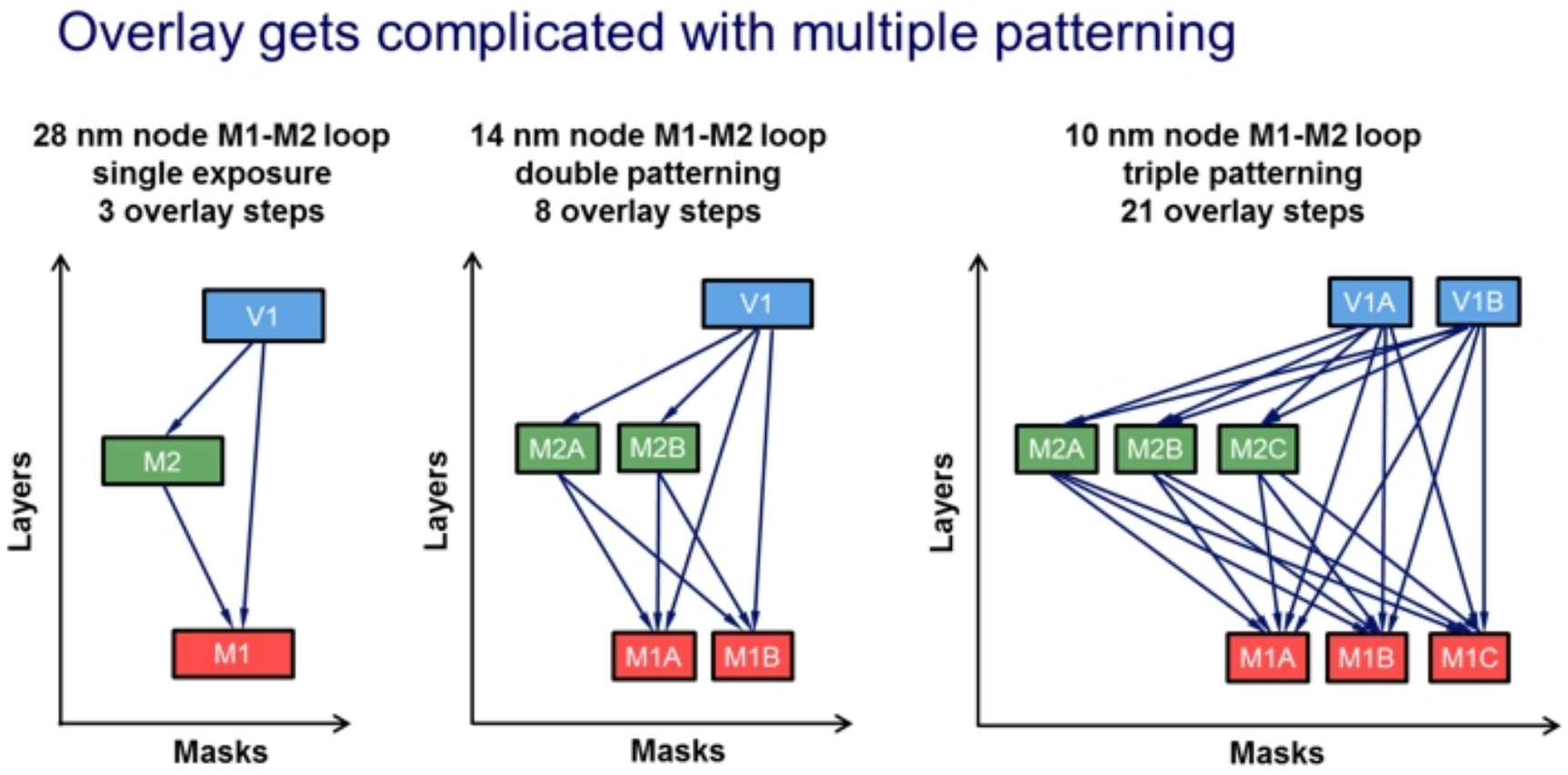
Xiao Figure 6.63 Top view of the SADP process: (a) the first mask, (b) the photoresist pattern of the first mask, (c) low-temperature oxide spacer formation, (d) hard mask etch and spacer removal, (e) the second mask, and (f) hard mask and final pattern etch.

Advantages and Disadvantages of SADP

- Accurate pattern critical dimension control
- Less strict overlay requirements for the second mask
- Low line edge roughness (LER)

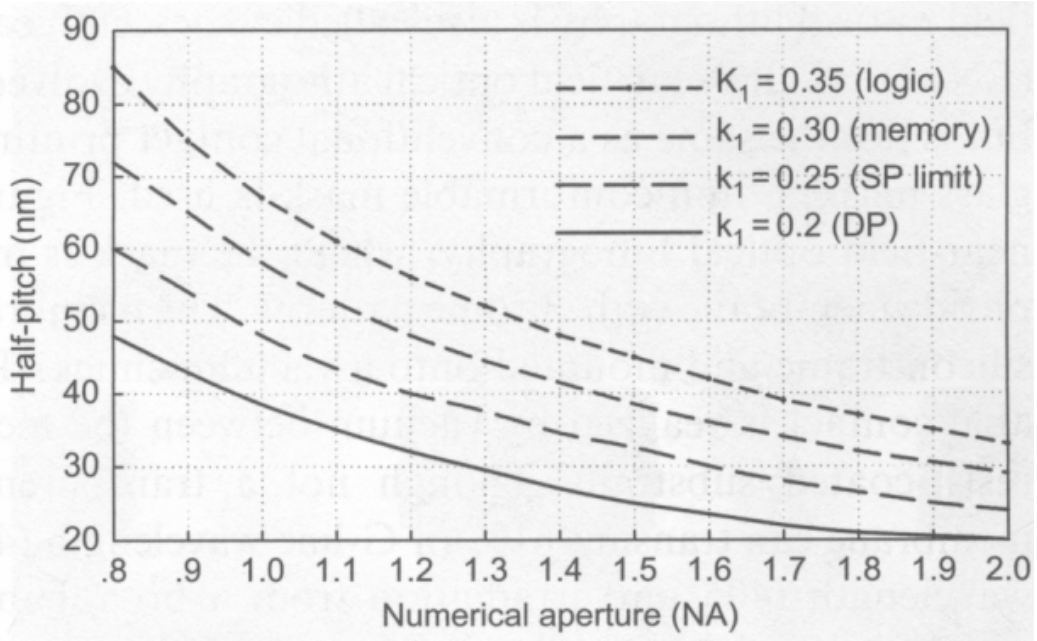
- Requires more steps, e.g. oxide CVD and spacer etch
- More expensive

Cost for Multiple Patterning: Overlay



http://www.extremetech.com/wp-content/uploads/2016/01/MP-F2.jpg

Outlook of Multiple Patterning (as of 2006)



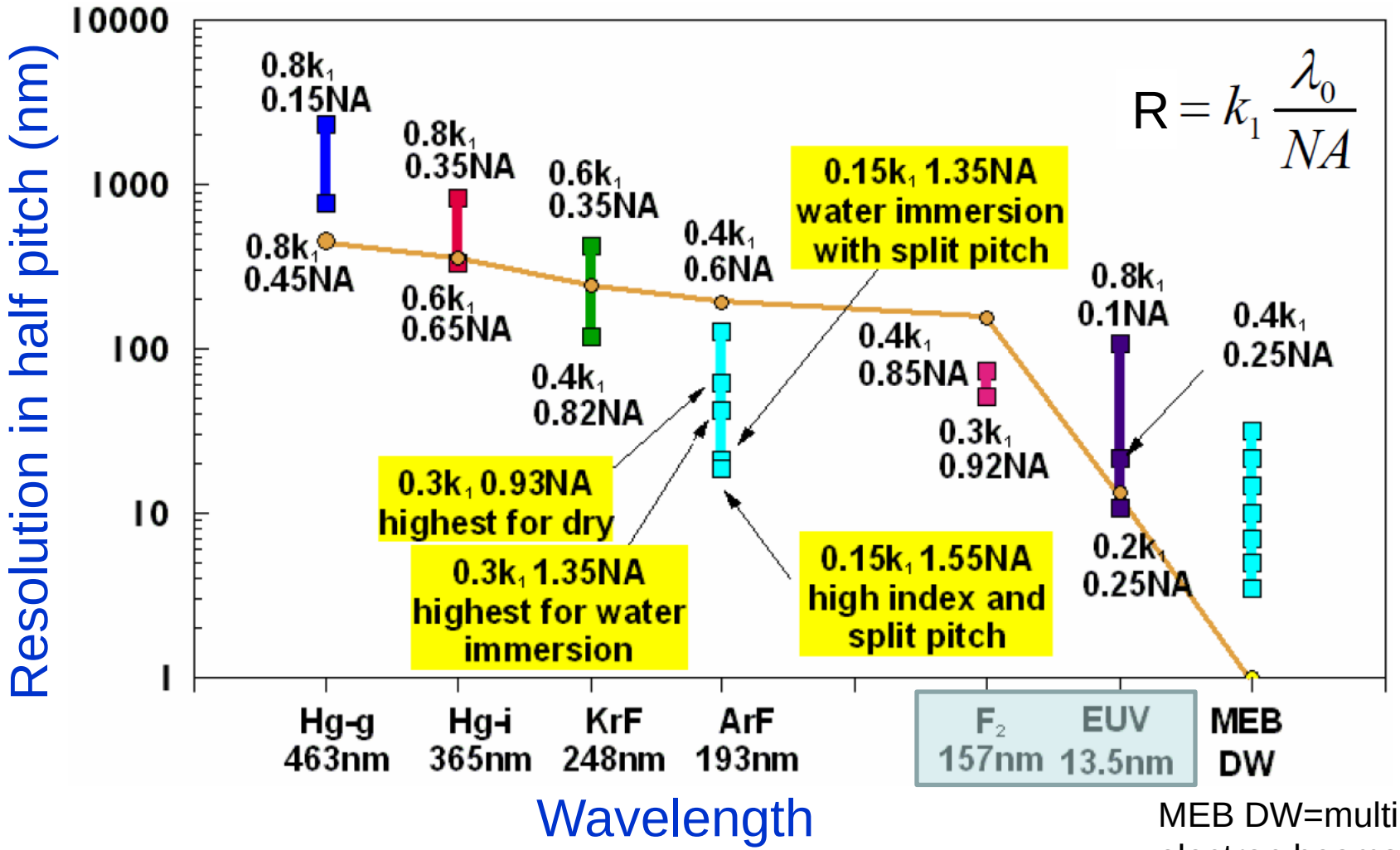
$$R = k_1 \frac{\lambda}{NA}$$

K_1 factor:

- The practical limit for single processing is 0.25
- Double processing can bring it to < 0.2

- Lowest risk route to 32nm half pitch in time
- But worst in terms of CoO (cost of ownership)
  - Two masks per critical layer
  - Reduced throughput by a factor of 2
  - Add cost to second etch step
  - Need very precise alignment between the two exposures.
- Therefore, any development improving CoO is a plus for double processing

Resolution Chart of Exposure Tools



MEB DW=multiple electron beams direct write

Discrepancy between technology nodes and minimum feature sizes

Pitch Counts

Year	Node	Half-pitch	Gate length*
2009[a]	32	52	29
2007[a]	45	68	38
2005[b]	65	90	32
2004[b]	90	90	37
2003[b]	100	100	45
2001[c]	130	150	65
1999[c]	180	230	140
1997[d]	250	250	200
1995[d]	350	350	350
1992[d]	500	500	500

* Here, gate width is defined as the physical gate length, which in recent years became smaller than the printed gate length.

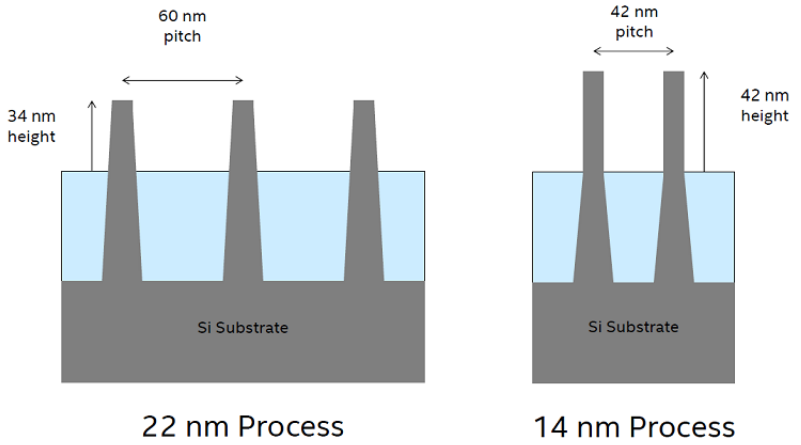
[a] ITRS data 2008 update [b] ITRS data 2006 [c] ITRS data 2001
[d] ITRS data 1997

Note that each year skipped is identified on the ITRS as between nodes.

Minimum Feature Size

	Intel 22 nm	Intel 14 nm	TSMC 16 nm	Samsung 14 nm
Transistor Fin Pitch	60 nm	42 nm	48 nm	48 nm
Transistor Gate Pitch	90 nm	70 nm	90 nm	84 nm
Interconnect Pitch	80 nm	52 nm	64 nm	64 nm
SRAM Cell Area	.1080 um^2	.0588 um^2	.0700 um^2	.0645 um^2
			S.-Y. Wu 2014 IEDM p. 48	T. Song 2014 ISSCC p. 232

Transistor Fin Improvement



http://www.extremetech.com/wp-content/uploads/2016/01/lithot1.jpg