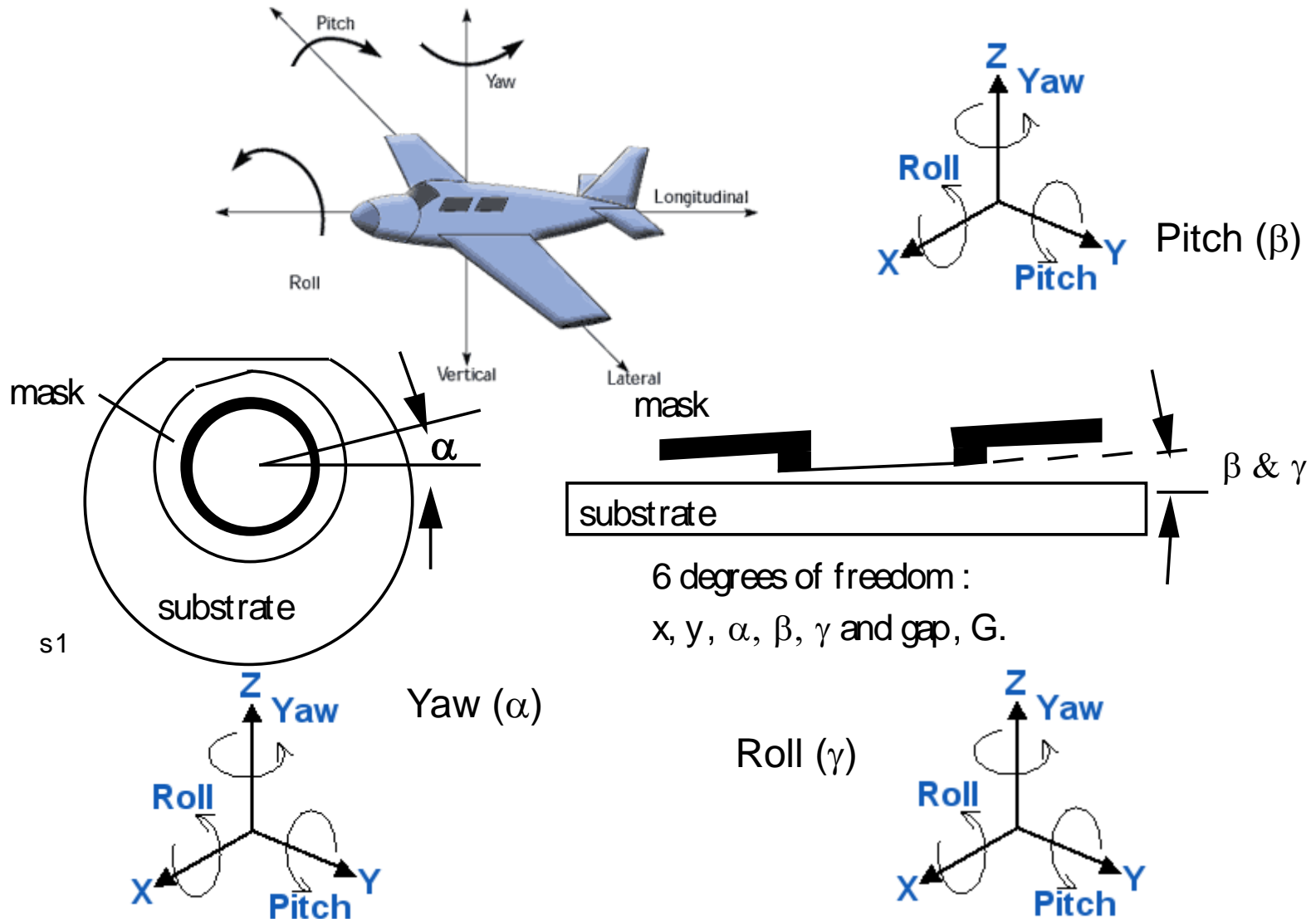

Nanometer Scale Patterning and Processing

Spring 2016

Lecture 8

Optical Lithography – Alignment

Degrees of freedom in alignment



Misalignment

- Registration: x , y , θ (yaw)
- Pitch and Roll: Mask and wafer are not perfectly placed in parallel
- Gaps are important for proximity printing using a point source (X-ray lithography)
 - Magnification error (or run-in and run-out)
- For steppers:
 - Global registration
 - Site-by-site registration
- Total misalignment $T = \left[\sum T_i^2 \right]^{1/2}$

Run-in and Run-out

Misalignment

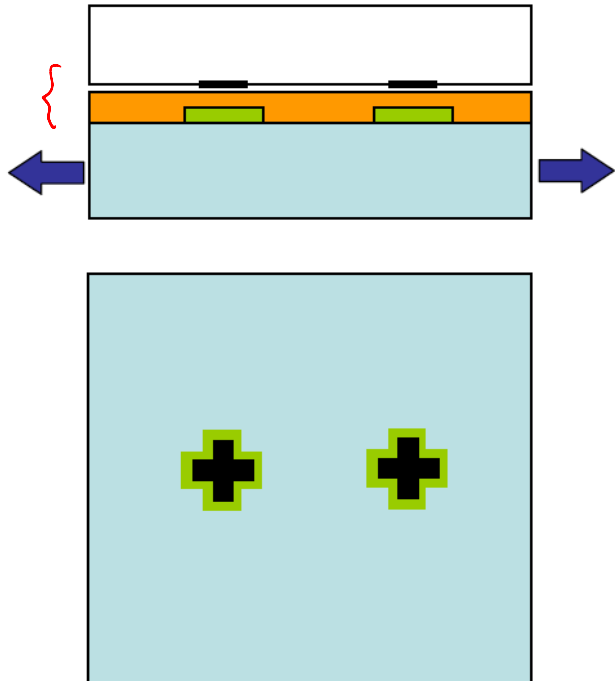
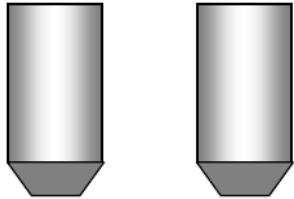
Runout

- Mask expansion
 - Fused silica thermal expansion coefficient: $5 \times 10^{-7} \text{ } ^\circ\text{C}^{-1}$
 - $< 20 \text{ nm}$ over 8 inch $\rightarrow \Delta T < 0.15 \text{ } ^\circ\text{C}$
 - Large amount of optical energy transmitted through masks
- Magnification Error in X-ray lithography systems

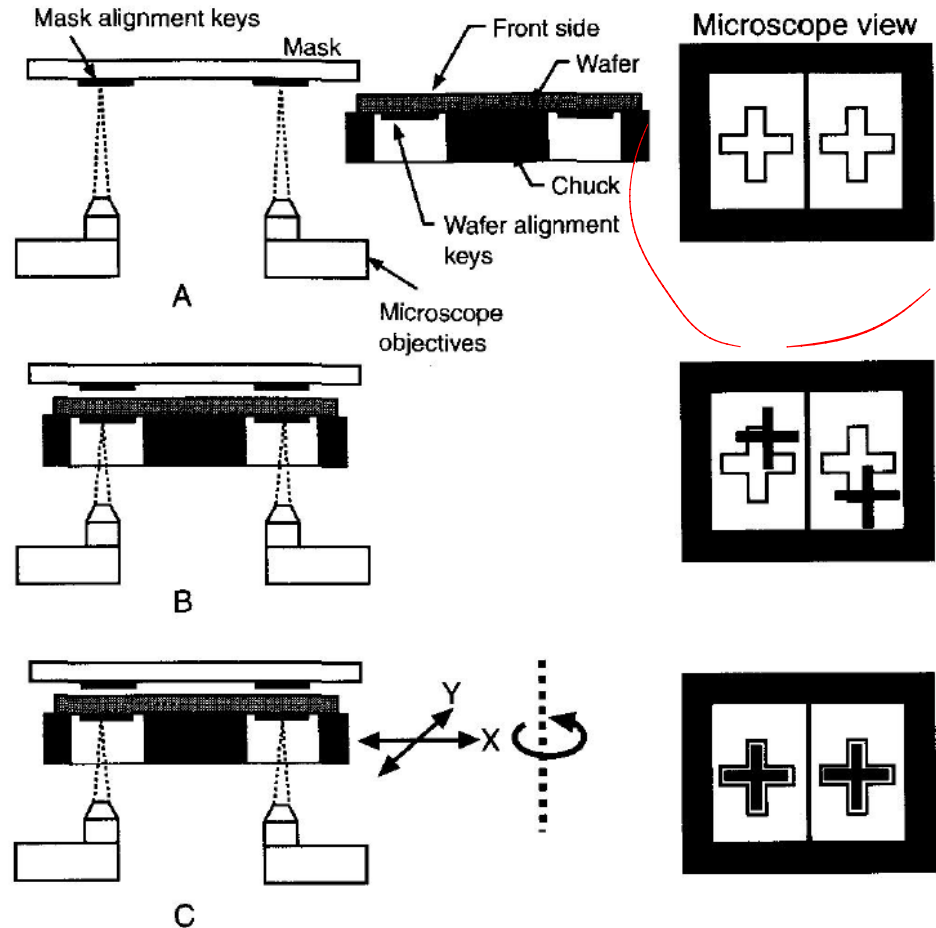
Alignment in Contact Optical Lithography

Front Side

Microscope objective lenses

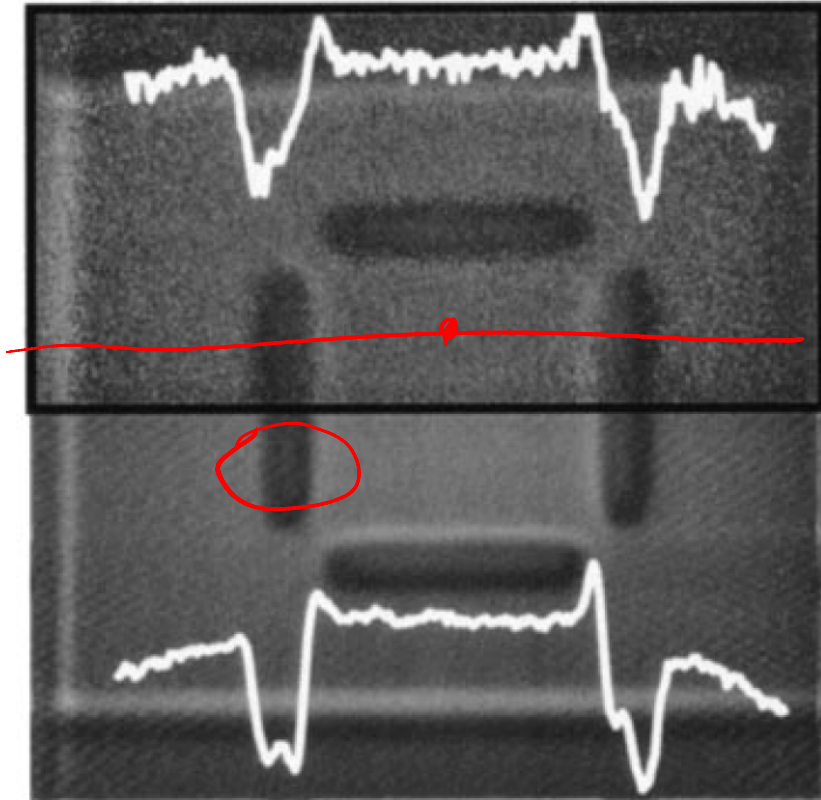


Back Side

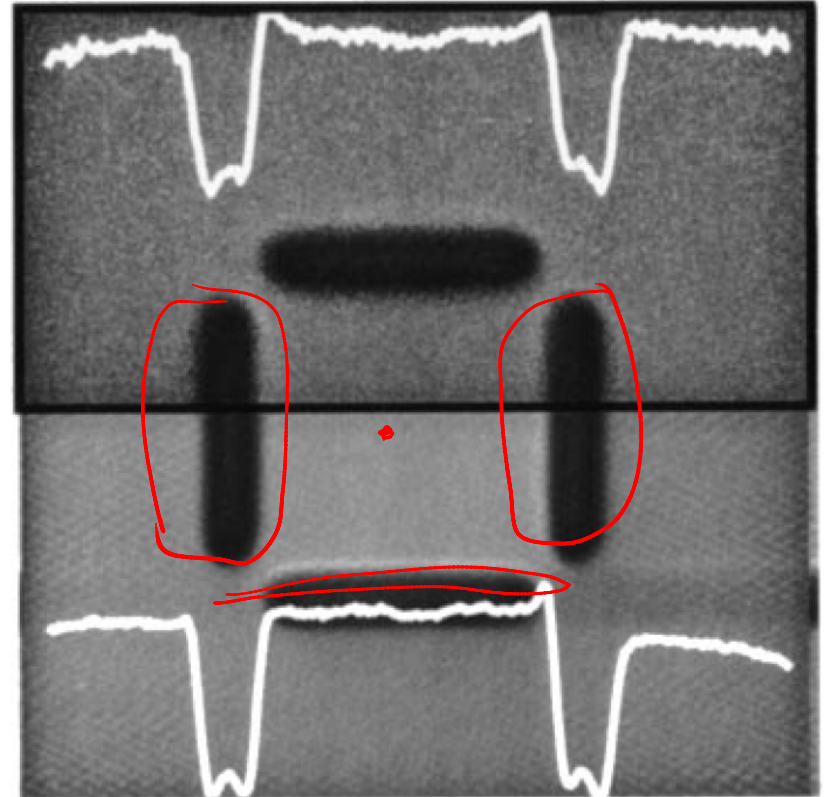


Detection of alignment marks

Low contrast



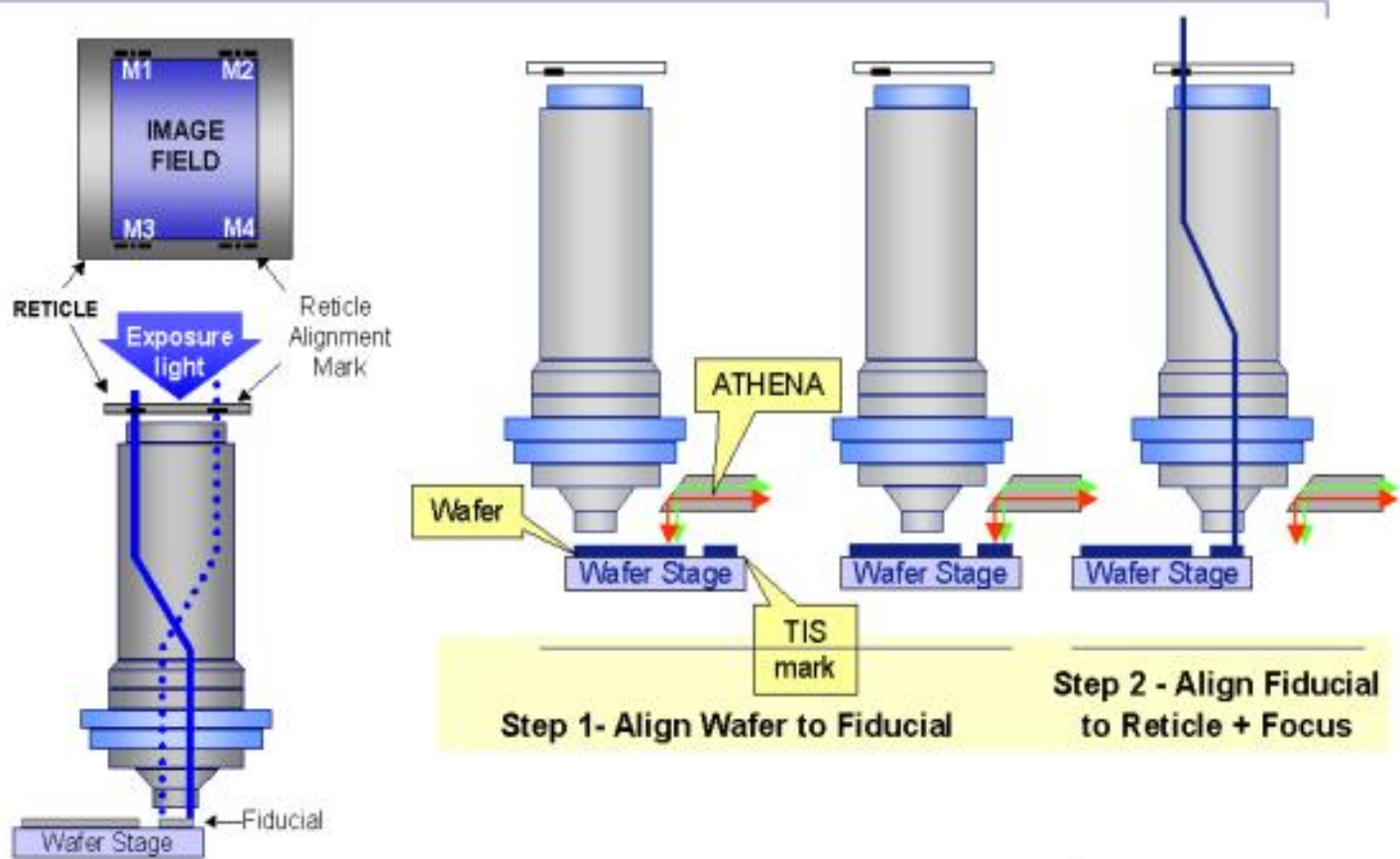
High contrast



- Algorithm looks for symmetry and calculates the center of the mark
- Alignment mark quality is the X-factor in lithography systems!

Alignment in Projection Optical Lithography

ATHENA and Reticle Blue Align



PASS500/600 Introduction
January 2001

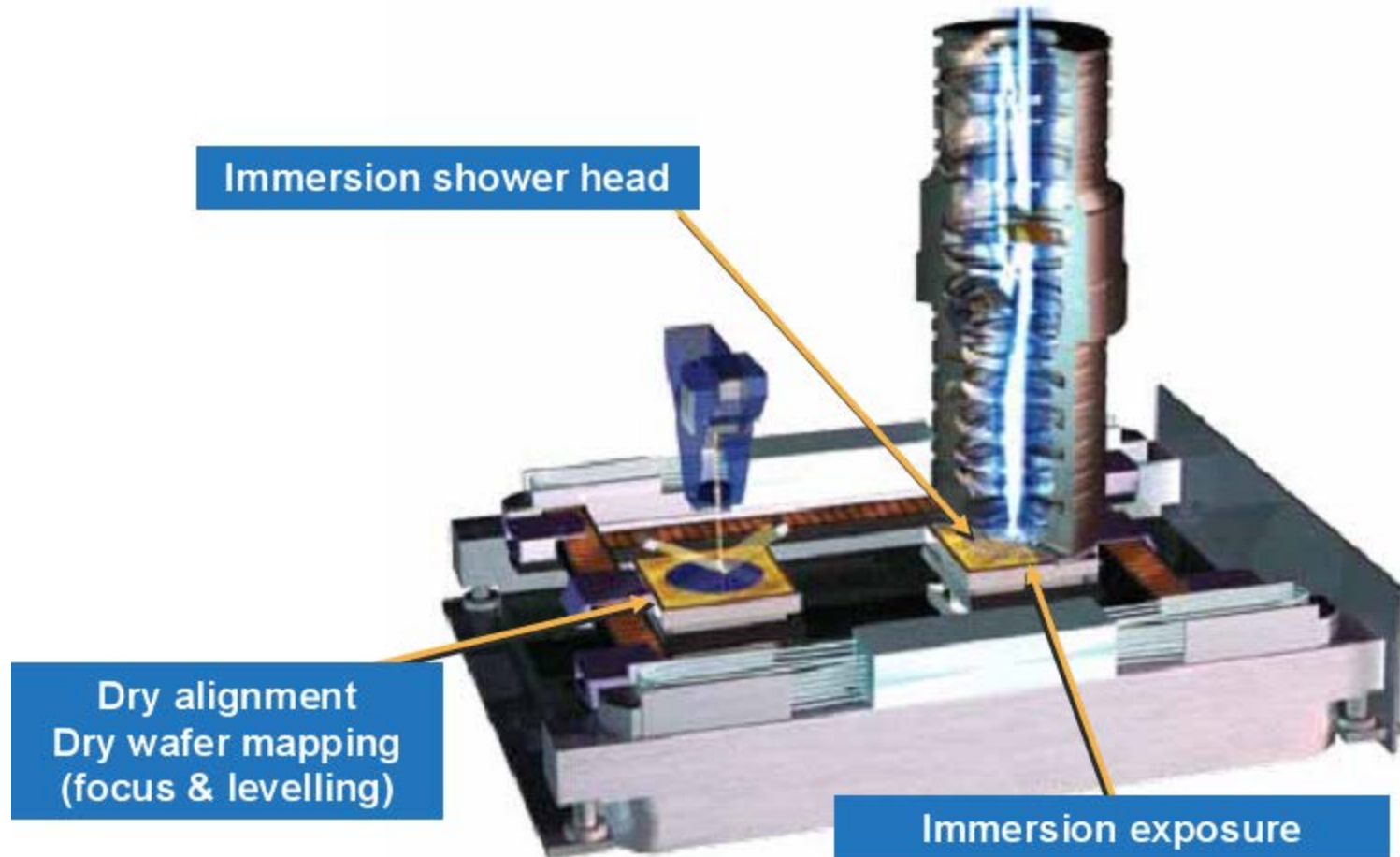


Lithography Throughput

$$T = \frac{1}{O + n \cdot [E + M + S + A + F]}$$

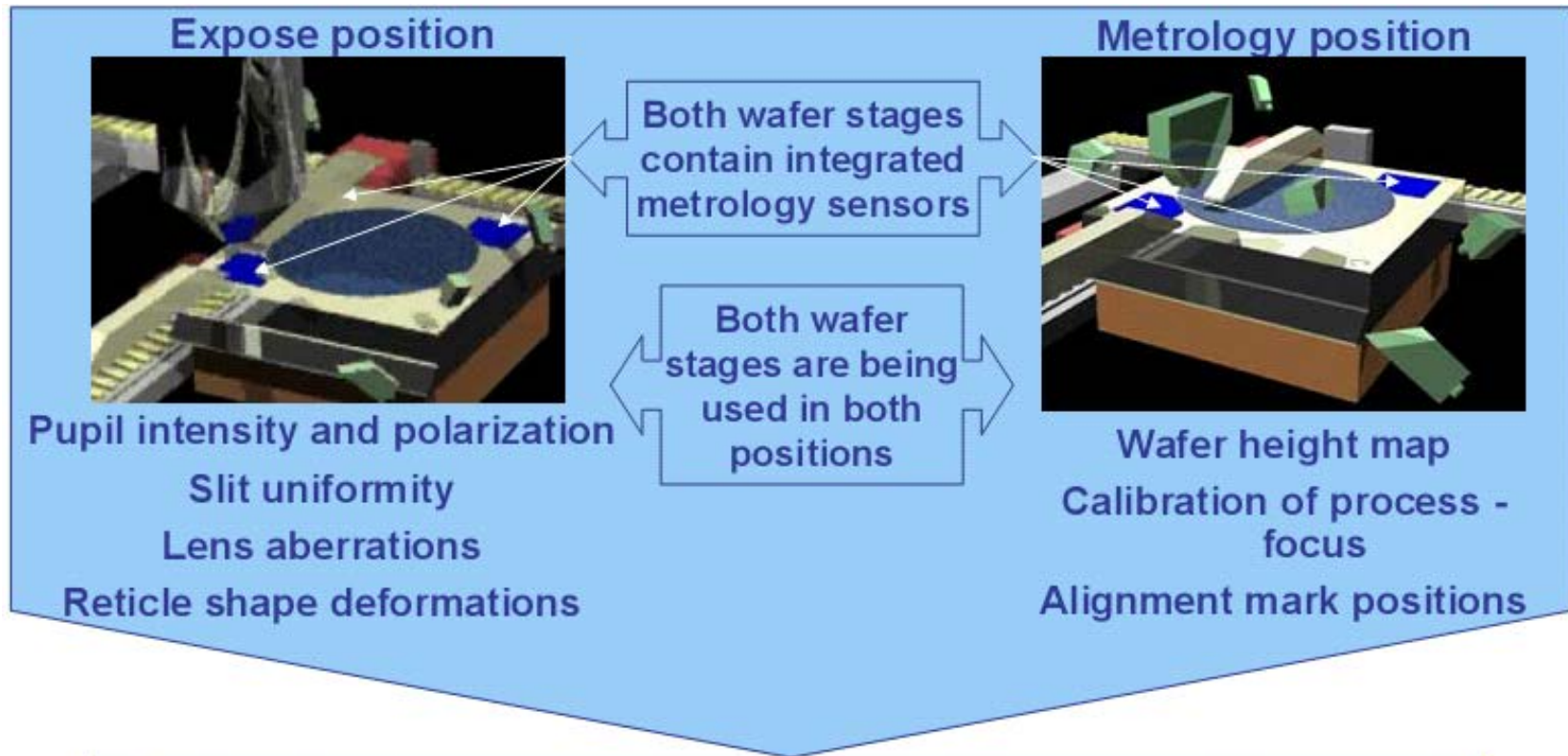
- n : number of die per wafer
- E : exposure time
- M : stage movement time per exposure
- S : stage settling time
- A : site-by-site alignment time (if used)
- F : auto-focus time (if used)
- O : overhead associated with loading/unloading, pre-alignment, moving the stage or wafer under the column and performing the global alignment

Dual Stages or “TwinScan”



- Eliminates A , F , O

Integrated Metrology and Calibration



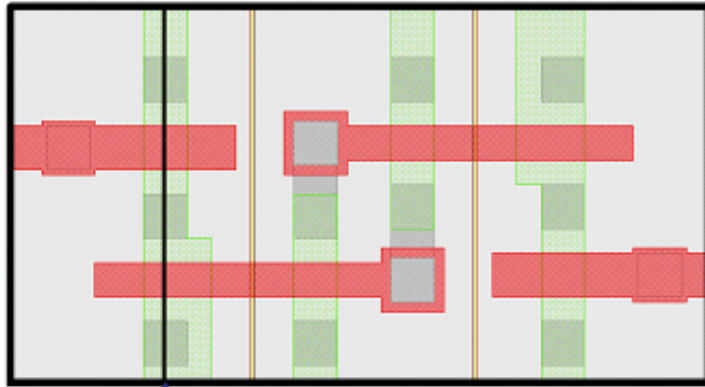
Dual wafer stage concept is key enabler for automatic integrated
MEASUREMENT - CALIBRATION - OPTIMIZATION

Increased Lithography Requirements

Resolution, CD uniformity & overlay drive shrink

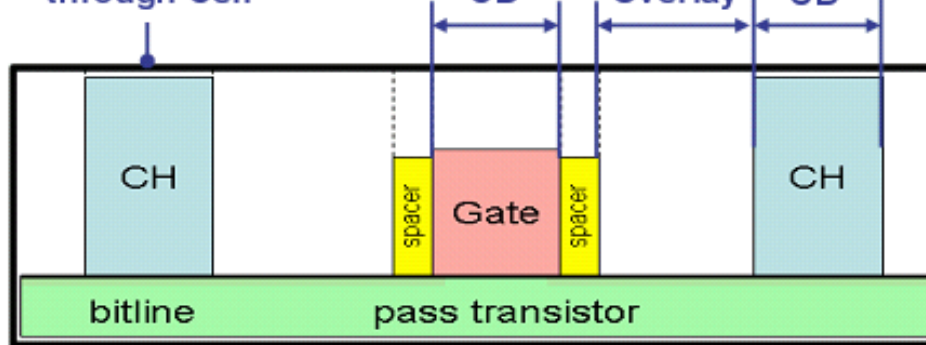
Layout 6 transistor SRAM Cell

Design Rule & Cell Area [μm^2]

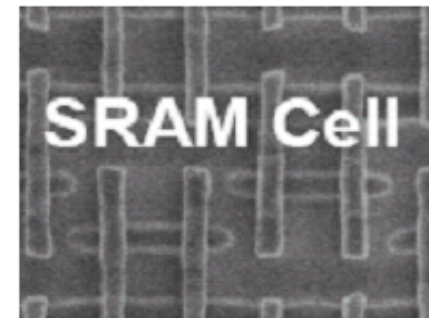


Node	Aggressive	Typical	Relaxed
130 nm	2.00	2.50	3.00
90 nm	1.00	1.25	1.50
65 nm	0.45	0.55	0.80
45 nm	0.20	0.27	0.34
32 nm	0.10	0.13	0.19

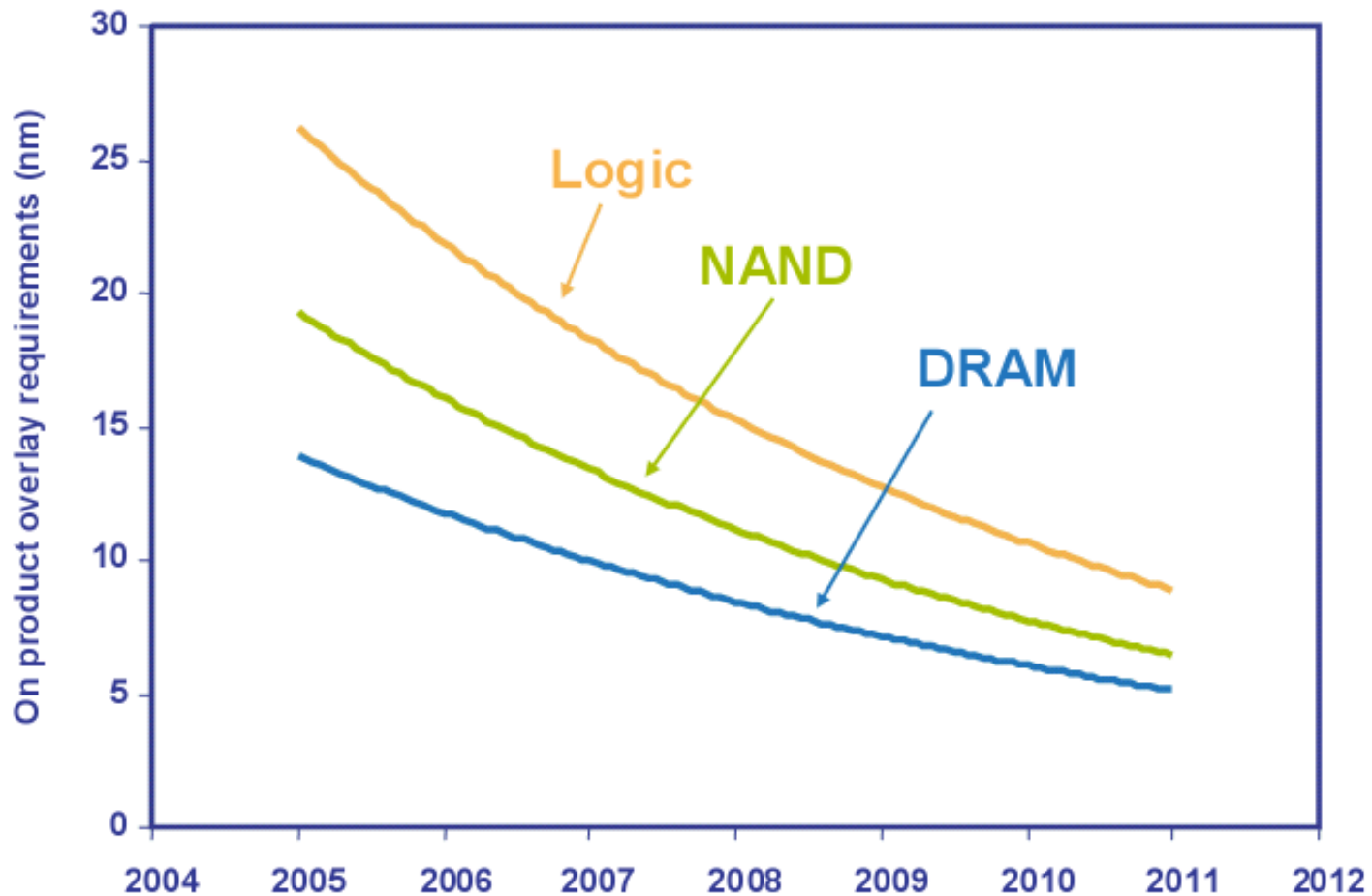
X-section through Cell



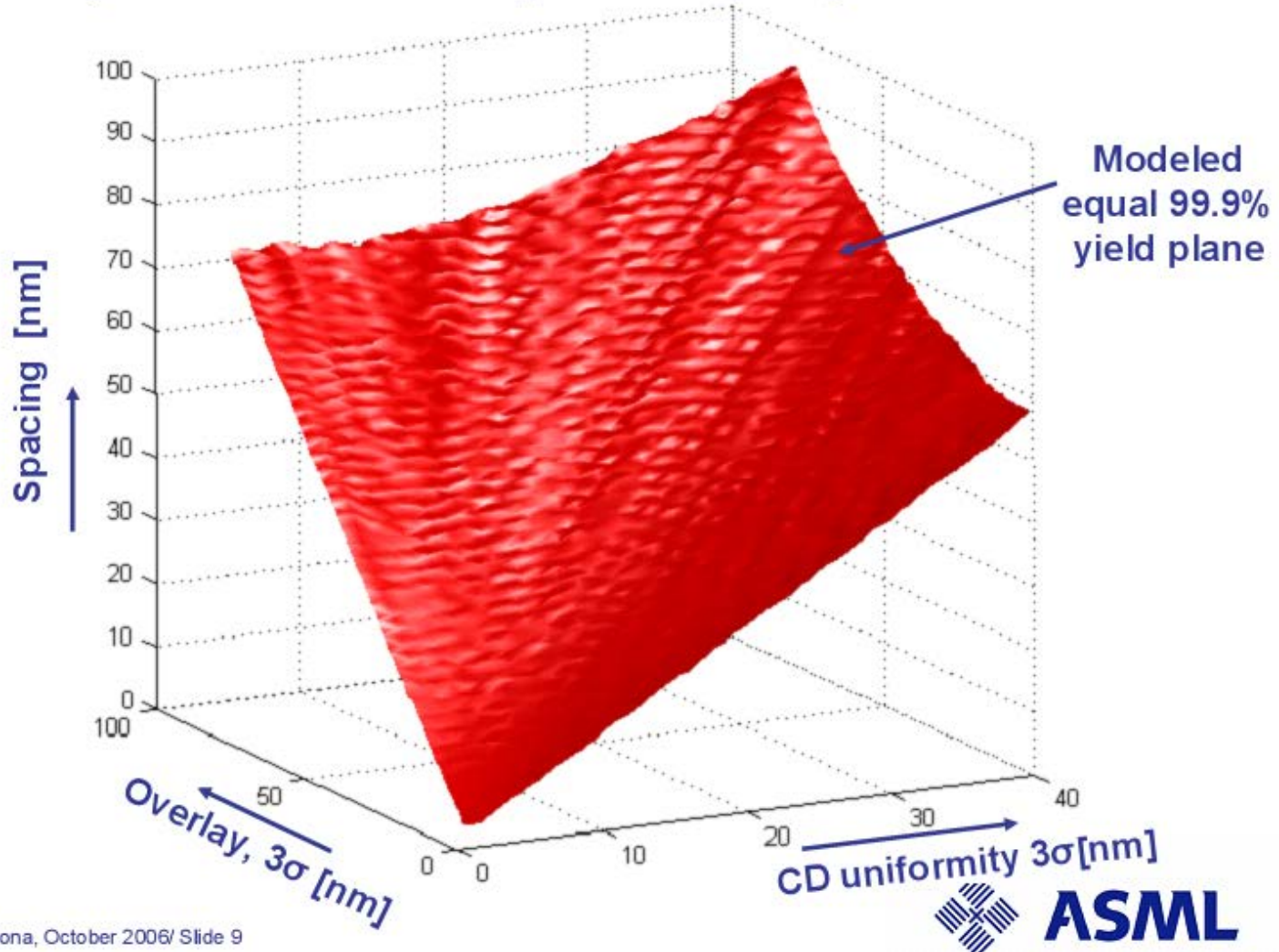
cell area 0.24 μm^2
metal pitch 130nm
ArF immersion



Shrink drives overlay requirements

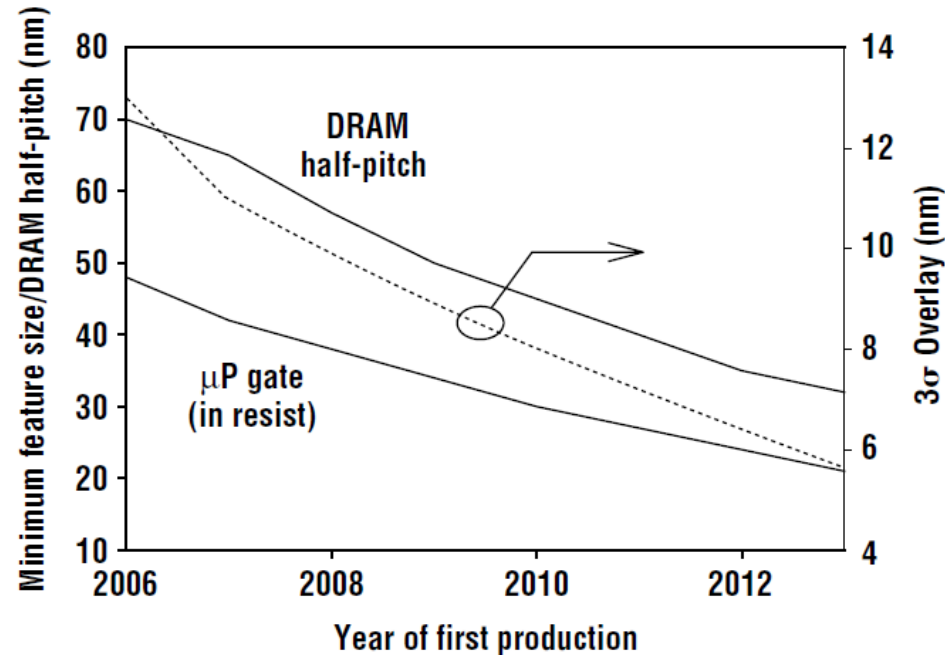


Overlay and resolution (-control) key for device scaling



Barcelona, October 2006/ Slide 9

Resolution and Alignment Requirements



- Requirements are application specific
- Six-standard-deviation: 6σ
- Line width variation: $6\sigma < 10\%$ Minimum Line width (ML)
- Misalignment: $6\sigma \sim 1/3$ ML
 - Recently this requirement has been relaxed because registration at few nm is challenging