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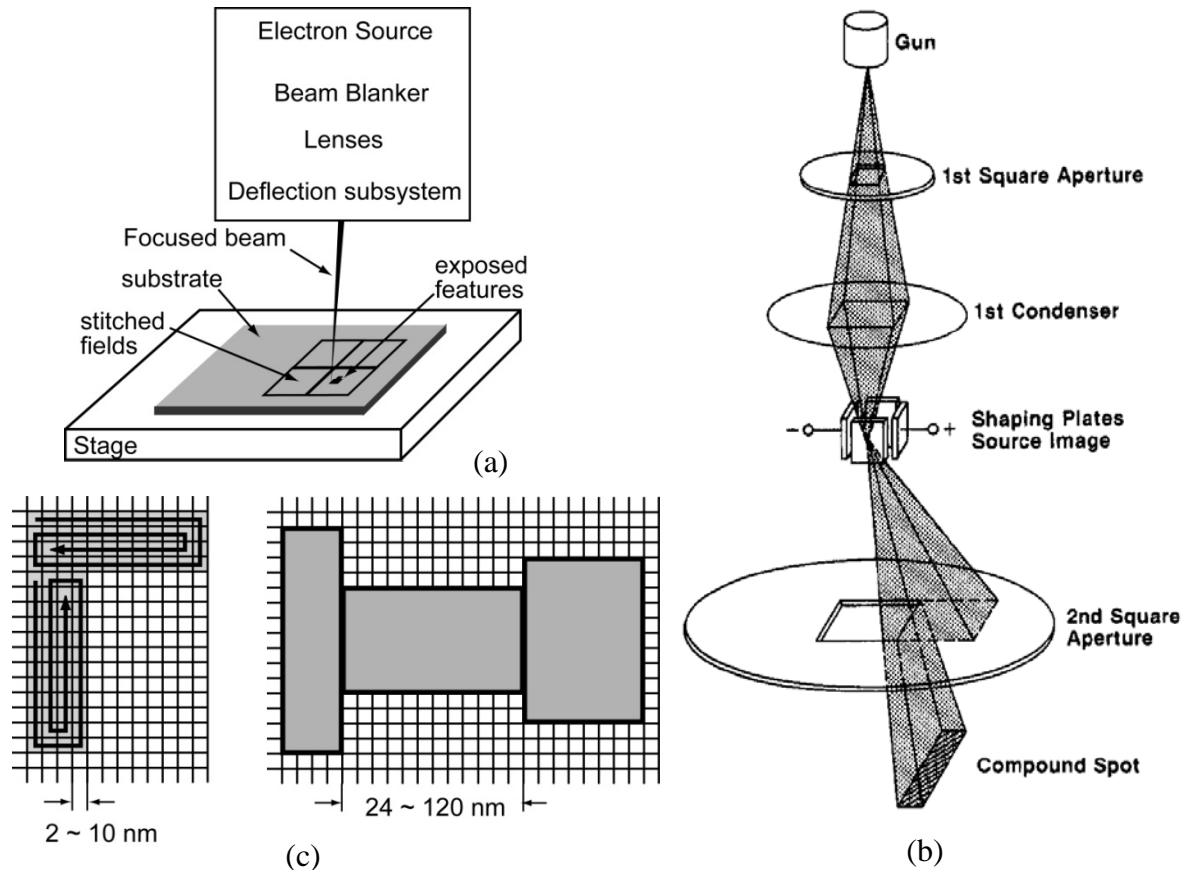
# Nanometer Scale Patterning and Processing

Spring 2016

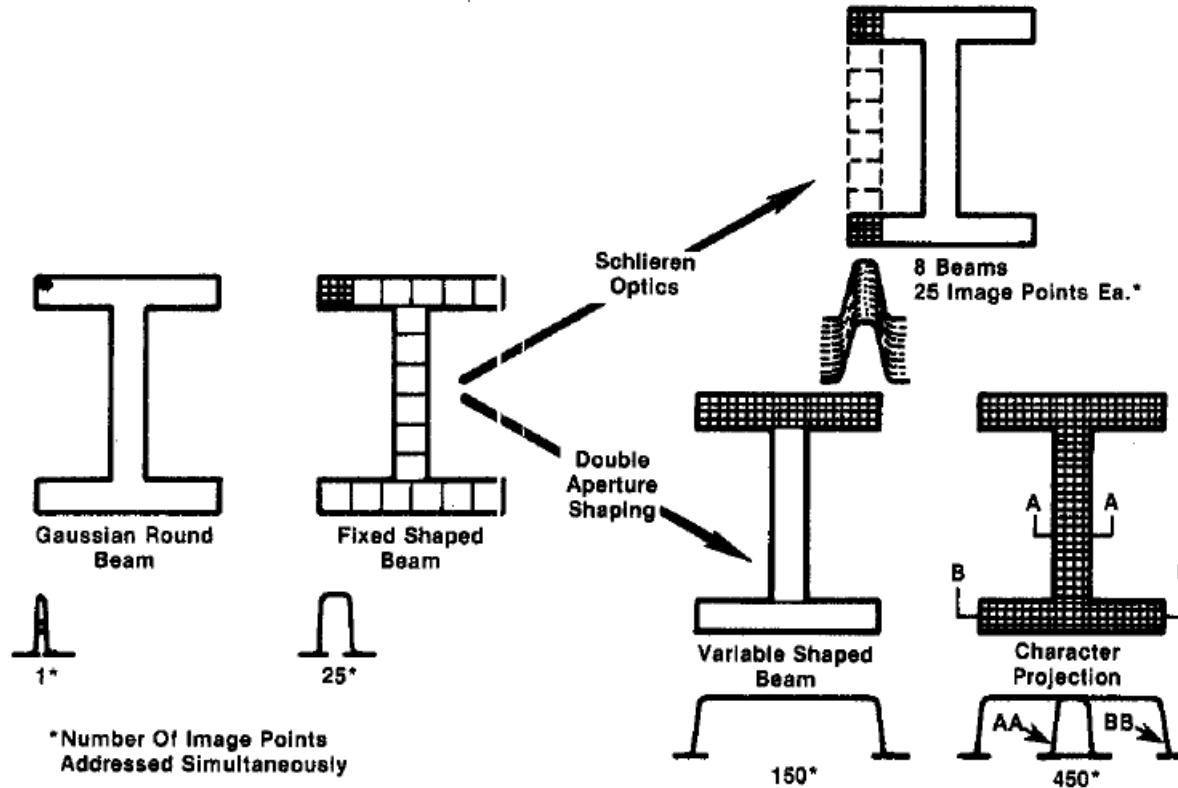
## Lecture 22

### Shaped-Electron-Beam Lithography

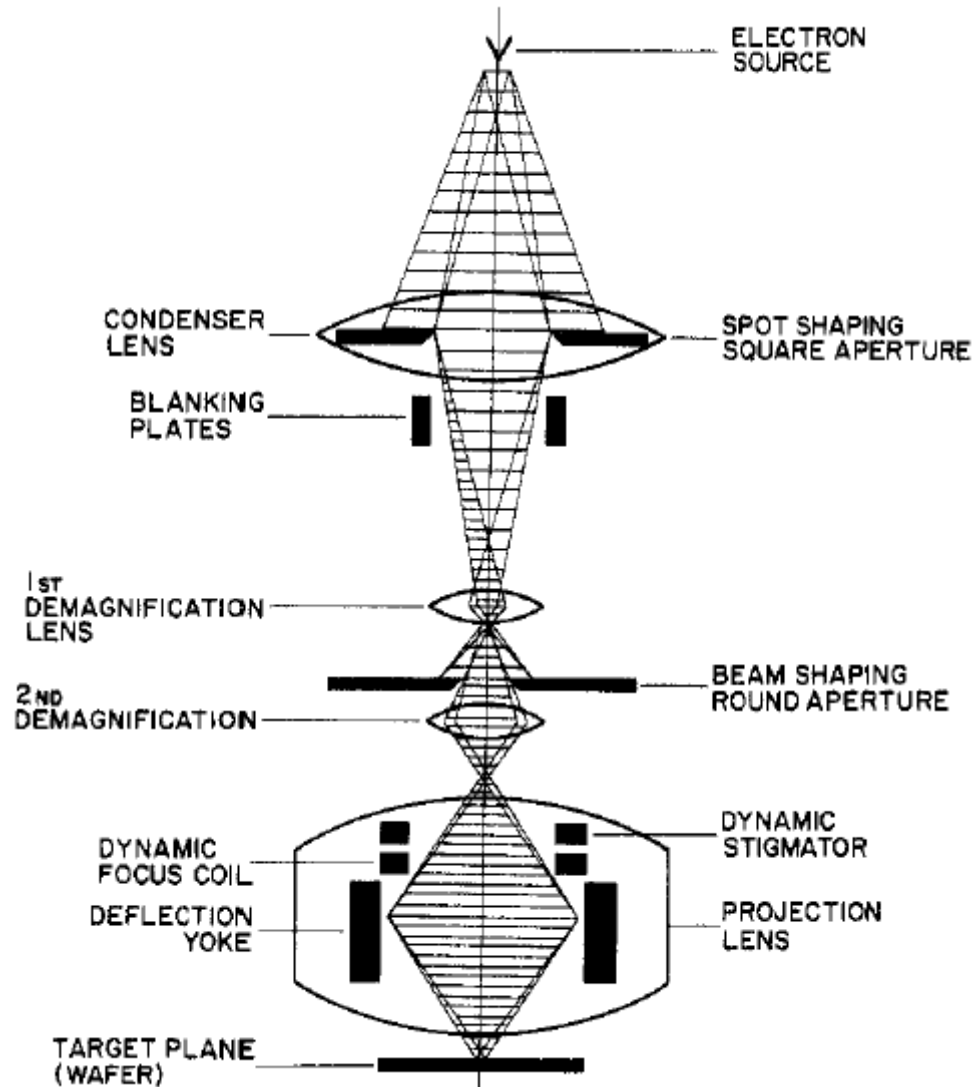
# The Need for Shaped-Beam: Throughput



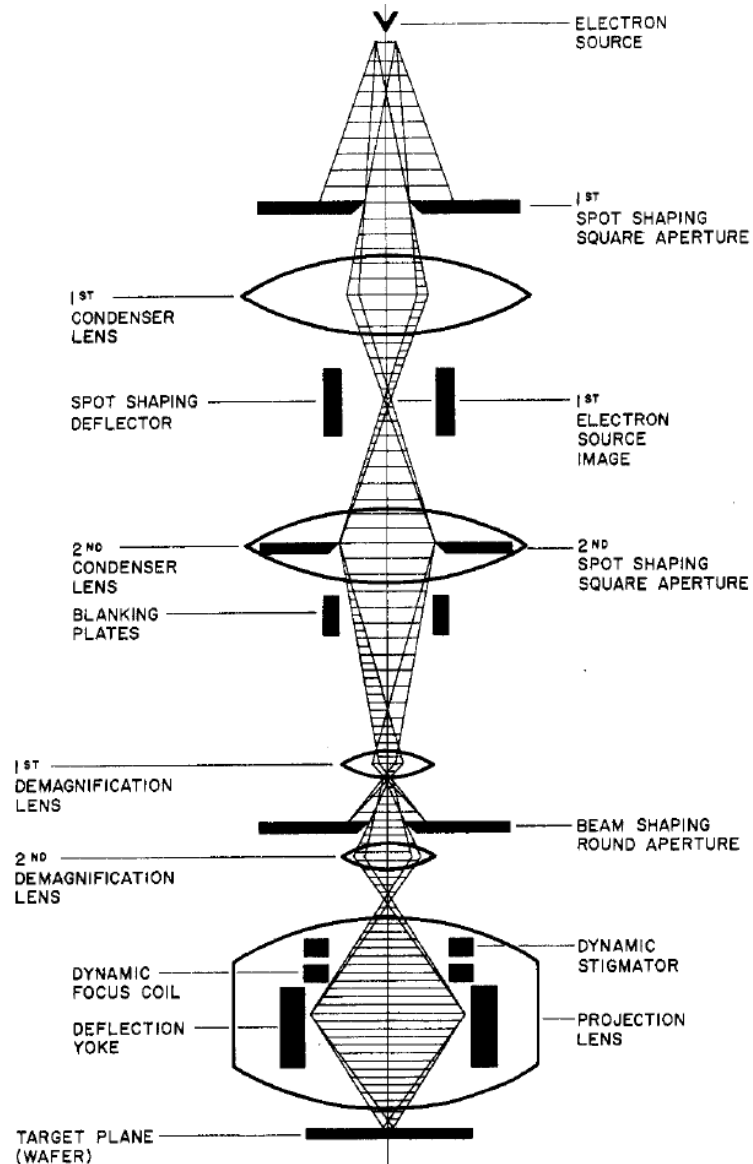
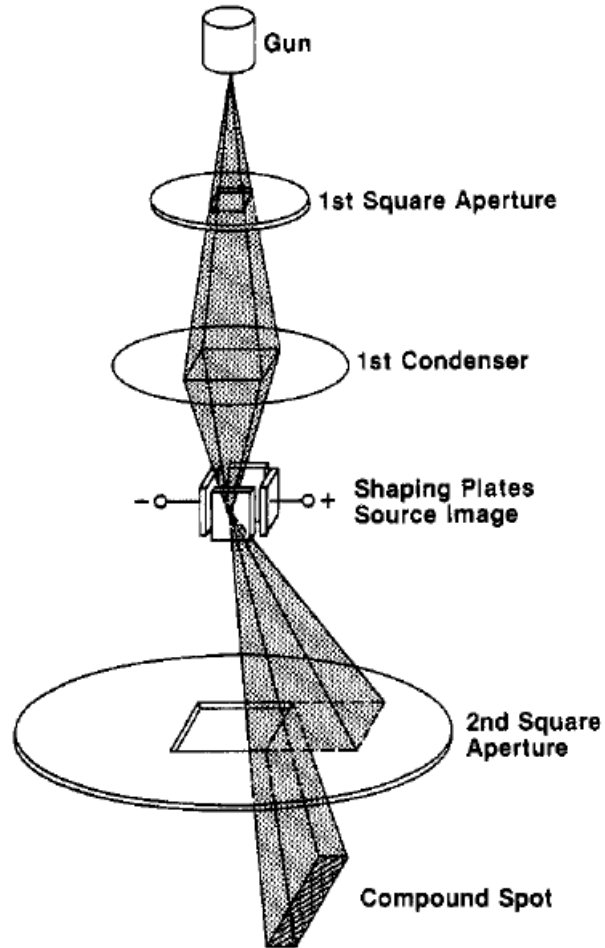
# Various Beam Profiles



# Fixed-shaped-beam imaging



# Variable Shaped Beam Imaging

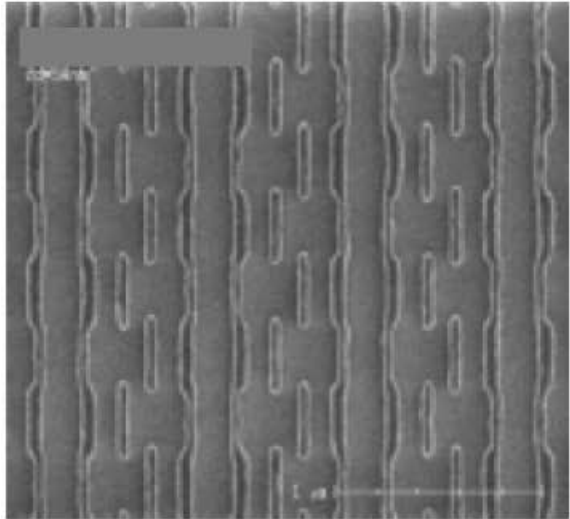


# IBM's EL5 Shaped Beam System

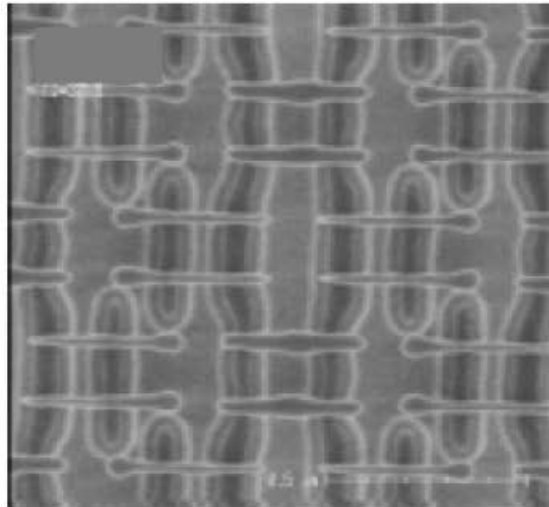
**TABLE 1. PERFORMANCE SPECIFICATIONS OF EL5**

Stage travel	300 mm+
Substrate compatibility	Carrier based – compatible with all existing mask and wafer standards
Accelerating voltage	50 kV
Current density	100 A/cm <sup>2</sup>
Magnetic deflection range (field)	2.16 mm
Electrostatic deflection range (subfield)	24 μm
Magnetic lsb	<1 nm
Electrostatic position lsb	1 nm
Maximum spot size	2 × 2 μm
Spot shaping lsb	1 nm
Image placement	<20 nm 3 sigma
Minimum image	70 nm
Maximum effective pixel transfer rate (70 nm)	8 GHz

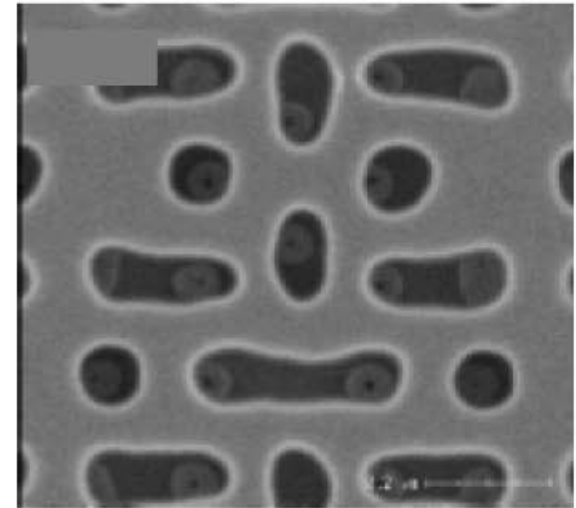
# Performance of the Latest Variable Shaped Electron-Beam lithography tool



OD



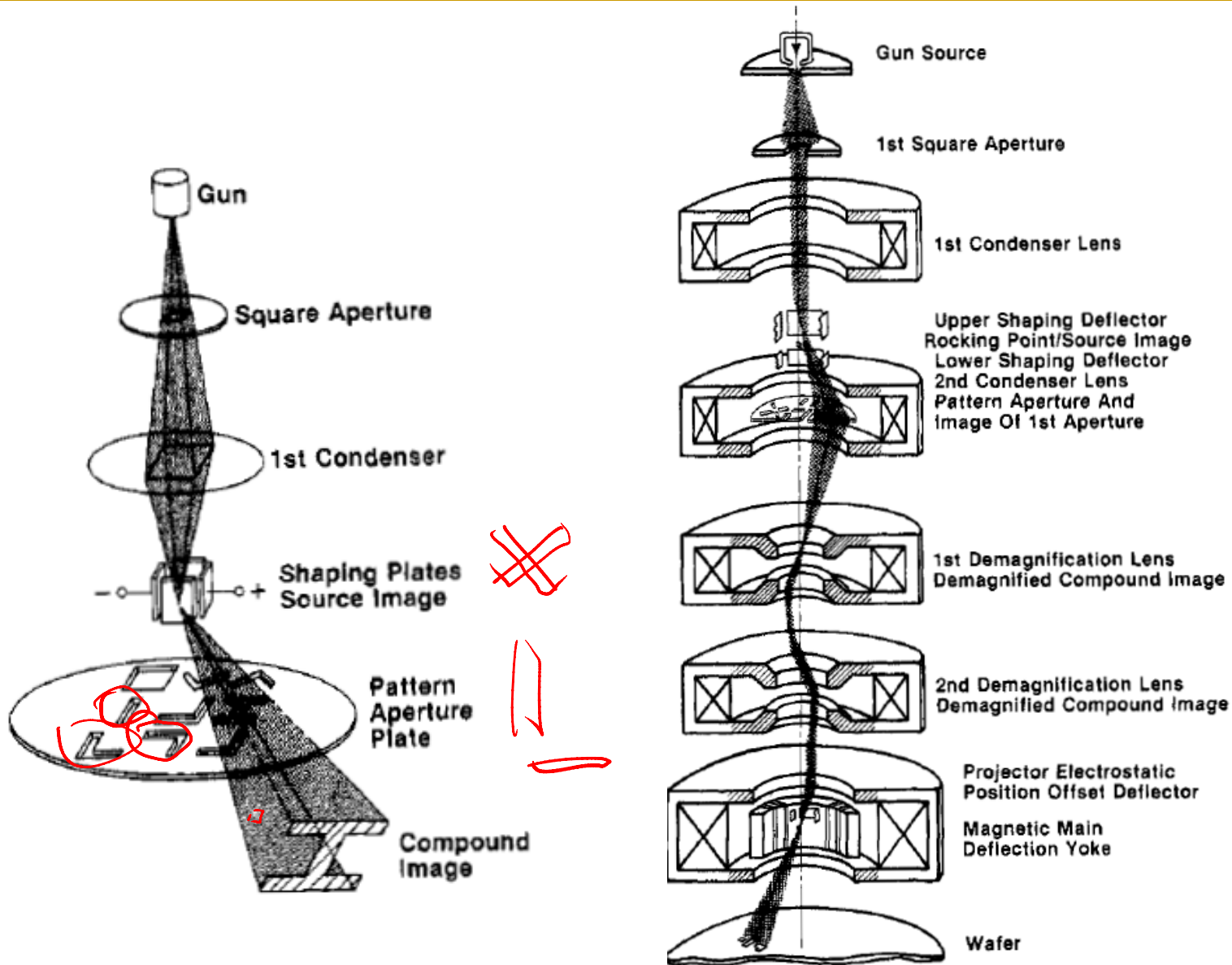
Gate



Contact and Metal 1

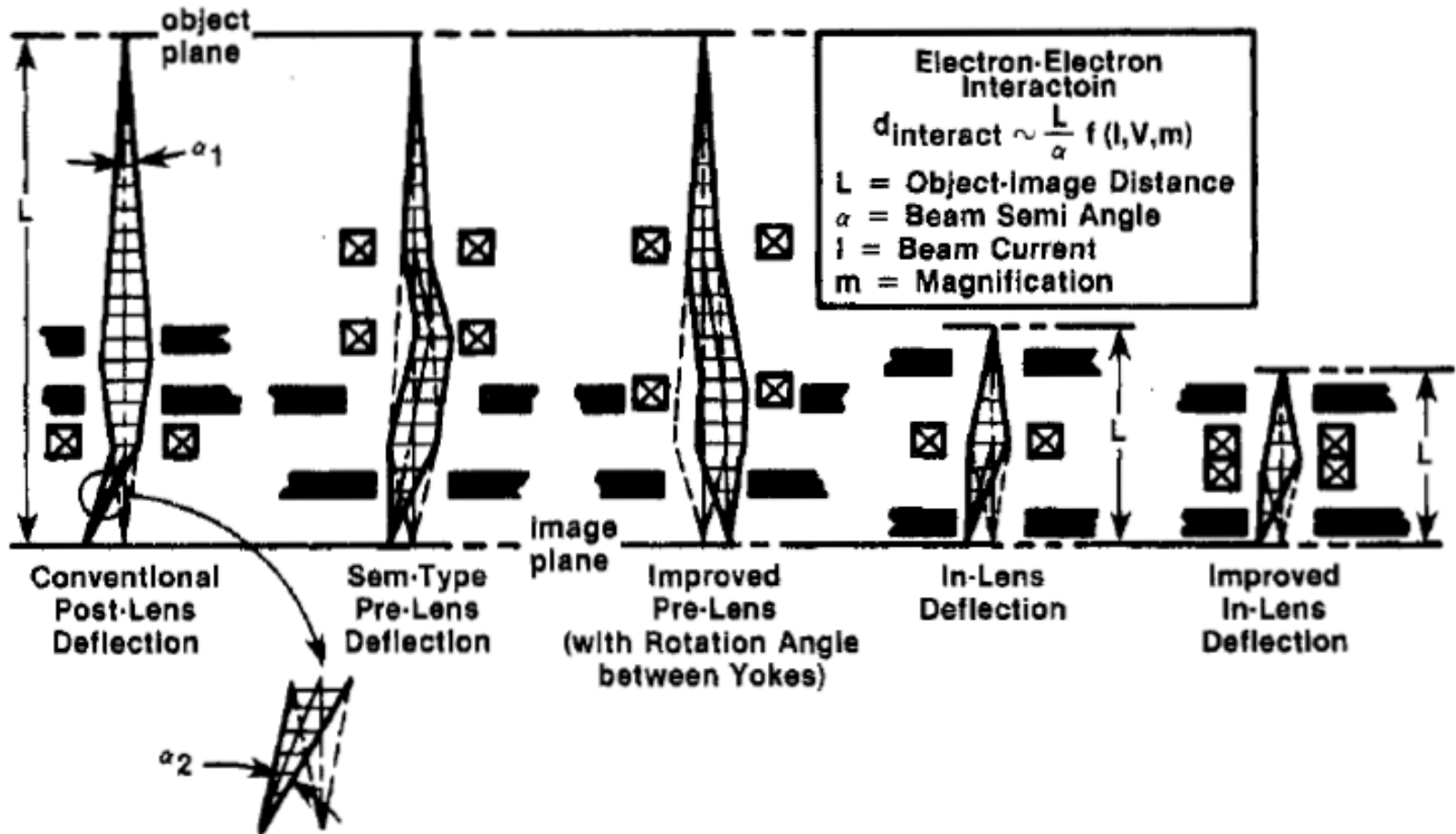
- Vistec SB35x DW
- 45nm SRAM patterns.

# Character Aperture Shaping





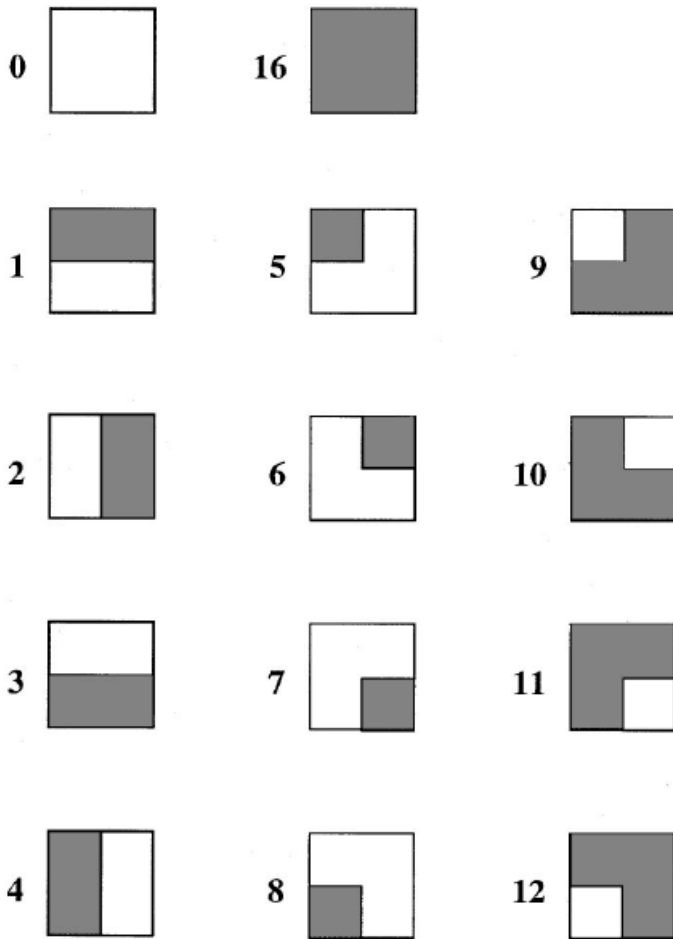
# Vertical Landing of focused e-beam



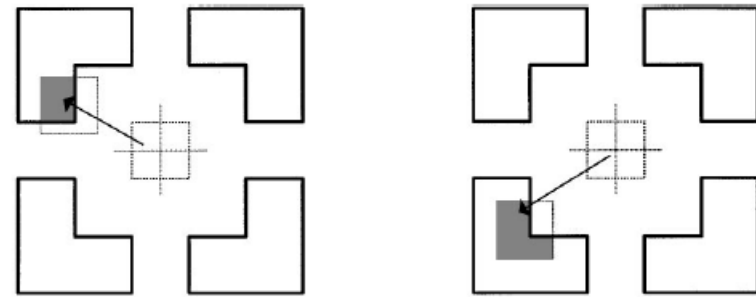
Reference: Hans C. Pfeiffer, *IEEE Transactions on Electron Devices*, ED-26, No. 4, p663, April 1979.

ECE 695 Nanometer Scale Patterning and Processing

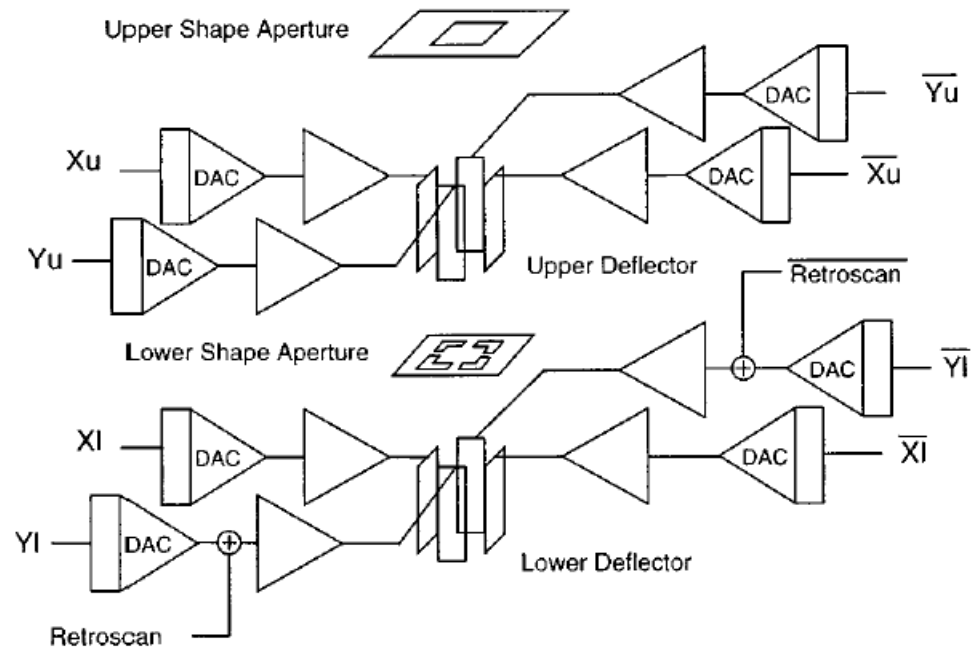
# Raster Shaped beam pattern generation



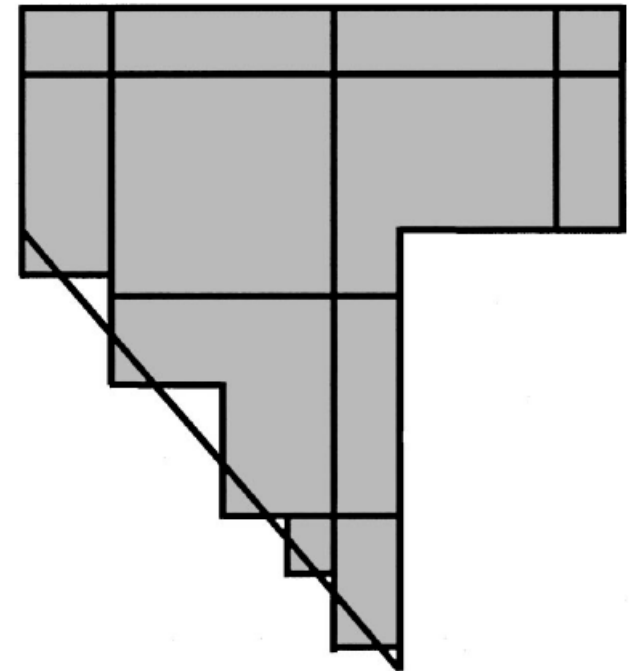
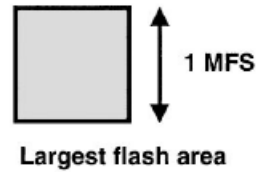
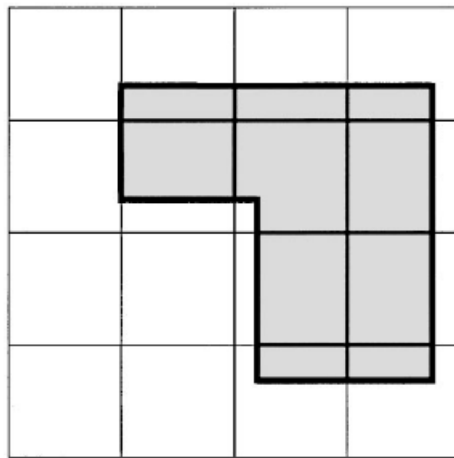
Shape classes



Formation of the Shapes via apertures



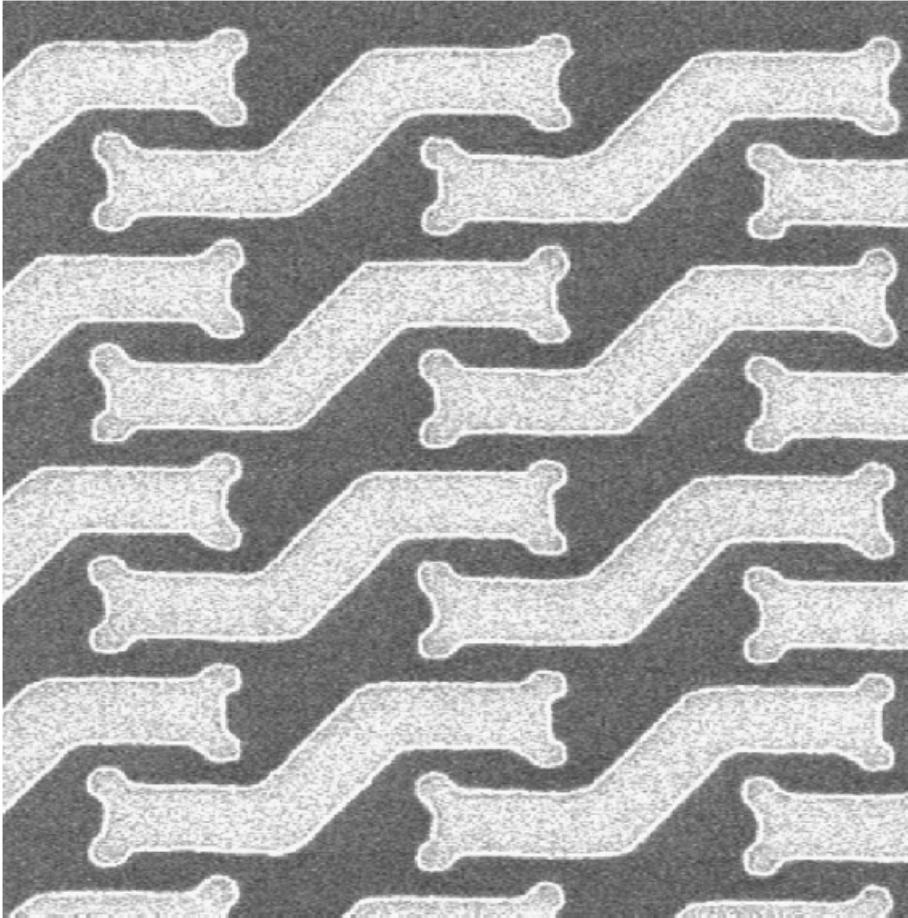
# Image formation



- Edges need not lie on gridlines
- Diagonal features are accommodated

# Results of Raster Shaped Beam

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500nm features with 200 nm  
OPC serifs

100 MHz flash rate

0.9  $\mu\text{A}$  current,

2200  $\text{A}/\text{cm}^2$  current density