Nanomaterials

Lecture 13: Nanoscale CMOS
"No Exponential is Forever … but We Can Delay ‘Forever’,”
Silicon-on-Insulator (SOI) Technology

Limitations of CMOS at the Nanoscale

(7) Operating speed

→ Speed is limited by charging time (i.e., $RC$ time constant).

→ Low-k minimizes $C$ and copper minimizes $R$ for interconnects.

→ Transistor speed is limited by carrier mobility

→ Carrier mobility is enhanced by intentionally introducing strain into the channel.
Transistor Strain Technologies

PMOS Strain Technology: Enhancing Hole Mobility Through Uniaxial Compressive Strain

Embedded geometry + compressive source/drain = Large uniaxial compressive strain

Strained PMOS Process Flow

• SiGe introduced late in the process flow ➔ source-drain

• Si Recess Etch + SiGe Epi deposition inserted post spacer formation to standard non-strained process

• Ease of implementation

NMOS Strain Technology: Enhancing Electron Mobility Through Uniaxial Tensile Strain

Highly tensile silicon nitride capping film

Limitations of CMOS at the Nanoscale

(8) Cost

→ Revenues increase by 16%/year

→ Factory cost increases by 19%/year

→ Plus, advanced lithographies (e-beam, ion beam, X-ray, EUV) are currently more expensive than DUV lithography

→ Costs are expected to rise more quickly than revenues in the future
“Moore’s Law” for CMOS Economics

FIGURE 3. A compilation of estimates of the required capital investment for a large semiconductor fabrication line taken from the SEMATECH[165] and the estimated worldwide semiconductor electronics (IC) sales taken from DataQuest, Makimoto[10] and Bois[11]. The year for introduction of a particular technology, denoted by the design rule, e.g. 0.35 μm, is plotted versus millions of U.S. dollars.
“No Exponential is Forever … but We Can Delay ‘Forever’,”
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## Start Dates for New Materials

<table>
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<tr>
<th>Process Name</th>
<th>P856</th>
<th>P858</th>
<th>Px60</th>
<th>P1262</th>
<th>P1264</th>
<th>P1266</th>
<th>P1268</th>
<th>P1270</th>
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<tr>
<td>1st Production</td>
<td>1997</td>
<td>1999</td>
<td>2001</td>
<td>2003</td>
<td>2005</td>
<td>2007</td>
<td>2009</td>
<td>2011</td>
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<tr>
<td>Process Generation</td>
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<td>0.13µm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32 nm</td>
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<td>Wafer Size (mm)</td>
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<td>300</td>
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<td>Inter-connect</td>
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<td>Al</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>?</td>
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<td>Channel</td>
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<td>Si</td>
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<td>Strained Si</td>
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<td>Gate dielectric</td>
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<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>High-k</td>
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<tr>
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<td>High-k</td>
<td>Metal</td>
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</tr>
</tbody>
</table>

*Introduction targeted at this time*

Subject to change

“No Exponential is Forever … but We Can Delay ‘Forever’,”
Fabricated Tri-Gate Transistor

Complete Depletion of Tri-Gate Transistor

Multi-Channel Tri-Gate Transistors Enable More Drive Current

Technology Generations to Come

Double the Density
Reduce Line Width by 0.7x

130nm → 90nm → 60nm → 45nm → 30nm → ?

2 or 3 years between generations

~10 ± 2 Years

“No Exponential is Forever … but We Can Delay ‘Forever’,”
Complete Depletion of Tri-Gate Transistor

Semiconductor Industry Roadmap