History of SiC Power Devices and a Vision for the Future

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March 30, 2017
Purdue University

Outline

1. Why Wide Band Gap Semiconductors for Power Switching
2. SiC IGBTs for 10-40 kV
3. A Short History of the Development over the Past 25 Years
4. My Initiatives at US Department of Energy - 40 mins

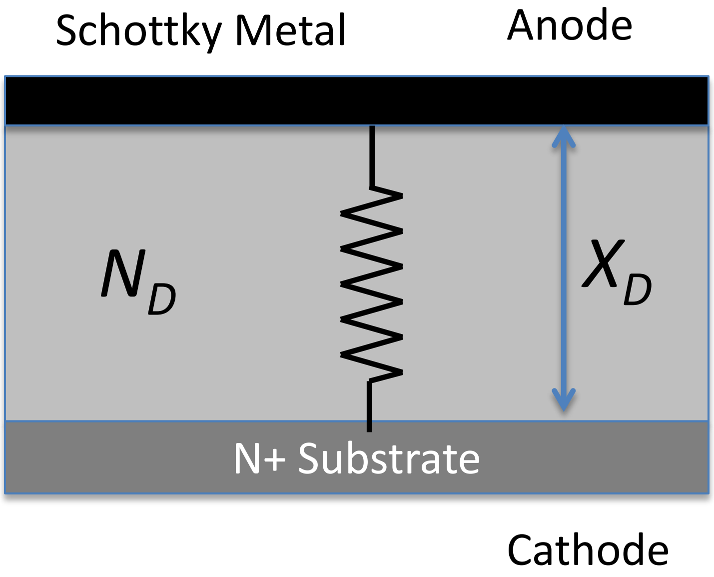
5. About My Vision for the Future
6. Research and Funding Opportunities – 15 mins

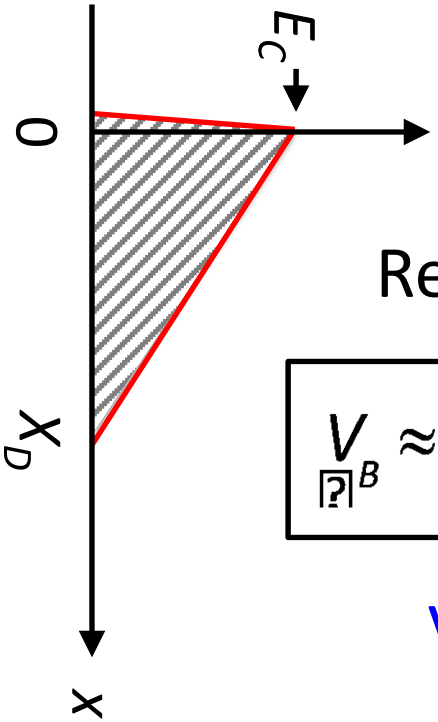
Why Wide Band Gap Semiconductors for Power Switching

Basic Material Properties

Property	Silicon	4H-SiC	GaN
E_G (eV)	1.12	3.26	3.4
μ_N (cm^2/Vs)	1400	1000	1200
E_C (MV/cm)	~ 0.4	~ 2.8	~ 3.0
Thermal Cond. (W/cm K)	1.3	3.3	1.3

7x of E_C(Si)





Reverse Bias

$$\boxed{V_B \approx \left(\varepsilon_S E_C^2\right) / \left(2qN_D\right)}$$

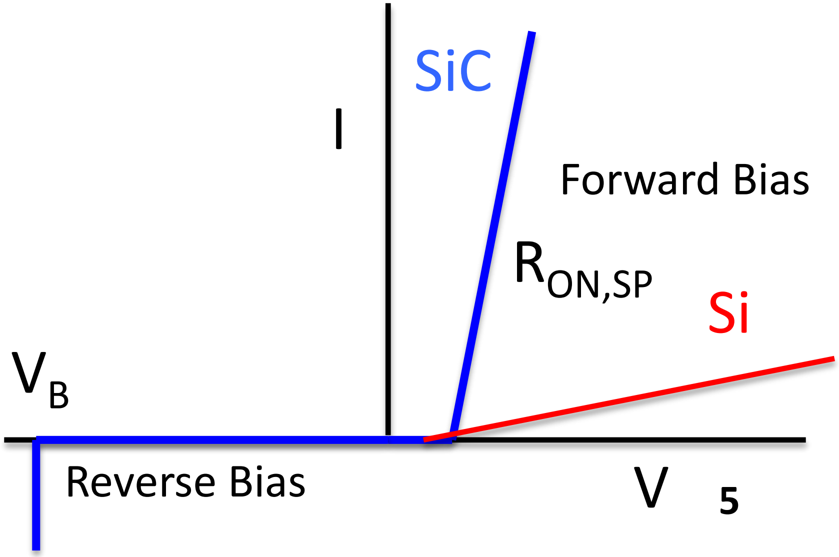
V_B = 600 V

Forward Bias

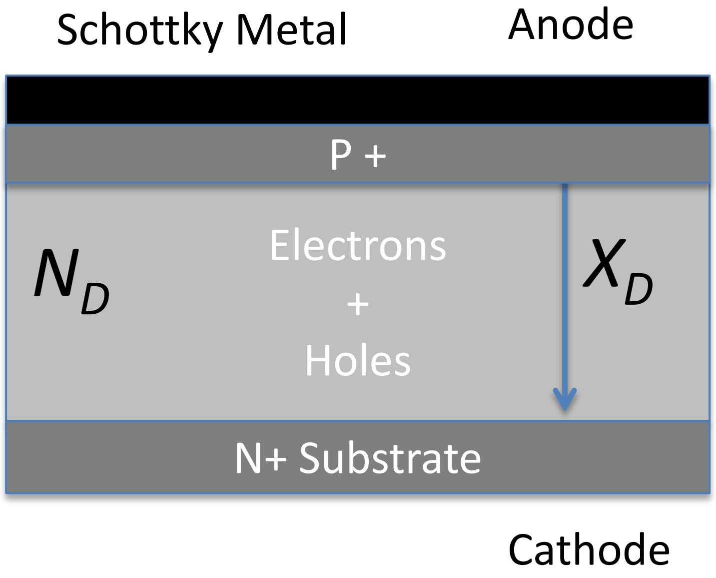
$$\boxed{R_{ON,SP} \triangleq R \bullet A = \frac{4V_B^2}{\mu_N \varepsilon_S E_C^3}}$$

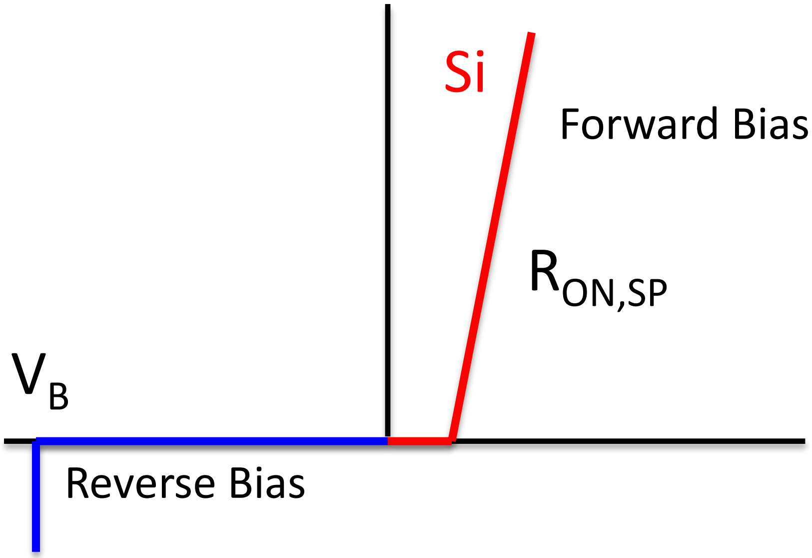
Si: $R_{on,SP}$ = 22 mohm-cm^2

SiC: $R_{on,SP}$ = 0.06 mohm-cm^2



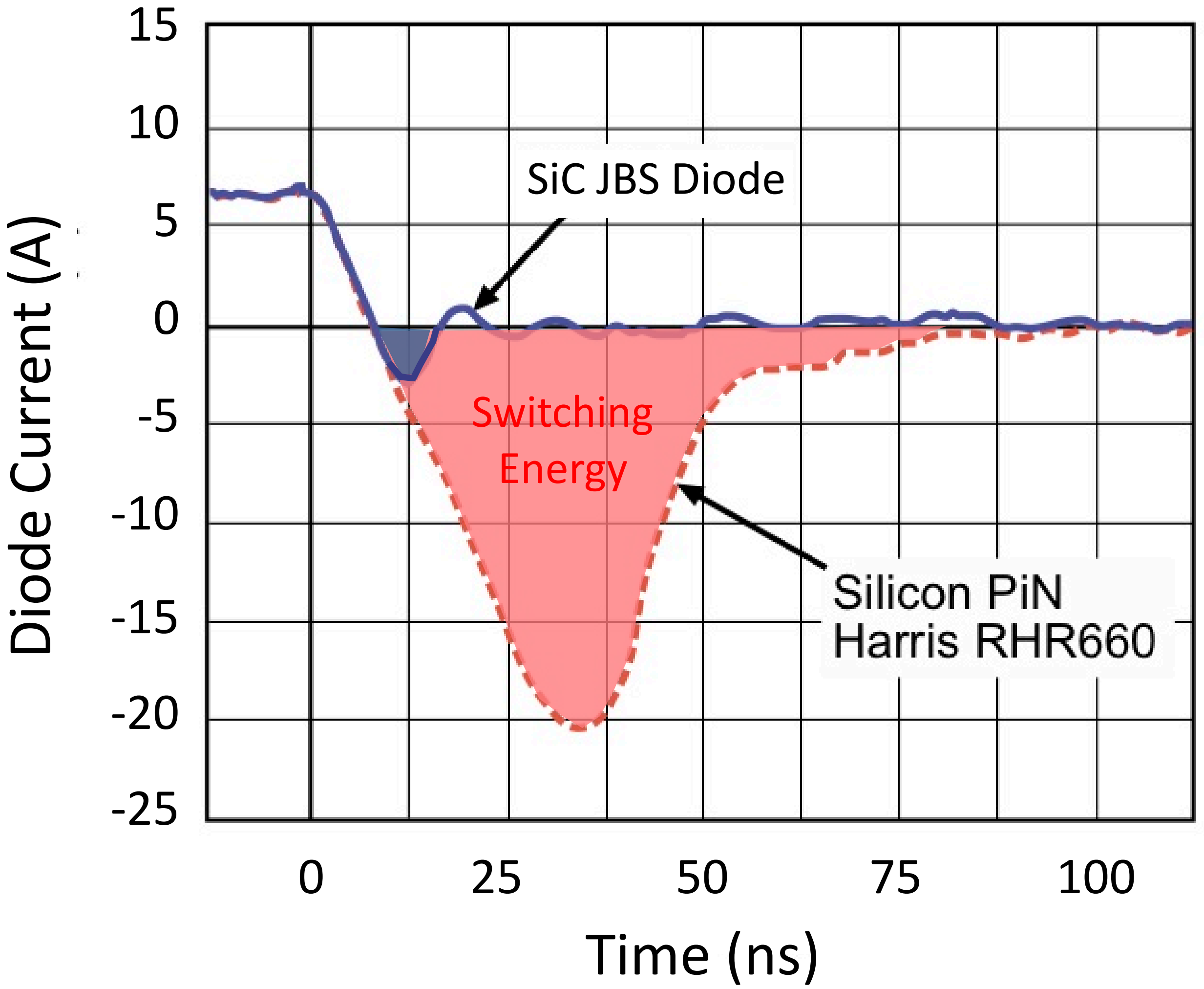
Si overcomes the high resistance issue with PiN Diode



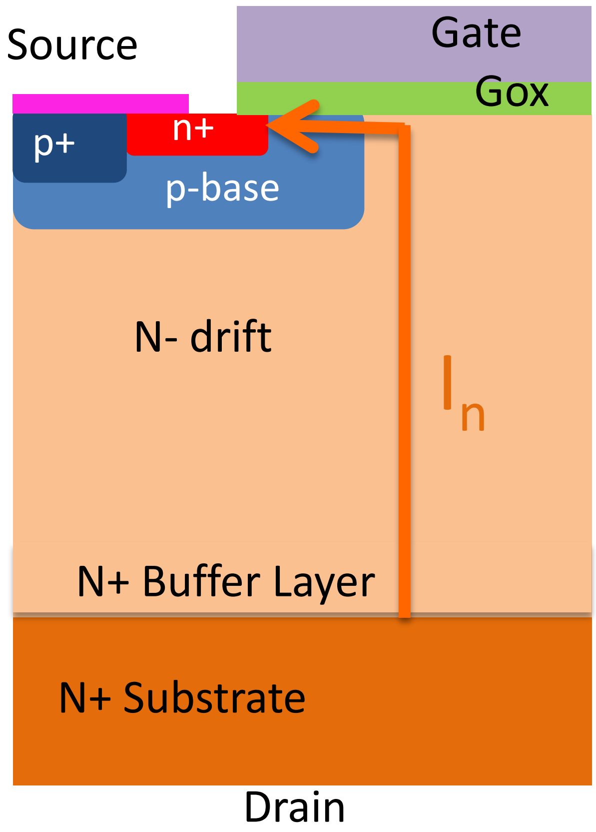


Minority carriers (holes) are stored in the drift layer which have to be removed during turn-off

Diode Turn-Off Transient



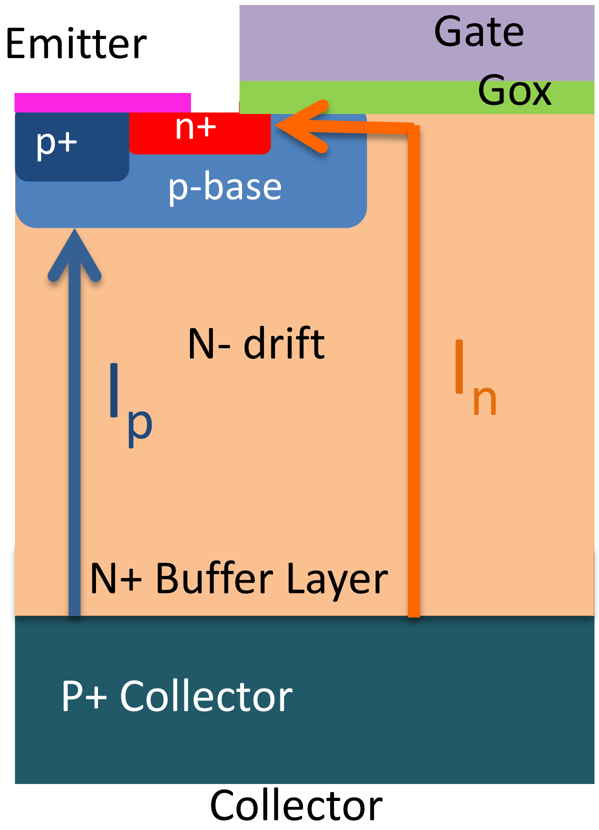
MOSFET



Si: 100 V - 600 V

SiC: 600 V – 10 kV

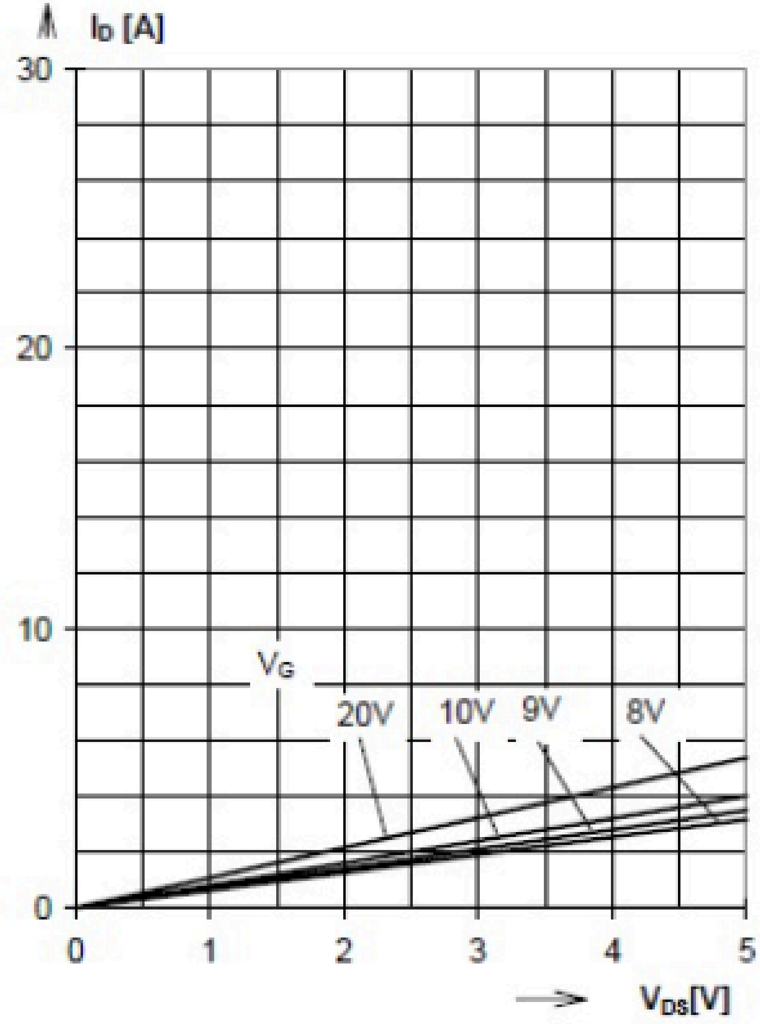
n-Channel IGBT



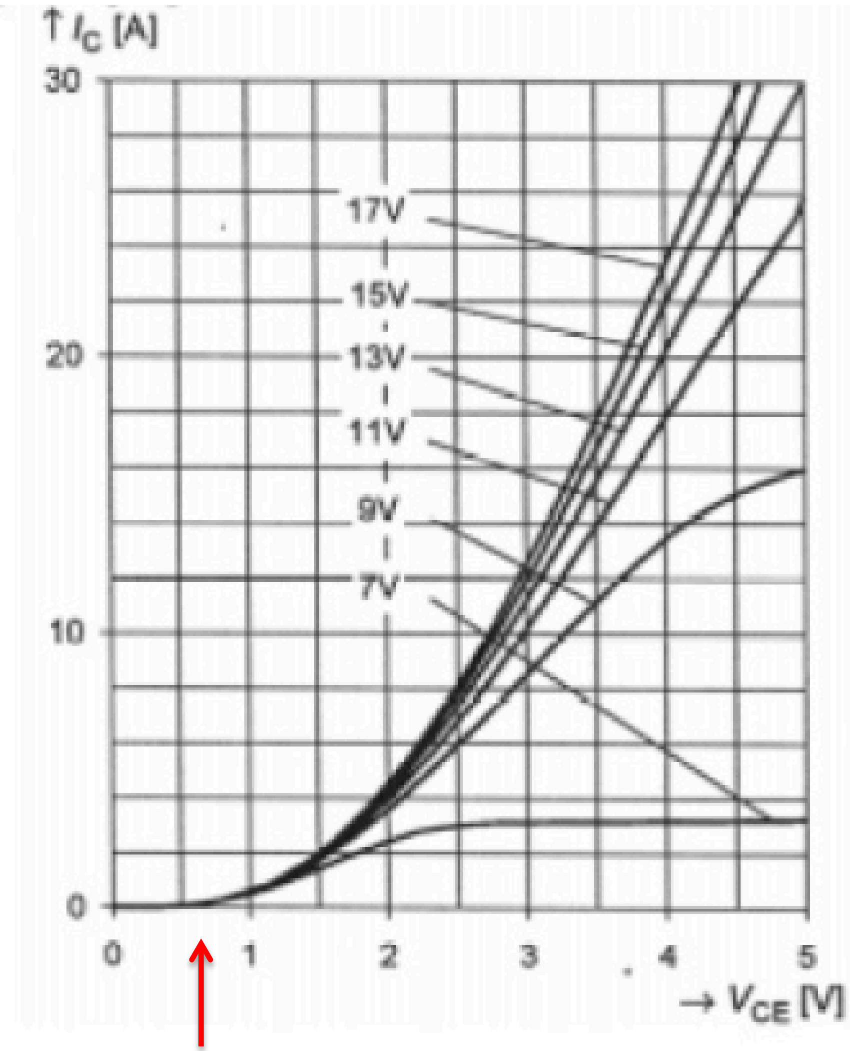
Si: 600 V – 6.5 kV

SiC: 10 kV – 40 kV

1 kV Si MOSFET

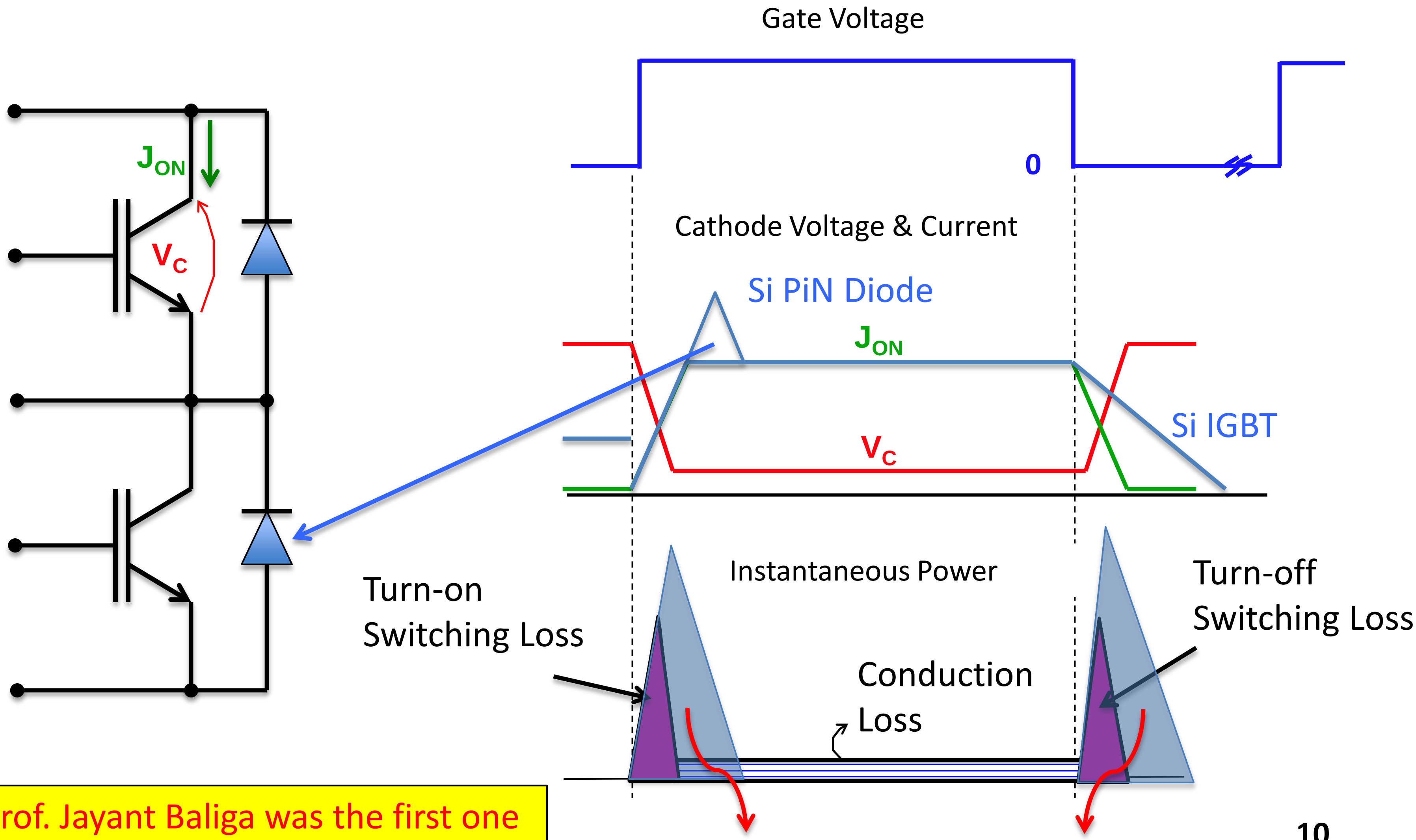


1 kV Si IGBT



1 junction drop

Si PiN diode, IGBT => SiC Schottky diode, MOSFET results in 75% reduction in total losses, 2-3% higher efficiency



Much worse at high temperatures and High voltage

Prof. Jayant Baliga was the first one to point this out.

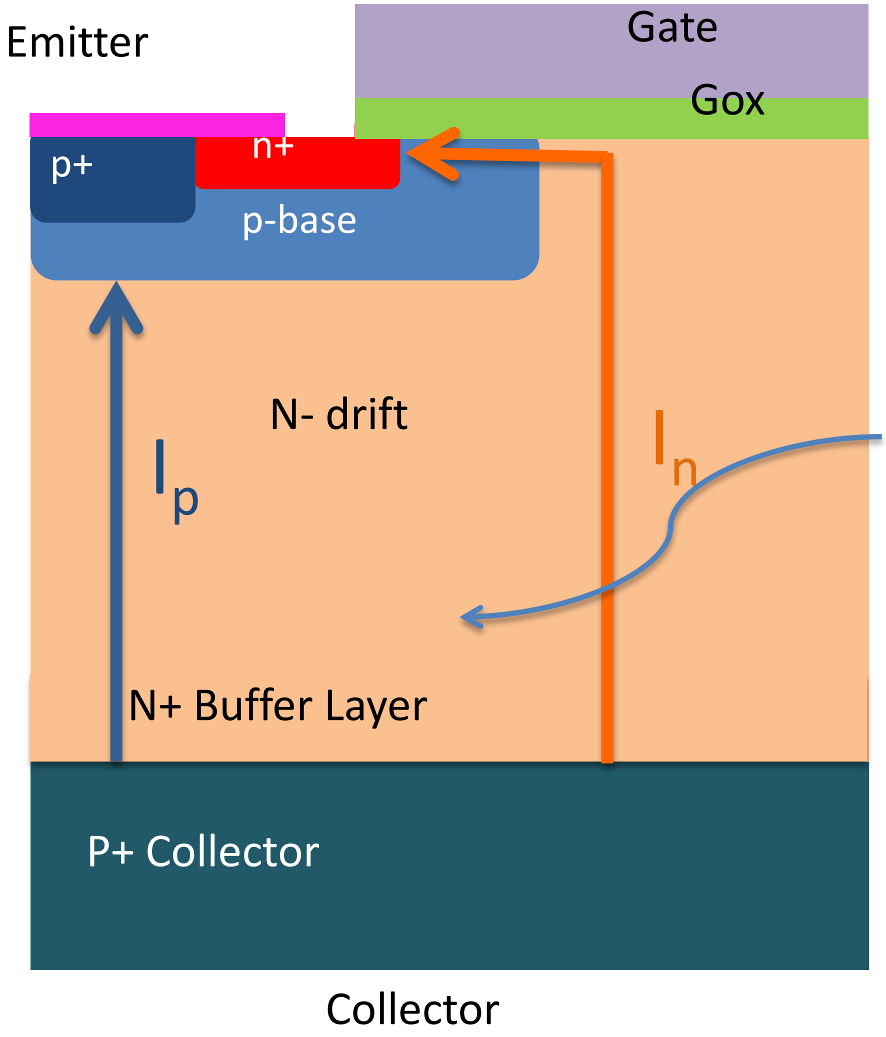
Silicon PiN can be replaced by SiC SBD up to ~10 kV

Silicon IGBT/GTO can be replaced by SiC MOSFET up to ~10kV

SiC IGBTs for 10 – 40 kV

SiC IGBT for 10 – 40 kV Applications

n-Channel IGBT



Ambipolar Diffusion Equation

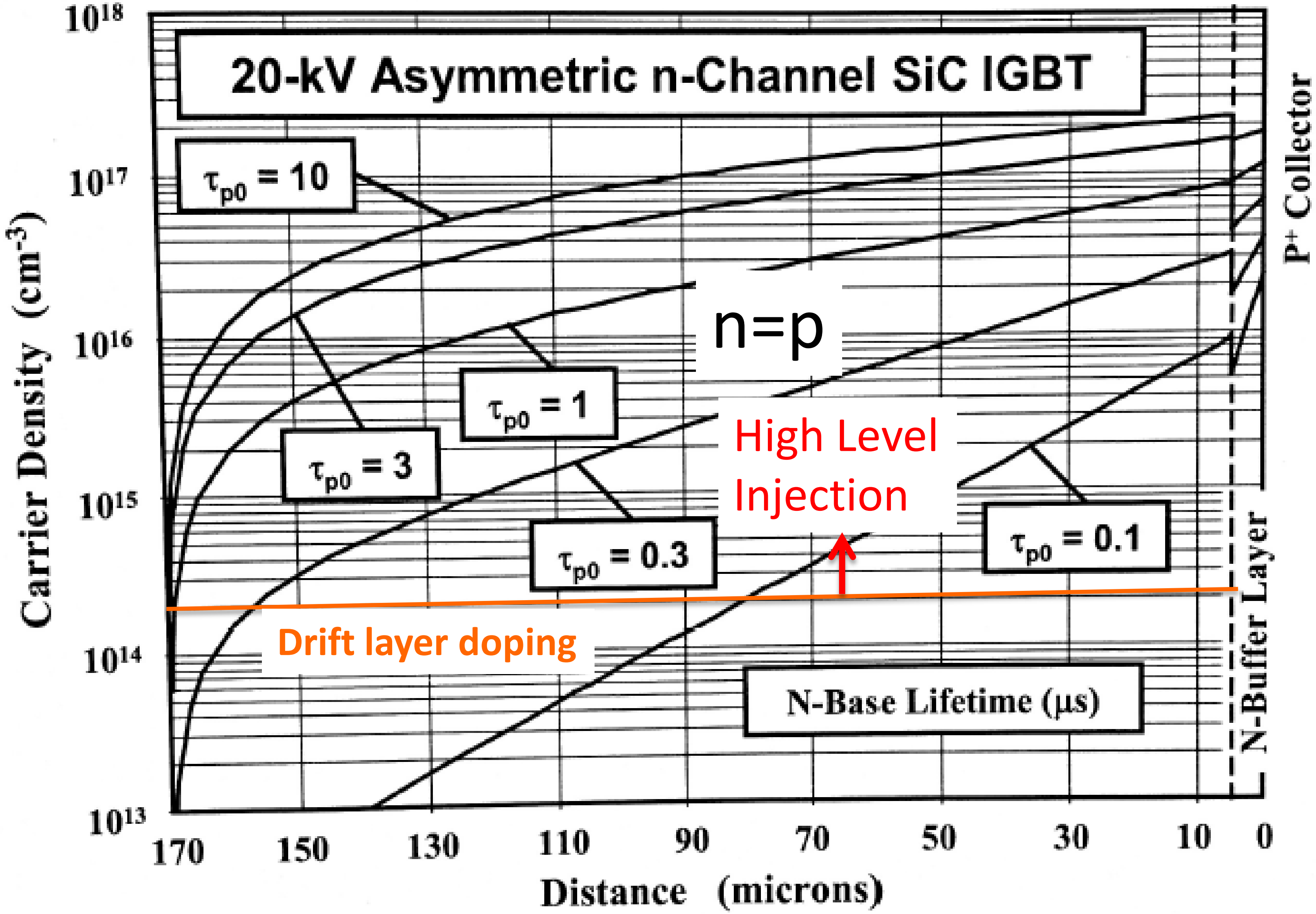
$$\frac{\partial^2 p(x)}{\partial x^2} = \frac{p(x)}{L^2} + \frac{1}{D}\frac{\partial p(x)}{\partial t}$$

$$L = \sqrt{D\tau_{HL}} \qquad \tau_{HL} \approx 2\tau_{p0}$$

ambipolar diffusion coefficient

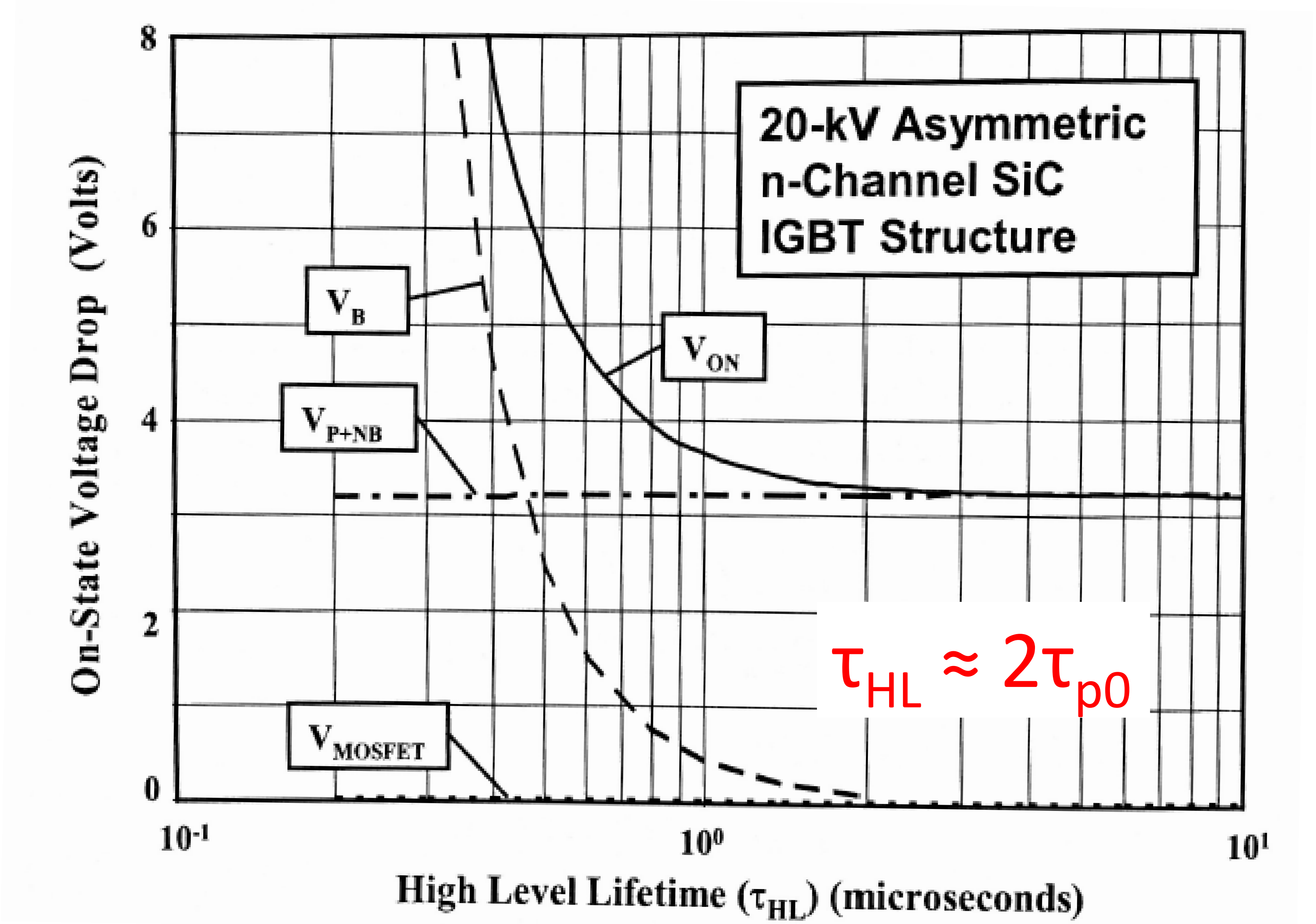
$$D = \frac{nq\mu_n D_p + pq\mu_p D_n}{nq\mu_n + pq\mu_p} .$$

Analytical Solution of Ambipolar Diffusion Equation



B Jayant Baliga, “Gallium Nitride and Silicon Carbide Power Devices,” p. 477, World Scientific, 2017

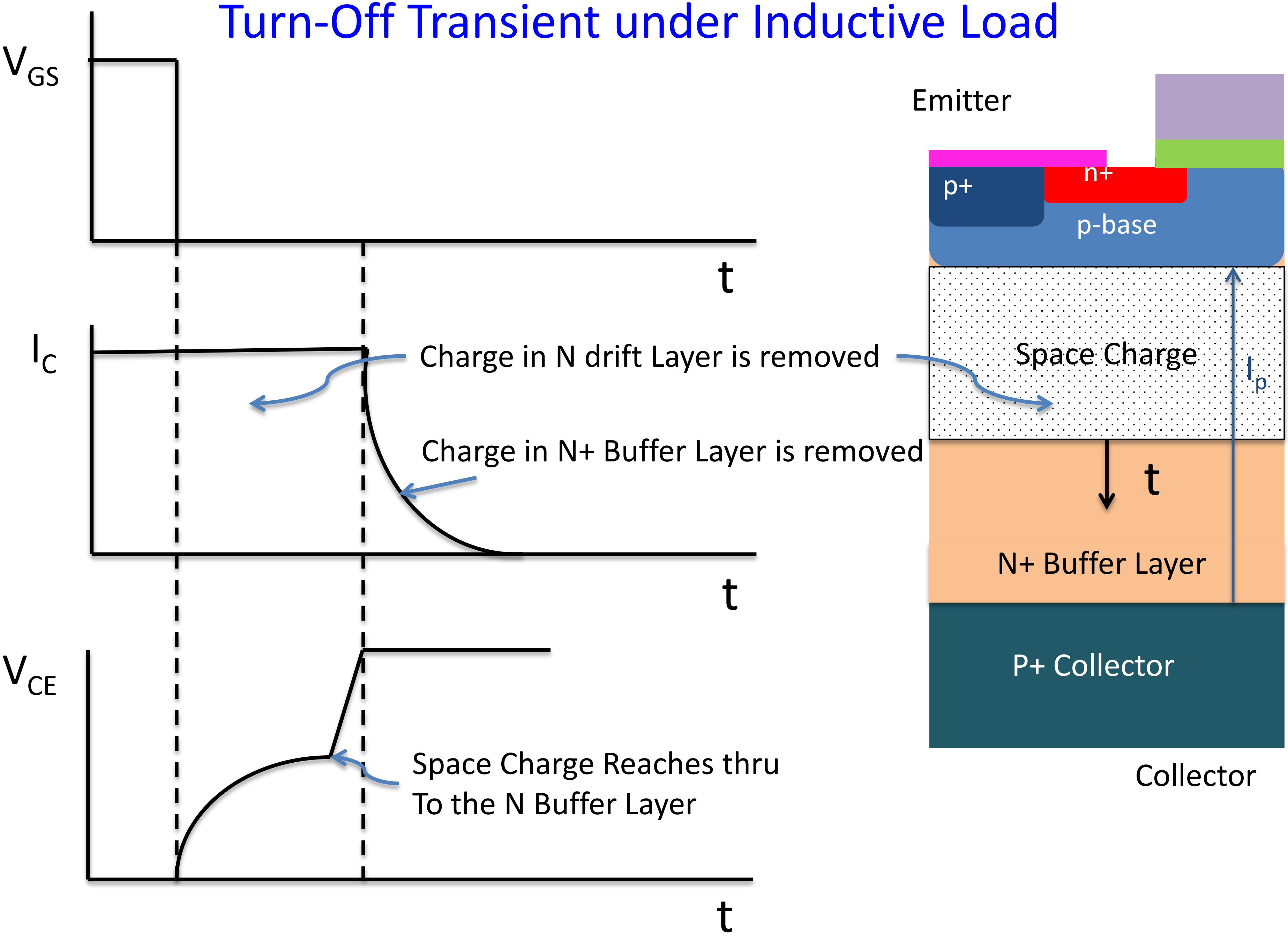
On-State Voltage Drop Increases with Reducing Lifetime



$$\tau_{HL} \approx 2\tau_{p0}$$

B Jayant Baliga, "Gallium Nitride and Silicon Carbide Power Devices," p. 480, World Scientific, 2017

Turn-Off Transient under Inductive Load

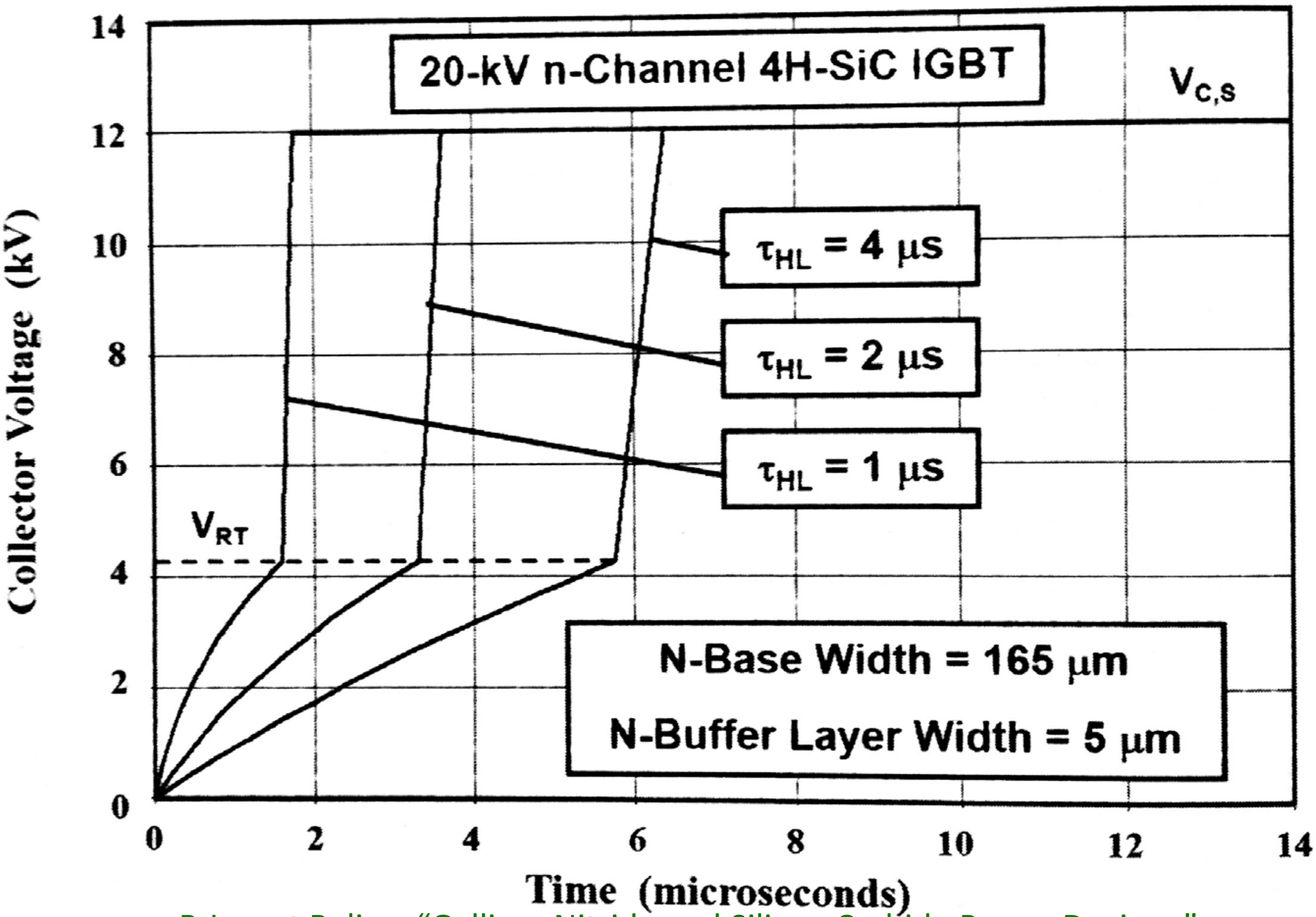


Charge in N drift Layer is removed

Charge in N+ Buffer Layer is removed

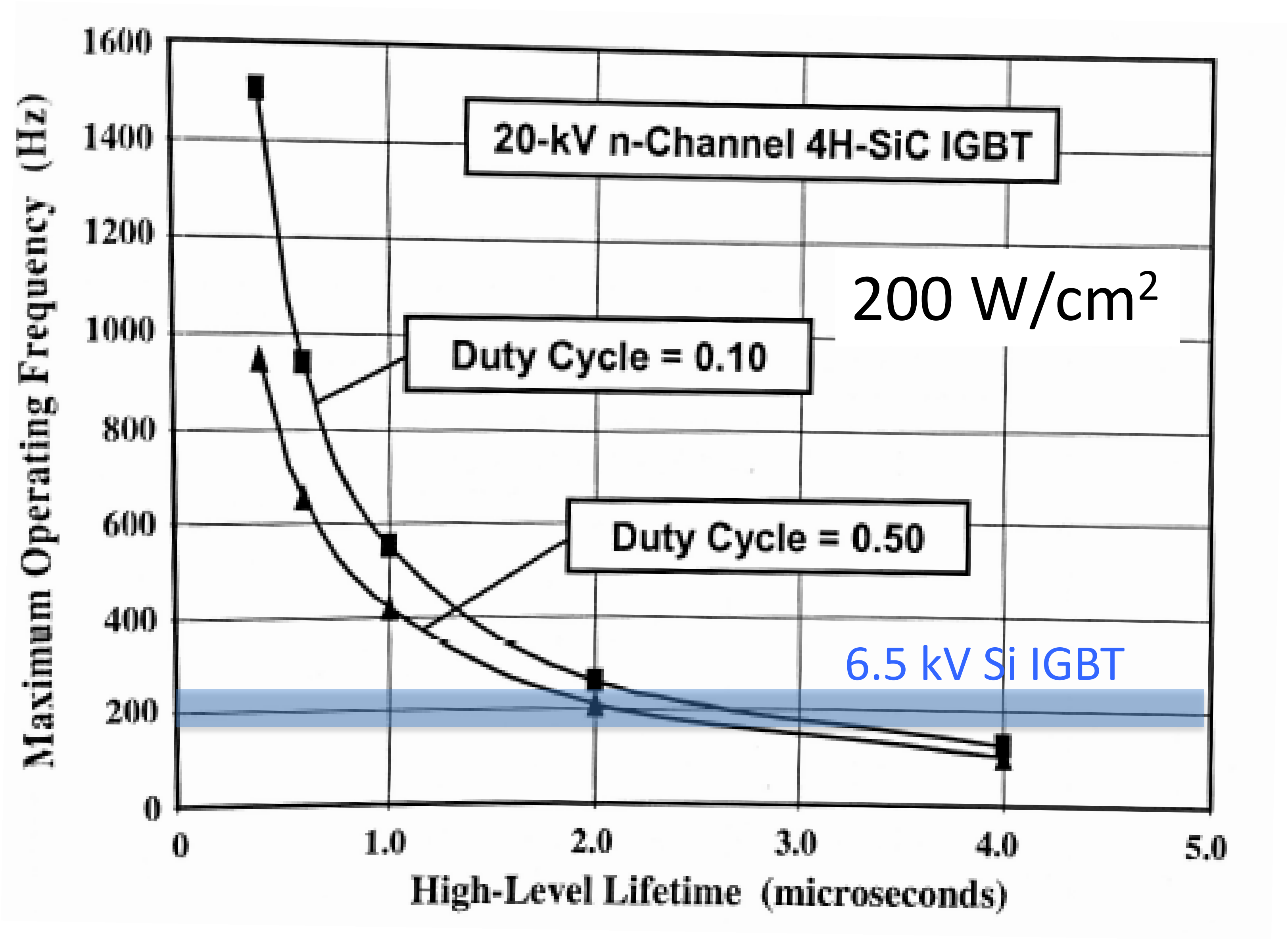
Space Charge Reaches thru
To the N Buffer Layer

Switching Transients become faster with Reducing Lifetime



B Jayant Baliga, “Gallium Nitride and Silicon Carbide Power Devices,” p. 494, World Scientific, 2017

Maximum Operating frequency for 20 kV n-Channel SiC IGBT

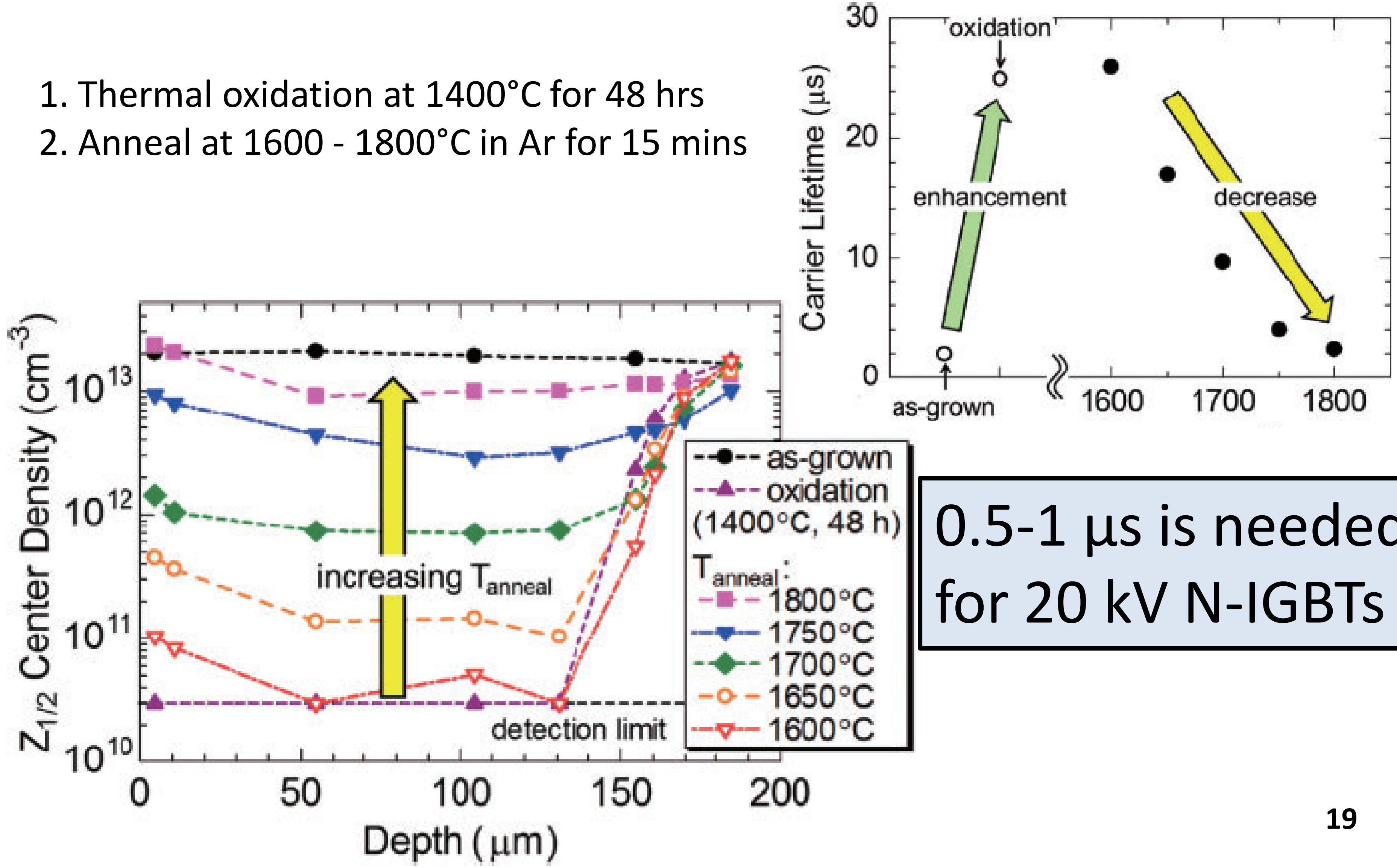


B Jayant Baliga, “Gallium Nitride and Silicon Carbide Power Devices,” p. 494, World Scientific, 2017

Control of carrier lifetime of thick n-type 4H-SiC epilayers by high-temperature Ar annealing

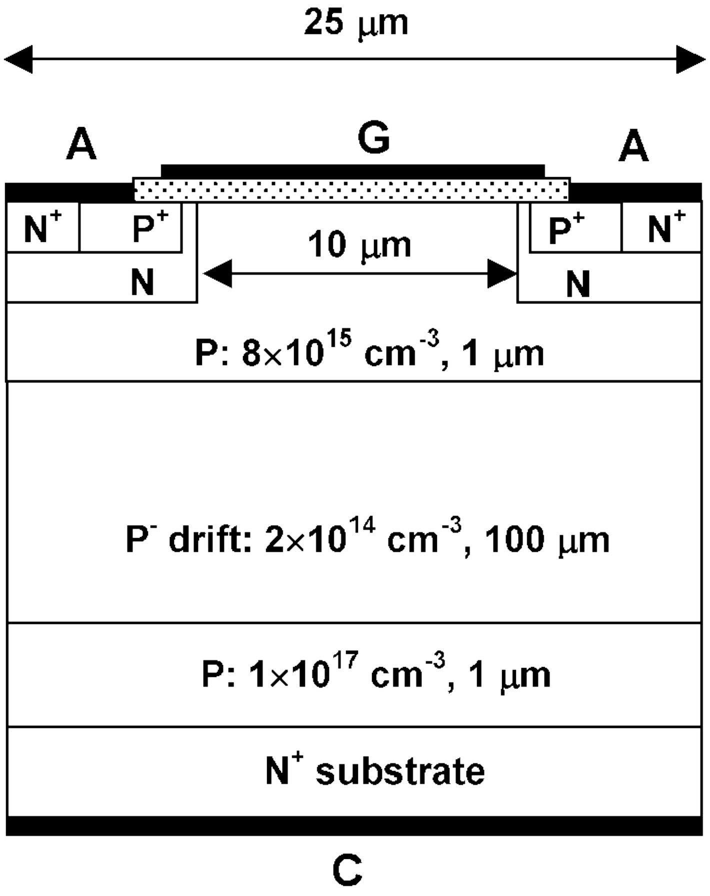
Eiji Saito*, Jun Suda, and Tsunenobu Kimoto, Applied Physics Express 9, 061303 (2016)

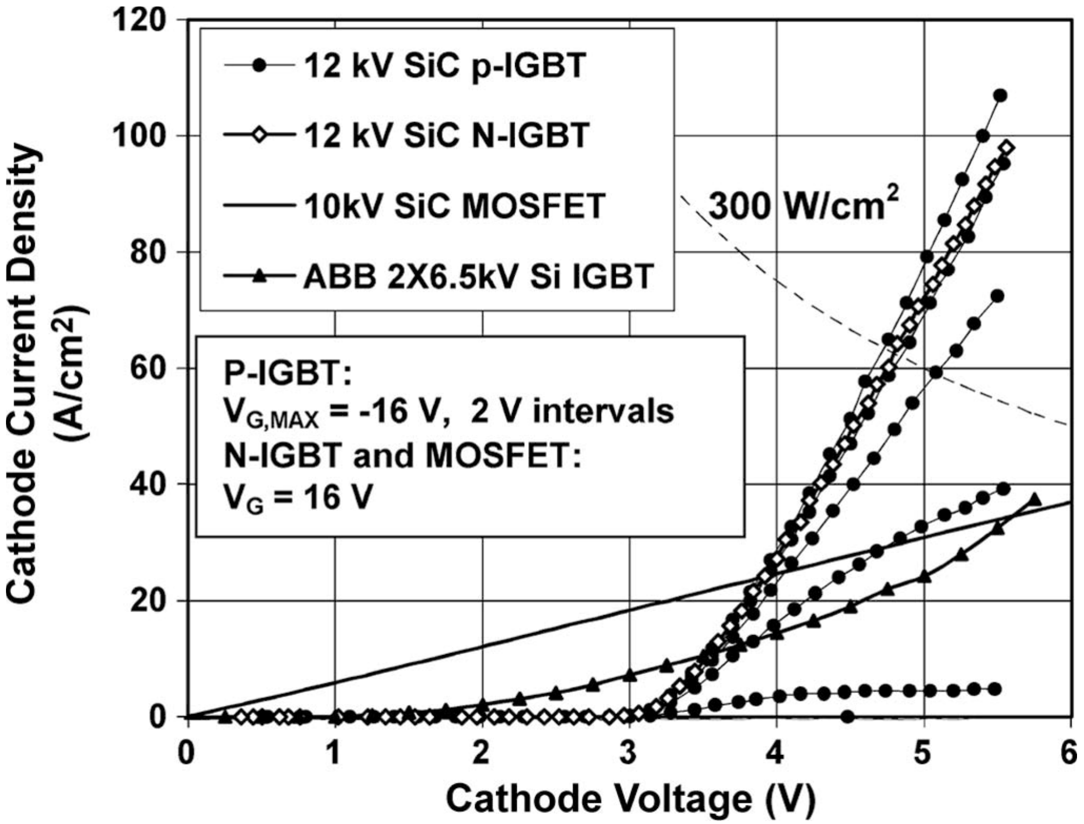
1. Thermal oxidation at 1400°C for 48 hrs
2. Anneal at 1600 - 1800°C in Ar for 15 mins



0.5-1 µs is needed for 20 kV N-IGBTs

We developed the First 12 kV p-IGBT in 2008





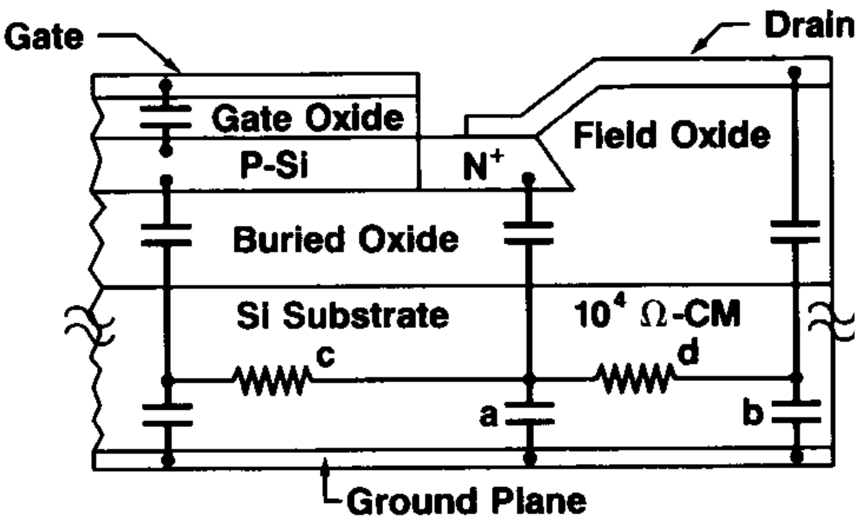
Qingchun Zhang, Mrinal Das, Joe Sumakeris, Robert Callanan and **Anant Agarwal**, “12-kV p-Channel IGBTs with Low On-Resistance in 4H-SiC,” ***IEEE Electron Device Letters***, Vol. 29, No. 9, September 2008. pp. 1027-1029.

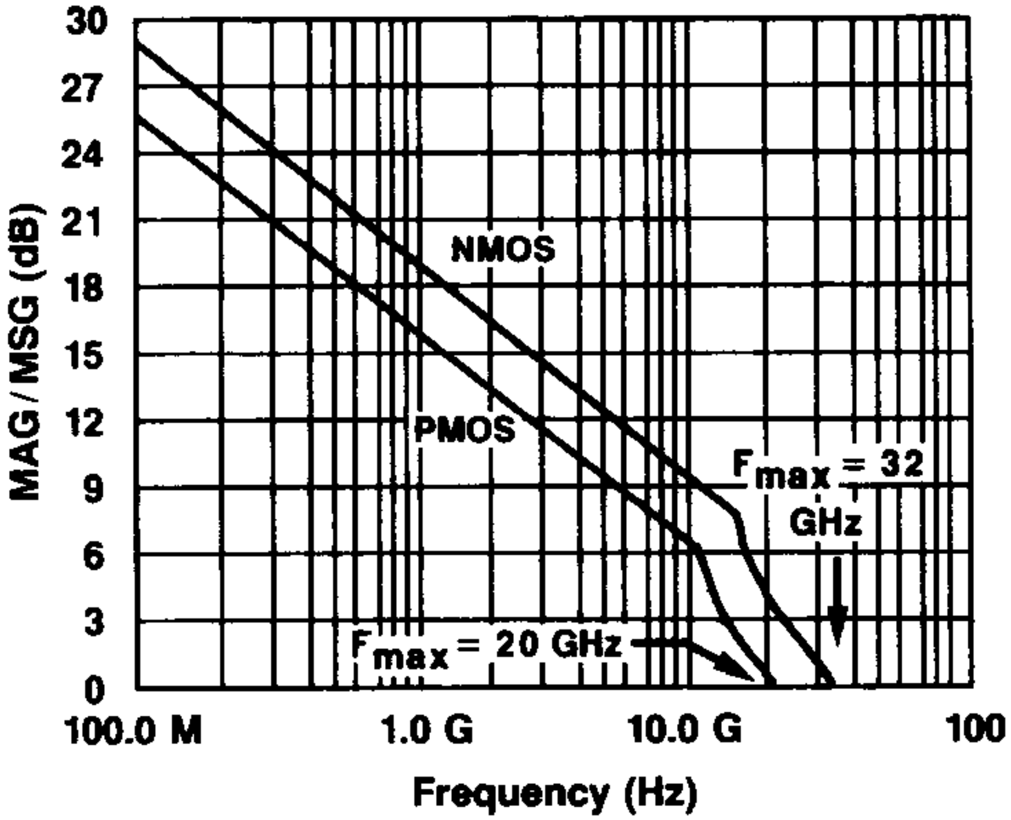
N-IGBTs are preferred for lower VF, faster speed and lifetime control in N- drift layer

The Last 25 Years

MICROX^{TM}-An All-Silicon Technology for Monolithic Microwave Integrated Circuits

Maurice H. Hanes, Anant K. Agarwal, T. W. O'Keeffe, H. M. Hobgood, John R. Szedon, T. J. Smith, R. R. Siergiej, Paul G. McMullin, H. C. Nathanson, Michael C. Driver and R. Noel Thomas IEEE Electron Device Letters, VOL. 14, p.219, 1993.





Si Thickness = 120 nm

P-doping = 2x10^{17} cm^{-3}

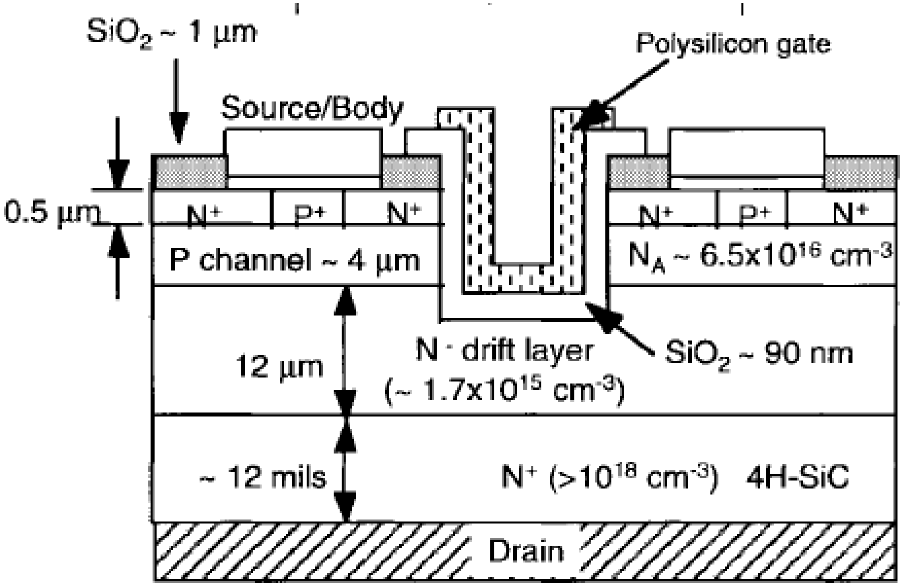
L=0.35 µm, W= 4x50 µm

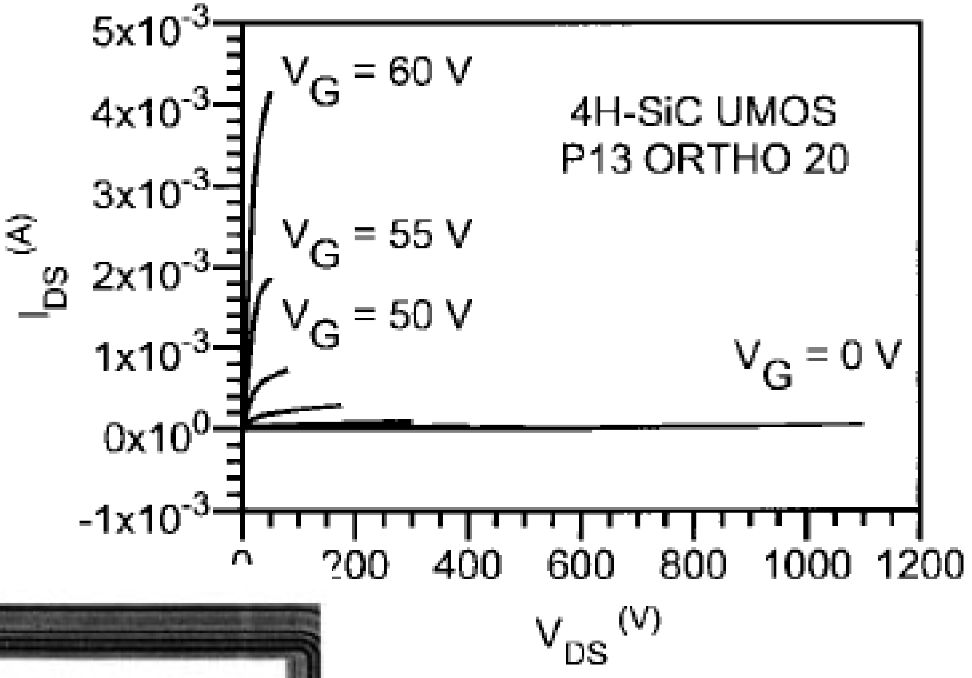
Polysilicon Gates metallized

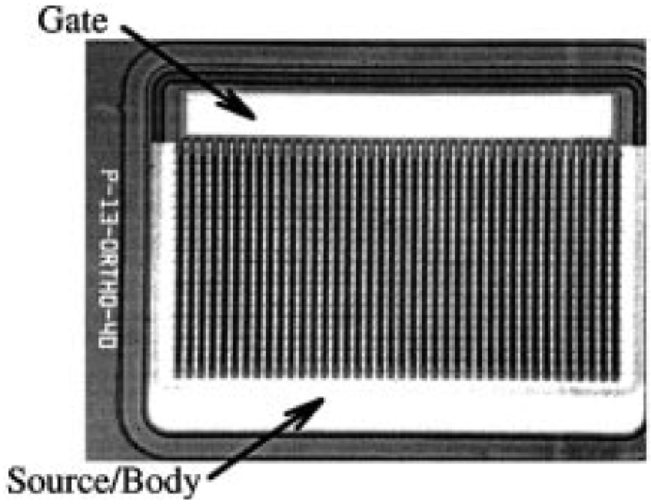
1.1 kV 4H-SiC Power UMOSFET’s

A. K. Agarwal, J. B. Casady, L. B. Rowland, W. F. Valek, M. H. White, and C. D. Brandt

IEEE Electron Device Letters, Vol. 18, No. 12, pp. 586-588, December 1997

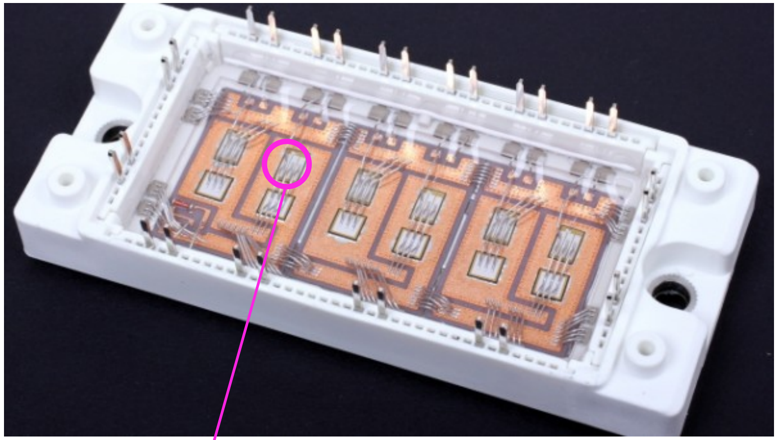






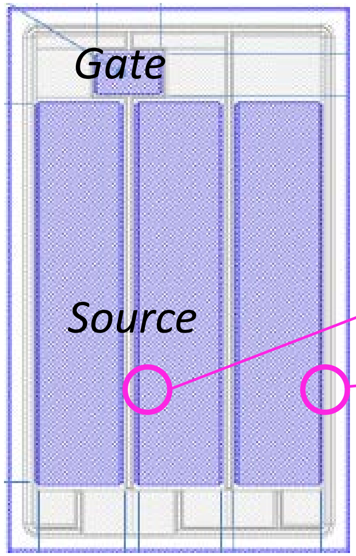
Design of the Power Device

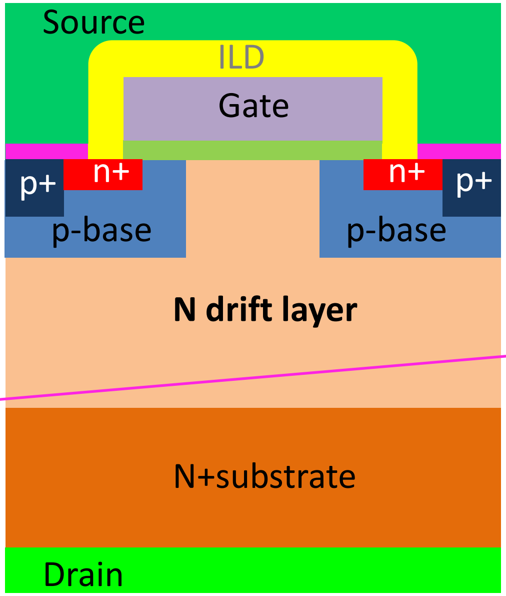
1200V 20A SiC Six-pack Power Module (Cree)

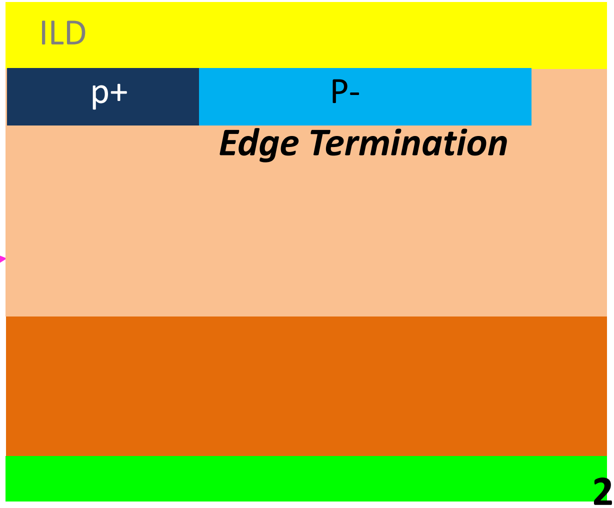


- **Design of the drift layer**: thickness, and doping concentration of drift layer for targeted BV
- **Edge termination design**: JTE or Rings
- **Optimization of the cell**: to reduce the on-resistance (by simulation)
- **Layout**: determine # of fingers, size of cell area, place edge termination structure
- **Fabrication, dicing, packaging**

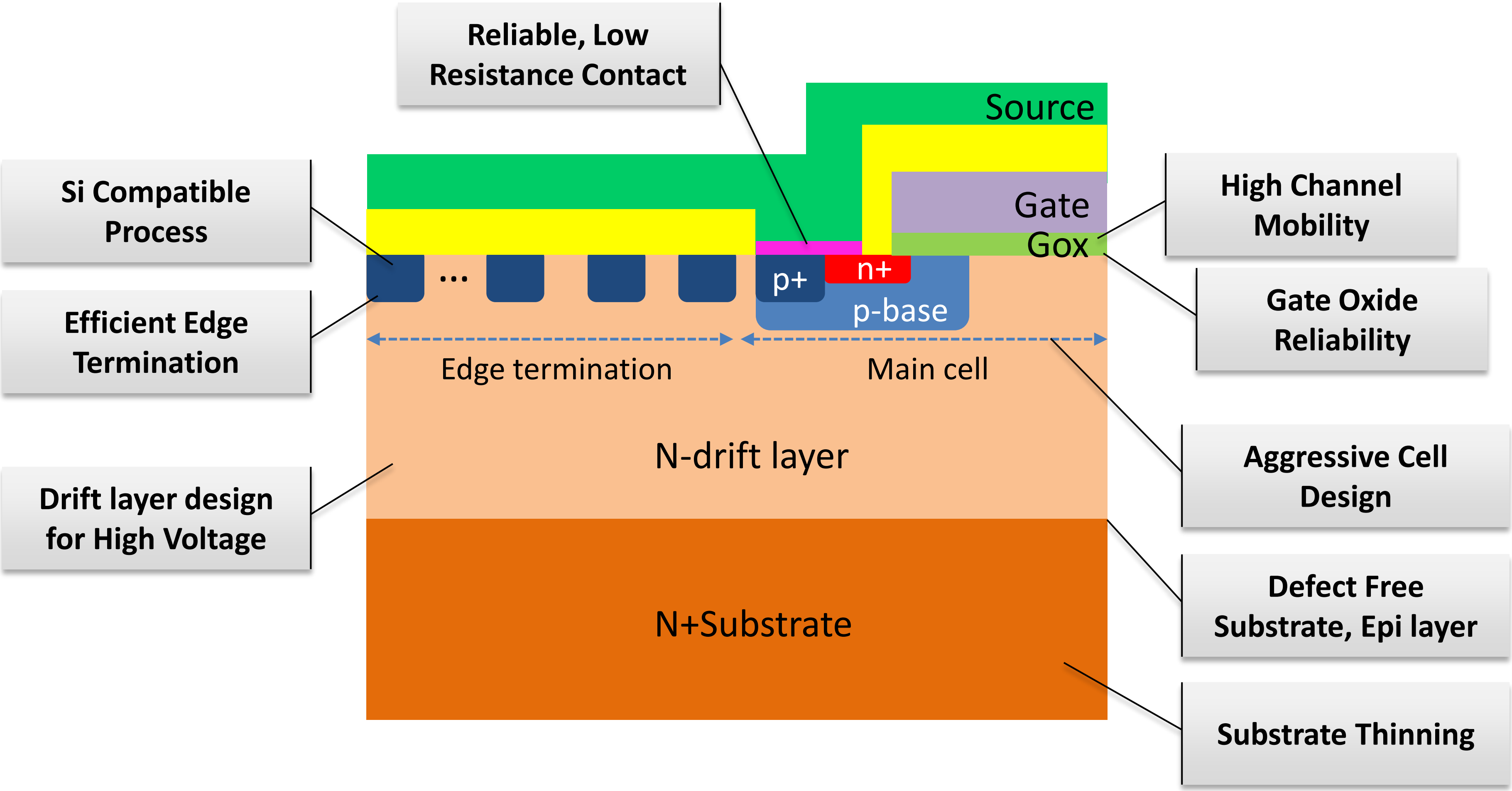
CPM2-1200-0025B Layout view



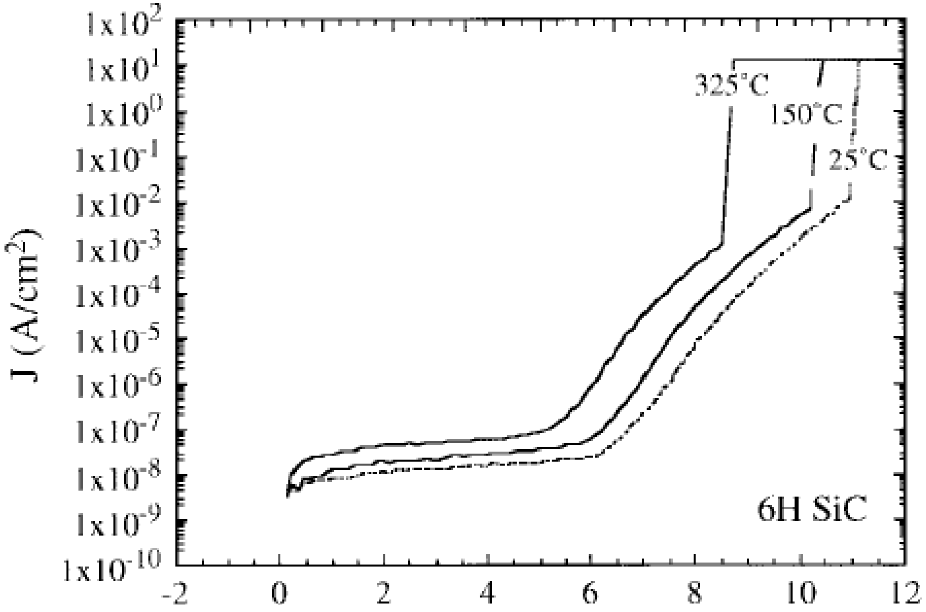


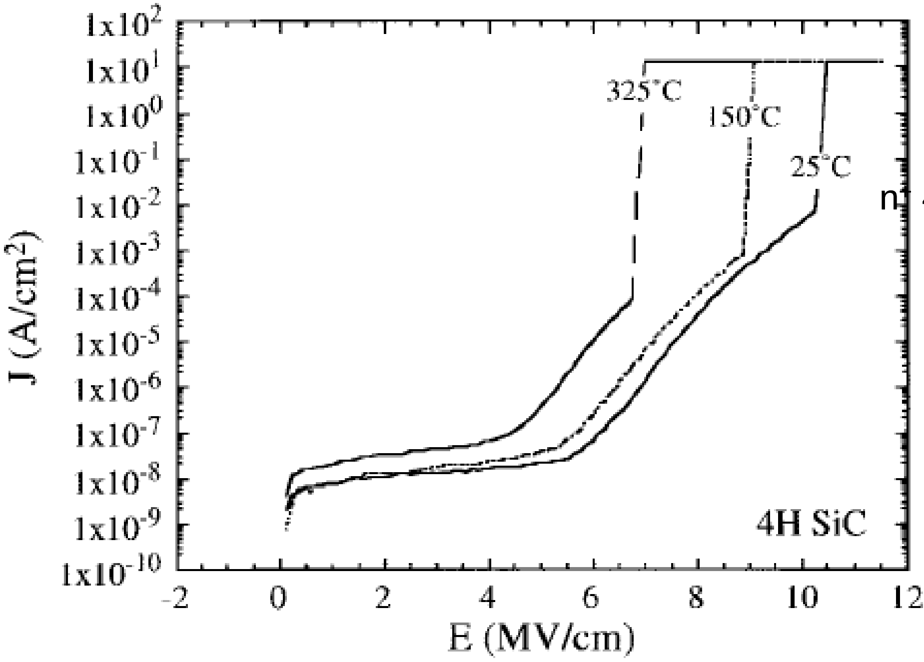


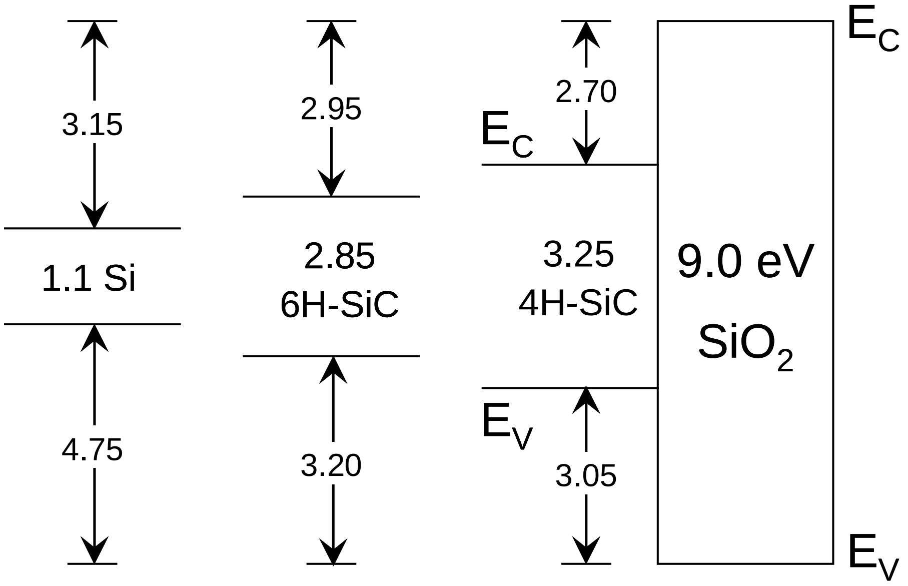
SiC MOSFET


Reliable, Low Resistance Contact
Si Compatible Process
Efficient Edge Termination
Drift layer design for High Voltage
Source
Gate
Gox
p+
n+
p-base
...
Edge termination
Main cell
N-drift layer
N+Substrate
High Channel Mobility
Gate Oxide Reliability
Aggressive Cell Design
Defect Free Substrate, Epi layer
Substrate Thinning

A. K. Agarwal, etal. IEEE Electron Device Letters, vol. 18, No. 12, pp. 592-594, 1997.







3.15

1.1 Si

4.75

2.95

2.85
6H-SiC

3.20

E_C

2.70

3.25
4H-SiC

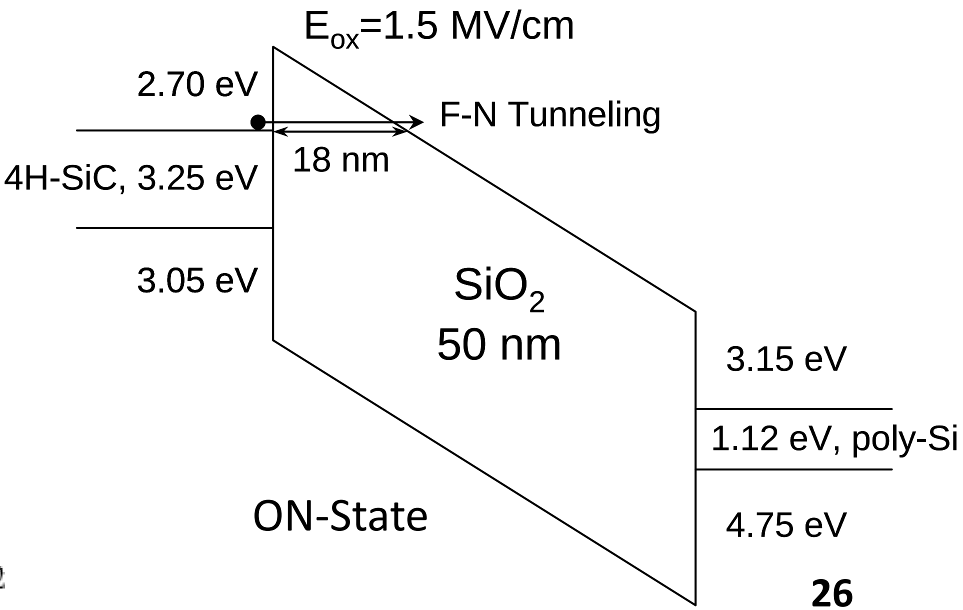
E_V

3.05

9.0 eV
SiO$_2$

E_C

E_V



E_{ox}=1.5 MV/cm

2.70 eV

F-N Tunneling

18 nm

n$^+$ 4H-SiC, 3.25 eV

3.05 eV

SiO$_2$
50 nm

3.15 eV

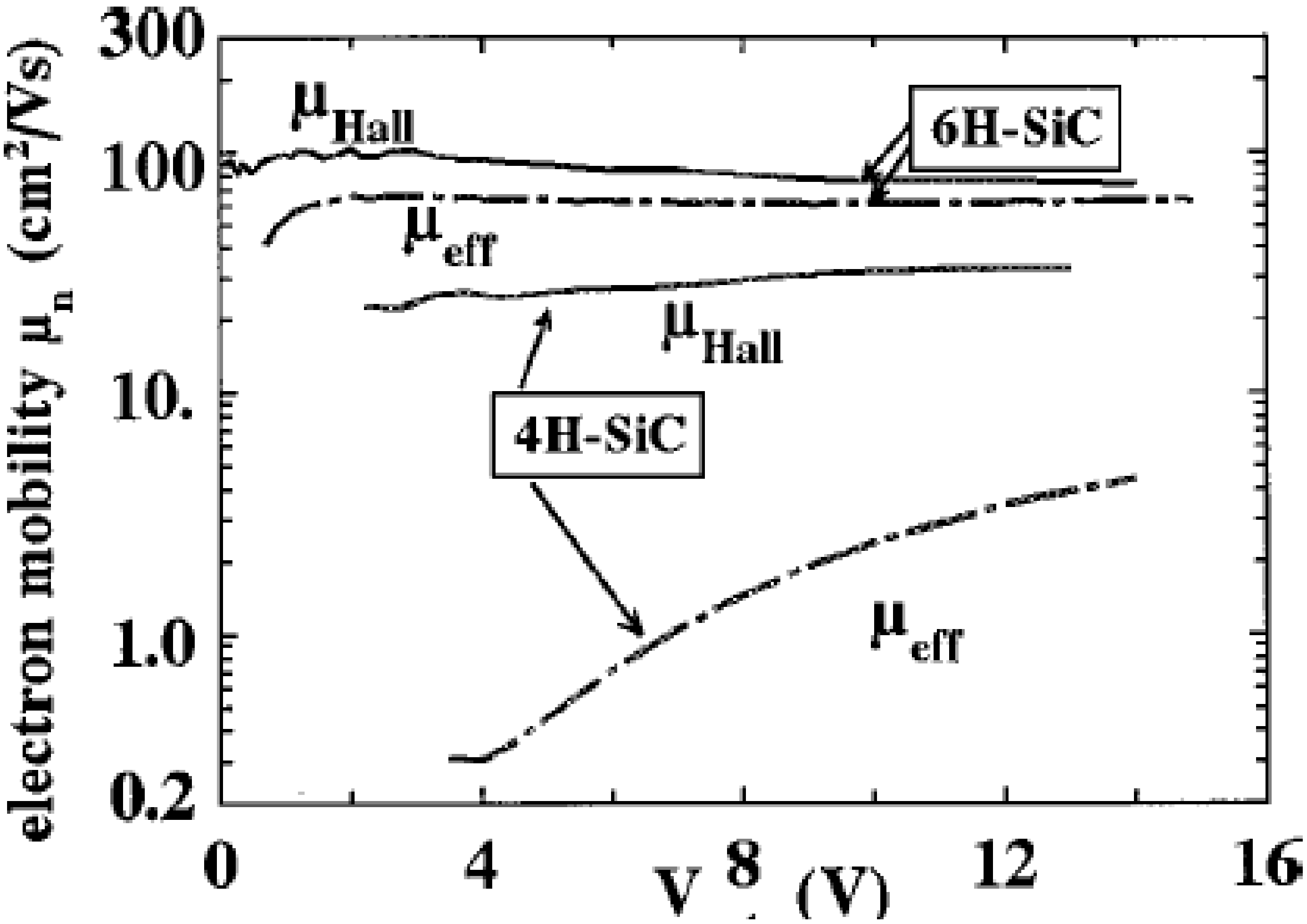
1.12 eV, poly-Si

4.75 eV

ON-State

Hall mobility and free electron density at the SiC/SiO$_2$ interface in 4H–SiC

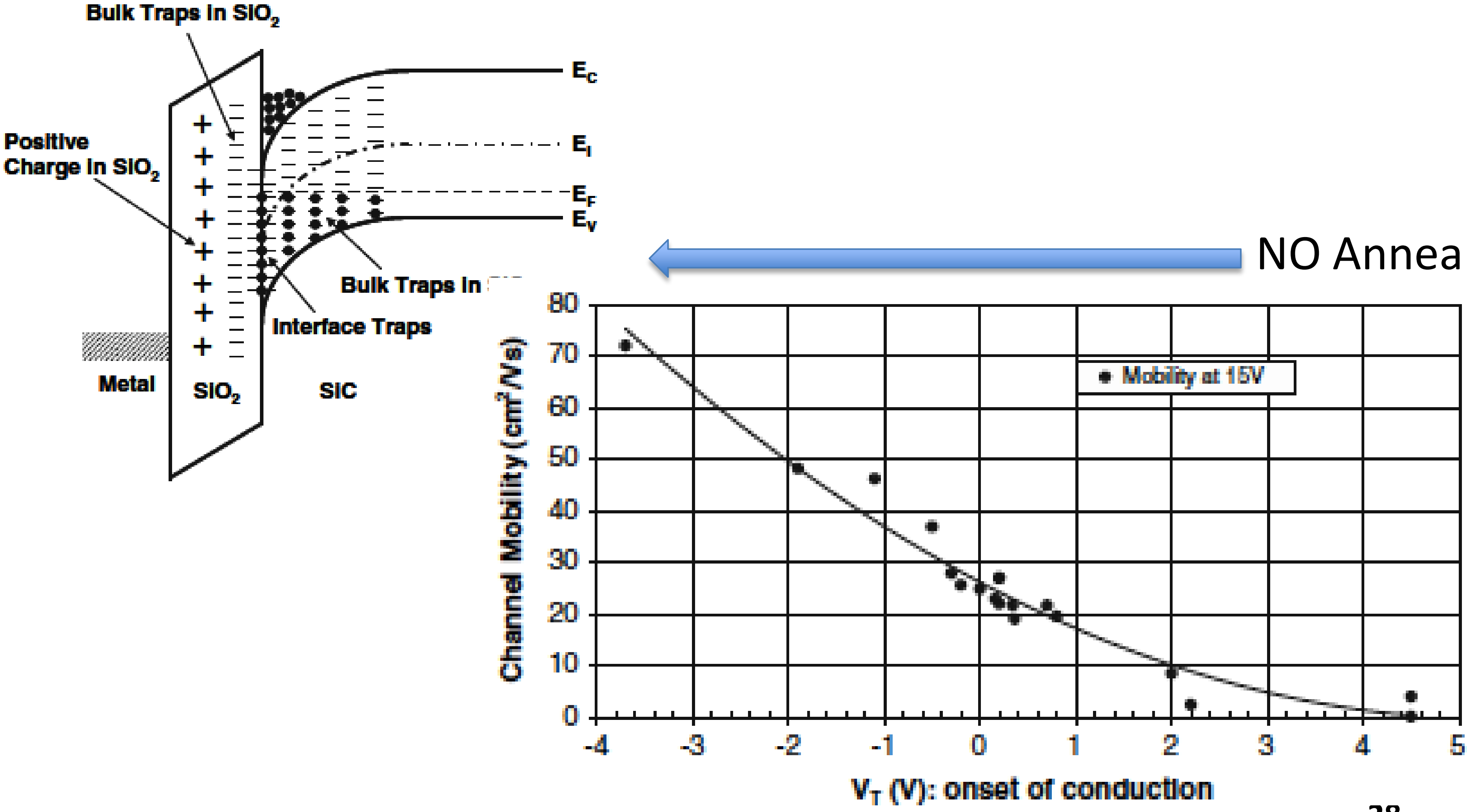
N. S. Saks, **A. K. Agarwal**, Applied Physics Letts. vol. 77, Nov. (2000)



$$\mu_n \cong Lg/[WC_{ox}(V_{gate} - V_{th})] \equiv \mu_{eff}$$

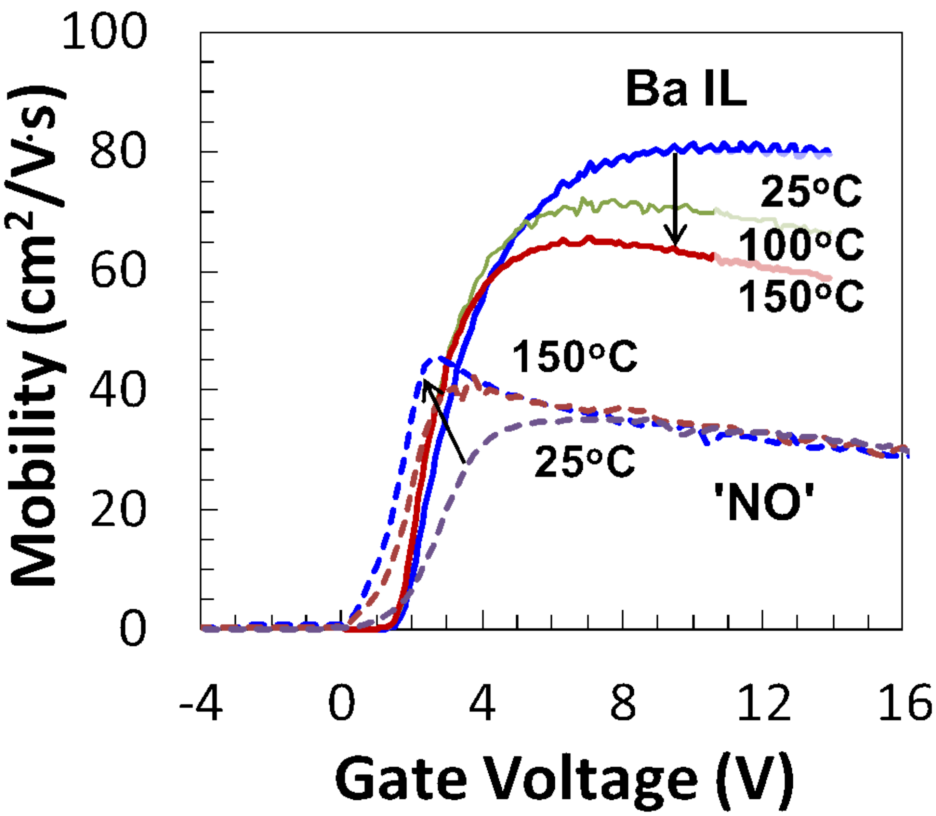
Some Critical Materials and Processing Issues in SiC Power Devices

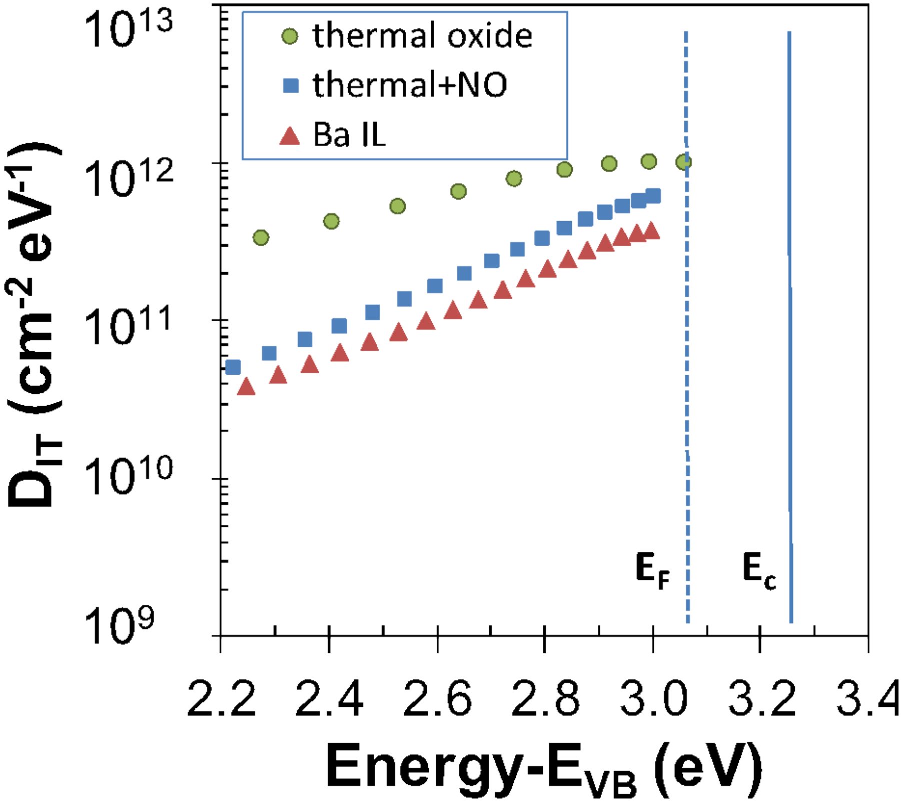
ANANT AGARWAL and SARAH HANEY, Journal of ELECTRONIC MATERIALS, Vol. 37, No. 5, 2008



NO Anneal

A 2-3 nm of Ba interlayer between SiC and SiO_2 significantly improves Field Effect Mobility



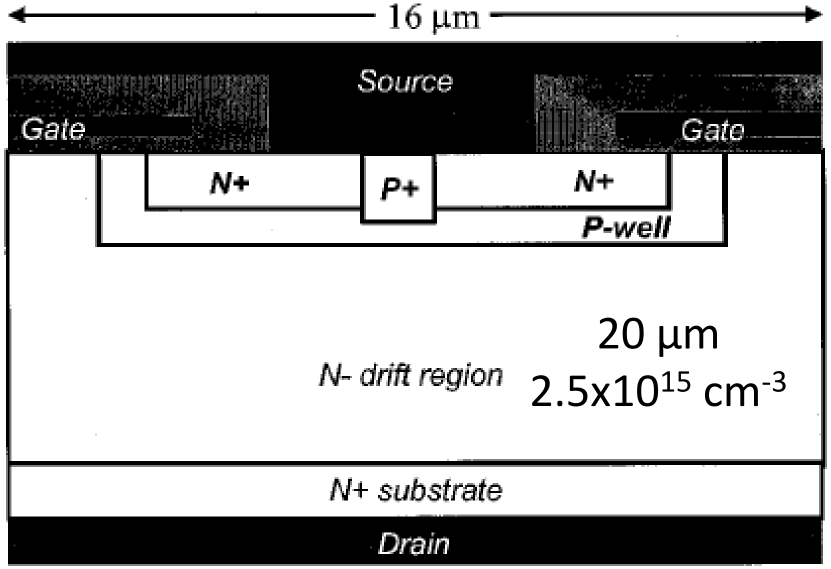


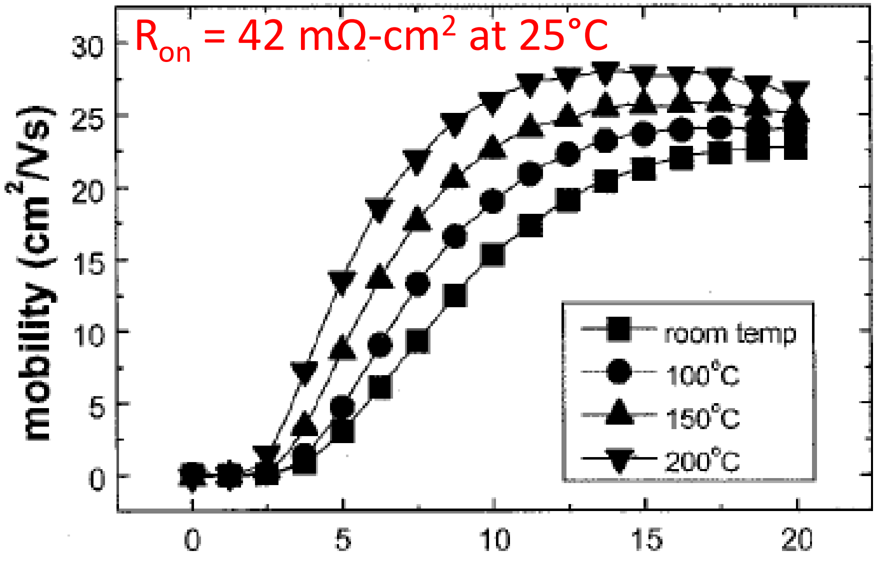
High mobility 4H-SiC (0001) transistors using alkali and alkaline earth interface layers
Daniel J. Lichtenwalner, Lin Cheng, Sarit Dhar, **Anant Agarwal** and John W. Palmour,
Appl. Phys. Lett. 105, 182107 (2014)

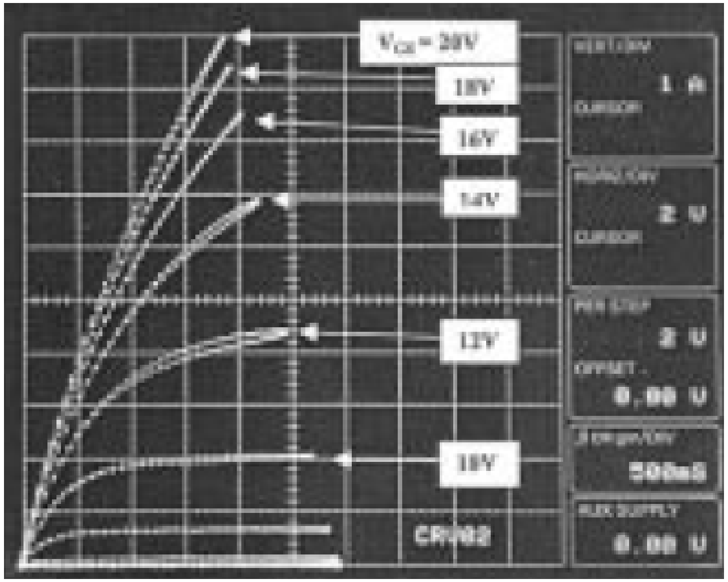
10 A, 2.4 kV Power DiMOSFETs in 4H-SiC

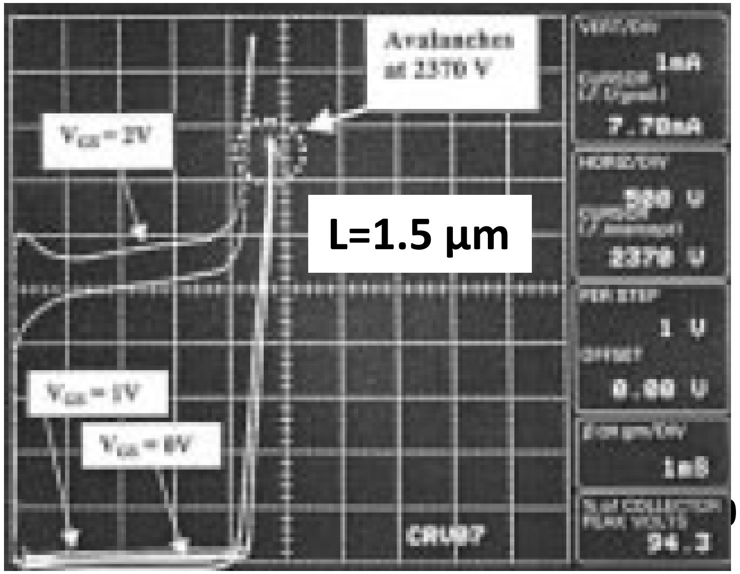
Sei-Hyung Ryu, **Anant Agarwal**, James Richmond, John Palmour, Nelson Saks, and John Williams

IEEE Electron Device Letters, Vol. 23, No. 6, June 2002. pp. 321-323

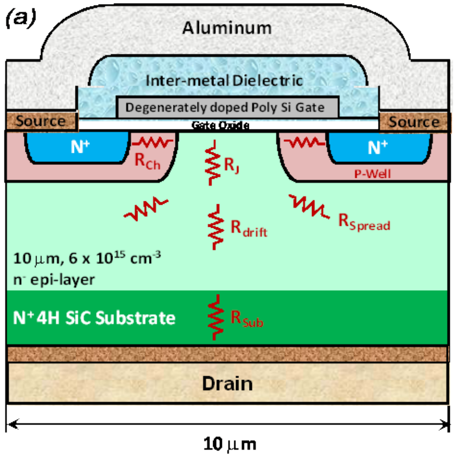


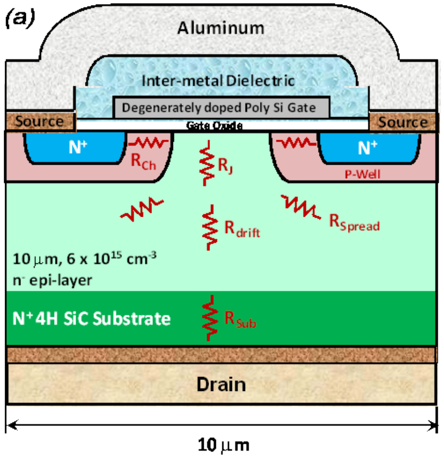

R$_{on}$ = 42 mΩ-cm^2 at 25°C

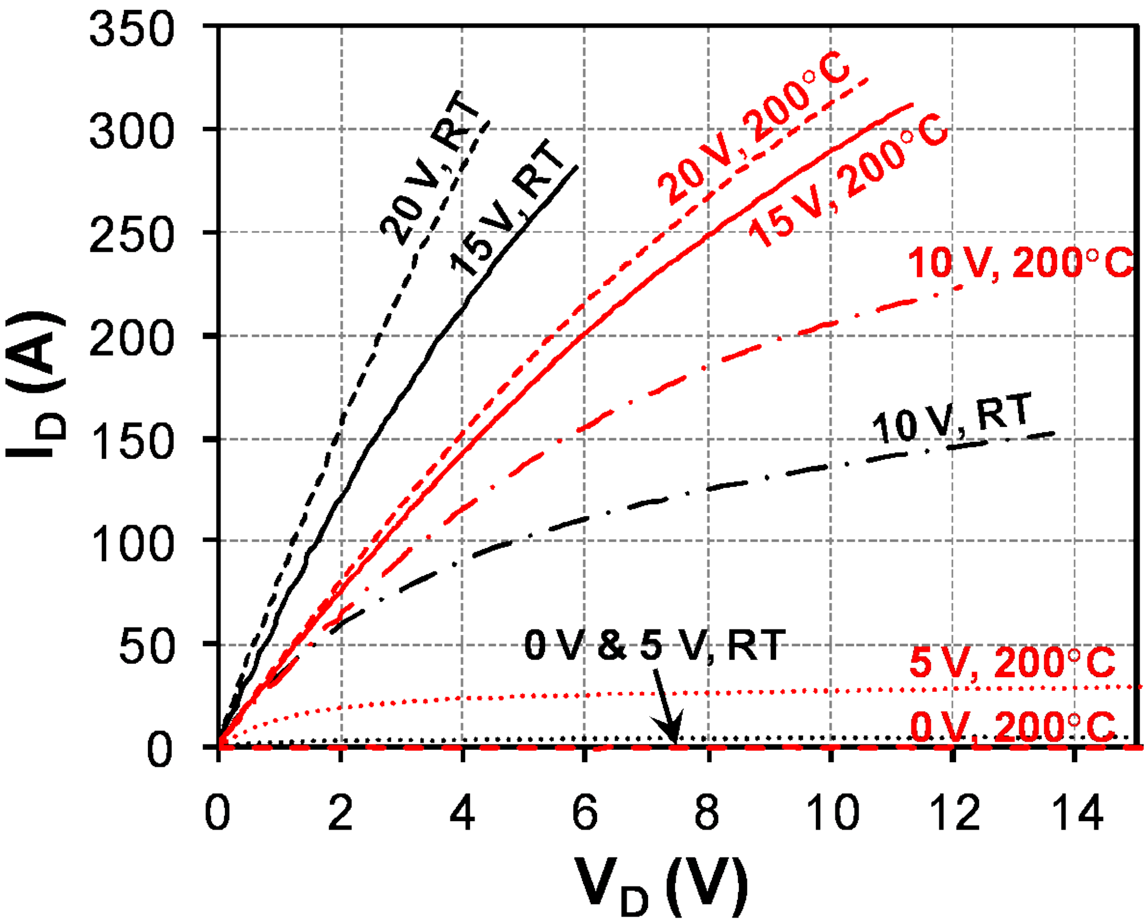



L=1.5 µm

Large Area, 1600 V / 150 A, 4H-SiC DMOSFET







L. Cheng; **A. K. Agarwal**; M. Schupbach; D. A. Gajewski; D. J. Lichtenwalner; V. Pala; S. H. Ryu; J. Richmond; J. W. Palmour; W. Ray; J. Schrock; A. Bilbao; S. Bayne; A. Lelis; C. Scozzie, "High performance, large-area, 1600 V / 150 A, 4H-SiC DMOSFET for robust high-power and high-temperature applications", **2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD)**, pp. 47-50, 2013

Some Products my R&D Team Helped Develop at Cree

http://www.wolfspeed.com/

Bare Die

Product	BV	Rds(on)	Current
CPM3-0900-0010A	900 V	10 mohm	196 A
CPM3-0900-0065B	900	65	36
CPM3-1000-0065B	1000	65	36
CPM2-1200-0025B	1200	25	98
CPM2-1200-0040B	1200	40	63
CPM2-1200-0080B	1200	80	36
CPM2-1200-0160B	1200	160	19
CPM2-1700-0045B	1700	45	72

My R&D team at Cree created products that are highly reliable and robust

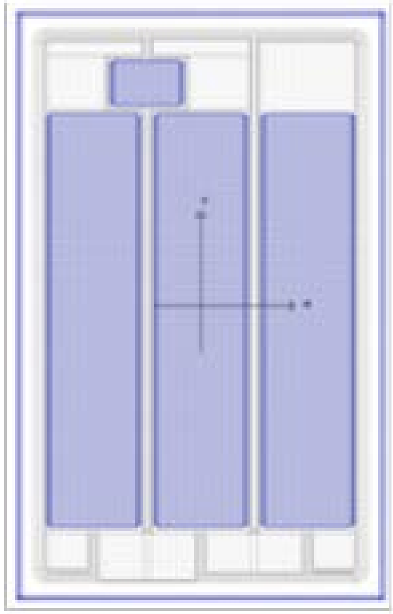
CPM2-1200-0025B

Silicon Carbide Power MOSFET

C2M™ MOSFET Technology

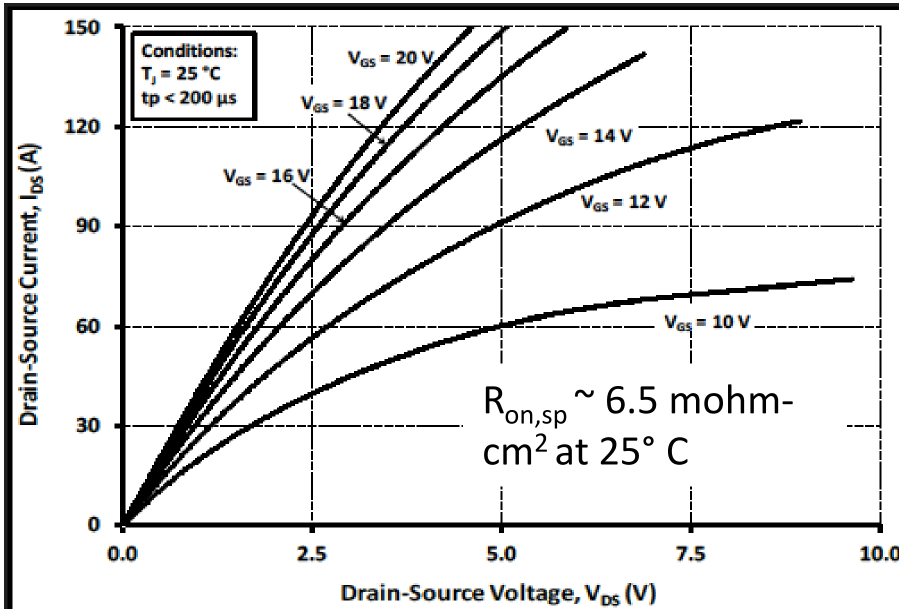
N-Channel Enhancement Mode

V_{DS}	1200 V
I_{D} @ 25˚C	98 A
$R_{DS(on)}$	25 mΩ

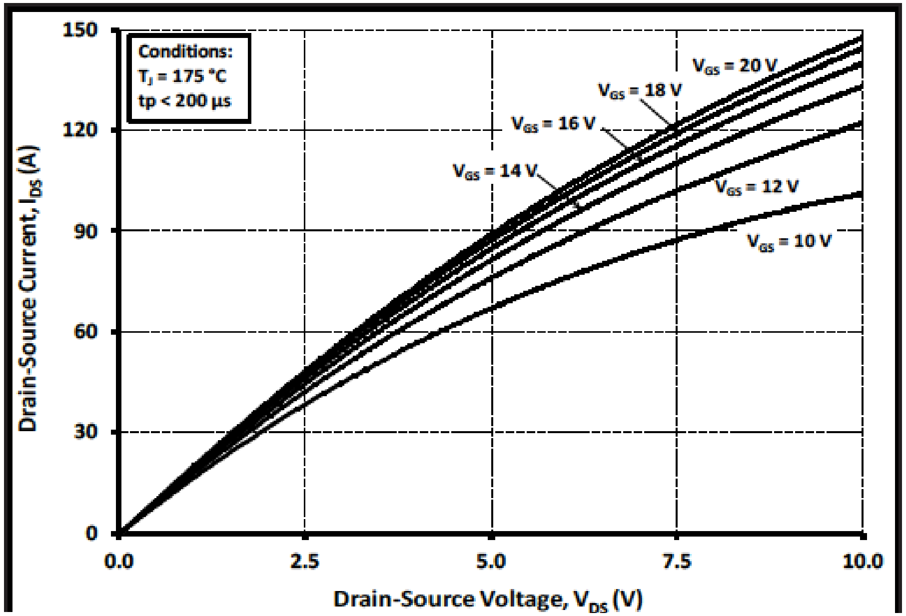


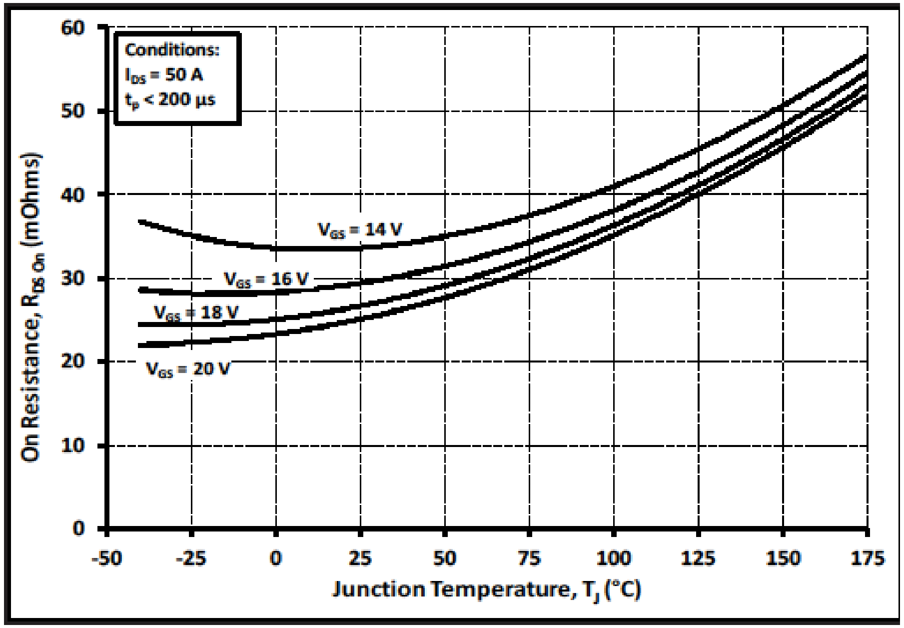
Part Number	Die Size (mm)
CPM2-1200-0025B	4.04 x 6.44

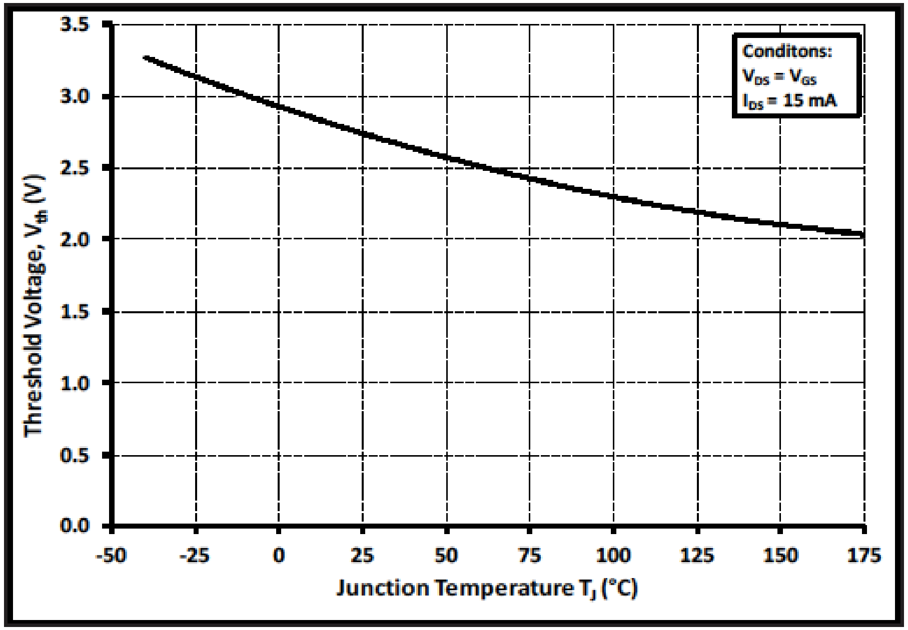
A lot can be learned from the spec-sheet for 1200 V, 25 mohm product



$R_{on,sp}$ ~ 6.5 mohm-cm^2 at 25° C



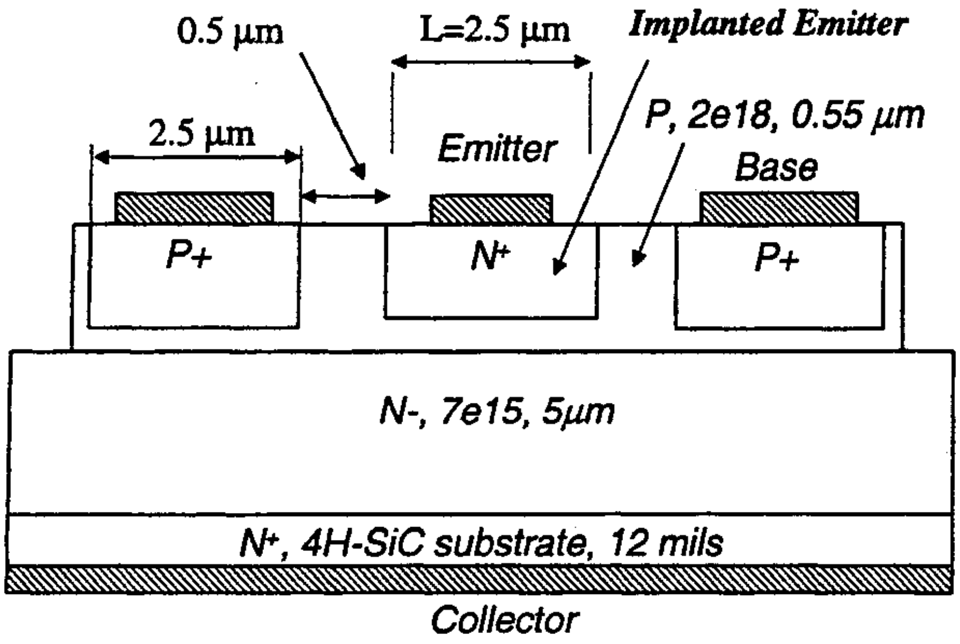


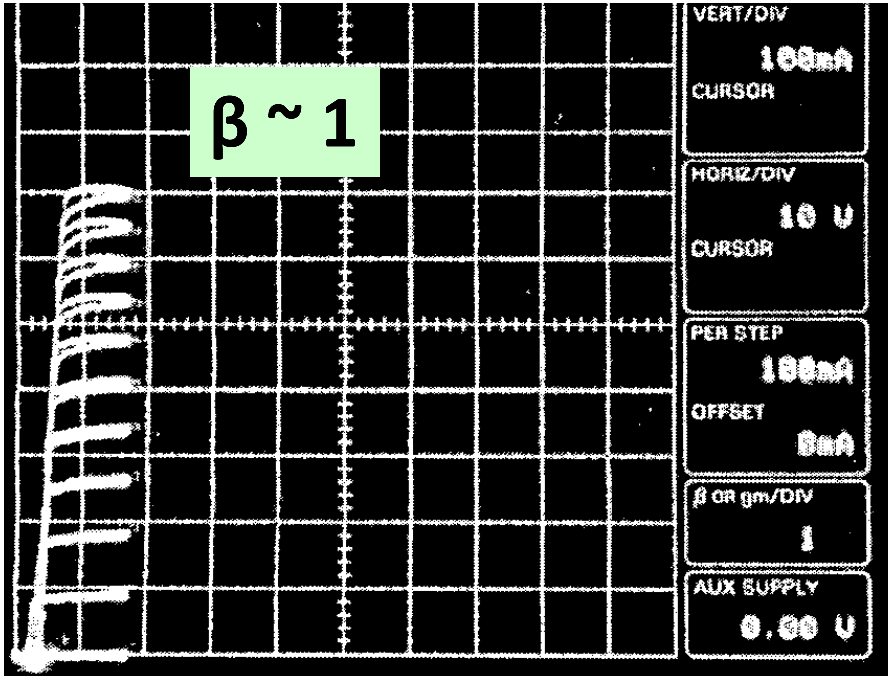


Ion-Implanted Emitter in BJTs does not work!

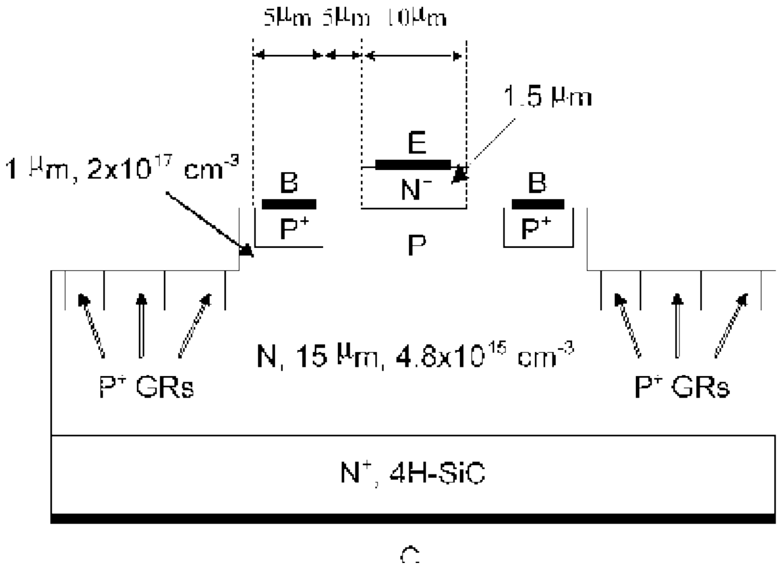
Anant Agarwal, Craig Capell, Binh Phan, James Milligan, John W. Palmour, Jerry Stambaugh, Howard Bartlow and Ken Brewer

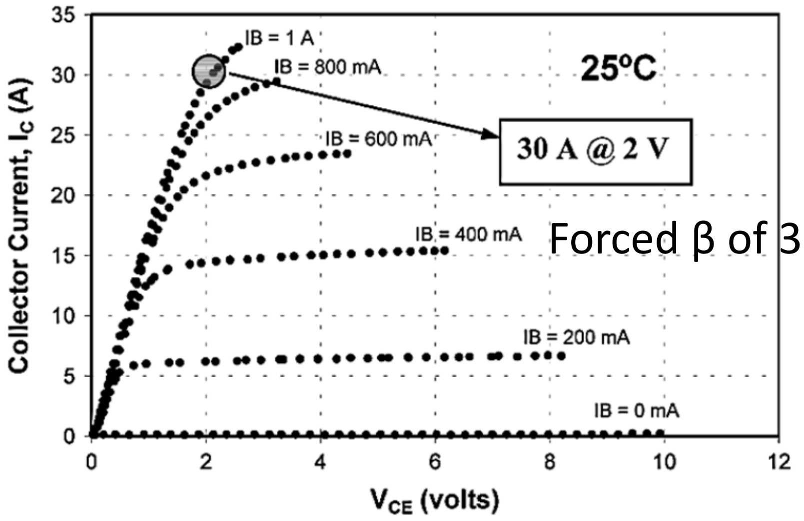
Materials Science Forum Vols. 433-436 (2003), pp. 785-788.



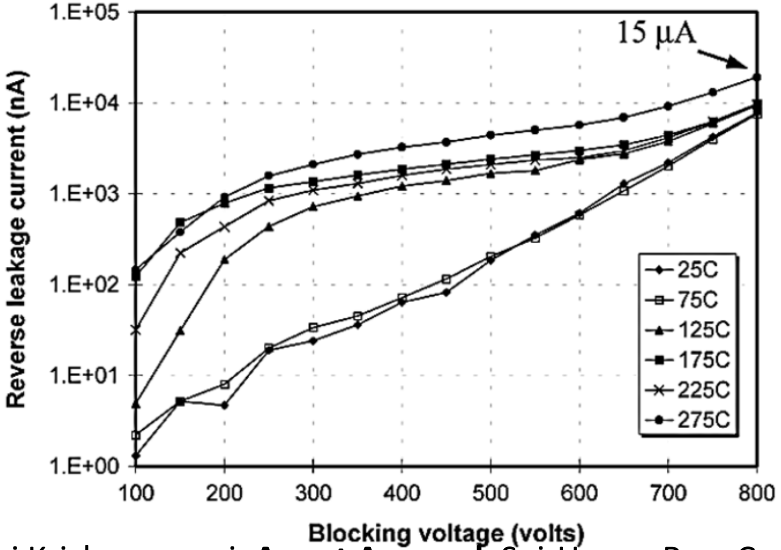


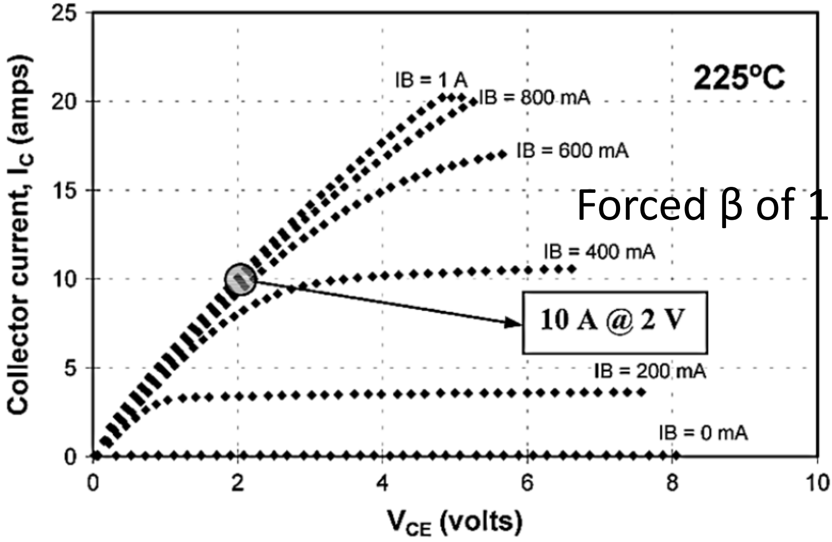
SiC BJTs have been successfully fabricated but are not easy to manufacture because implanted emitter does not work.





Forced β of 30



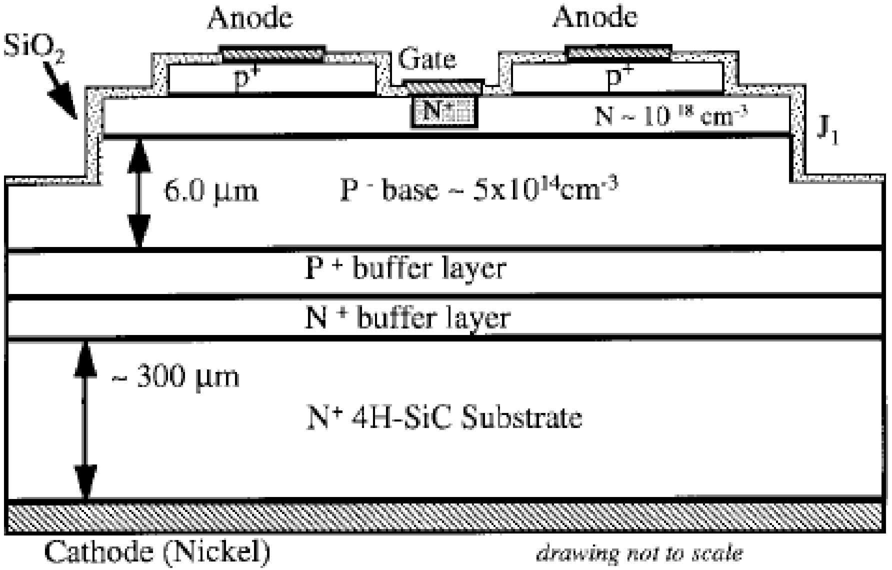


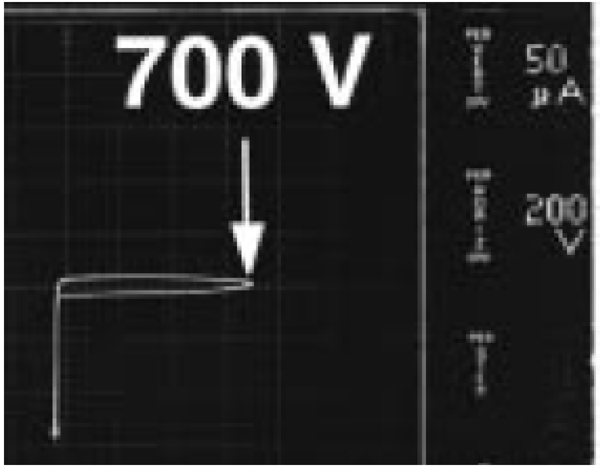
Forced β of 10

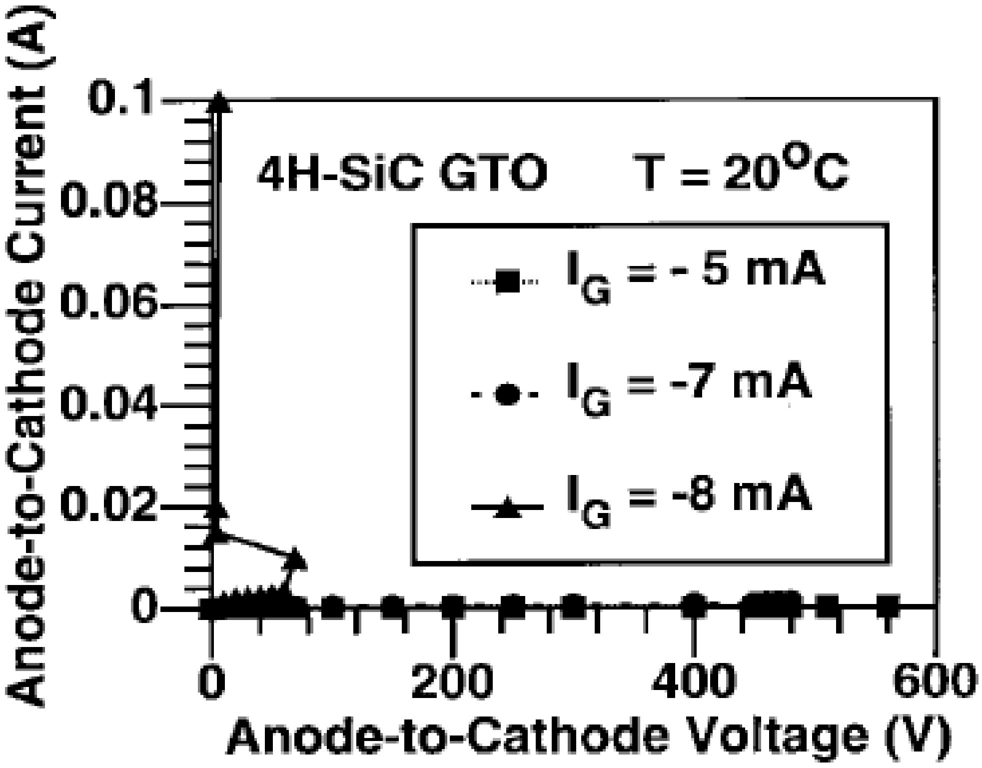
Sumi Krishnaswami, **Anant Agarwal**, Sei-Hyung Ryu, Craig Capell, James Richmond, John Palmour, Santosh Balachandran, T. Paul Chow, Stephen Bayne, Bruce Geil, Kenneth Jones and Charles Scozzie, "1000-V, 30-A 4H-SiC BJTs with High Current Gain," **IEEE Electron Device Letters**, Vol. 26, No. 3, pp. 175-177, March 2005.

700-V Asymmetrical 4H-SiC Gate Turn-Off Thyristors (GTO's)

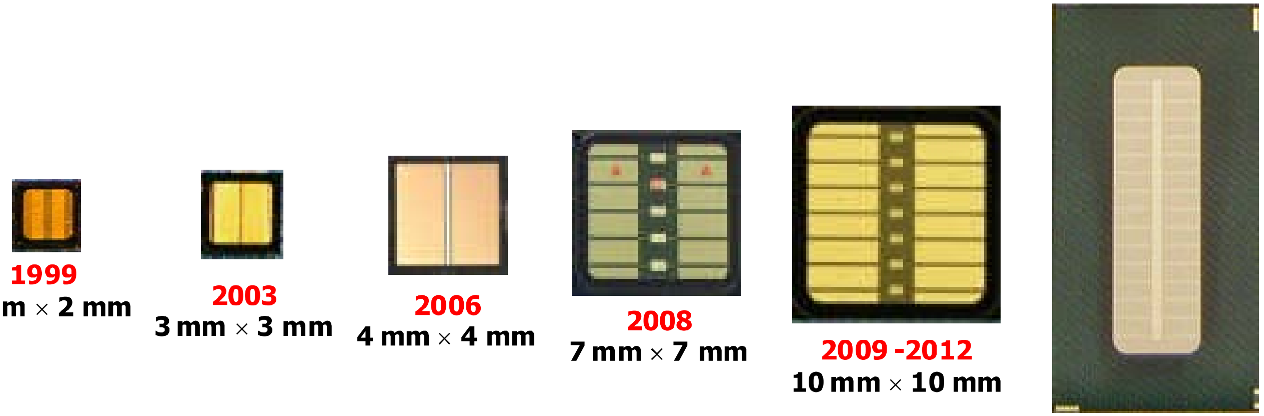
A. K. Agarwal, Jeffrey B. Casady, L. B. Rowland, S. Seshadri, R. R. Siergiej, W. F. Valek, and C. D. Brandt, IEEE Electron Device Letters, Vol. 18, No. 11, pp. 518-520, November 1997







SiC Thyrsitors and GTOs have come a long way – suitable for grid and pulse power



Year	2006	2008	2009 - 10	2011	2012	2013
Chip Size (cm x cm)	0.4 x 0.4	0.7 x 0.7	1 x 1	1 x 1	1 x 1	2 x 1
BV (kV)	5	6	7 - 9	10 - 12	15 +	17 - 20
t_{drift} (μm)	60	75	75 - 90	90	120 - 160	160
Wafer φ (mm)	76	76	100	100	100	100 / 150
V_F degradation	Yes	Yes	No	No	No	No

L. Cheng; **A. K. Agarwal**; C. Capell; M. O'Loughlin; K. Lam; J. Richmond; E. Van Brunt; A. Burk; J. W. Palmour; H. O'Brien; A. Ogunniyi; C. Scozzie, “20 kV, 2 cm^2 4H-SiC gate turn-off thyristors for advanced pulsed power applications”, **2013 19th IEEE Pulsed Power Conference (PPC)**, 2013