ME290R: Topics in Manufacturing
Fall 2017

Nanoscale manipulation of materials

Lecture 2.2: Lithography Performance Criteria - Point Defects (Yield Modeling)
August 28, 2017

Hayden Taylor
hkt@berkeley.edu

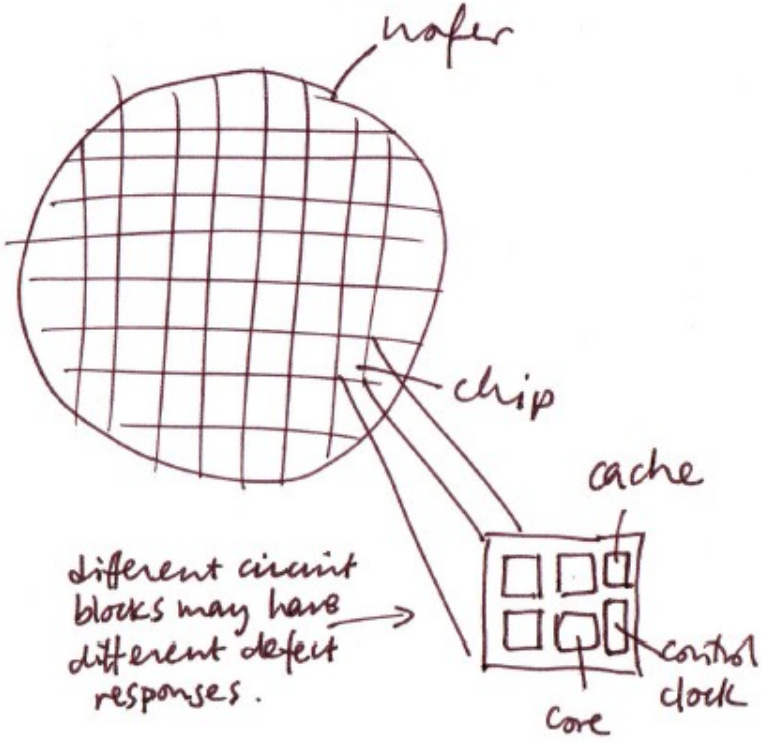
What factors need to be borne in mind when evaluating a lithography process?

- **Technical**
  - Dimensional accuracy and variability
  - Pattern edge roughness
  - Overlay accuracy
  - **Point defects**
- **Economic**
  - Throughput (*vs*. yield)
  - Materials, tooling, equipment, and energy costs
- **Environmental**
  - Materials usage and disposal (toxicity)
  - Energy used in process
  - Embodied energy

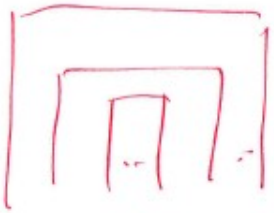
Yield modeling

Characterize yield at several stages/scales:

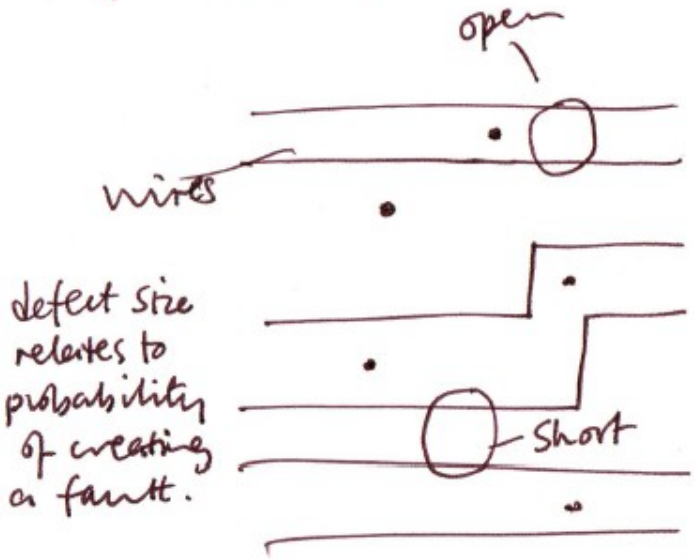
- "Wafer yield" – how many make it to probing?
  - Probe-testing – simple electrical testing
  - final testing – built in test structures.

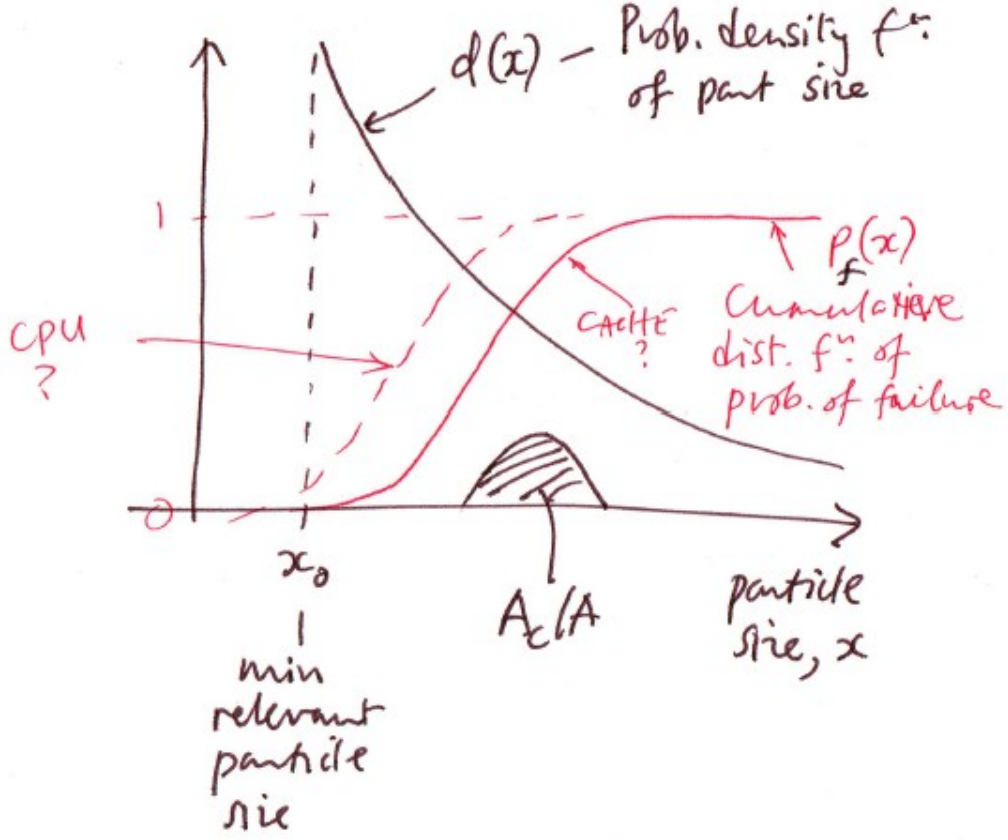


- Die-by-die (chip-chip)
  - → functional yield / "hard" → binary decision – does it work?
  - → parametric yield / "soft" → max clock speed?
    power consumption?
    core-scale characterization?
    } "binning"



Critical area





CRITICAL AREA, A_c:

$$A_c = \frac{A}{\text{chip area}} \int_{x_0}^{\infty} P_f(x)\, d(x)\, dx$$

Suppose D_0 is average # defects per unit area leading to a fault

Expected # defects on wafer $M = A_c D_0 C$, where C = # chips on wafer

Yield modeling continued...

- Possible permutations of the locations of the M defects

$$C^M$$

- If one chip is defect-free, # permutations is now $(C-1)^M$

$\therefore$ probability that a given chip is defect-free: $\frac{(C-1)^M}{C^M} = \left(1-\frac{1}{C}\right)^M$

$$\text{Yield} = \lim_{C\to\infty}\left(1-\frac{1}{C}\right)^{CA_cD_0} = \exp(-A_cD_0)$$

Yield: Functional (fraction of chips that work)

A_c: property of design of chip

D_0: Property of process

Probability of N chips having no defects:

$$\exp(-A_cD_0)^N = \exp(-NA_cD_0)$$

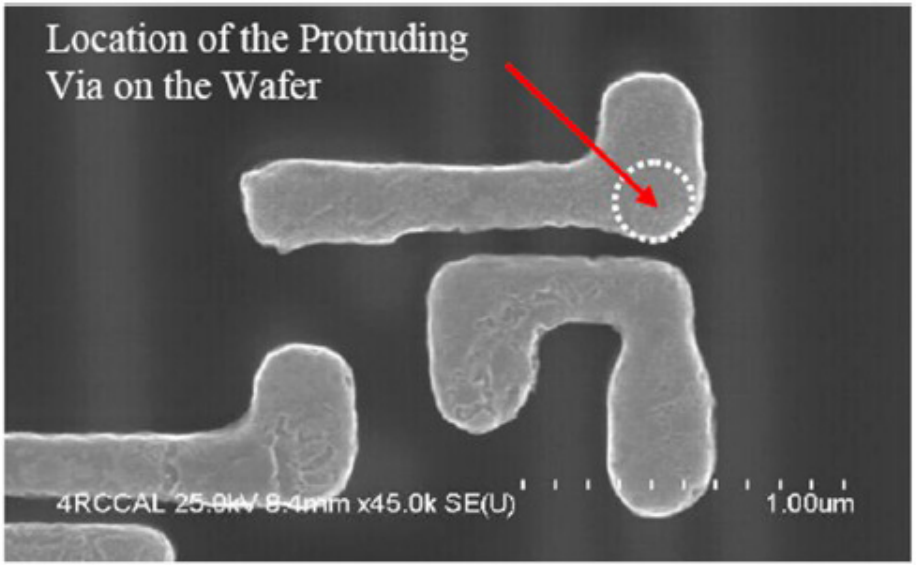
How can we characterize manufactured patterns?

- Dimensionally
  - Scanning electron microscopy
  - Atomic force microscopy
  - Optically: microscopy, *scatterometry*, interferometry
- Functionally
  - Electrical measurements – *e.g.* serpentine test structures
  - Optically, in the case of optical interconnect

Scanning electron microscopy: CDSEM

- Widespread use in semiconductor metrology
- Top-down imaging can give CD and LER information without destroying the wafer
- For cross-sectional (sidewall angle) information, cross-sectioning (typically with focused ion beam (FIB) milling) is needed

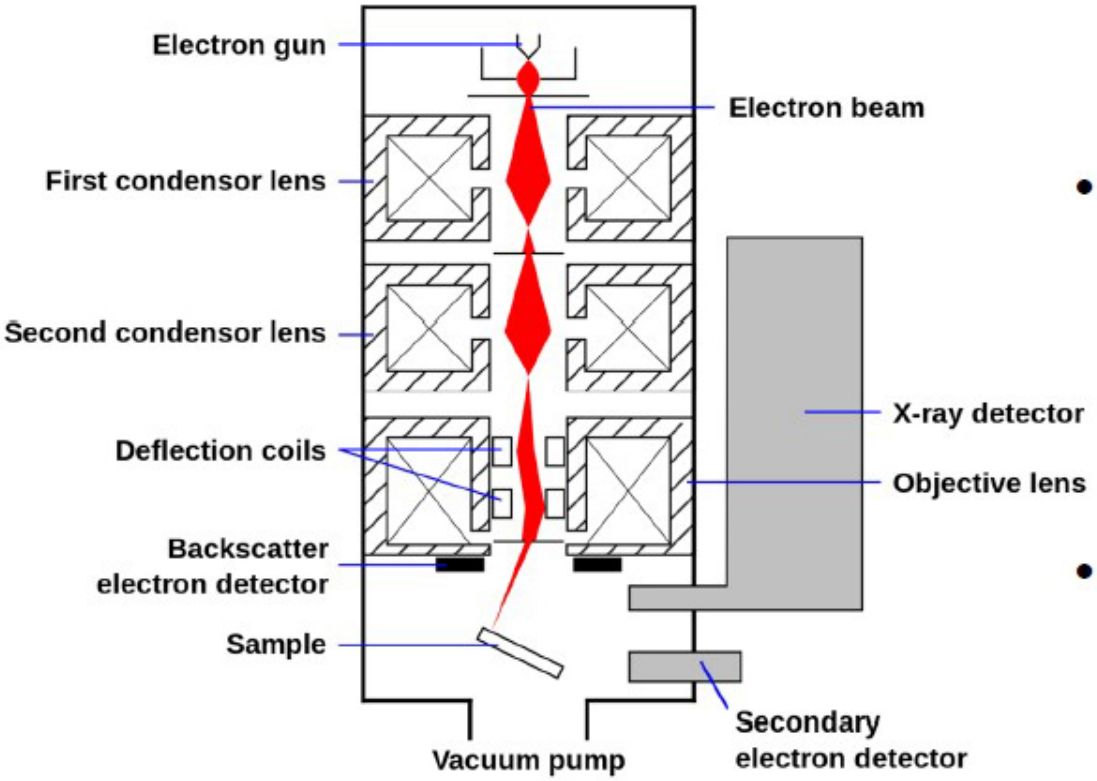
Soluris



http://www.eejournal.com/archives/articles/20101026-synopsys/?printView=true

CD SEM – working principle

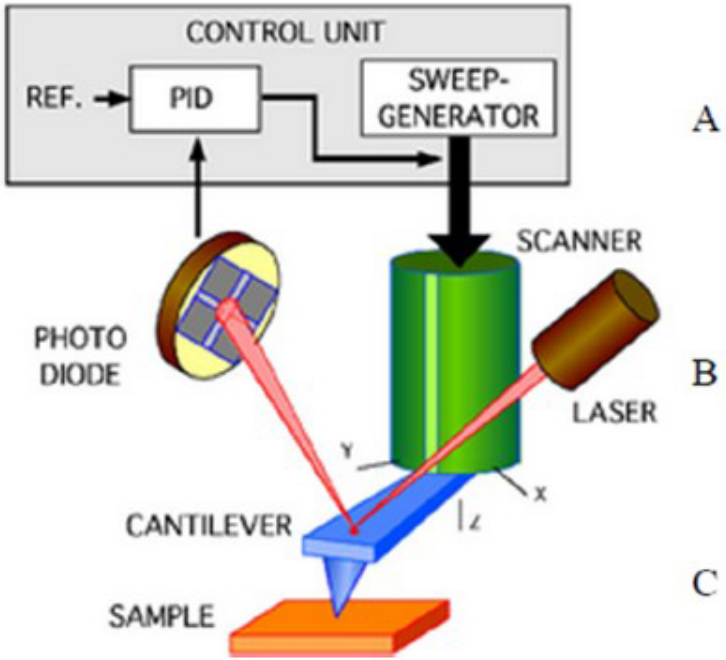
- Resolution < 1 nm
- Can determine topography and chemical composition
- Raster scanning of sample



- Both backscattered and secondary electrons can be sensed and used to create an image
- Secondary electrons are ejected from the sample atoms as a result of inelastic scattering interactions with beam electrons
- Backscattered electrons are reflected beam electrons – used to detect chemical composition

Atomic force microscopy

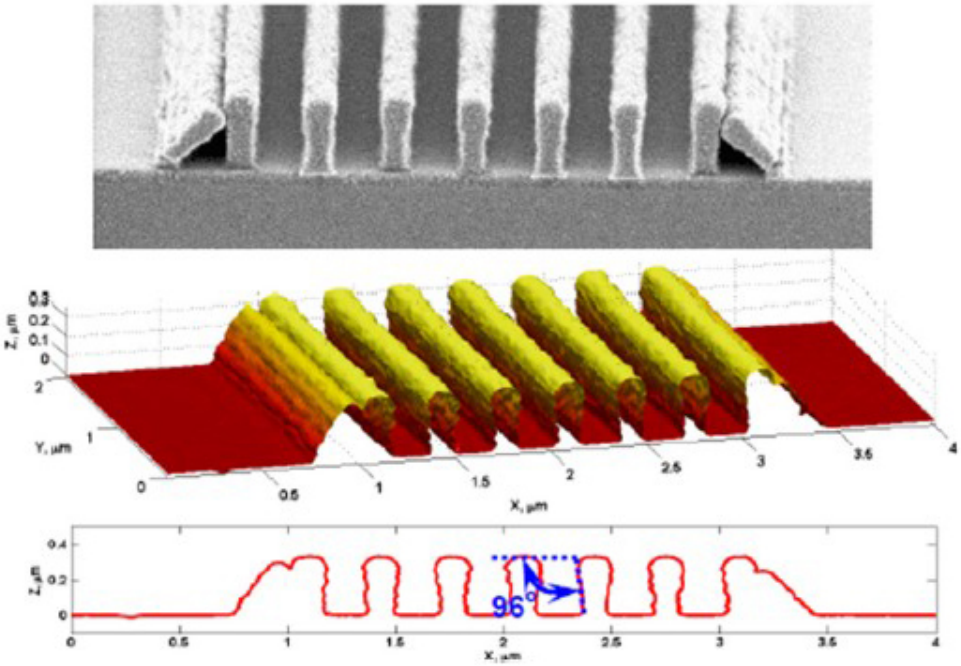
- Potential to give some sidewall information without sectioning the wafer
- However, the measurement obtained is the convolution of tip shape with the true topography.



A

B

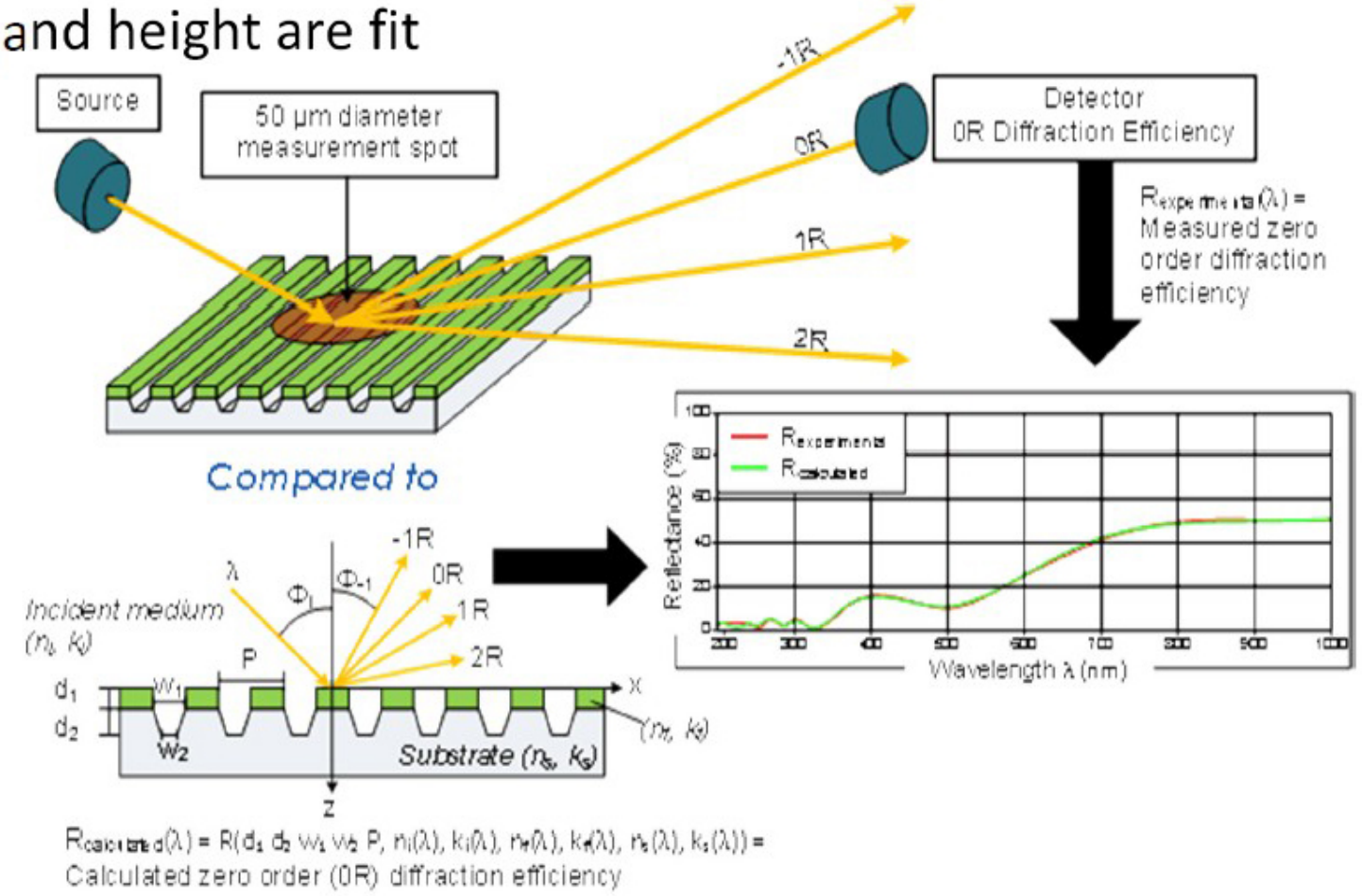
C



http://www.cds.caltech.edu/~murray/amwiki; http://www.parkafm.com/

Scatterometry – gathers average pattern geometry information from arrays of features

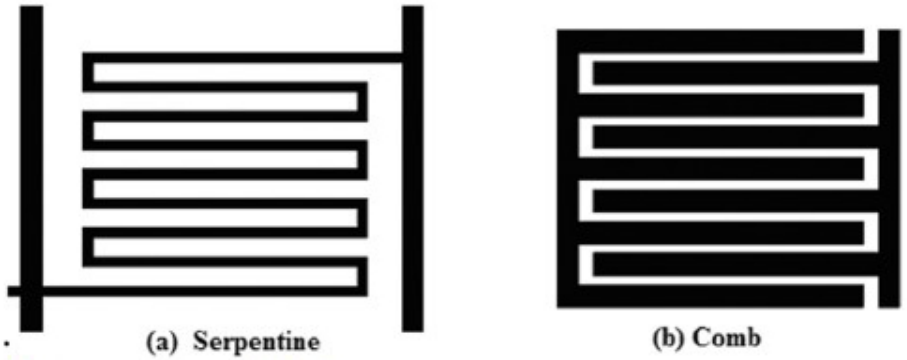
- Scattered intensities at several diffraction orders or wavelengths are compared to a model – geometric parameters such as CD, sidewall angle, and height are fit



http://www.halbleiter.org/en/oxidation/metrology/

Electrical/functional test structures

- Basic electrical test structures
  - *Serpentine* – detect open circuits
  - *Comb* – detect short circuits
  - Must cover a large enough area to offer a reasonable probability of detecting an error without encountering an error on *every* chip



- BIST – Built-In Self-Test circuits

Jaiswal et al., *J. Micro/Nanolith. MEMS MOEMS*. 9(4), 041303, 2010.