Self-Heating and Scaling of Silicon Nano-Transistors

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Advisors: Profs. Kenneth Goodson and Robert Dutton

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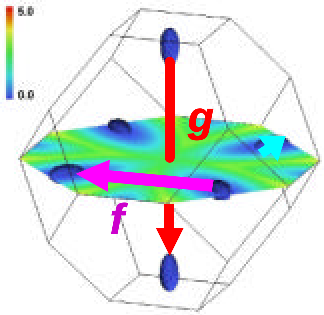
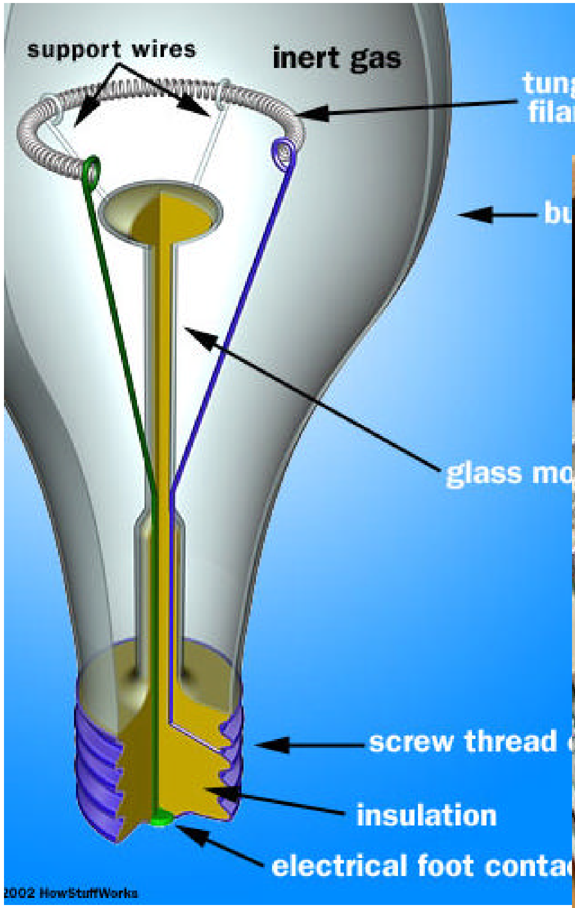
Summary

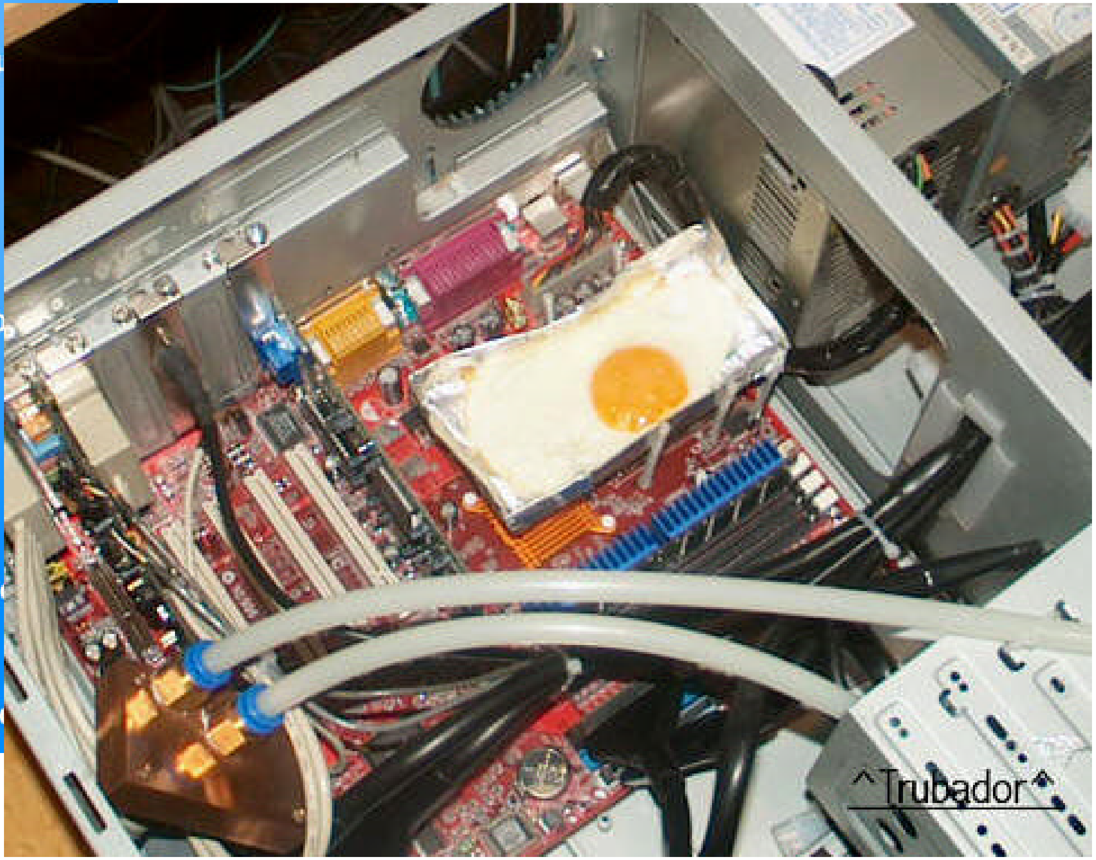
- Self-heating in bulk and strained silicon
- Monte Carlo code (MONET):
  - Implementation → electron and phonon model
  - Validation → vs. data and commercial codes
  - Results → heat generation details
- Thermal scaling limits of nano-transistors
  - Compact model for thin-body devices
  - Electro-thermal design guidelines
  - Device geometry optimization



Why is Heat Bad for Electronics?

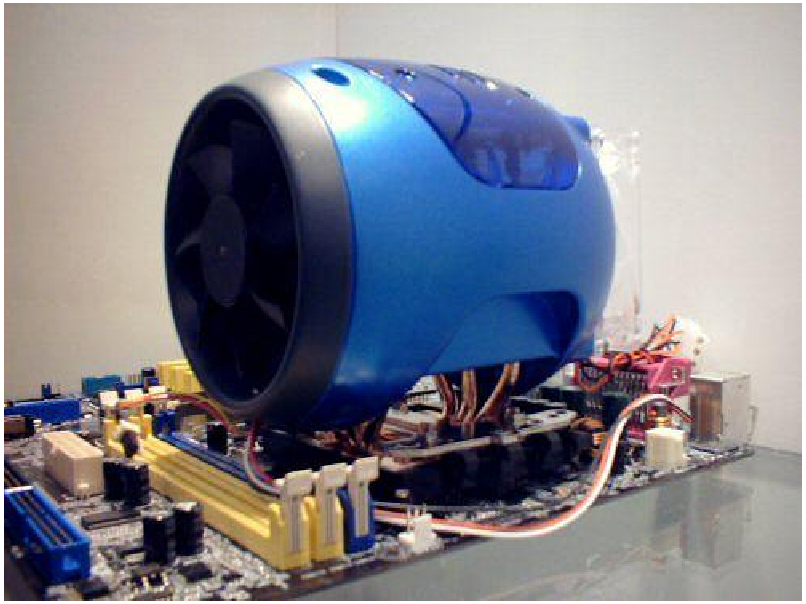


CPU Power Density ~ 100 W/cm^2



http://phys.ncku.edu.tw/~htsu/humor/fry_egg.html

... and for End Users



ASUSTeK cooling solution (!)

The industry now calls them "portables" not "laptops"

You are in: Health

Friday, 22 November, 2002, 12:55 GMT

Burned groin blamed on laptop

Hot stuff: Could laptopping be a painful business?

A Swedish scientist who rested his laptop computer on his lap for just an hour needed medical treatment for extensive blistering.

A concerned doctor wrote to The Lancet medical journal after encountering the distressed patient.

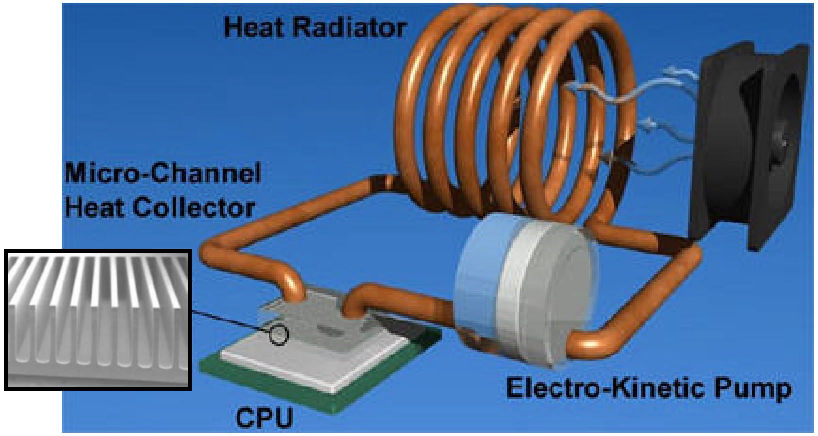
He is warning the public of the potential dangers of using a laptop "in the literal sense".

The 50-year-old father-of-two used the laptop machine, of unknown origin, to write a report while sitting in an armchair.

Dr Claes-Goran Ostenson, from Sweden's Karolinska Institute, told the journal: "He had placed his laptop computer on his lap while writing for about one hour.

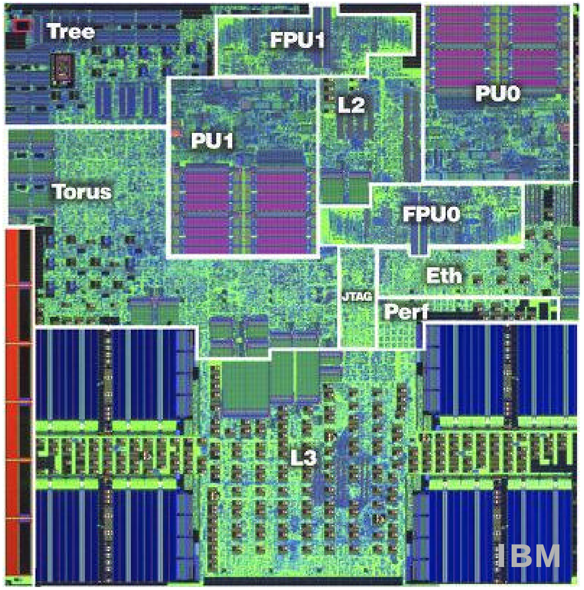
"The next day he noticed irritation."

Thermal Management Methods



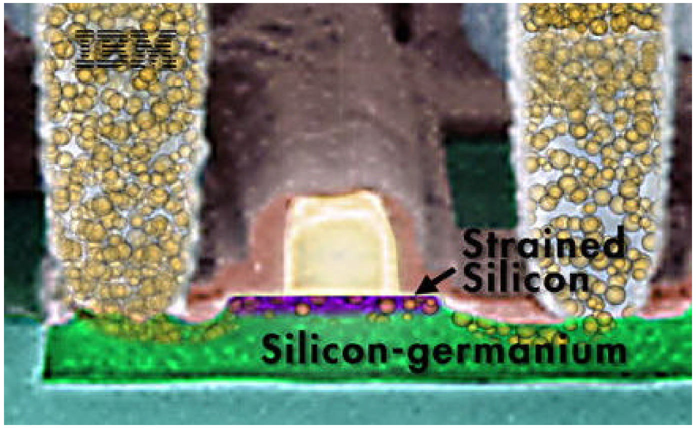
System Level

→ Active Microchannel Cooling (Cooligy)



Circuit + Software Level

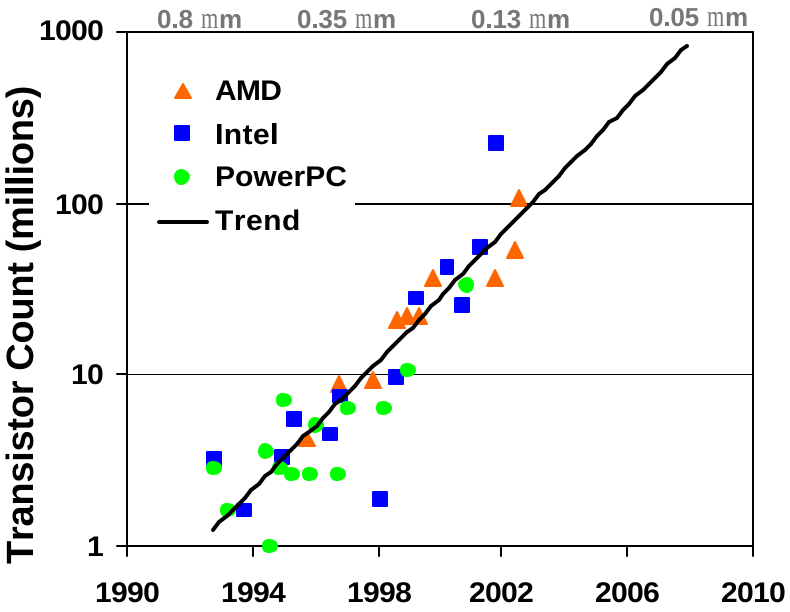
→ active power management
(turn parts of circuit on / off)

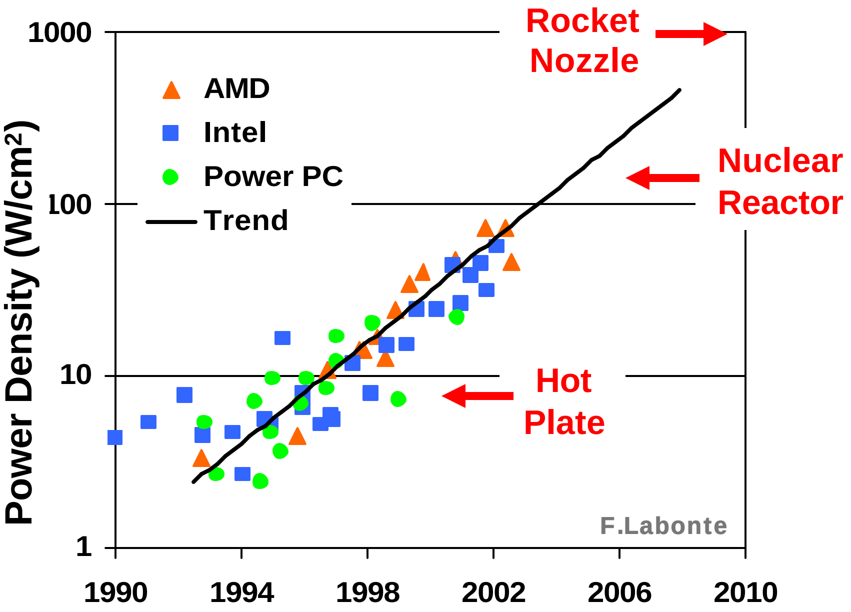


Transistor Level ?

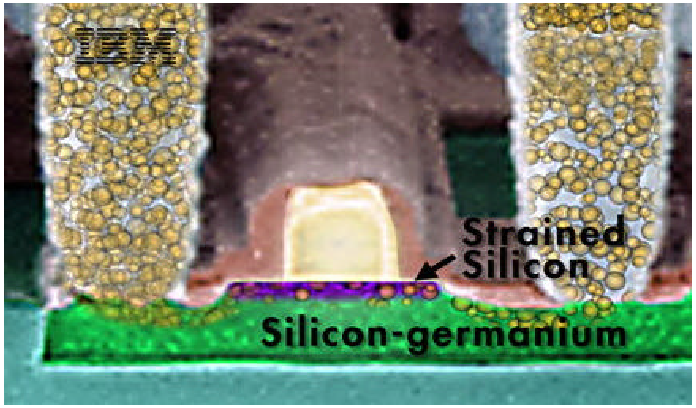
→ electro-thermal device design

Transistor Thermal Challenges



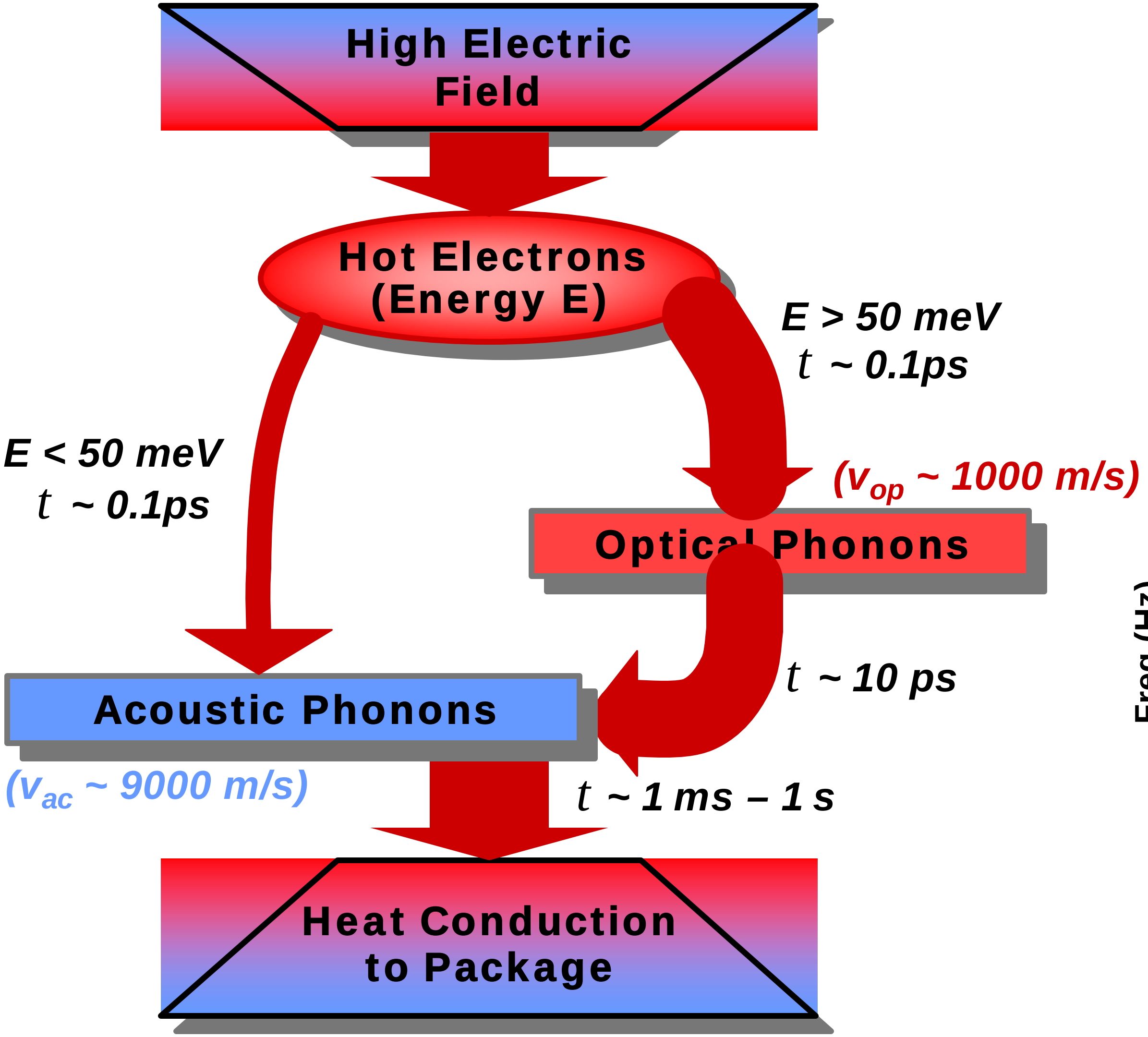


Confined Geometries, Novel Materials



Material	k_{th} (W / mK)
Si	148
Ge	60
Silicides	40
Si (10 nm)	13
SiO$_2$	1.4

Details of Joule Heating in Silicon



High Electric Field

Hot Electrons (Energy E)

E > 50 meV
t ~ 0.1ps

E < 50 meV
t ~ 0.1ps

(v_{op} ~ 1000 m/s)

Optical Phonons

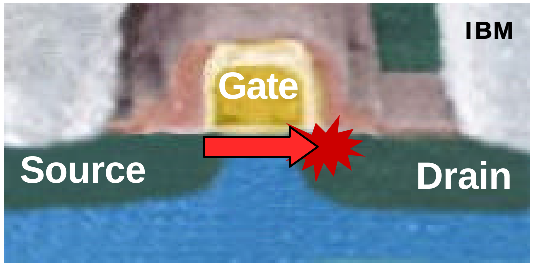
t ~ 10 ps

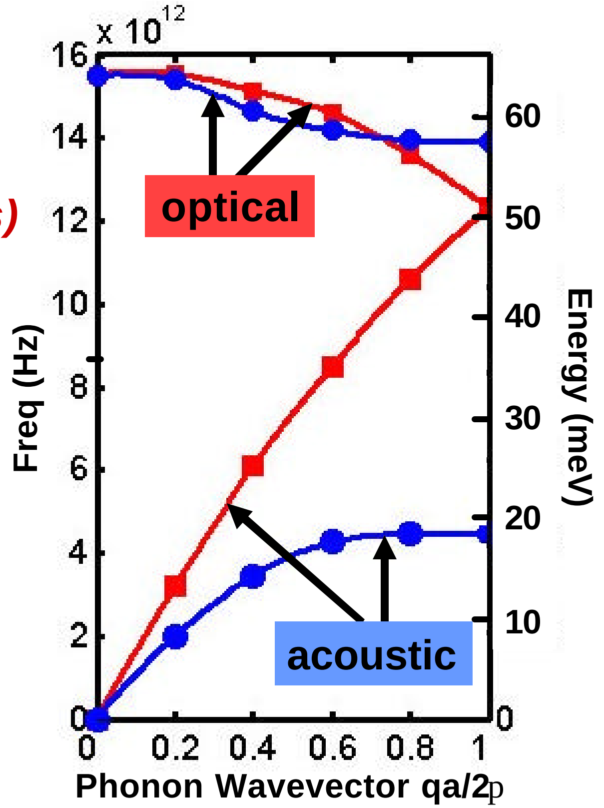
Acoustic Phonons

(v_{ac} ~ 9000 m/s)

t ~ 1 ms – 1 s

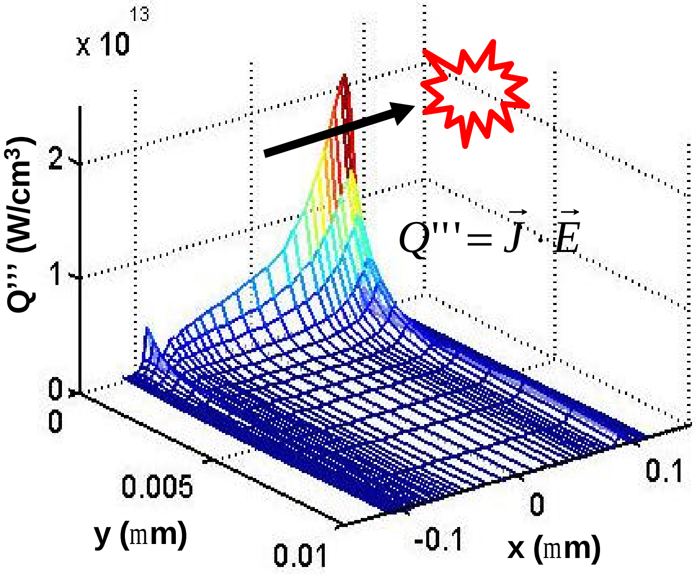
Heat Conduction to Package





Methods to Compute Heat Generation

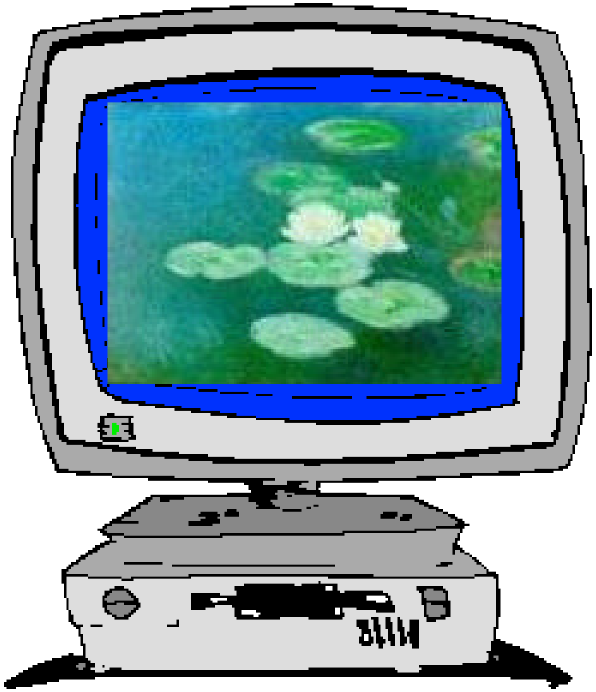
- **Drift-diffusion:** $Q''' = \vec{J} \cdot \vec{E}$
  - **Does not capture non-local transport**
- **Hydrodynamic:** $Q''' = \dfrac{3k_B}{2} \dfrac{T_e - T_L}{t_{e-p}} n$
  - **Needs some average scatt. time**
  - **(Both) no info about generated phonons**



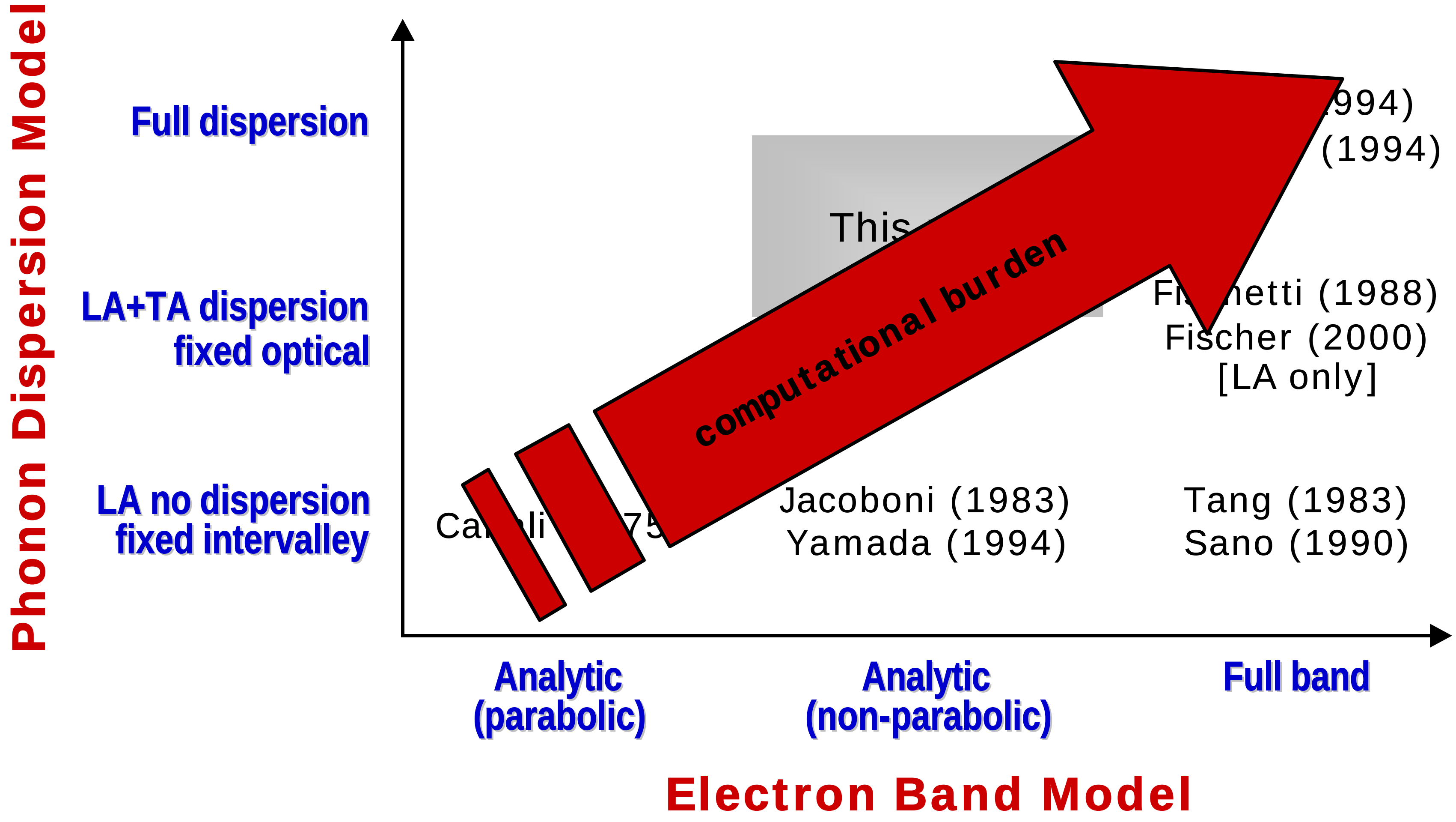
- **Monte Carlo:**
  - **Pros: Great for non-local transport**
  - **Complete info about generated phonons:** $Q''' = \dfrac{1}{t} \dfrac{d}{dV} \sum \left(\hbar w_{gen} - \hbar w_{abs} \right)$
  - **Cons: *slow* (but there are some short-cuts)**

Heat Generation with MONET

- Electrons treated as semi-classical particles, not as “fluid”
- Drift (free flight), scatter and select new state
- Must run long enough to gather useful statistics
- Main ingredients:
  - Electron energy band model
  - Phonon dispersion model
  - Device simulation:
    - Impurity scattering, Poisson equation, boundary conditions
    - Import grid from Medici (commercial drift-diffusion simulator)



Where the Present Work Fits In



Phonon Dispersion Model

Full dispersion

LA+TA dispersion fixed optical

LA no dispersion fixed intervalley

994)

(1994)

This

computational burden

Fi hetti (1988)
Fischer (2000)
[LA only]

Ca li 75

Jacoboni (1983)
Yamada (1994)

Tang (1983)
Sano (1990)

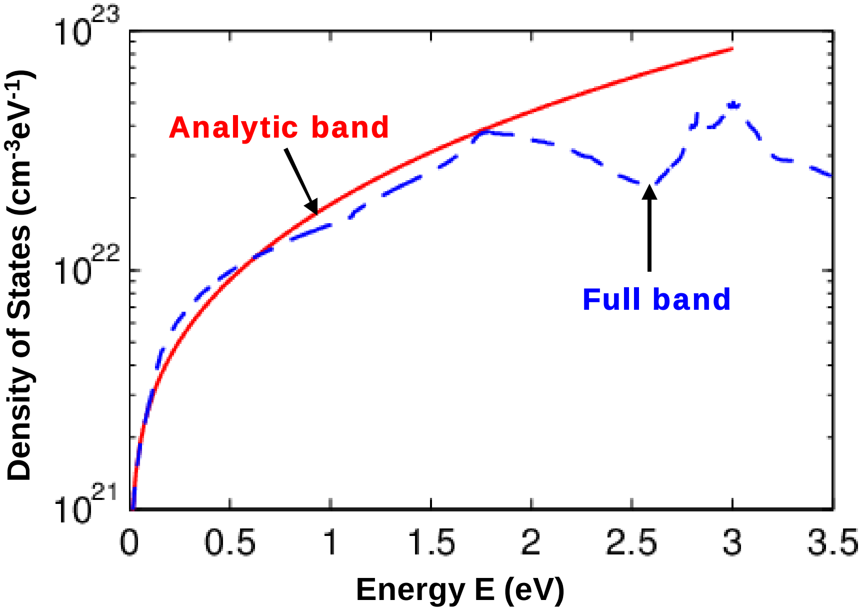
Analytic (parabolic)

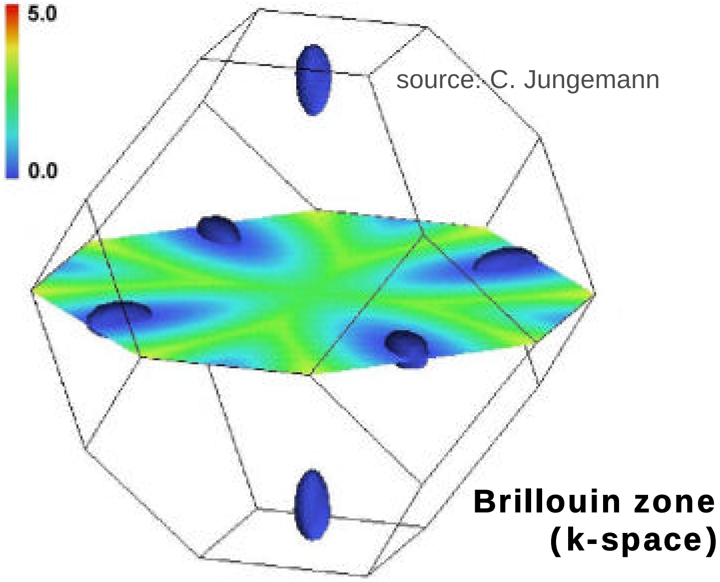
Analytic (non-parabolic)

Full band

Electron Band Model

Electron Energy Band Model



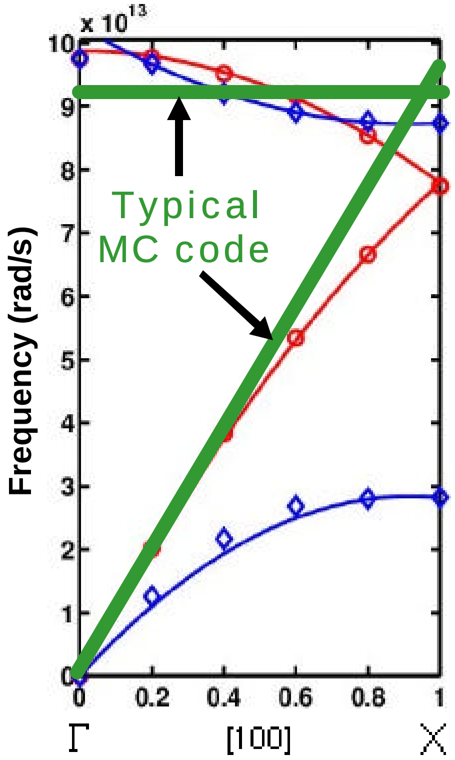


source: C. Jungemann

- **Analytic “non-parabolic” band approximation (a = 0.5 eV^{-1})**
- **Good choice for V$_{dd}$ £ 1.1 V**
  - **No impact ionization**
  - **No X-L valley scattering**
  - **Fast and reasonable for future technologies**

$$E(1+a\,E)=\frac{\hbar^2}{2}\left(\frac{k_x^2}{m_x}+\frac{k_y^2}{m_y}+\frac{k_z^2}{m_z}\right)$$

Phonon Dispersion Model



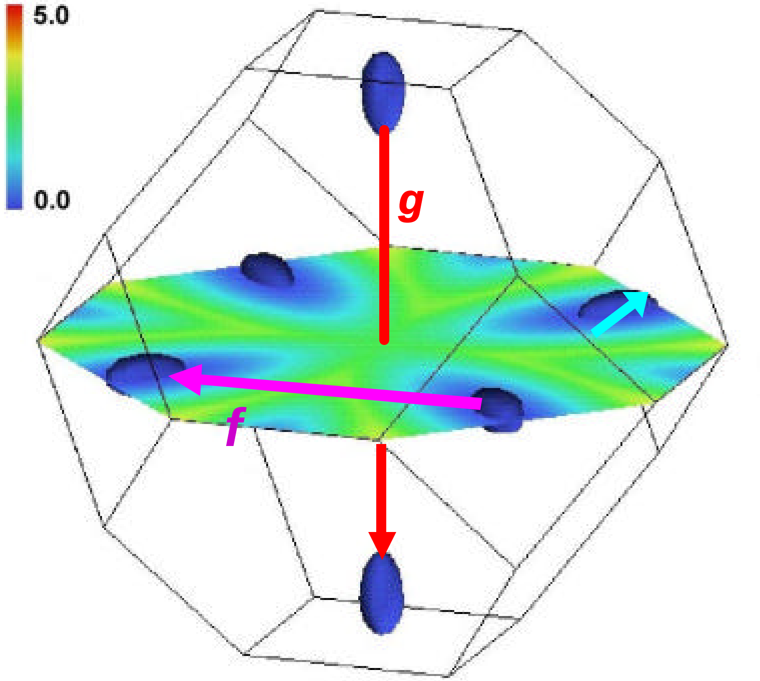
- **Quadratic approximation**

$$w(q) = w_o + v_s q + cq^2$$

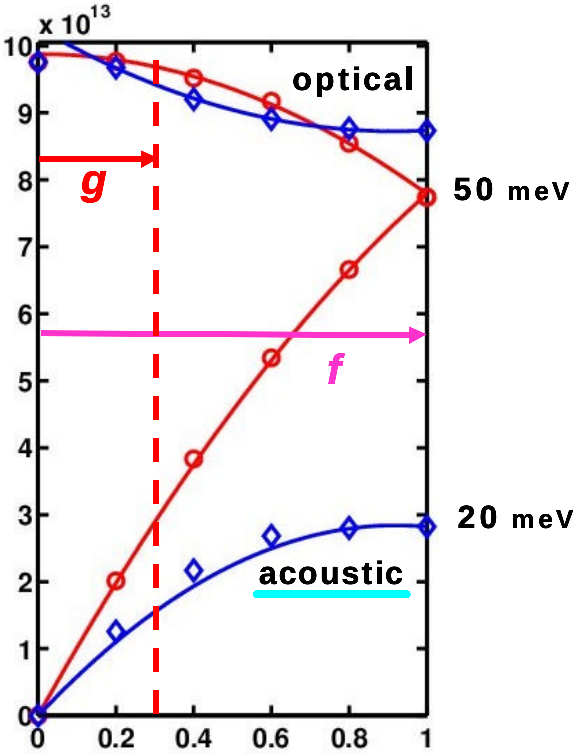
- **Isotropic assumption**
- **Included for**
  - **intra-valley scattering rate**
  - **inter-valley scattering rate**
  - **selection of final state**
- **Easy to invert** $q = f(w)$

- **MONET: first analytic-band Monte Carlo code to distinguish between *ALL* phonon dispersion branches**
- **Easy to extend to other materials, strain, confinement**

Electron-Phonon Scattering



$$\mathbf{k}' = \mathbf{k} \pm \mathbf{q} + \mathbf{G}$$



- *Intra*-valley scattering → acoustic, E < 50 meV *(Normal)*
- *Inter*-valley scattering → *3x* f- and *3x* g-type phonons *(Umklapp)*
- Phonon (q,w) given by geometrical selection rules and dispersion

Scattering (Deformation) Potentials

E. Pop et al, J. Appl. Phys. 2004

$$\boxed{\Gamma_{scat} \sim D_p^2 \left(N_q + \frac{1}{2} \mp \frac{1}{2} \right) g\left(E \pm \hbar w_q\right)}$$

Intra-valley

$$\boxed{\begin{aligned} \Xi_{LA} &= \Xi_d + \Xi_u \cos^2 q \\ \Xi_{TA} &= \Xi_u \sin q \cos q \end{aligned}}$$

Herring & Vogt, 1956

$$\Xi_d \sim 1\,\mathrm{eV}$$
$$\Xi_u \sim 8-10\ \mathrm{eV}$$

Yoder, 1993
Fischetti & Laux, 1996

This work (isotropic, average over q***)***

$$D_{TA} = \sqrt{\left.\left\langle \Xi_{TA}^2 \right\rangle\right|_q} = \frac{\sqrt{p}}{4}\Xi_u$$

$$D_{LA} = \sqrt{\left.\left\langle \Xi_{LA}^2 \right\rangle\right|_q} = \left[\frac{p}{2}\left(\Xi_d^2 + \Xi_d \Xi_u + \frac{3}{8}\Xi_u^2 \right) \right]^{1/2}$$

Average values: D_{LA} = 6.4 eV, D_{TA} = 3.1 eV
(Empirical X_u = 6.8 eV, X_d = 1eV)

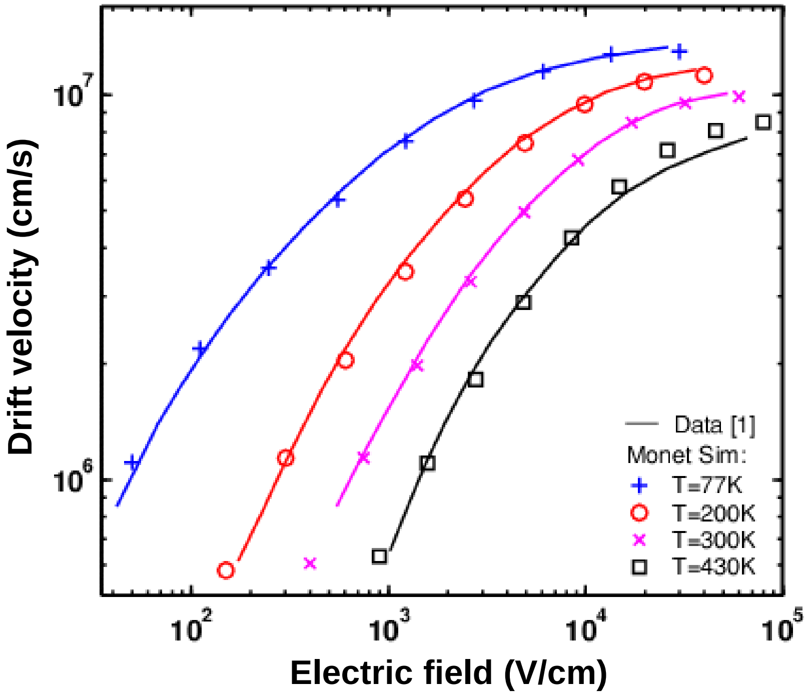
Inter-valley

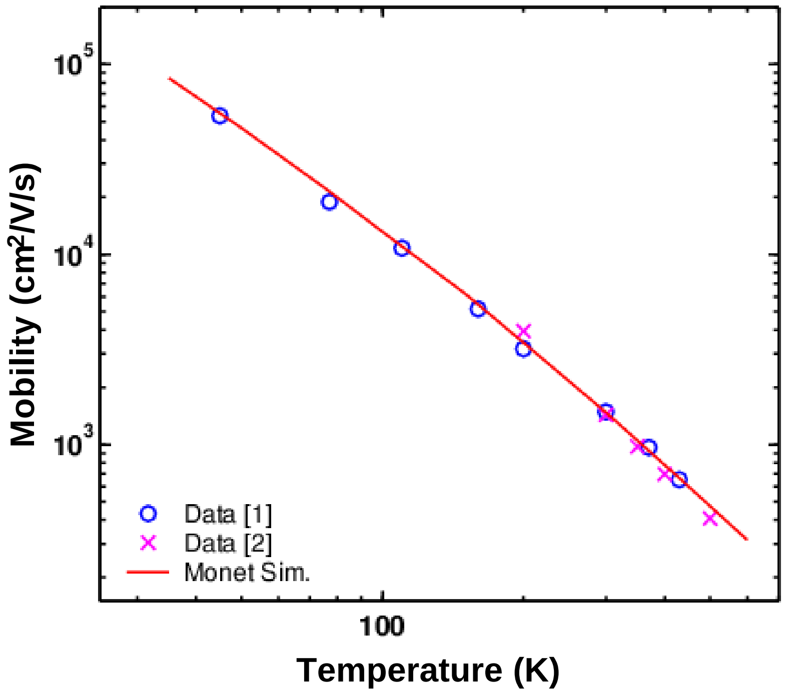
Phonon type	Energy (meV)	Old model* (x 10^8 eV/cm)	This work
f-TA	19	0.3	0.5
f-LA	51	2	3.5**
f-TO	57	2	1.5
g-TA	10	0.5	0.3
g-LA	19	0.8	1.5**
g-LO	63	11	6**

* old model = Jacoboni 1983
** consistent with recent ab initio calculations (Kunikiyo, Hamaguchi et al)

Validation with Bulk Si Transport Data

E. Pop et al, J. Appl. Phys. 2004



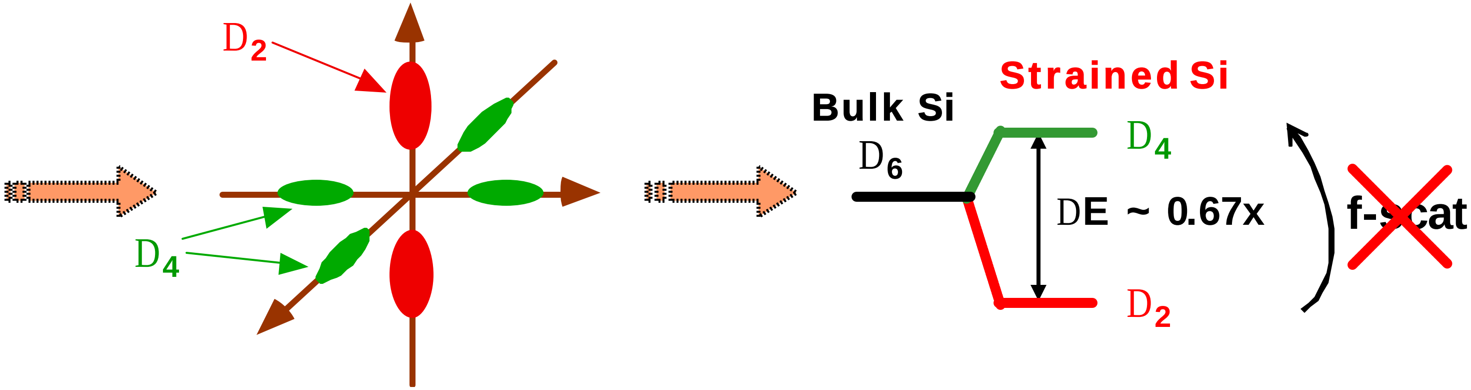


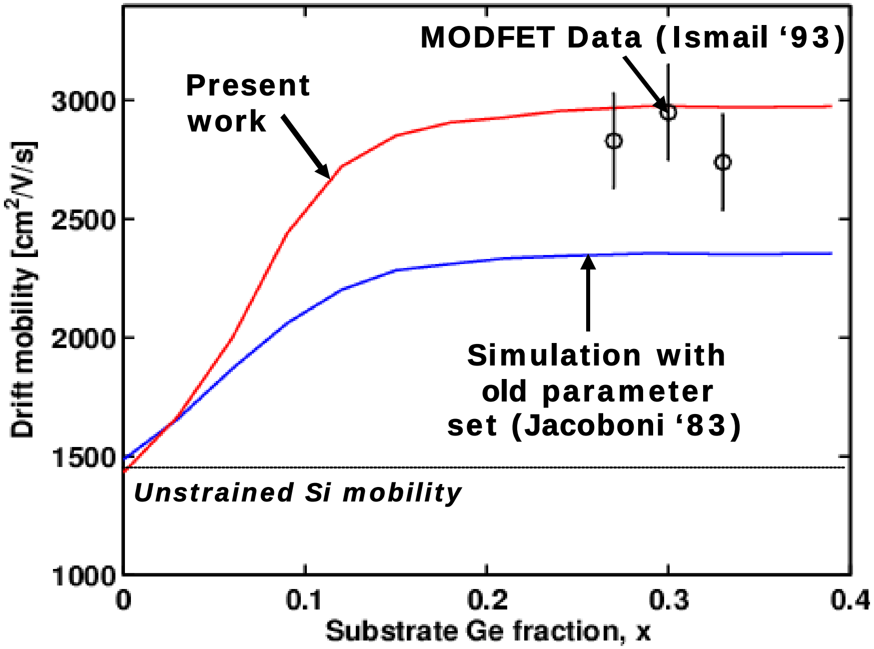
- **Experimental data from [1] Canali ’75, [2] Green ’90**
- **Velocity-field agreement over 77 – 430 K range**
- **Mobility-temperature agreement over 45 – 600 K range**

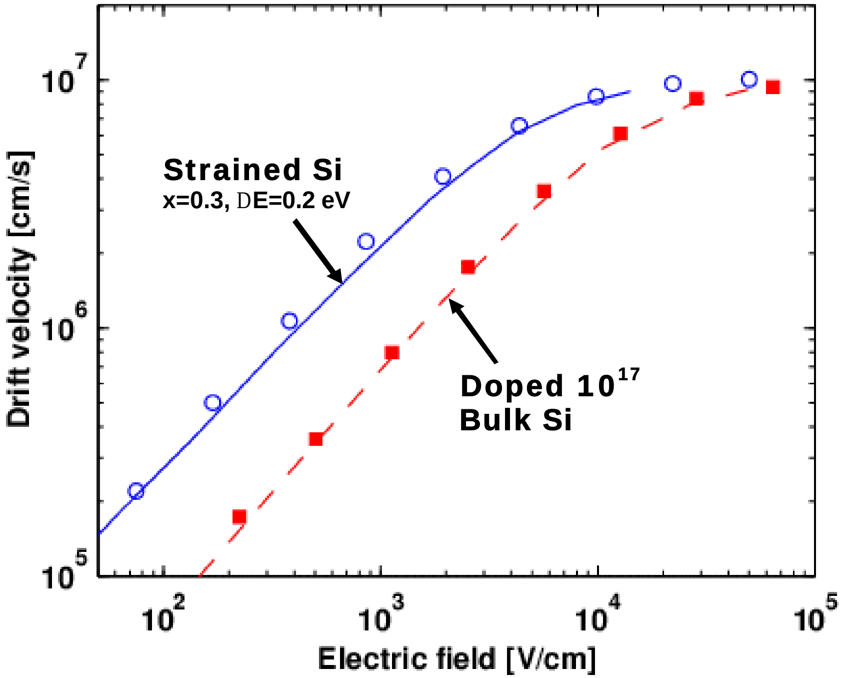
Transport in Strained Si on $Si_{1-x}Ge_x$

E. Pop et al, J. Appl. Phys. 2004

Biaxial tension

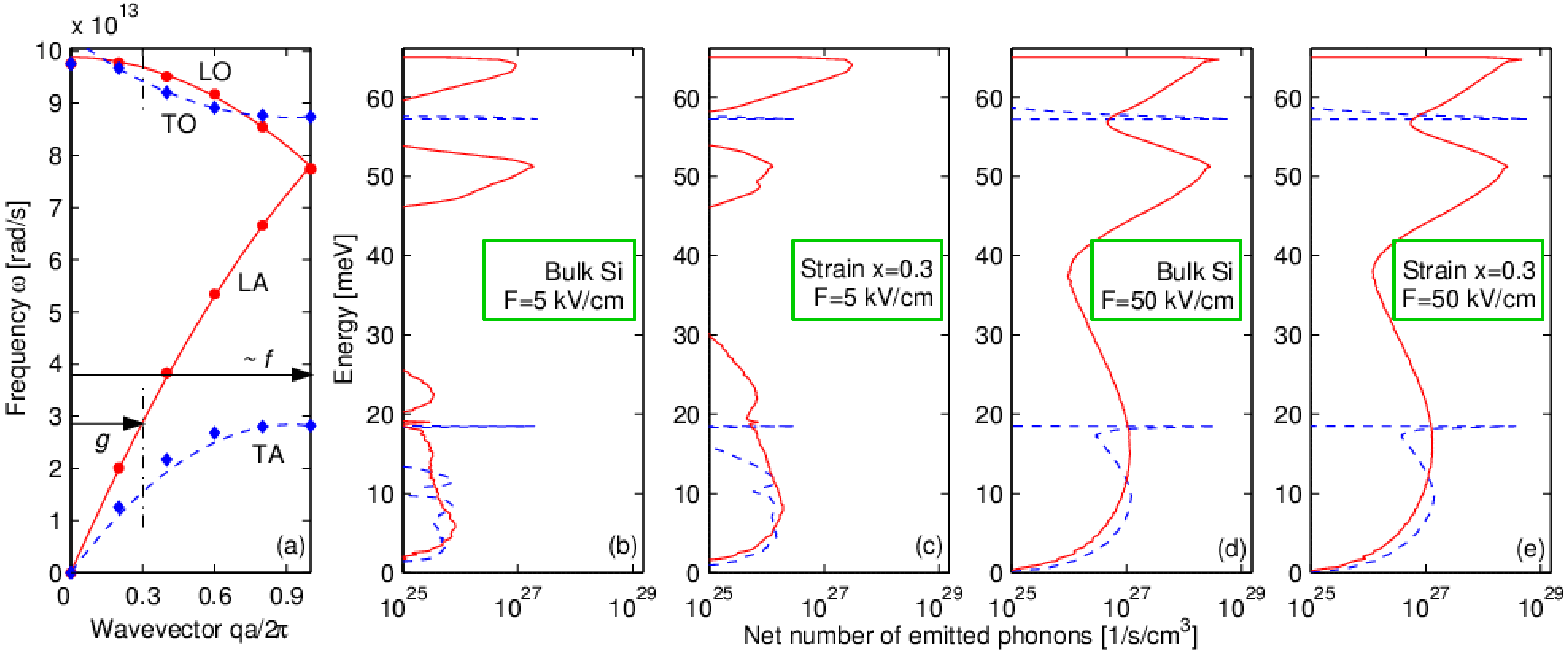






Computed Phonon Generation

E. Pop et al, SISPAD 2003, Appl. Phys. Lett. 2004

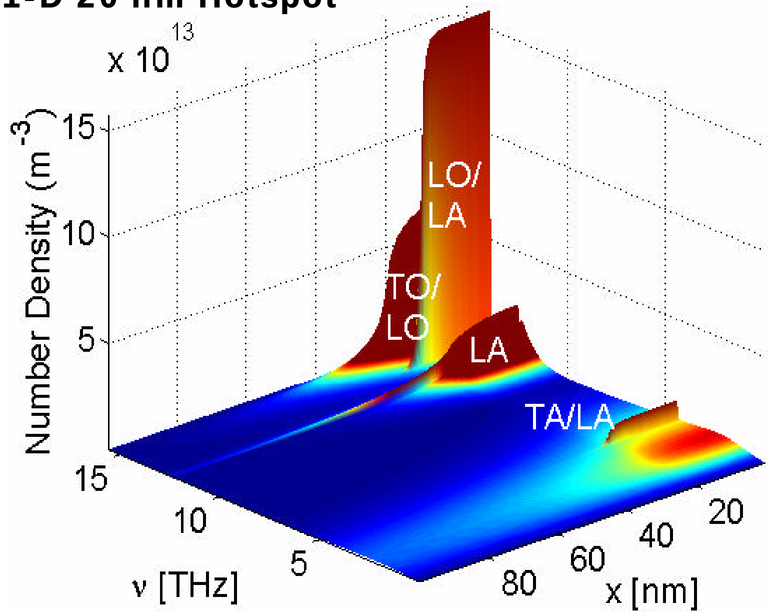


- Complete *spectral* information on phonon generation rates
- Note: effect of scattering selection rules (less f-scat in strained Si)
- Note: same heat generation at high-field in Si and strained Si

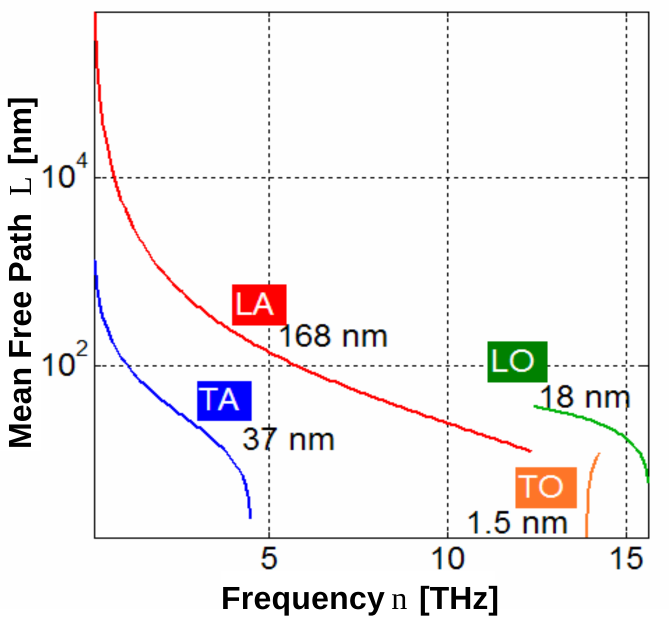
Evolution of Generated Phonons

S. Sinha, E. Pop et al, IMECE 2004 + Thesis work of Sanjiv Sinha

1-D 20 nm Hotspot

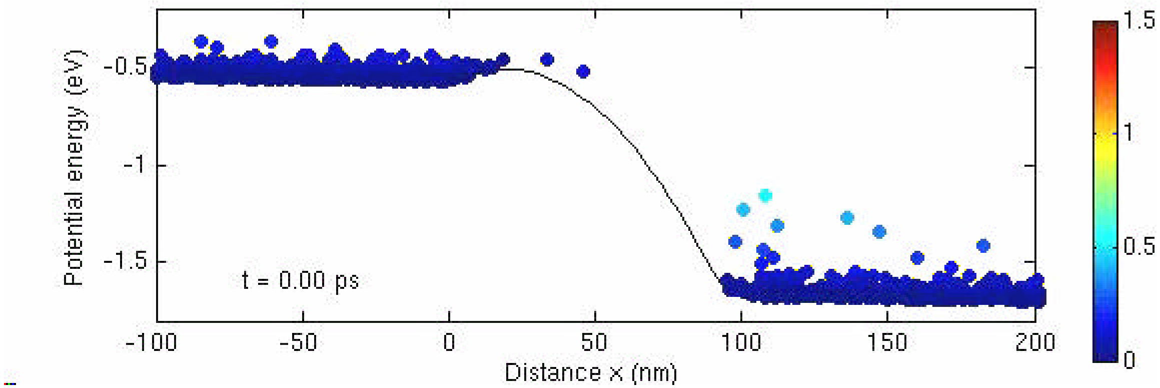


Phonon Mean Free Path (MFP)



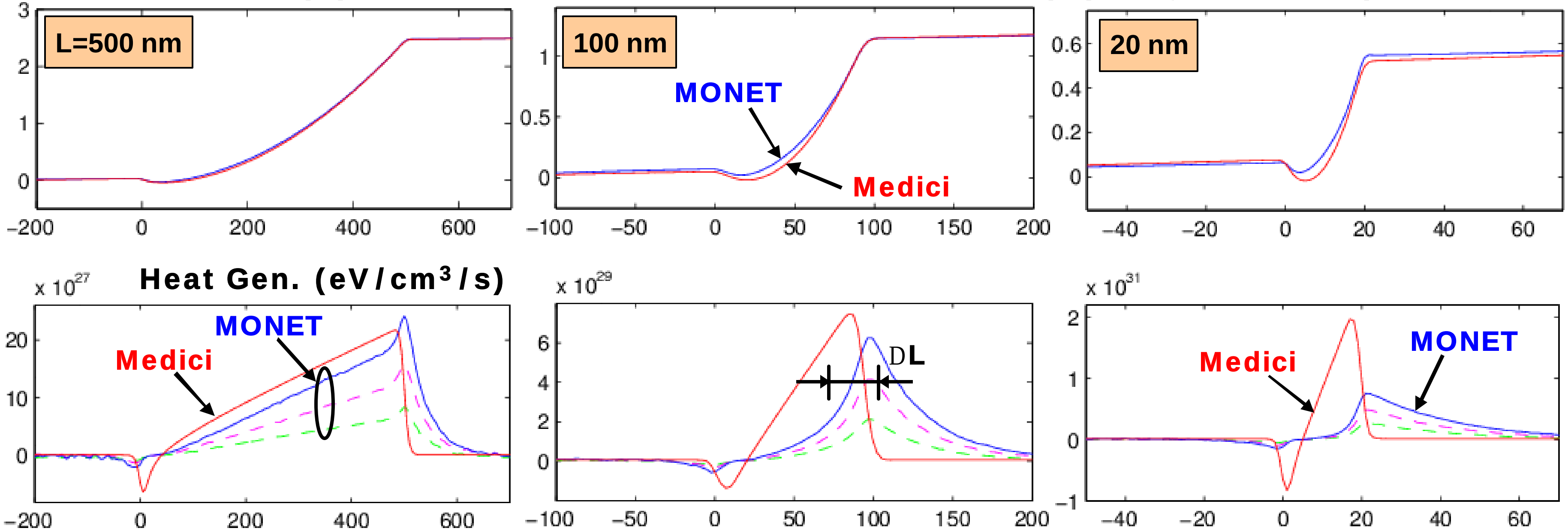
- **Localized temperature near nanoscale heat generation region**
- **Mean free path (MFP) of emitted phonons << MFP of thermal phonons**
- **Phonon relaxation rates depend on peak generation rate in device**

1-D: “N-i-N” Device (Setup)



1-D: “N-i-N” Device (Results)

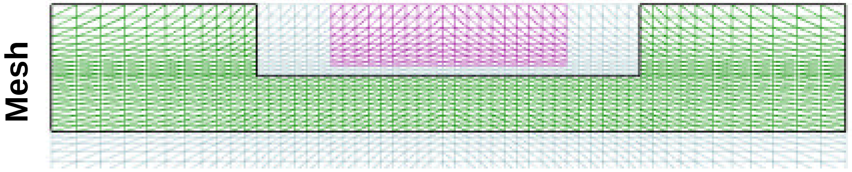
Potential (V) – MONET: self-consistent with Poisson eq. (every DT=0.5 fs)

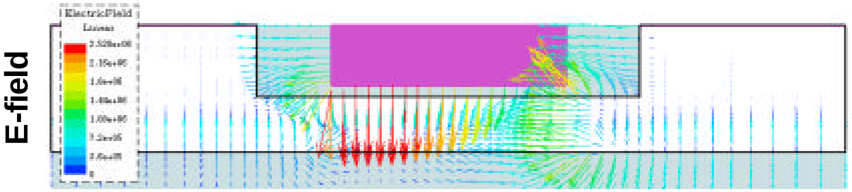


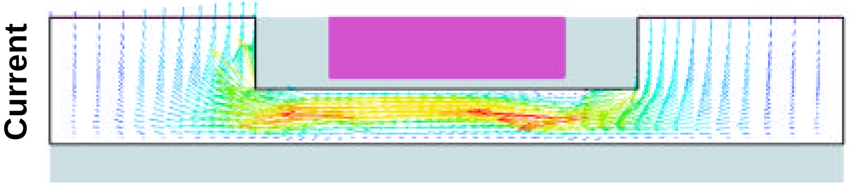
Error: ΔL/L = 0.10 **ΔL/L = 0.38** **ΔL/L = 0.80**

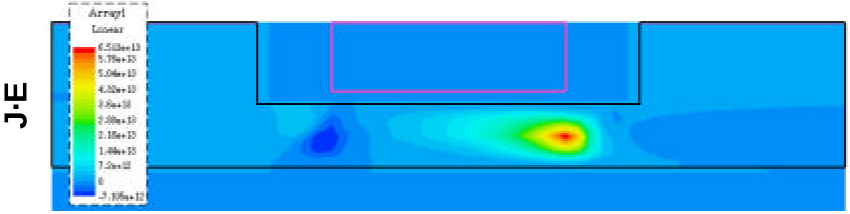
- MONET vs. Medici (commercial code):
    - “Long” (500 nm) device: same current, potential, nearly identical
    - Importance of non-local transport in short devices
    - MONET gives heat gen. rate *location* and *make-up* (optical, acoustic)

2-D: Thin Body SOI (L_g = 18 nm)









Engineer to ITRS Specs:

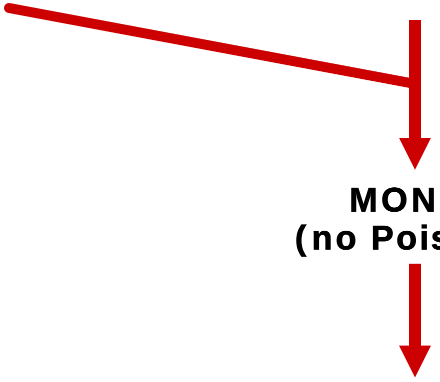
L_G=18 nm, t_{SI}=4.5 nm, t_{OX}=1 nm

N_{SD}=1e20 cm^{-3}, N_{CH}=1e15 cm^{-3}

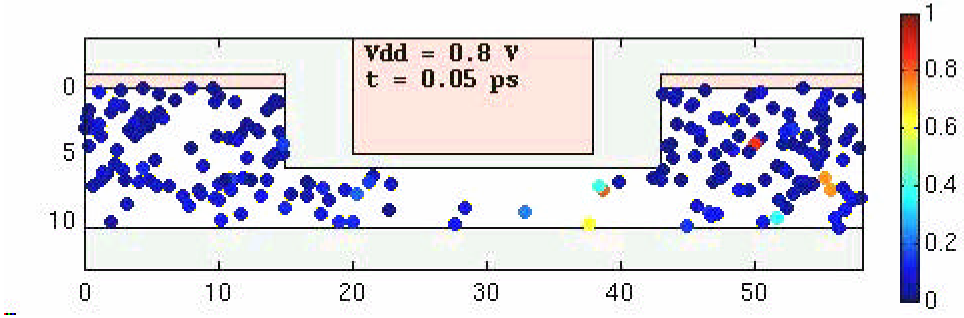
I_{ON}=1000 mA/mm, I_{OFF}=1 mA/mm

F $_{GATE}$=4.53 eV (Mo), V_{DD}=0.8 V

if W/L = 4 then N_{elec} ~ 2500 total!



MONET
(no Poisson)



URL: `http://nanoheat.stanford.edu`
`http://nanohub.org (soon)`

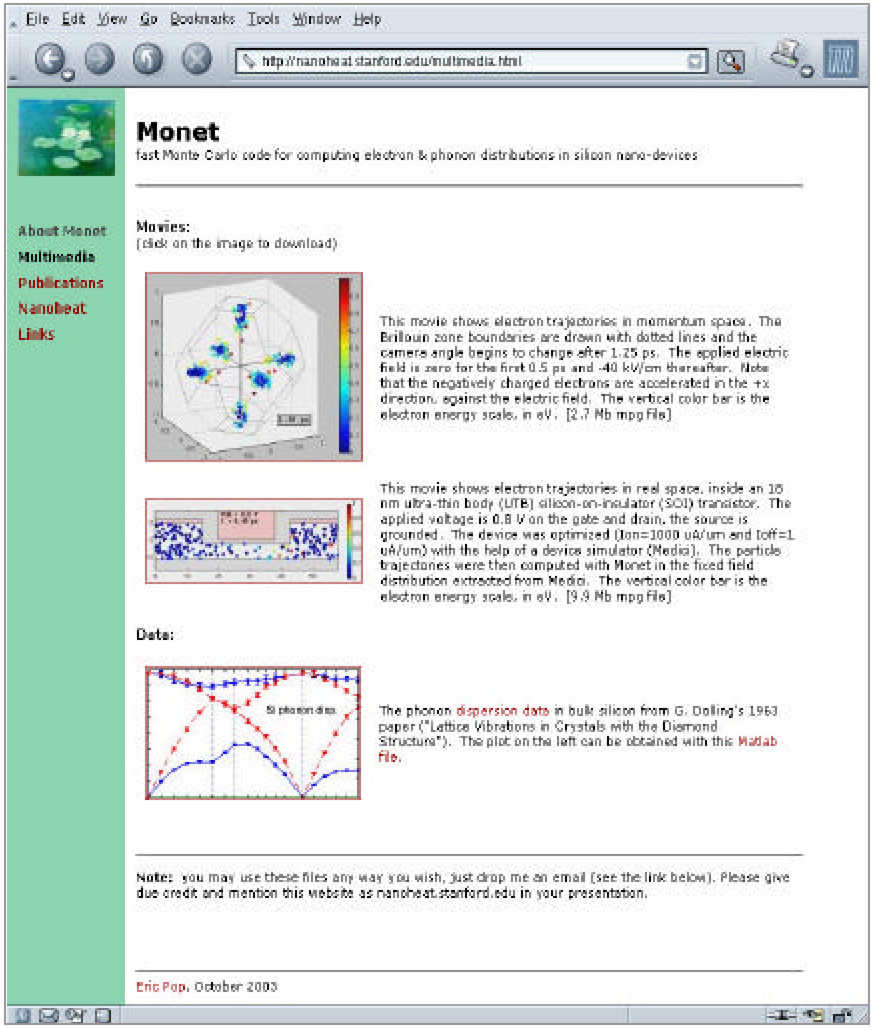
nanoheat.stanford.edu

Monet
Fast Monte Carlo for electron and phonon distributions in nanoelectronic devices

Microheat
Prof. Goodson's Microscale Heat Transfer Group

TCAD
Prof. Dutton's TCAD Group

Seminars
Short list of Stanford Talks, Seminars or Colloquia



Monet

fast Monte Carlo code for computing electron & phonon distributions in silicon nano-devices

Movies:
(click on the image to download)

This movie shows electron trajectories in momentum space. The Brillouin zone boundaries are drawn with dotted lines and the camera angle begins to change after 1.25 ps. The applied electric field is zero for the first 0.5 ps and -40 kV/cm thereafter. Note that the negatively charged electrons are accelerated in the +x direction, against the electric field. The vertical color bar is the electron energy scale, in eV. [2.7 Mb mpg File]

This movie shows electron trajectories in real space, inside an 18 nm ultra-thin body (UTB) silicon-on-insulator (SOI) transistor. The applied voltage is 0.8 V on the gate and drain, the source is grounded. The device was optimized (Ion=1000 uA/um and Ioff=1 uA/um) with the help of a device simulator (Medici). The particle trajectories were then computed with Monet in the fixed field distribution extracted from Medici. The vertical color bar is the electron energy scale, in eV. [9.9 Mb mpg File]

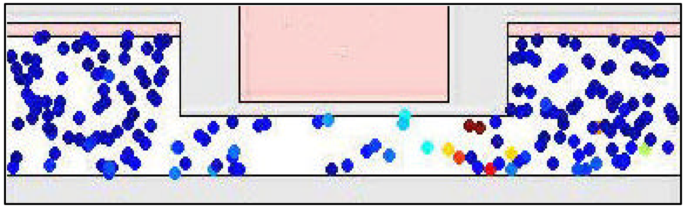
Data:

The phonon dispersion data in bulk silicon from G. Dolling's 1963 paper ("Lattice Vibrations in Crystals with the Diamond Structure"). The plot on the left can be obtained with this Matlab File.

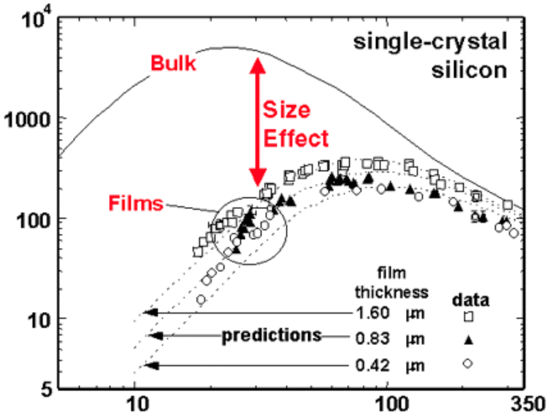
Note: you may use these files any way you wish, just drop me an email (see the link below). Please give due credit and mention this website as nanoheat.stanford.edu in your presentation.

Eric Pop, October 2003

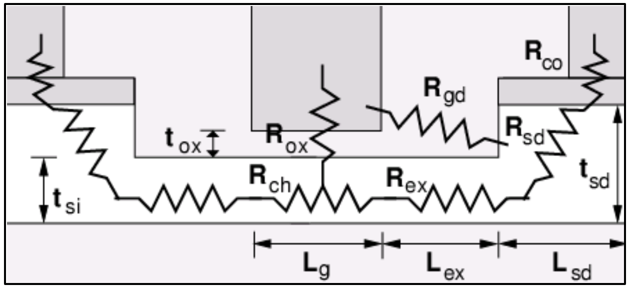
What About Device Design?



Monte Carlo Analysis

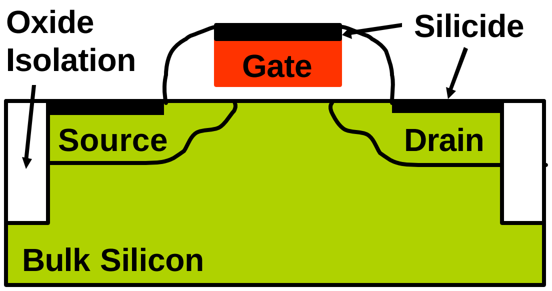


Thermal Conductivity

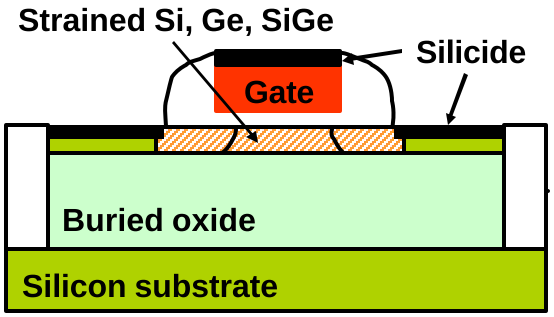


Design and Scaling

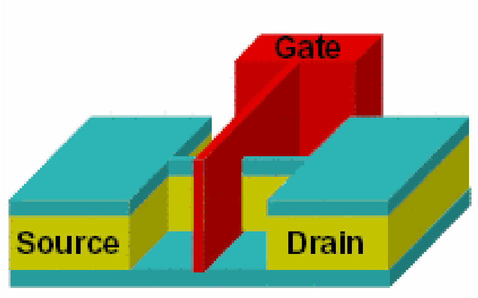
Evolution of Transistor Designs



Bulk FET



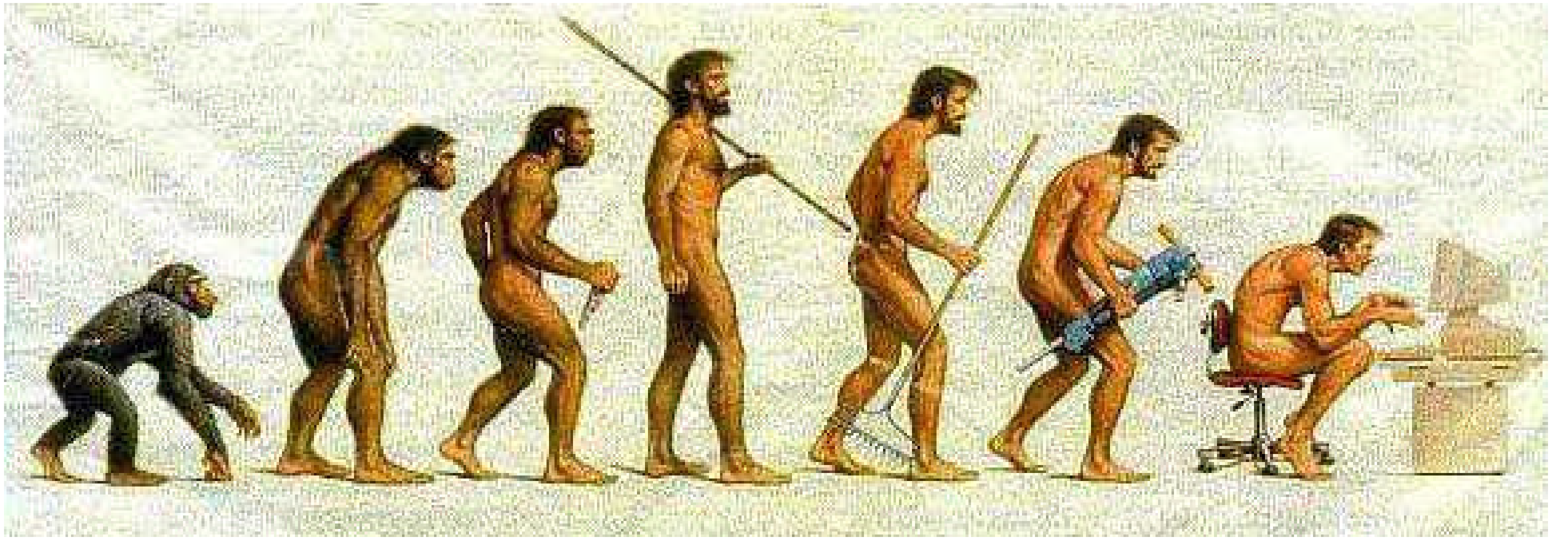
(Strained) Si/Ge-O-I



FinFET

- **Bulk FET: “workhorse” of semiconductor industry**
- **Strained Si or Ge channel: mobility improvement**
- **Thin Body on Insulator (SOI, GOI) and FinFET: less parasitics and better channel control, *poor thermal properties***

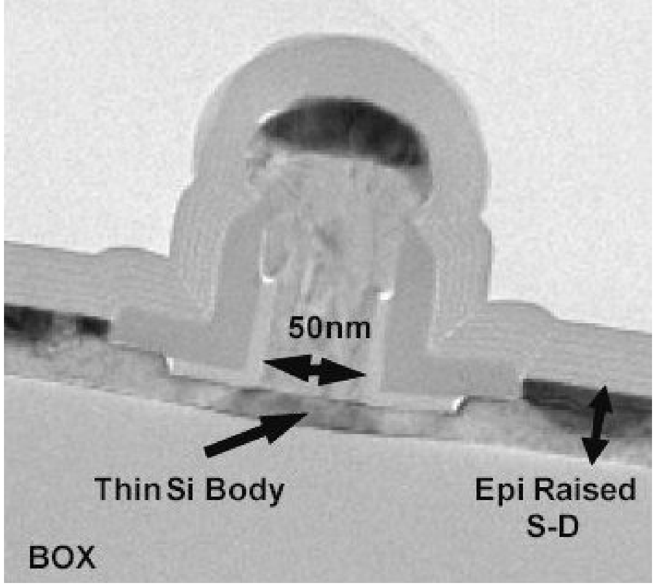
...transistor evolution, from a *thermal* perspective, is not going so well.



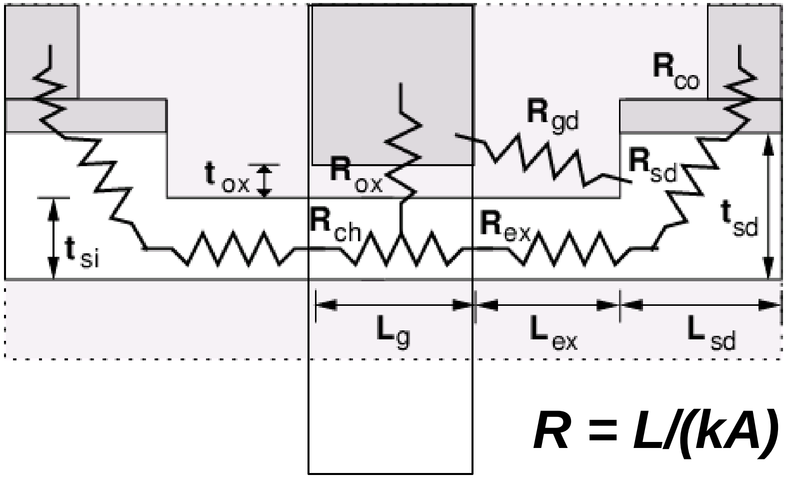
Somewhere, something went terribly wrong.

Ultra-Thin Body Transistor

E. Pop et al, IEDM 2003, IEDM 2004



Intel DST/SOI Transistor (*IEDM 2001*)



$R = L/(kA)$

Scaling:

$L_{ex} \sim L_g/2$
$L_{sd} \sim L_g$
$t_{si} \sim L_g/4$

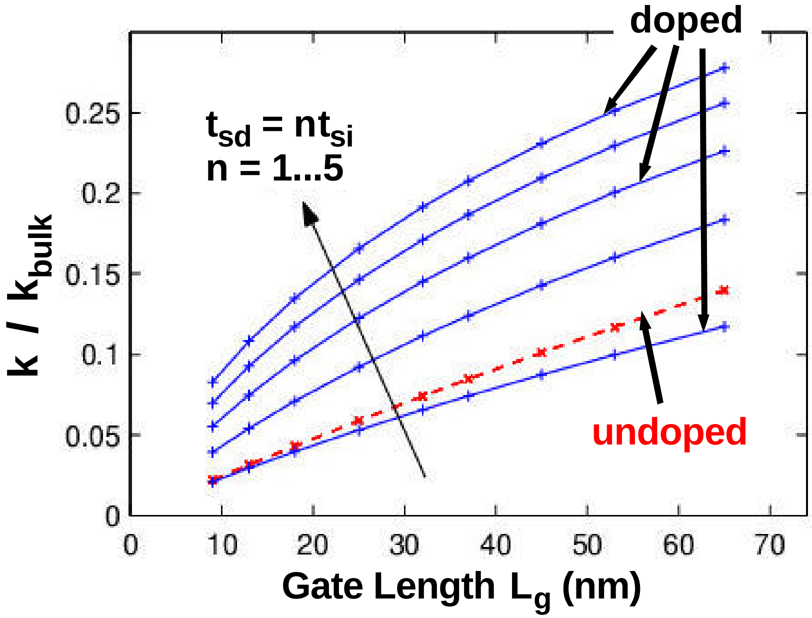
$t_{sd} \sim 2t_{si}$
$W \sim 3L_g$
$A_{co} \sim 2L_g \times L_g$

I_{on}, V_{dd}, t_{ox} from ITRS guidelines.

Metal gate sets V_t

FinFET: $t_{si} \sim L_g/2$, $h_{fin} \sim 4t_{si}$

Thin Film Thermal Conductivity



$$k = \frac{1}{3} C v \Lambda$$

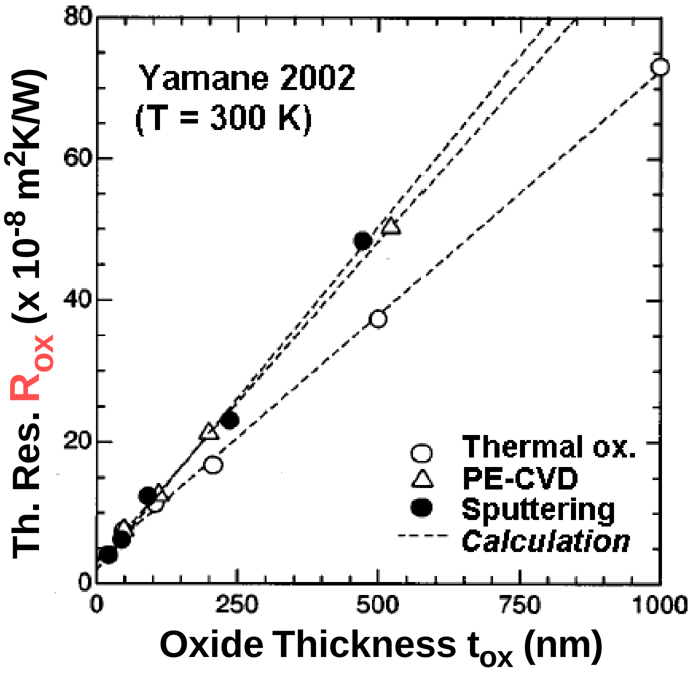
$$\Lambda^{-1} \cong \Lambda_{bulk}^{-1} + t_{si}^{-1} + \Lambda_{imp}^{-1}$$

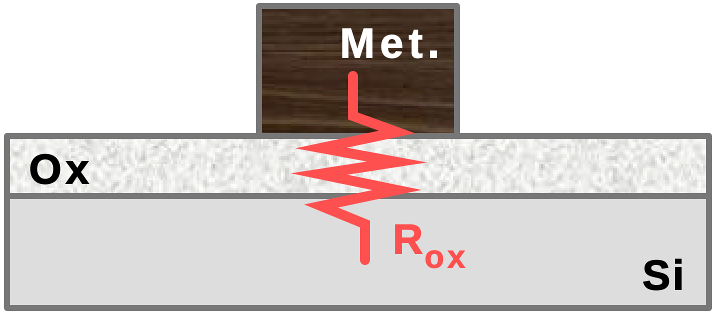
$$k_{bulk} = 148\ \mathrm{W/m \cdot K} \quad \mathrm{(Si)}$$

- **Phonon boundary and impurity scattering**

  → strong decrease of thermal conductivity (*k*)
- **Thin Si: 20 nm → 22 W/m·K (expt), 10 nm → 13 W/m·K (theory)**
- **Assume t_{si} ~ L_g/4 for fully depleted thin-body SOI devices**

Metal-Ox-Si Thermal Resistance



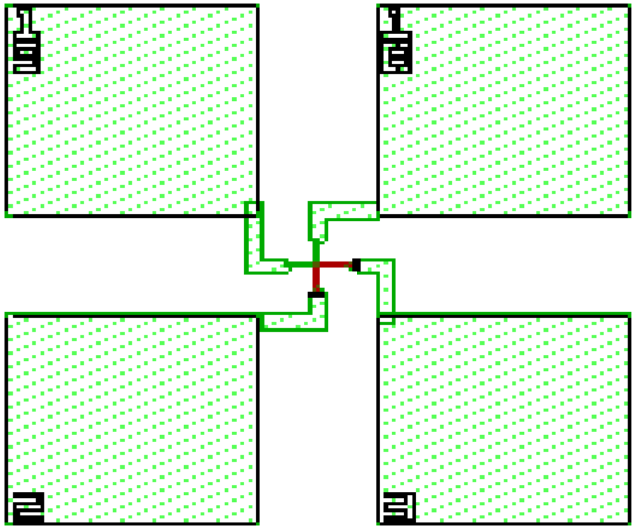


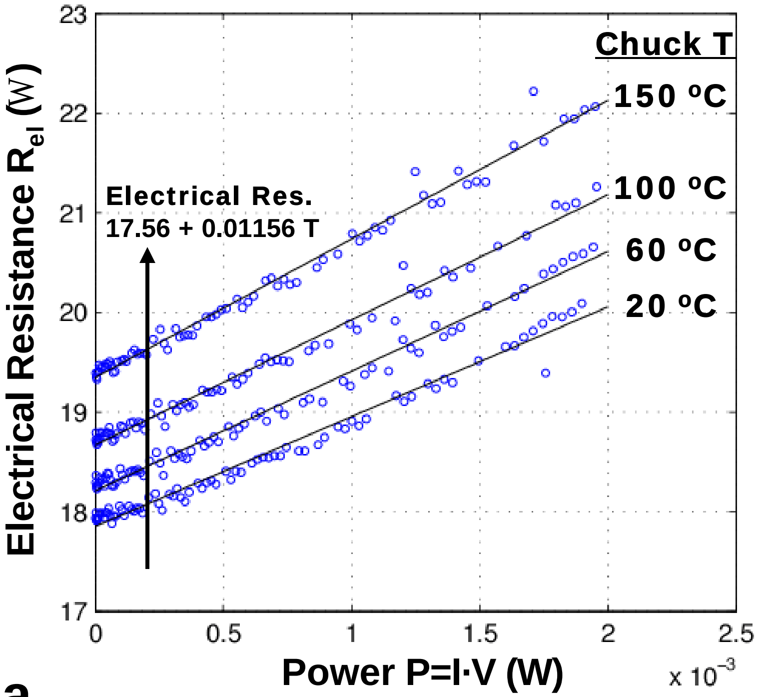
$$R_{ox} = t_{ox} / (k_{ox} A) + R_i / A$$

$$R_i \sim 2\times10^{-8}\ \mathrm{m^2K/W}$$
$\sim$ 20 nm oxide

- Where does MOS <u>boundary</u> thermal resistance come from?
  - Phonon dispersion mismatch between materials
  - Phonon (dielectric) → electron (metal) heat carrier conversion at boundary
  - Small (metal) grains or atomic roughness at boundary

Contact and Via *Thermal* Resistance





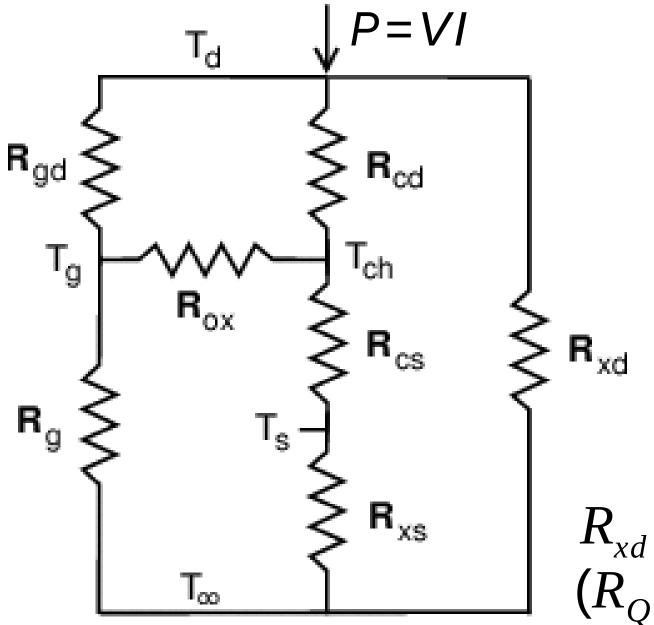
Electrical Res.
17.56 + 0.01156 T

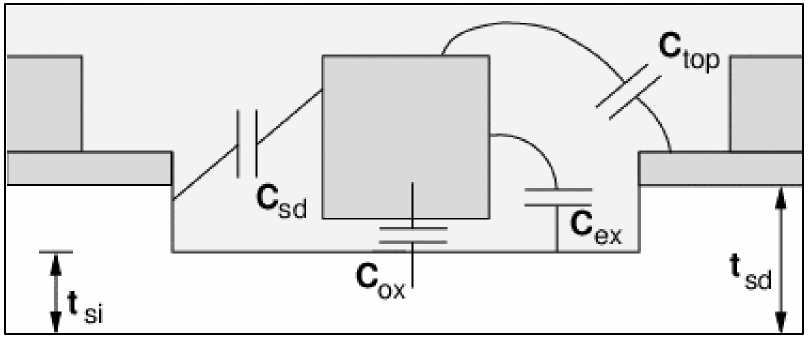
- Significant for small contact area
- Wafers (Kelvin probes) from T.I.
- Electrical resistance thermometry
- I-V measurements at various T:

T → R_{el}(T), then R_{el}(P=IV) → T(P) → R_{th}

Lumped Thermal Resistance
R_{th} ~ 1.1 x 10^5 K/W
(from via to thermal ground)

Self-Consistent Electro-Thermal Model

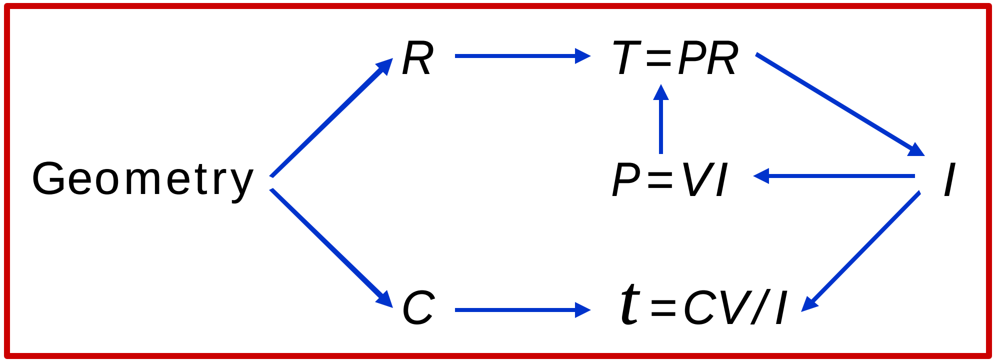




$$C_{ex} = 2\beta\epsilon_{sw} \ln\left(1 + L_{ex} / t_{ox}\right) / \pi$$

$$R_{xd} = R_{ex} \pm R_Q + R_{sd} + R_{co}$$

(R_Q due to heat source position)



Geometry

R

$T=PR$

$P=VI$

I

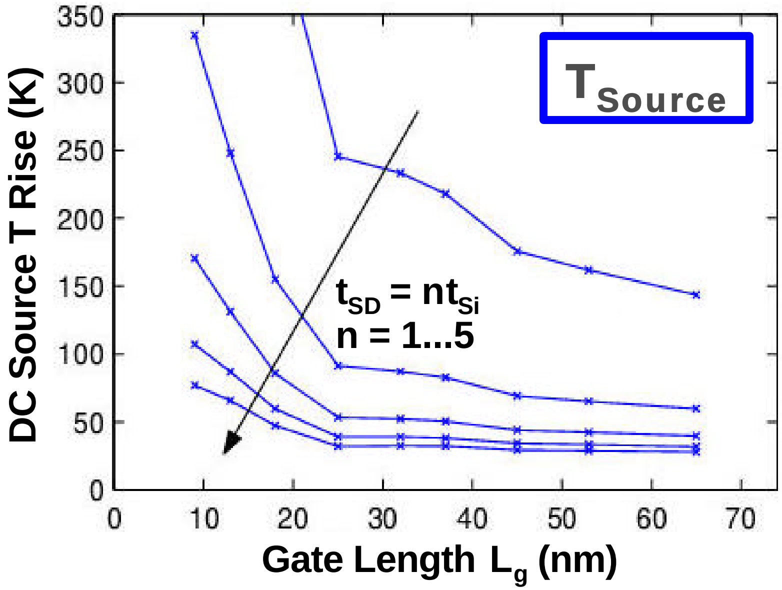
C

$t=CV/I$

$$I \sim \overset{T^{-1.4}}{\overset{\downarrow}{\mu}} \times \left(V_{dd} - \underset{-0.7\text{ mV/K}}{\underset{\uparrow}{V_t}}\right)^n$$

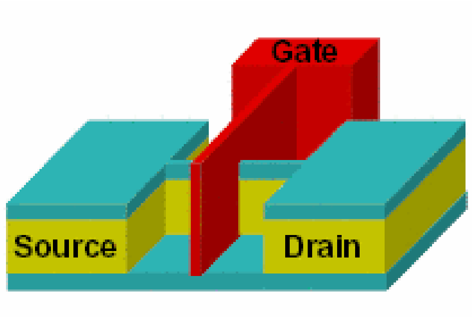
Temperature Rise along ITRS

E. Pop et al, IEDM 2003



- **Jenkins ’04: exp. observed ΔT = 100 °C (DC) in 100 nm SOI**
- **Plot source-side ΔT with S/D height (t_{SD}) as parameter**
- **Raised Source/Drain (S/D) adopted to reduce electrical R_{series}**
- **Extra thickness (t_{SD}) also reduces S/D *thermal* resistance → lower device T (with fixed L_{ex} ~ $L_g/2$)**

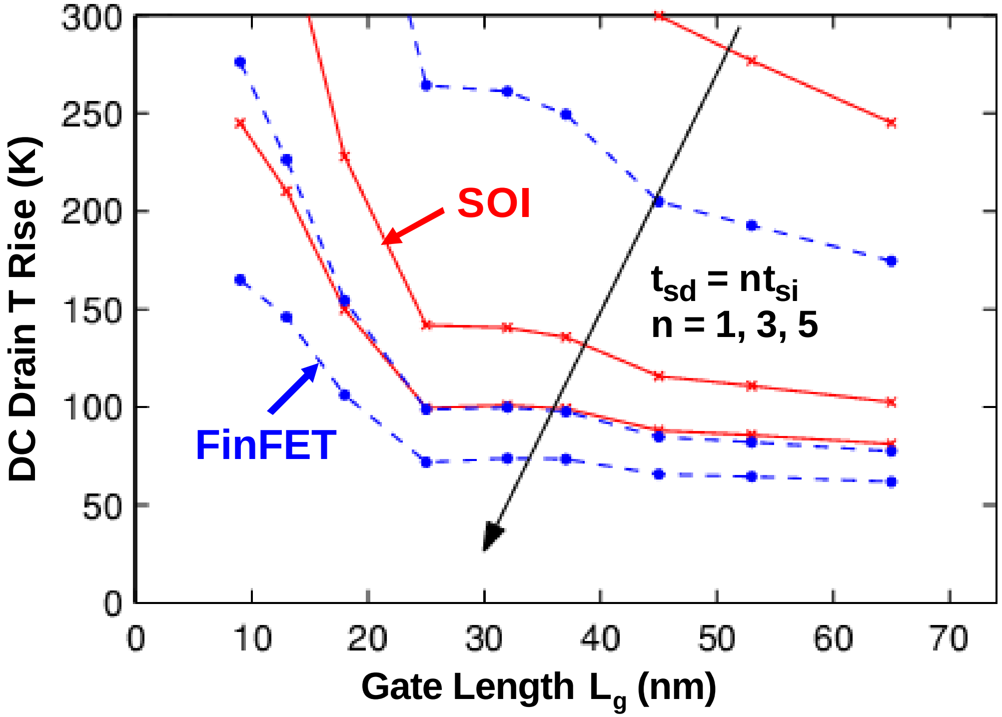
SOI Comparison with FinFET



SOI: t_{si} ~ $L_g/4$

vs.

FinFET: t_{fin} ~ $L_g/2$

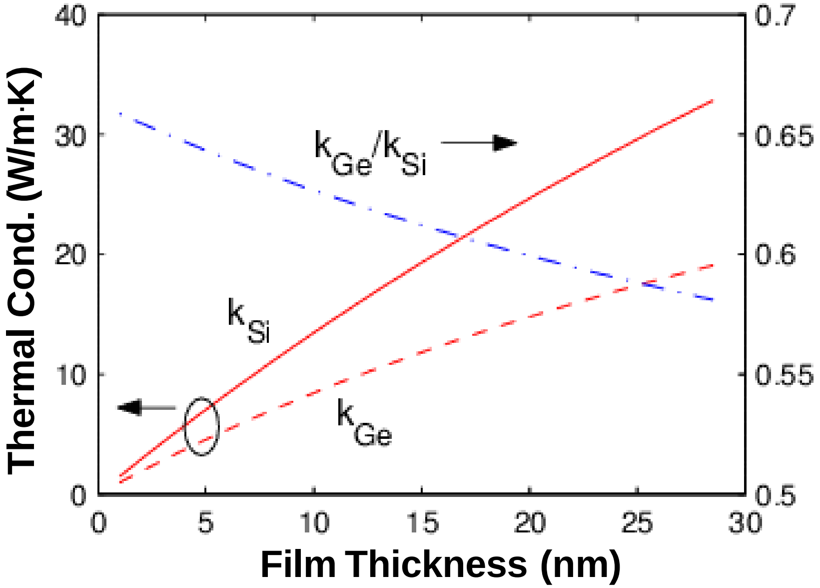


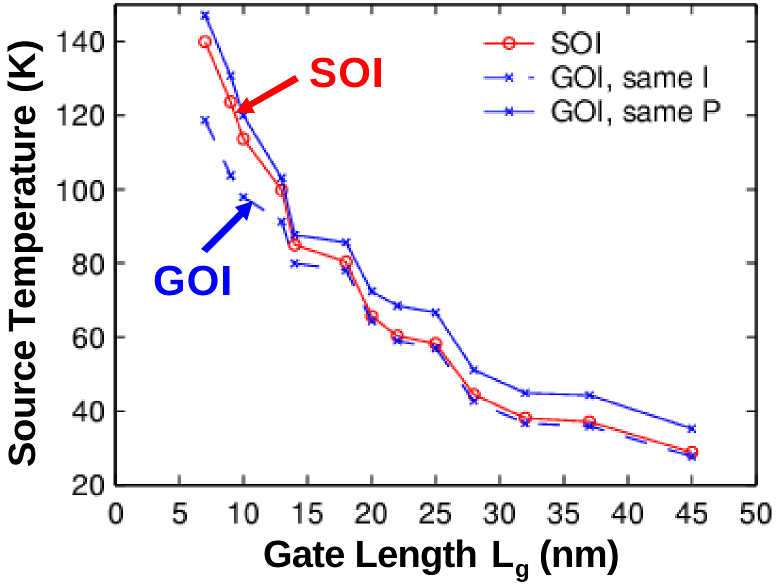
- **FinFET vs. SOI, thermally speaking:**
  - **Fin height assumed ~ L_g → k_{th} ¯ → T -**
  - **2x thicker body → k_{th} - → T ¯**
  - **2x oxide area → $R_{ox}/2$ → T ¯**

FinFET overall T ¯

SOI Comparison with G(ermanium)-O-I

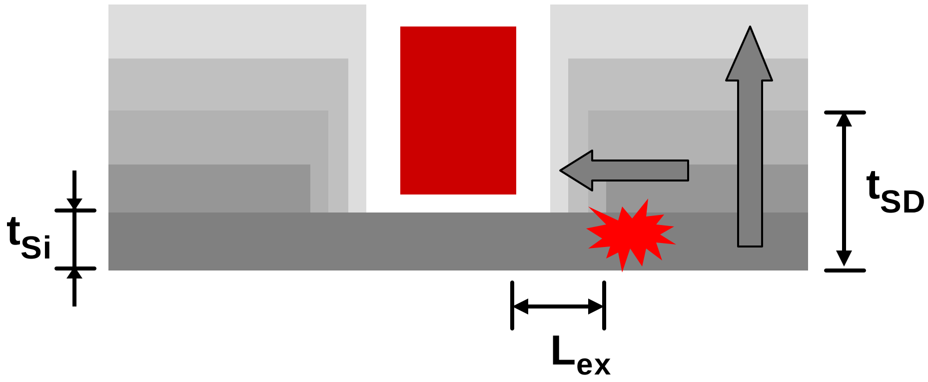
E. Pop, C.O. Chui et al, IEDM 2004

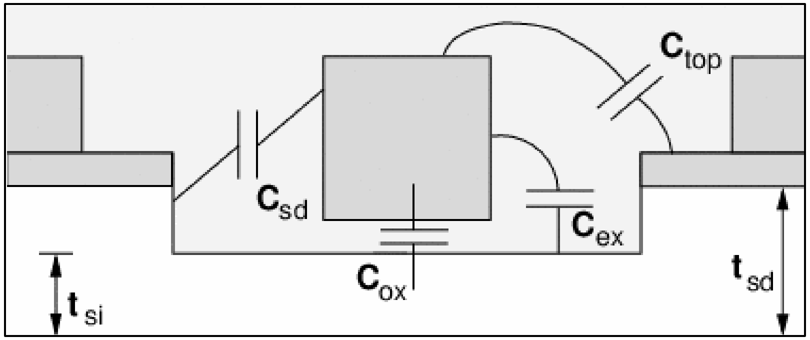




- Thin film $k_{Ge} < k_{Si}$ but not as badly as in bulk (60 vs. 148 W/m·K)
- Ge has 2x mobility advantage, 40% lower V_{dd}, lower power
- GOI devices → assume $t_{Ge} = 3/4t_{Si}$ where $t_{Si} = L_g/4$
- T about same, Ge retains mobility + current advantage

Extension and Raised Drain Design



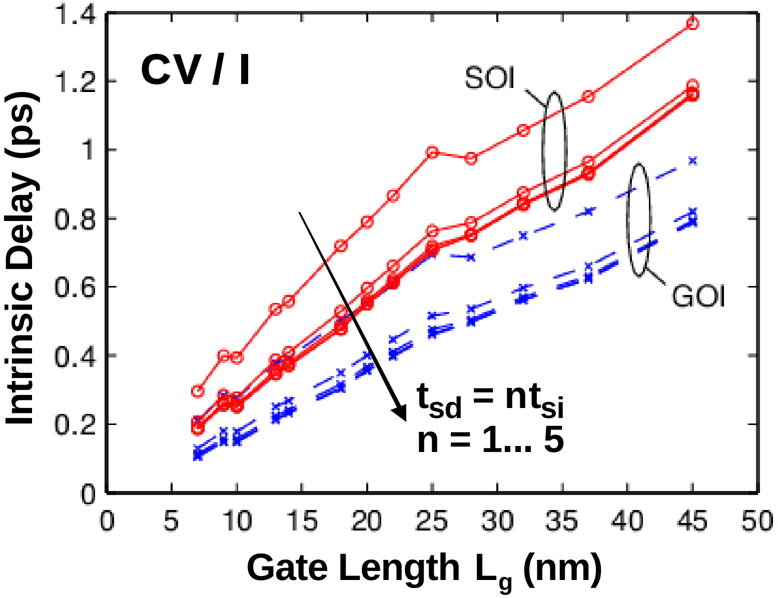


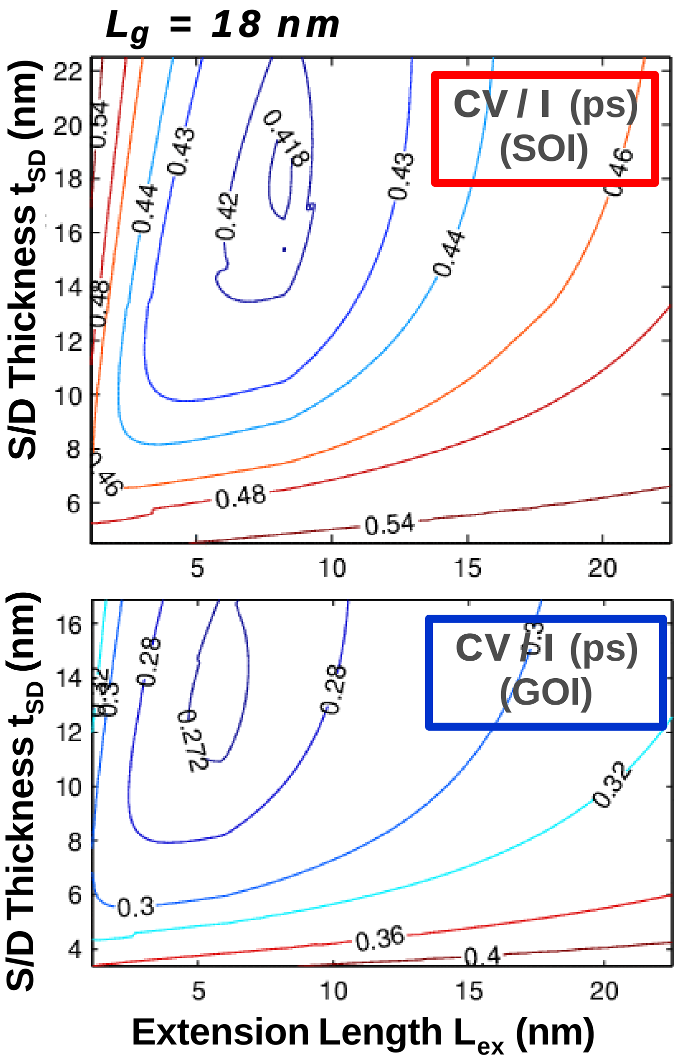
What about parasitic capacitance and speed?

- Choose channel extension length L_{ex} and S/D thickness t_{SD}
- Ideally want (*thermally*) → short L_{ex} and raised t_{SD}
- But... must also consider gate-drain capacitance, dopant diffusion, spacer control, silicide thickness

Intrinsic Gate Delay Optimization

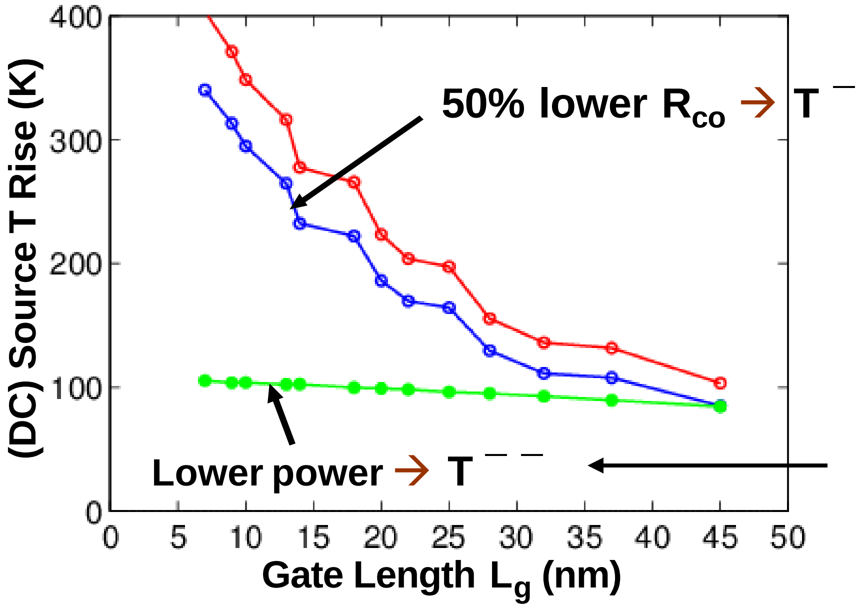
E. Pop et al, IEDM 2004





- Delay not lower for S/D > 3-4 x t_{film}
- Optimal extension length ~ $L_g/2$
- Optimized GOI devices 30% faster than optimized SOI

Role of Contact Resistance and Power



Power down-scaled *quadratically*:

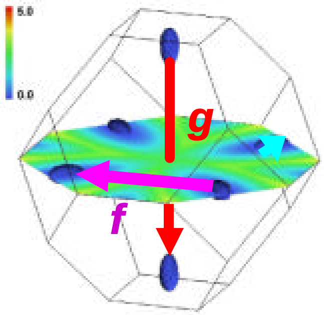
$$Q = I \cdot V = -0.17 L_g^2 + 27.5 L_g \quad (L_g \textit{ in nm})$$

- **Device contacts can be used to spread heat → more work must be done to better understand them thermally**
- **ITRS guidelines for power too high for shrinking device volumes**
  - **(either) Lower power reqt. (e.g. quadratically) for smallest SOI**
  - **(or) Use sparingly, operate at very low duty factor**

Summary

- **Self-heating in bulk and strained silicon**
- **Monte Carlo code (MONET):**
    - **Implementation → electron and phonon model**
    - **Validation → vs. data and commercial codes**
    - **Results → heat generation spectrum**

      → location and make-up of drain hotspot
- **Thermal scaling limits of nano-transistors**
    - **Compact model for thin body devices**
    - **Electro-thermal geometry optimization**
    - **FinFET, GOI advantage over SOI**



Contributions

- **E. Pop**, K. E. Goodson, R. W. Dutton, "Analytic Band Monte Carlo Model for Electron Transport in Si Including Acoustic and Optical Phonon Dispersion," (to appear) *J. Appl. Phys.*, vol. 96, no. 7, Oct. 1st 2004
- **E. Pop**, C. O. Chui, S. Sinha, R. W. Dutton, K. E. Goodson, "Electro-Thermal Comparison and Performance Optimization of Thin-Body SOI and GOI MOSFETs," (submitted to) *IEDM 2004*
- S. Sinha, **E. Pop**, K. E. Goodson, "A split-flux model for phonon transport near hotspots," *IMECE 2004*
- **E. Pop**, R. W. Dutton, K. E. Goodson, "Compact Thermal Model for Ultra-Thin Body SOI Devices," (submitted to) *Electron Device Letters*, 2004
- **E. Pop**, K. E. Goodson, R. W. Dutton, "Thermal Analysis of Ultra-Thin Body Device Scaling," *IEDM 2003*
- **E. Pop**, K. E. Goodson, R. W. Dutton, "Detailed Heat Generation Simulations via the Monte Carlo Method," *SISPAD 2003*
- **E. Pop**, K. E. Goodson, R. W. Dutton, "Monte Carlo Simulation of Heat Generation in Silicon Nano-Devices," *SRC TechCon 2003*, (Best Paper in Session Award)
- **E. Pop**, S. Sinha, K. E. Goodson, "Monte Carlo Modeling of Heat Generation in Electronic Nanostructures," *IMECE 2002*
- **E. Pop**, "Heat Generation in Three- and Two-Dimensional Nanostructures," *SRC GFP Conference 2002*, (Outstanding Research Presentation Award)
- **E. Pop**, K. Banerjee, P.G. Sverdrup, R. W. Dutton, K. E. Goodson, "Localized Heating Effects and Scaling of Sub-0.18 Micron CMOS Devices," *IEDM 2001*

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