

Demonstration of Vertical GaN PN Diode with Step-etched Triple zone JTE

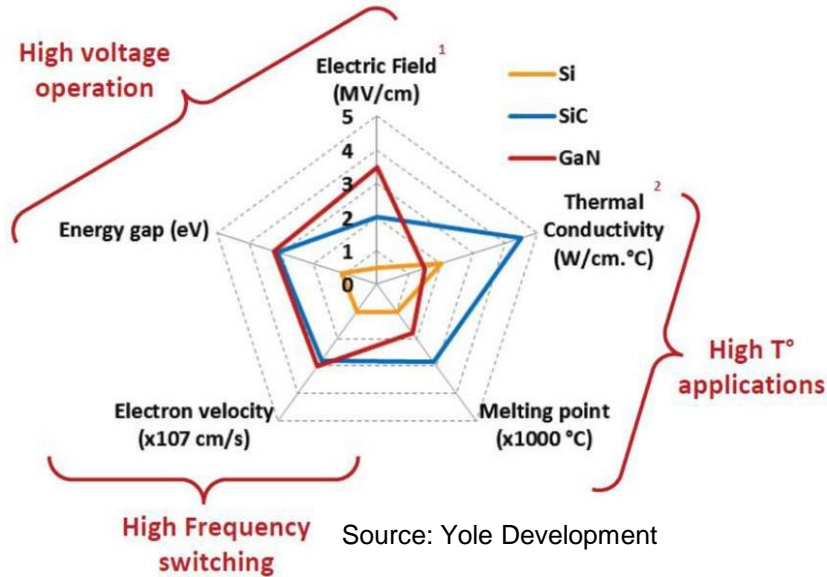
Hyun-Soo Lee, Yuxuan Zhang, Zhaoying Chen, Mohammad Wahidur Rahman,
Hongping Zhao, and Siddharth Rajan

Department of Electrical and Computer Engineering, The Ohio State University



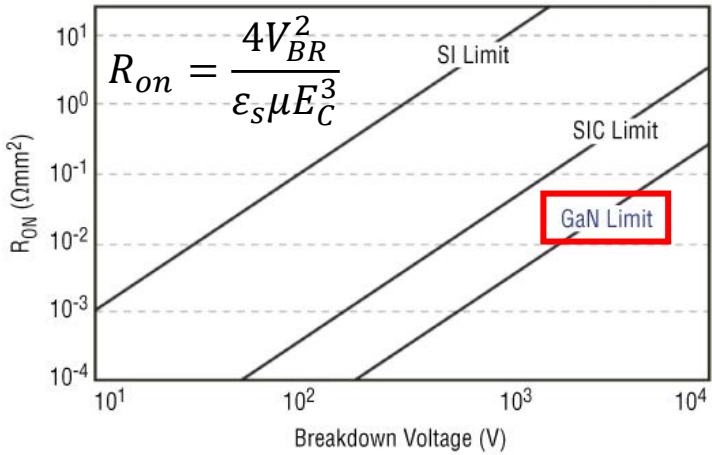
Sponsored by the Advanced Research Projects
Agency-Energy (ARPA-E), DE-AR0001036
Program Manager: Dr. Isik C. Kizilyalli

- 1. Edge Termination for GaN Power Devices**
2. Design of Edge Termination
3. Experimental Approach and Results



| Properties | Si | 4H-SiC | GaN |
|---|------|--------|------|
| E_g [eV] | 1.1 | 3.3 | 3.4 |
| E_C [MV/cm] | 0.3 | 2.5 | 3.3 |
| μ [$\text{cm}^2/\text{V}\cdot\text{s}$] | 1400 | 1000 | 1200 |
| BFOM [$\epsilon_s \mu E_C^3$] | 1 | 340 | 870 |

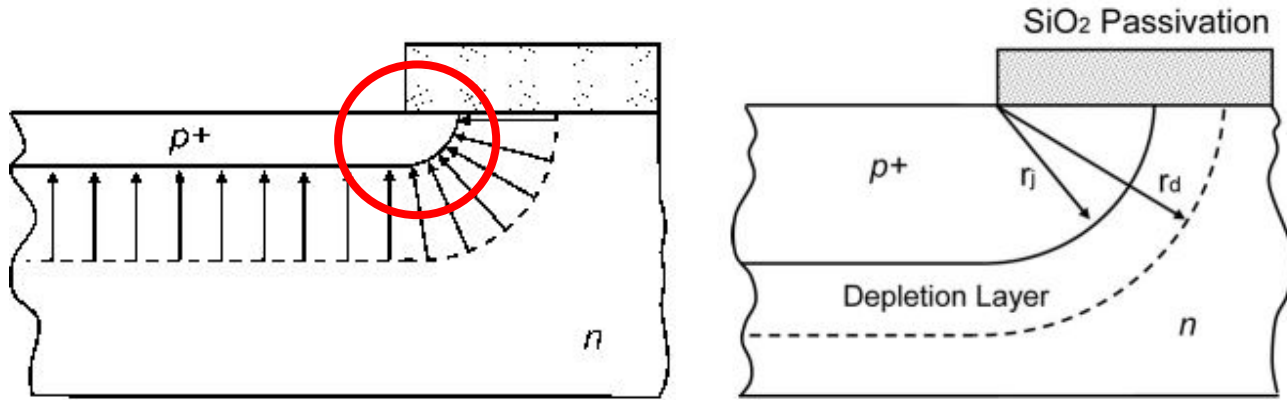
Source: ON Semiconductor



Key factors

- High electron mobility and critical electric field**
→ Promising material for power devices
- Vertical topology**
→ high current density with small area, easy to package
- Bulk substrate with low dislocation density (<math><10^6 \text{ cm}^{-2}</math>)**
→ Improved reliability, yield, and reverse characteristics

Edge Termination for Vertical Devices



r_d : depletion region edge
 r_j : junction depth

$$E_{max,Parallel} = \frac{qN_D r_d}{\epsilon_0 \epsilon_s}$$

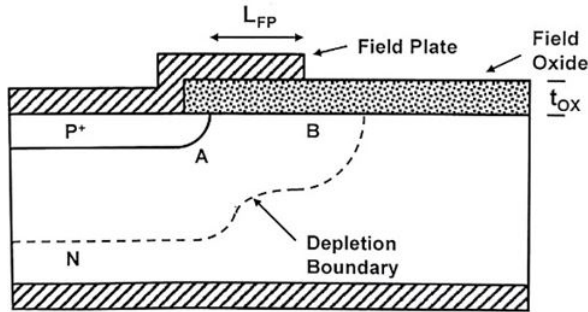
$$E_{max,Cylindrical} = \frac{qN_D r_d^2}{2\epsilon_0 \epsilon_s r_j}$$

$$\frac{E_{m,Cylindrical}}{E_{m,Parallel}} = \frac{r_d}{2r_j}$$

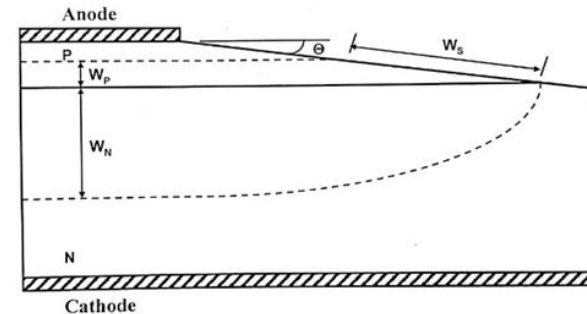
- ❖ **Proper edge termination techniques to achieve ideal breakdown voltage**
- ✓ **Premature breakdown of power devices without edge termination due to effects of field crowding at the junction periphery**
- ✓ **Make near-parallel junction (to avoid cylindrical junction)**
- If the junction depth is 1 μm and the depletion region is 10 μm , the maximum electric field at cylindrical junction will be 5 times larger than parallel junction case
- The maximum electric field at spherical junction is much higher than cylindrical junction case

Source: https://ebrary.net/82339/computer_science/cylindrical_junction

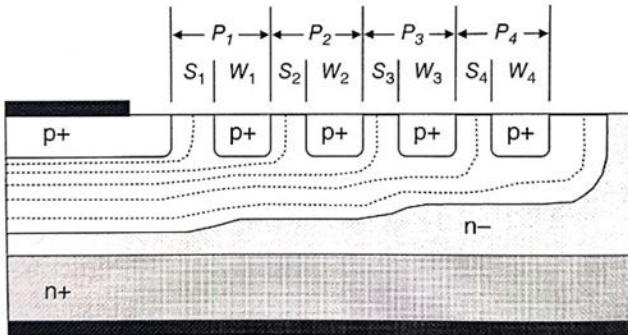
Edge Termination for Vertical Devices



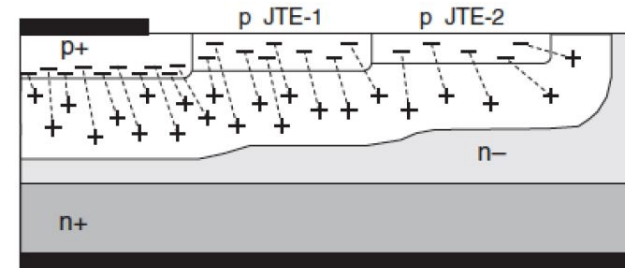
Field plate [1]



Bevel edge termination [1]



Guard ring [2]



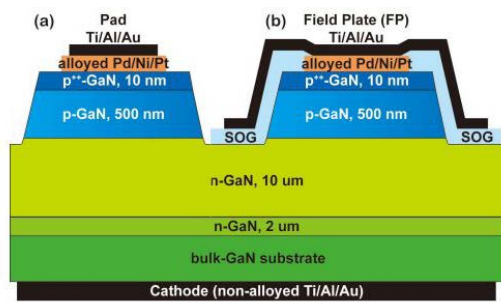
Junction Termination Extension (JTE) [2]

- **Field plates are limited in the case of high voltage (> 10 kV) devices**
 - **Bevel angle should be small (~10 °), which is hard to process**
 - **Patterned p-type doping using ion-implantation is required for guard ring and JTE**
- currently challenging for GaN**

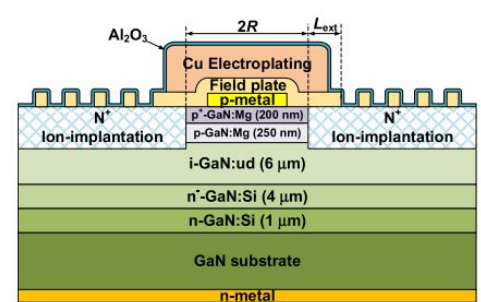
[1] B. J. Baliga, *Silicon Carbide Power Devices*. Singapore: World Scientific, 2005

[2] T. Komoto et al., *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*. Hoboken, NJ, USA: Wiley, 2014

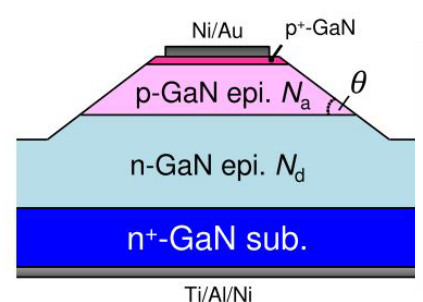
Current Status for GaN Edge Termination



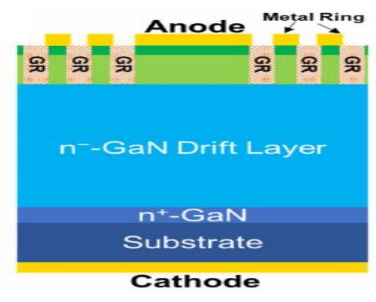
Field plate [1]
Cornell University



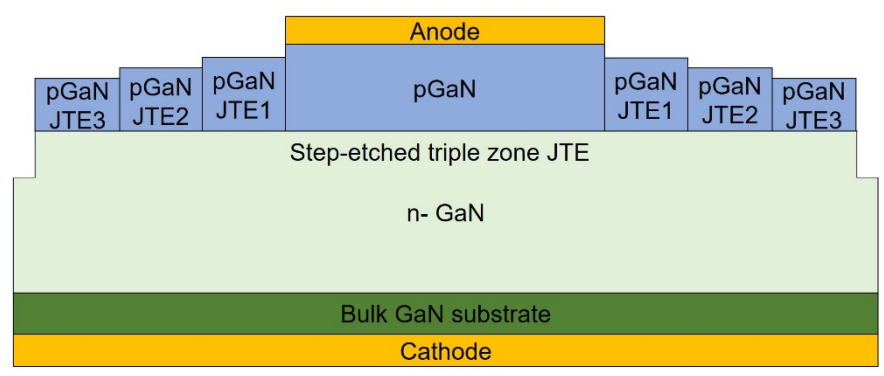
Nitrogen Ion-implantation [2]
Georgia Institute of Technology



Negative bevel edge termination [3]
Kyoto University



Hydrogen plasma-based Guard ring [4]
Arizona State University



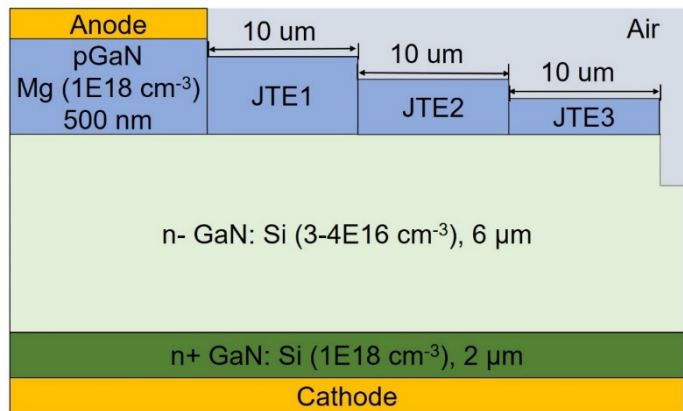
Proposed structure
Step-etched triple zone JTE (STJTE)

- Etching JTE structure that decreases in thickness as it goes outside → the mechanism is same to multiple JTE
- Patterned p-type doping using ion-implantation and precise control of bevel angle are not needed
- Power devices with high breakdown capability (>10 kV) using PN junction JTE unlike Field plate

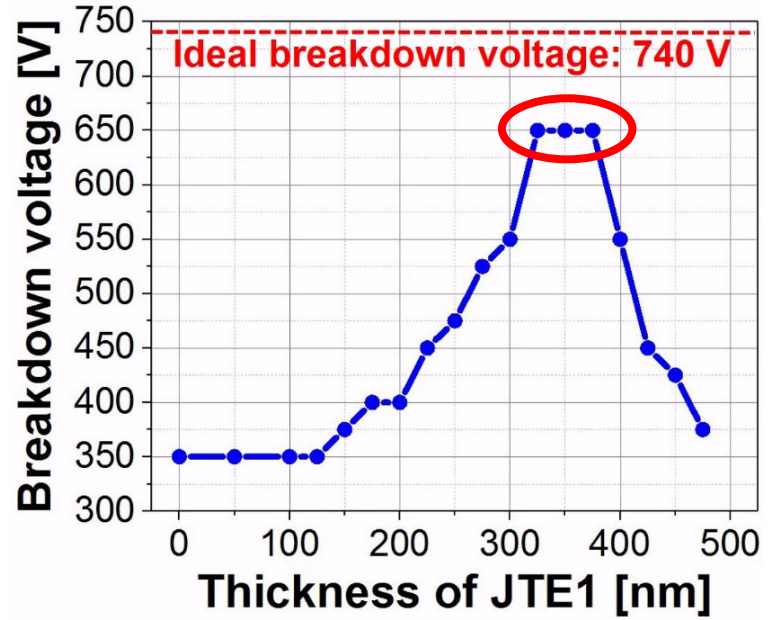
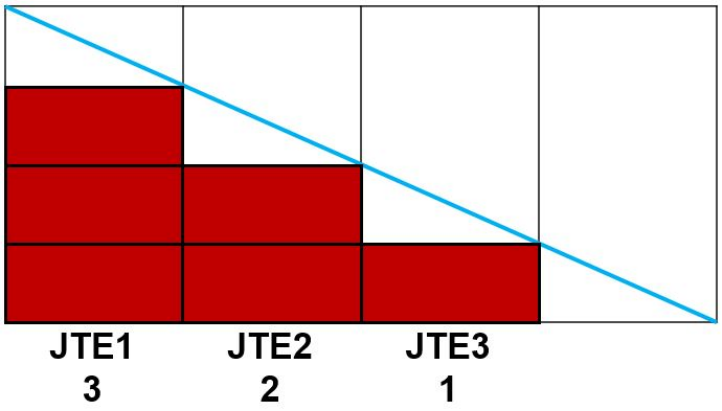
[1] K. Nomoto et al., *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 161-164, Feb. 2016.
 [2] C.-W. Tsou et al., *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4273-4278, Oct. 2019.
 [3] T. Maeda et al., *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 941-944, June. 2019.
 [4] H. Fu et al., *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 127-130, Jan. 2020.

1. Edge Termination for GaN Power Devices
- 2. Design of Edge Termination**
3. Experimental Approach and Results

Design of Junction Termination Layers

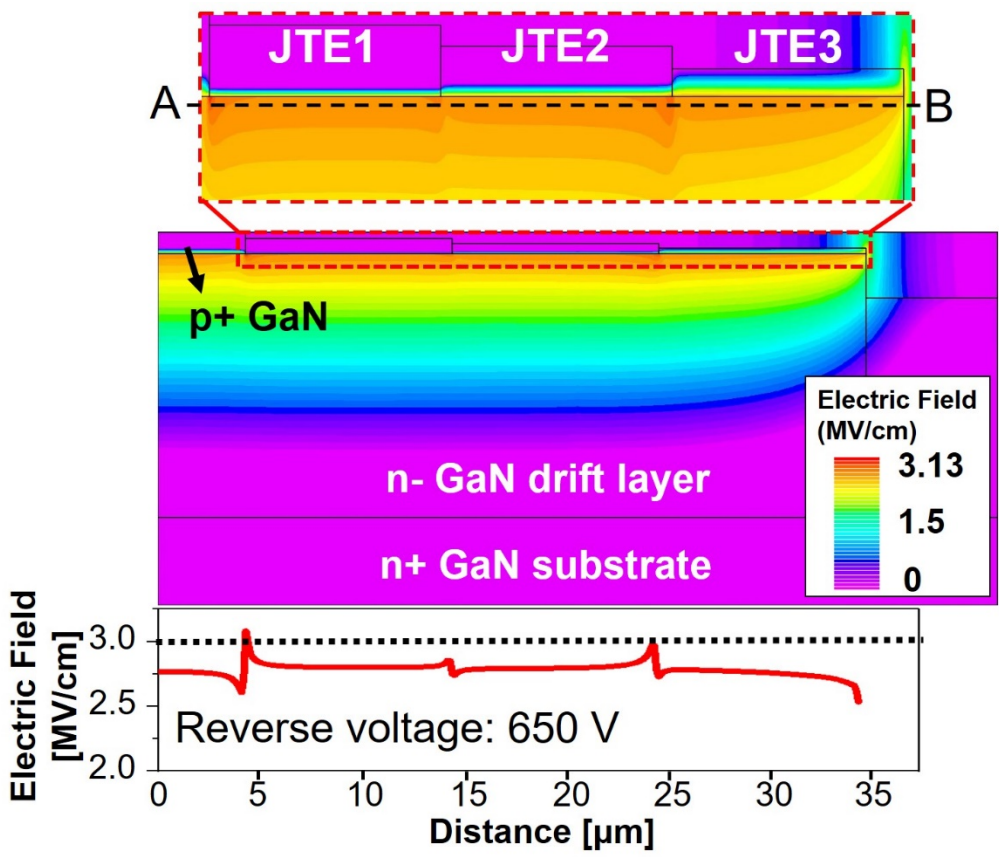
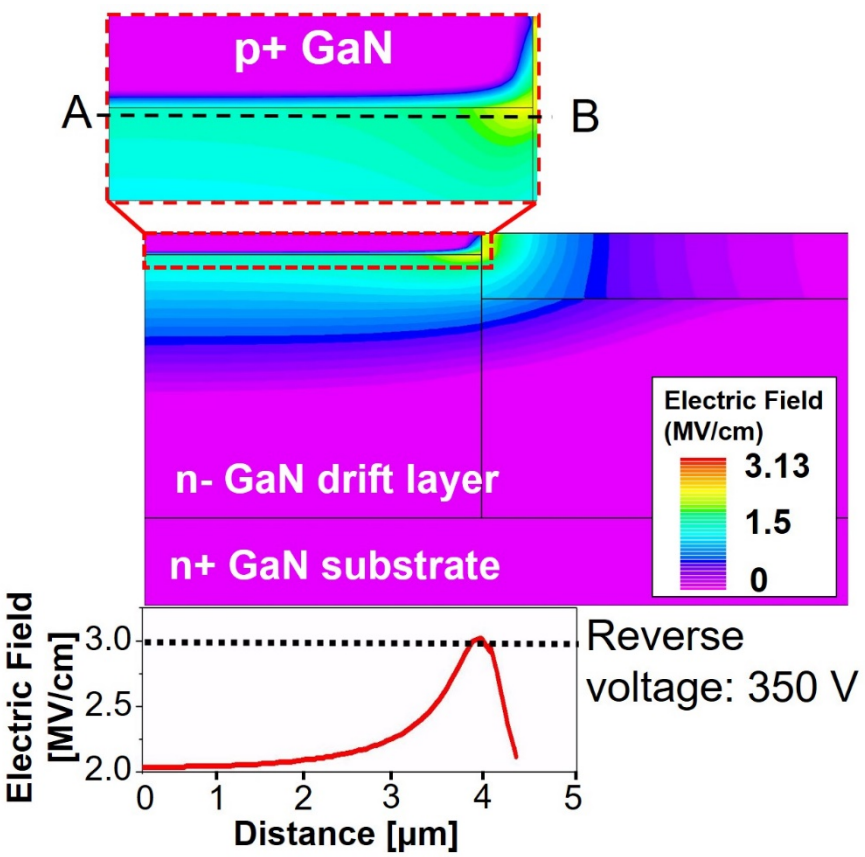


STJTE structure for simulation



- The total length of JTE region = 5 X the thickness of drift layer = 30 μm
- The ratio of each JTE thickness was fixed as JTE1:JTE2:JTE3 = 1 : 0.7 : 0.4
- The range of JTE1 thickness that has the highest breakdown voltage is 50 nm

Design of Junction Termination Layers



Conventional structure (without STJTE)
 → **47 %** JTE efficiency

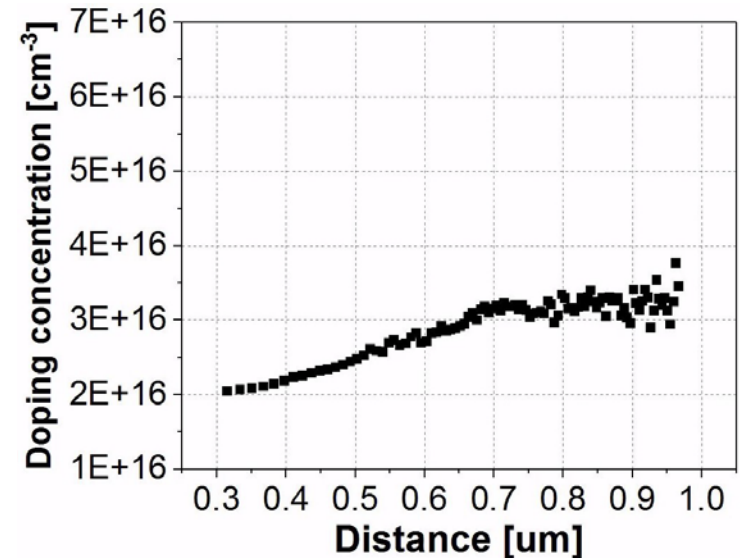
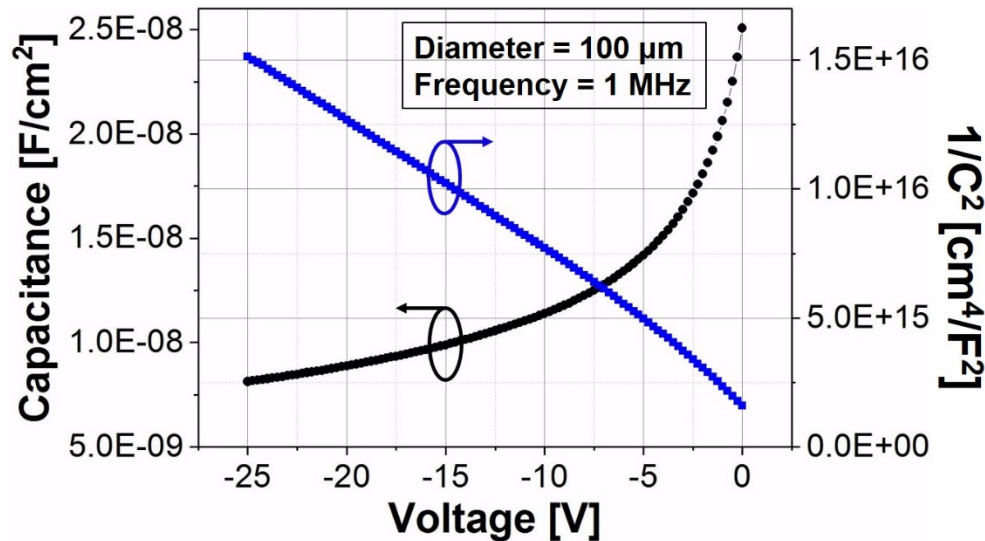
STJTE structure with the optimized JTE thickness
 → **88 %** JTE efficiency

$$\text{JTE efficiency} = [\text{Real breakdown voltage} / \text{Ideal breakdown voltage}] \times 100$$

1. Edge Termination for GaN Power Devices
2. Design of Edge Termination
- 3. Experimental Approach and Results**

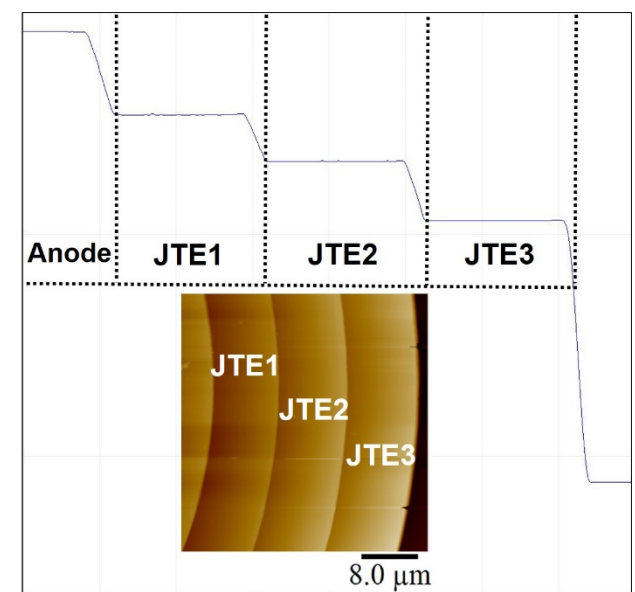
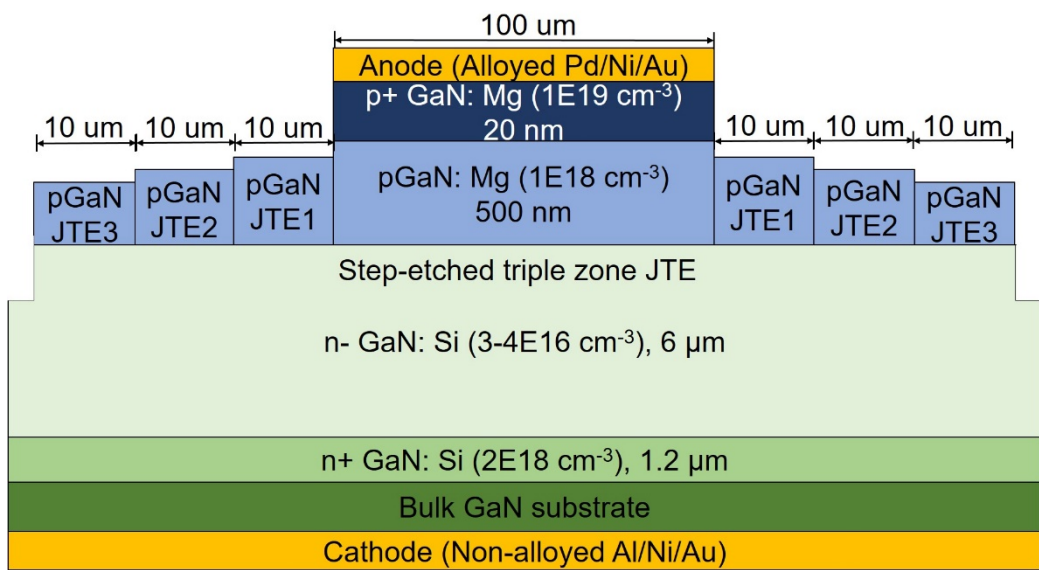
| |
|--|
| p+ GaN: Mg ($1E19\text{ cm}^{-3}$) 20 nm |
| pGaN: Mg ($1E18\text{ cm}^{-3}$) 500 nm |
| n- GaN: Si ($3\text{-}4E16\text{ cm}^{-3}$), 6 μm |
| n+ GaN: Si ($2E18\text{ cm}^{-3}$), 1.2 μm |
| Bulk GaN substrate |

- All epitaxial layers were grown by MOCVD
- Ideal breakdown voltage: 740 V
- Non-punch through case
- p-GaN layer
 - Mg density = $\sim 5E18\text{ cm}^{-3}$ (SIMS)
 - Hole density = $1E17\text{ cm}^{-3}$,
Mobility = $18.4\text{ cm}^2/\text{V}\cdot\text{s}$
(Hall measurement at RT)



- The net doping concentration ($N_D - N_A$) in the n-GaN drift layer was estimated to be $2-3 \times 10^{16} \text{ cm}^{-3}$ from C-V measurement
- Our MOCVD growth condition has reasonably low background impurity concentration ($C \sim 1 \times 10^{16} \text{ cm}^{-3}$ and $O < 1 \times 10^{16} \text{ cm}^{-3}$) based on SIMS measurement
- This is in agreement with extracted $N_D - N_A$ from C-V measurement

Fabrication of vertical GaN pn diode with STJTE

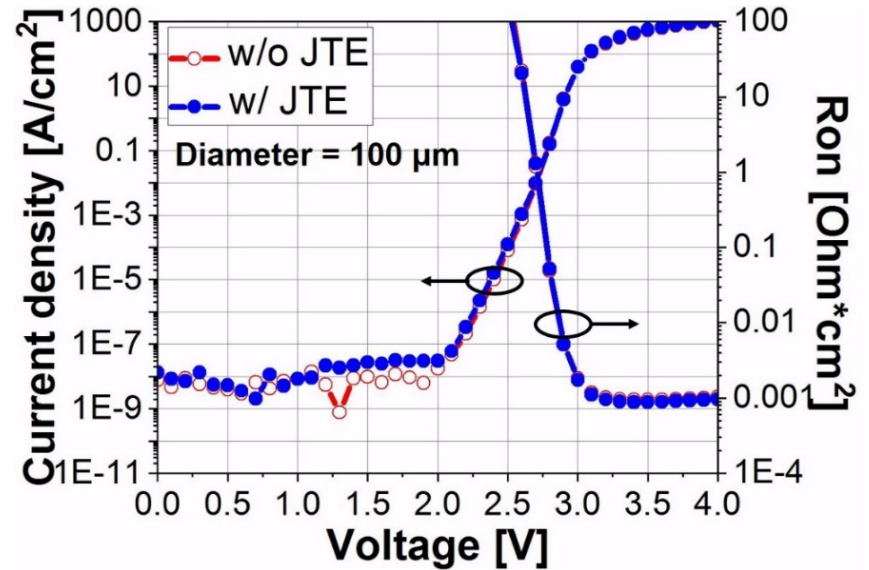
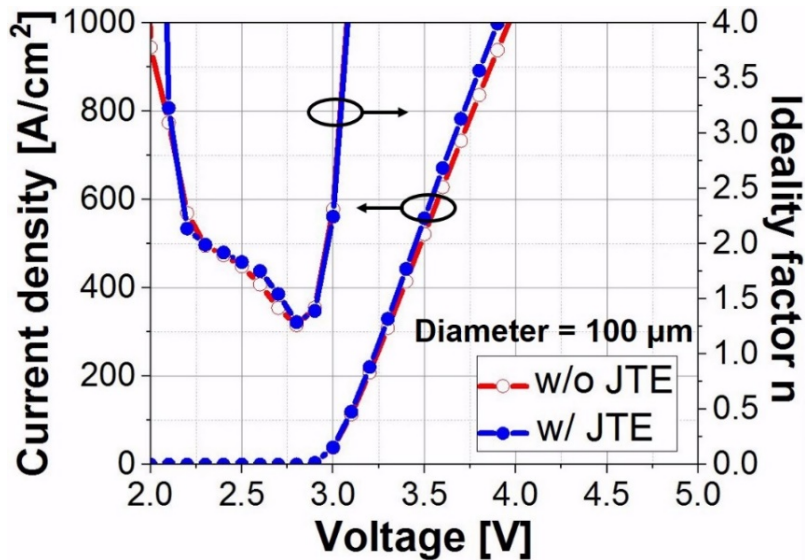


- Low power etching conditions which has $\sim 8.3 \text{ \AA/s}$ etch rate for etching JTE region was used to minimize etching damage
- p-GaN contact resistance = $\sim 1 \text{ m}\Omega \cdot \text{cm}^2$ from TLM

| Parameters | JTE1 | JTE2 | JTE3 |
|-------------------------------------|-----------|-----------|-----------|
| Optimal thickness (Simulation) [nm] | 325 ~ 375 | 228 ~ 263 | 130 ~ 150 |
| Fabricated JTE thickness [nm] | 335 | 230 | 105 |



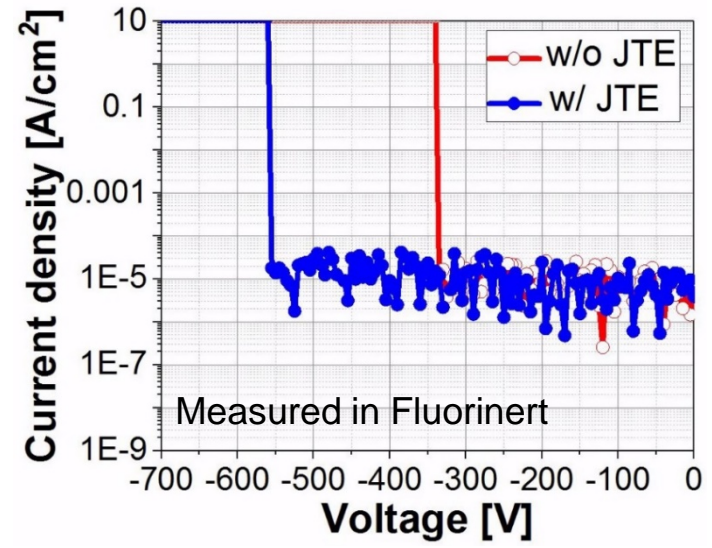
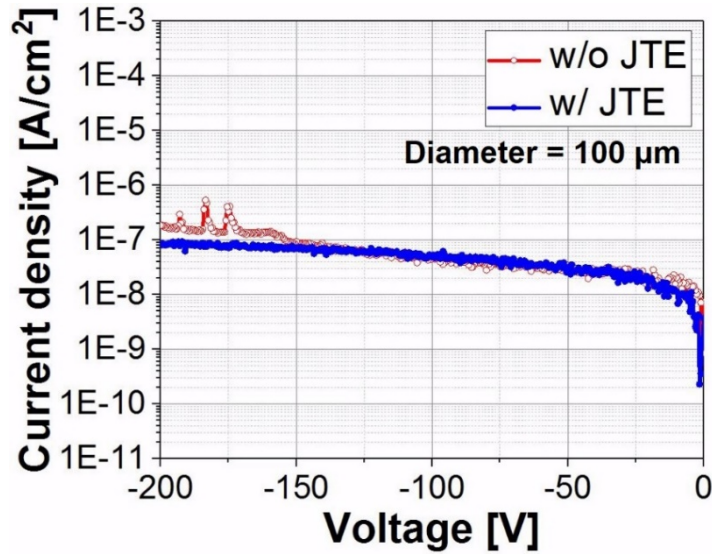
Forward Characteristics



| Parameter | Value |
|---|-------------------|
| Turn-on voltage @ 100 A/cm ² [V] | 3.1 |
| The lowest Ideality factor n | 1.3 |
| on / off ratio | ~10 ¹¹ |
| Total specific on-resistance @ 1kA/cm ² [mΩ·cm ²] | 1.3 |
| Total specific on-resistance – [p-GaN contact resistance (1 mΩ·cm ²) + thick substrate resistance (0.125 mΩ·cm ²)] | 0.175 |
| Calculated mobility of n-GaN drift layer [cm ² /V·s] | 715 |

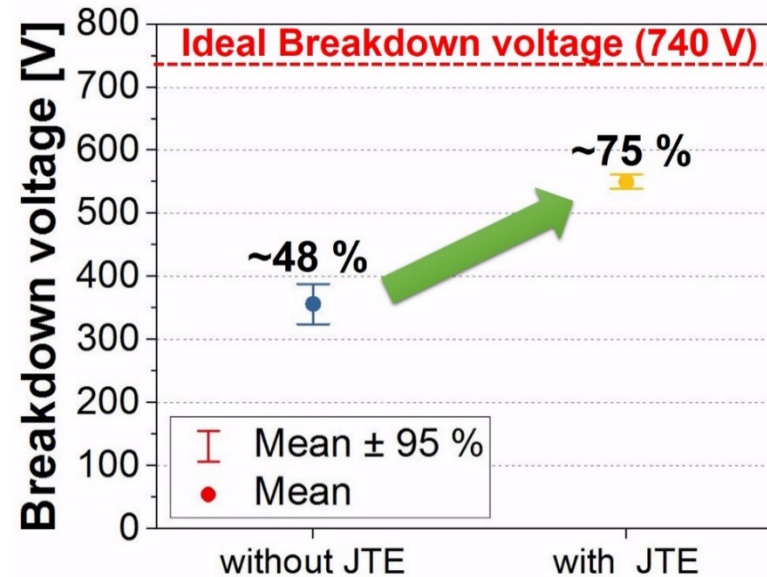


Reverse Characteristics



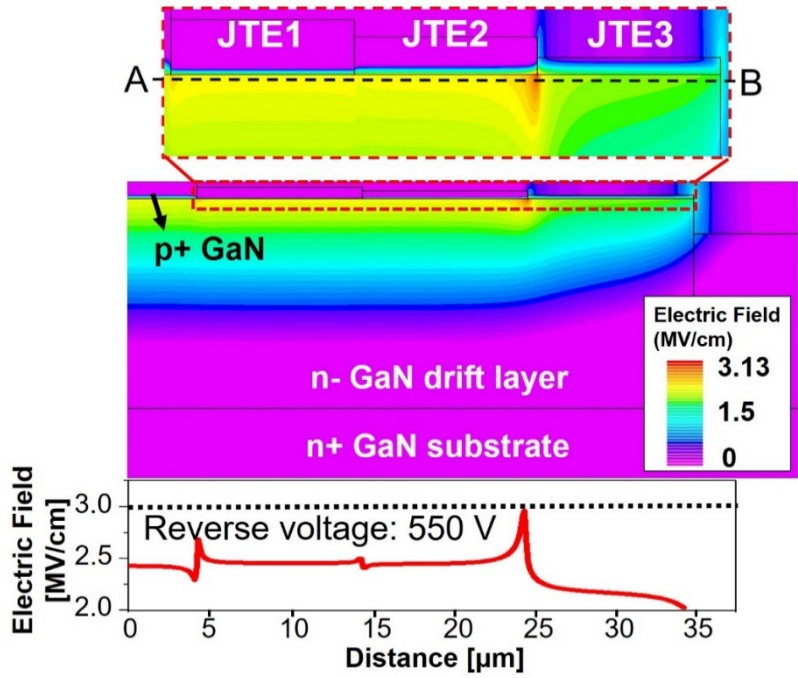
| Parameter | Without STJTE | With STJTE |
|--|---------------|------------|
| Leakage current @ -200 V [nA/cm ²] | 186 | 86 |
| Breakdown voltage [V] | 330 | 550 |
| Simulated breakdown voltage [V] | 350 | 650 |

- Higher leakage at > 200 V suggests higher electric field starts peaking in edge regions
- Leakage and breakdown behavior improved significantly after STJTE
- Breakdown improved from 330 V to 550 V with STJTE – breakdown was destructive, not avalanche breakdown



- 24 devices without STJTE and 80 devices with STJTE were measured
- The standard deviation was 50 V with STJTE
- The average breakdown voltage of **without** STJTE was 360 V corresponding to ~48 % JTE efficiency (Simulated value = 47 %) → **Well-matched**
- The average breakdown voltage of **with** STJTE was 550 V corresponding to 75 % JTE efficiency (Optimal simulated value = 88 %) → **Not matched**

Experimental versus Simulated Breakdown

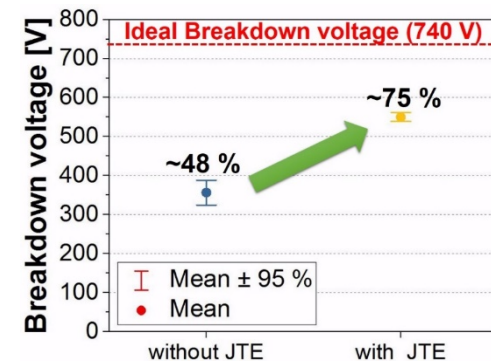
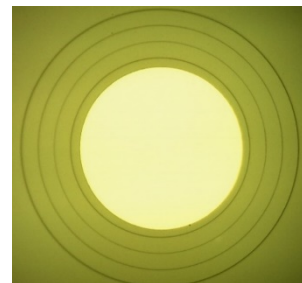
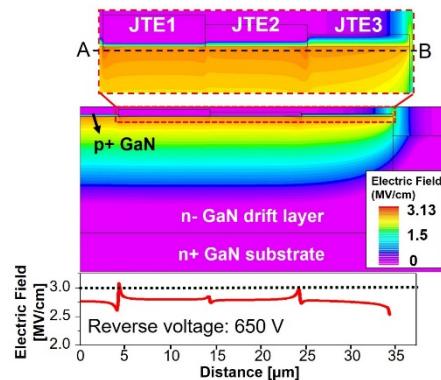
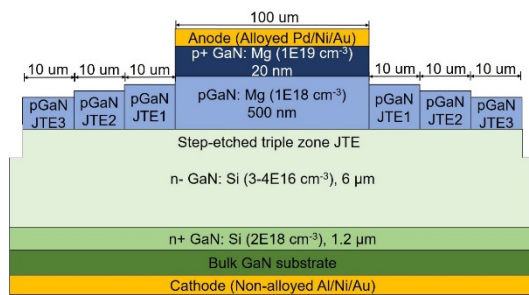


| Parameters | JTE1 | JTE2 | JTE3 |
|-------------------------------------|-----------|-----------|------------|
| Optimal thickness (Simulation) [nm] | 325 ~ 375 | 228 ~ 263 | 130 ~ 150 |
| Fabricated JTE thickness [nm] | 335 | 230 | 105 |

- Due to process variations, the optimal thickness was not achieved
- The simulated breakdown voltage using **actual JTE thickness** was 550 V corresponding to 75 % JTE efficiency → **Well-matched**
- **Excellent match with simulations shows robustness of the proposed approach**

Conclusion

- We have designed and demonstrated for the first time a step-etched edge termination approach for GaN PN diode
- The fabricated vertical GaN PN diode with step-etched triple zone JTE shows breakdown voltage of 550 V corresponding to 75 % JTE efficiency
- Very good match was obtained with the simulations, suggesting near-ideal behavior for the edge termination and minimal effect of etching damage
- Multi-step edge termination could be a promising approach for future multi kV-class GaN vertical power devices





Thank you