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Computational Research of CMOS Channel Material Benchmarking for Future Technology Nodes: Missions, Learnings, and Remaining Challenges

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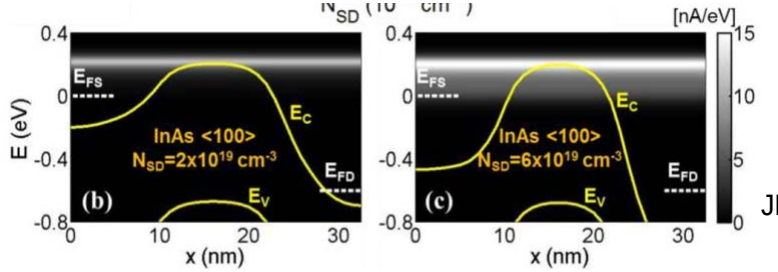
Components Research

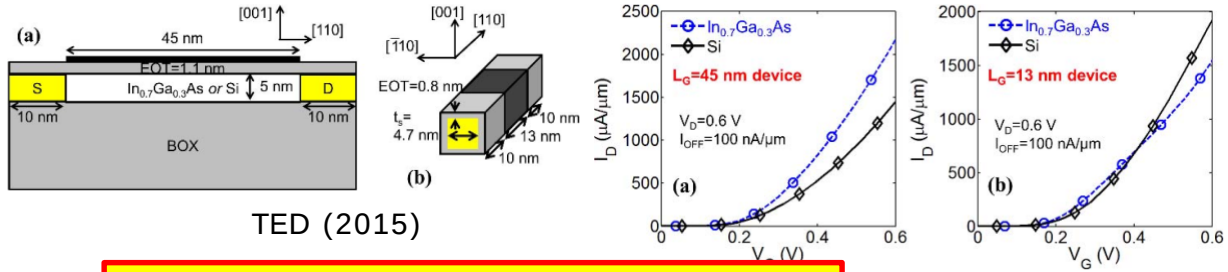
Intel Corporation

Overview

- **Goal**: Review our comprehensive computational research on CMOS channel material benchmarking
  - Projected performance of various novel CMOS channel materials using **rigorous physics-based models**
  - Obtained physical insights on the **key design considerations** for extremely scaled n/pMOS
- Remaining **research gaps and challenges** to provide ultimate theoretical guidance on the material choice in future CMOS



JEDS (2015)



TED (2015)

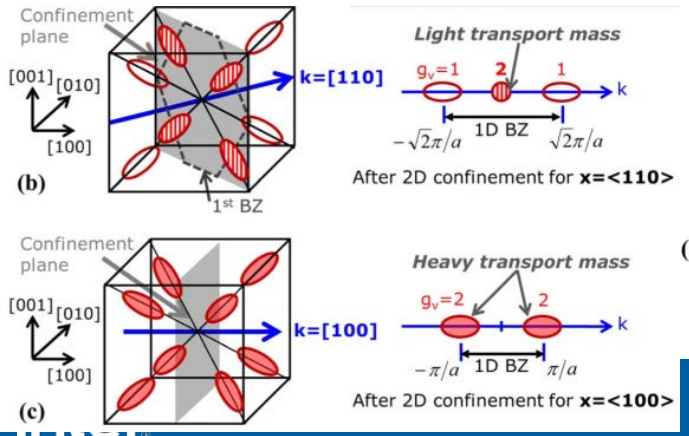
Highlight & Key Messages

IEDM (2015)

I_L @V_G=V_{DD}/2, V_D=V_{DD}	
$C_{eff,n\ or\ p}$	$\left[\begin{matrix}Q_G(V_G=V_{DD},V_D=0)\\ -Q_G(V_G=0,V_D=V_{DD})\end{matrix}\right]/V_{DD}$
R_{SD}	200 Ω-μm
C_{fringe}	0.6 fF/μm

$I_{eff,n+p}$	$1/I_{eff,n+p}=1/I_{eff,n}+1/I_{eff,p}$
$C_{eff,n+p}$	$C_{eff,n}+C_{eff,p}$
CV/I (gate- loaded)	$C_{eff,n+p}V_{DD}/I_{eff,n+p}$
CV/I (intercon.-loaded)	$C_wV_{DD}/I_{eff,n+p}$ (C_w: constant)

EDL (2015)



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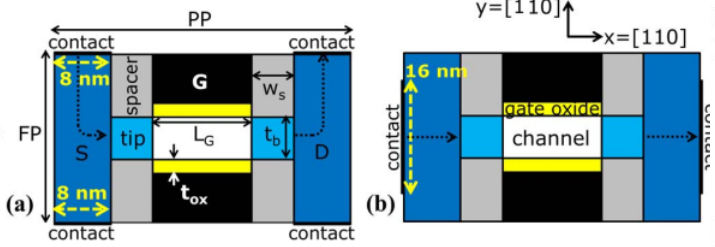

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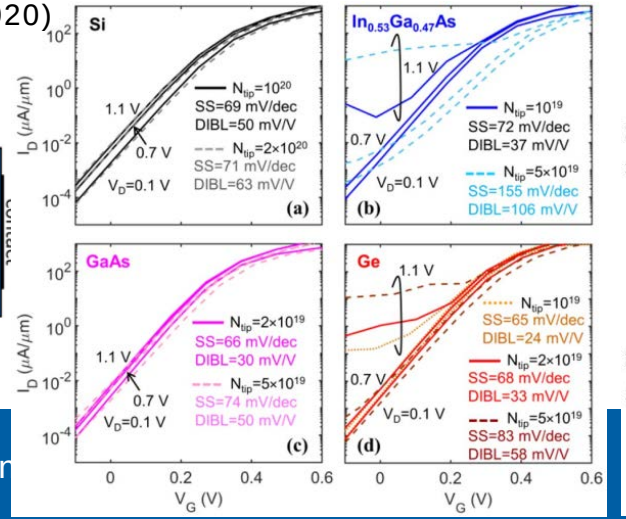

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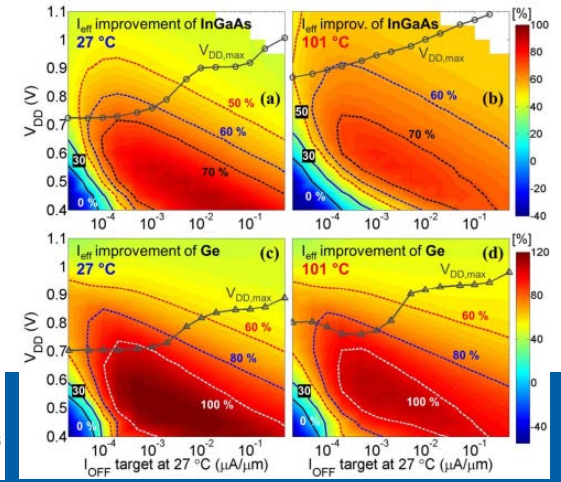

Outline

- Model device
- Material-dependent device optimization
  - S/D tip design
  - Crystal orientation
- Carrier transport model
- Performance metrics
- Temperature effects
- Remaining challenges

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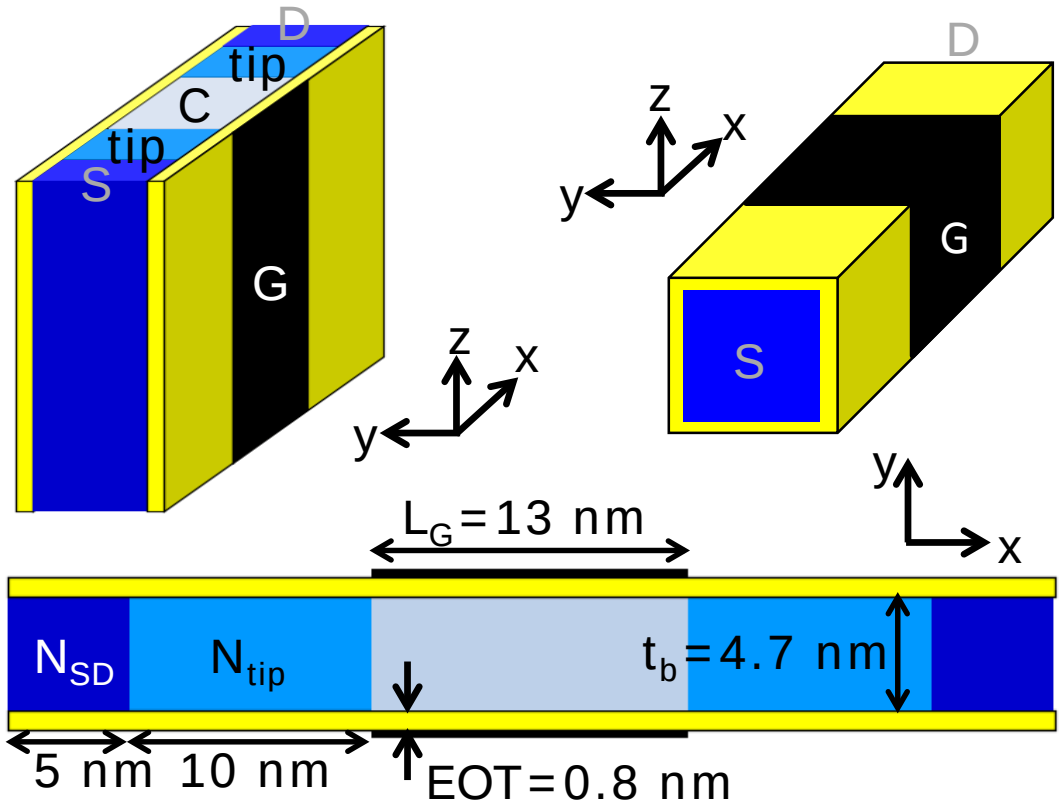
Model Device

- Double-gate (**DG**) thin body or gate-all-around (**GAA**) **NW** MOSFETs with **L_G=13 nm**
  - Various **nMOS** and **pMOS** materials
  - Device parameters (e.g. tip doping density (N_{tip})) **optimized for each material**
  - Assumed high S/D doping density (N_{SD}) as in actual devices (R_{SD} reduction)
  - Also explored **crystal orientation effects**



nMOS	Si	InAs	$In_{0.53}Ga_{0.47}As$	GaAs	Ge
N_{tip} (cm^{-3})	10^{20}	10^{19}	10^{19}	$2x10^{19}$	10^{19}, $2x10^{19}$, $5x10^{19}$
N_{SD} (cm^{-3})	$2x10^{20}$	$5x10^{19}$	$5x10^{19}$	$5x10^{19}$	10^{20}

pMOS	Si	Ge
N_{tip} (cm^{-3})	10^{20}	10^{19}, $2x10^{19}$, $5x10^{19}$
N_{SD} (cm^{-3})	$2x10^{20}$	10^{20}

x	y	z
[110]	[$\bar{1}$10]	[001]
[100]	[010]	[001]

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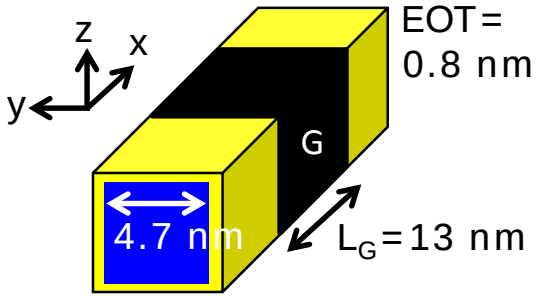
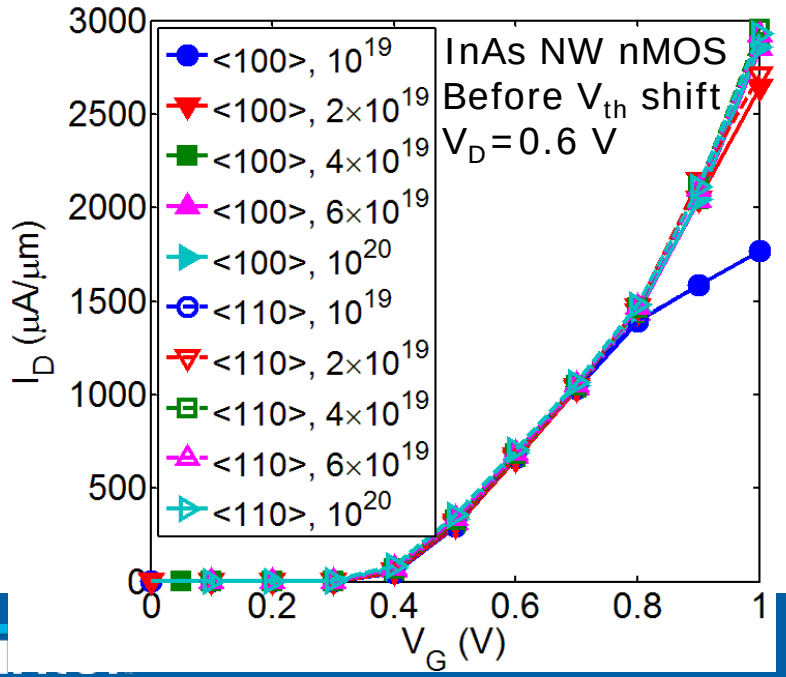
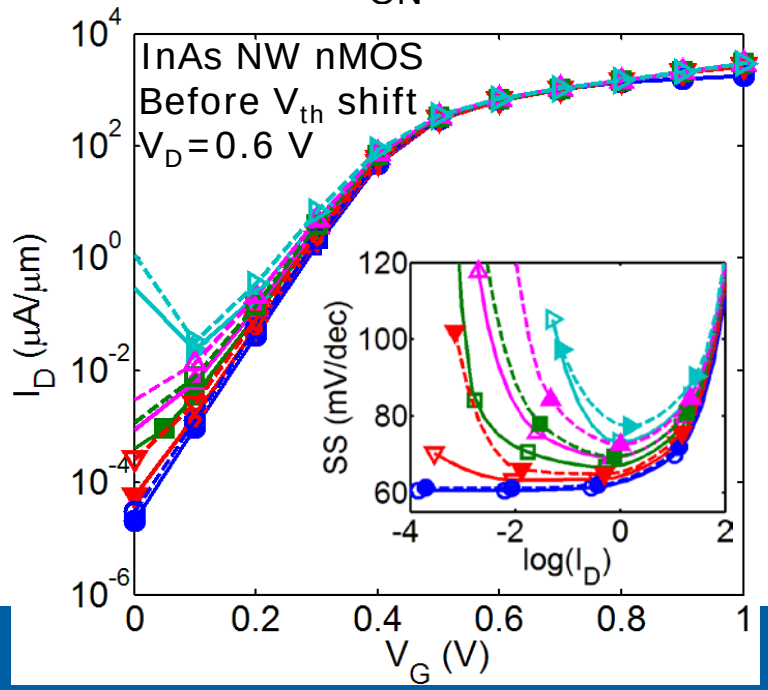
Optimizing S/D Tip Design



x	y	z	
[110]	[$\bar{1}$10]	[001]	"<110> NW"
[100]	[010]	[001]	"<100> NW"

- Materials with small E_g and m^* (such as III-V nMOS): Trade-off between **source exhaustion** and **tunneling leakage**
  - Trade-off between **ON-state** vs. **OFF-state** performance
    - ON-state: **High N_{tip}** helps (less source exhaustion)
    - OFF-state: **Low N_{tip}** helps (less tunneling leakage)
    - Note: Similar trade-off achieved using **gate underlap** (X_{UD})
  - For the given **performance target** (I_{OFF}, V_{DD}), there exists an **optimum N_{tip}** (or X_{UD}) that maximizes I_{ON}.





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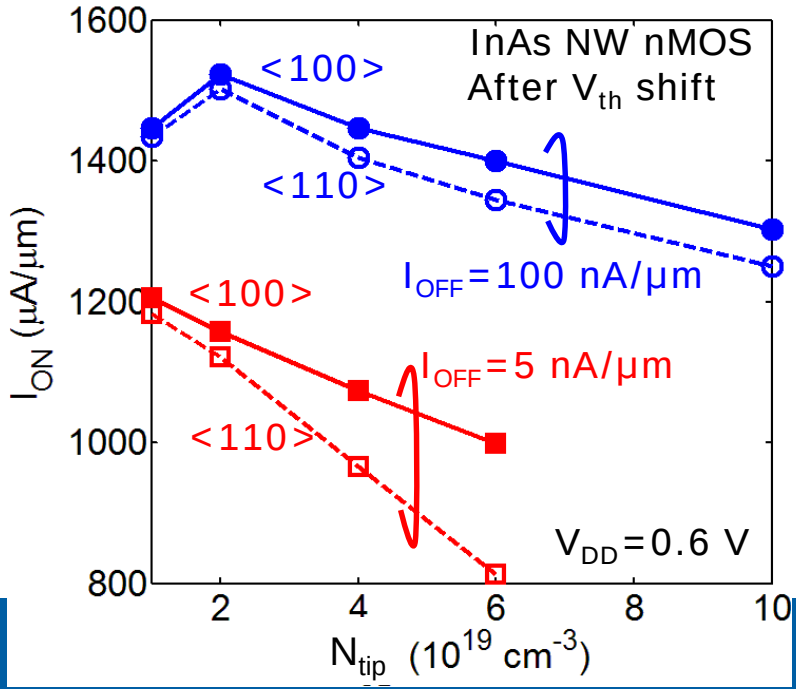

Tip Doping Effects and Material Dependence

- Physics of SS vs. N_{tip}
  - Electrostatics: $SS_{TOB} = \ln(10) \times \frac{k_B T}{q} \times \left(\frac{d\psi_{TOB}}{d(qV_G)} \right)^{-1}$
    - Monotonic increase with N_{tip}: "Classical" short channel effect (SCE)
  - Rapid increase of SS_{actual} with N_{tip}: Direct **S-D tunneling**
- **Band parameters** (E_g and m^*) depend on the material and crystal orientation.
  - The **S/D tip optimization** also depends on the material and crystal orientation.

TABLE 1. Extracted band parameters of nanowires and bulk reference [13].

NW type	E_g	m^* (lowest band)[a]	$E_{g,bulk}$	m^*_{bulk}
InAs <100>	0.871 eV	$0.0592m_0$	0.354 eV	$0.023m_0$
InAs <110>	0.853 eV	$0.0525m_0$		
GaAs <100>	1.788 eV	$0.0967m_0$	1.424 eV	$0.063m_0$
GaAs <110>	1.791 eV	$0.0859m_0$		
Si <100>	1.319 eV	$0.239m_0$	1.12 eV	$0.19m_0$
Si <110>	1.272 eV	$0.192m_0$		

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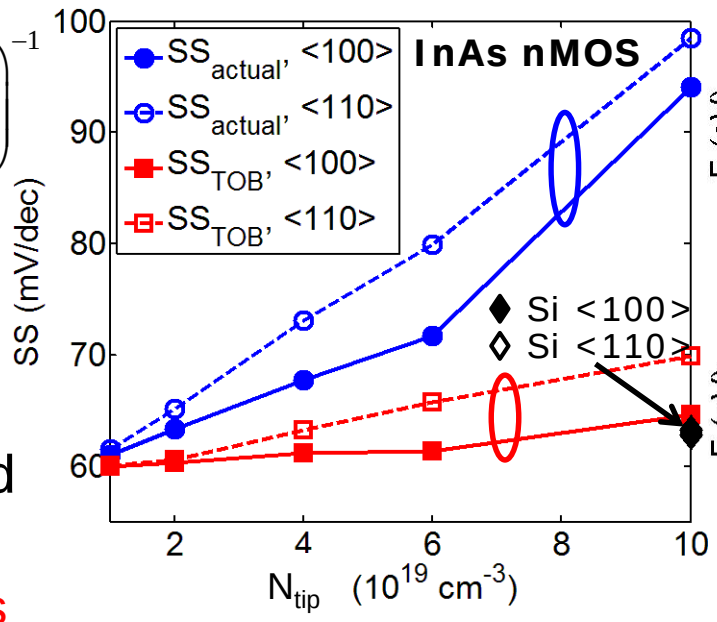

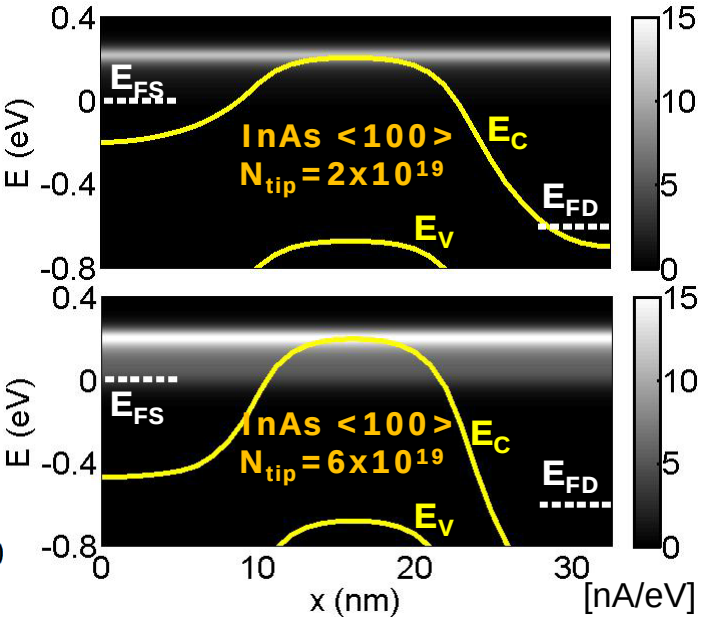

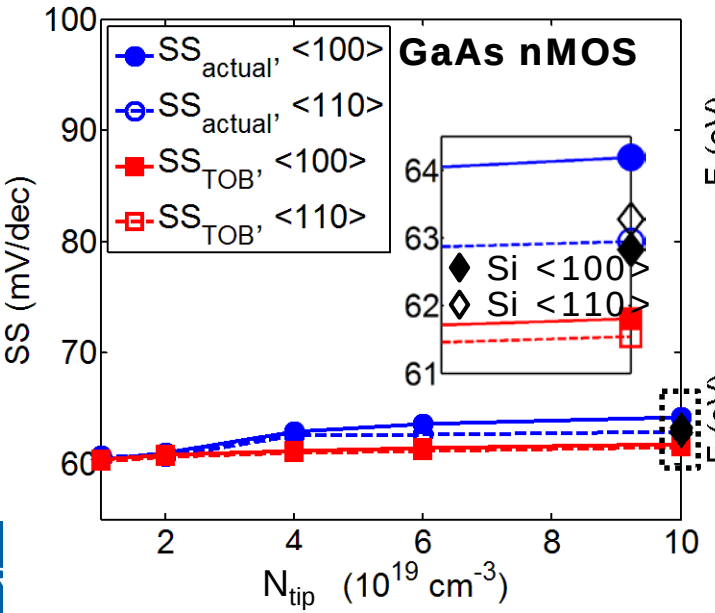

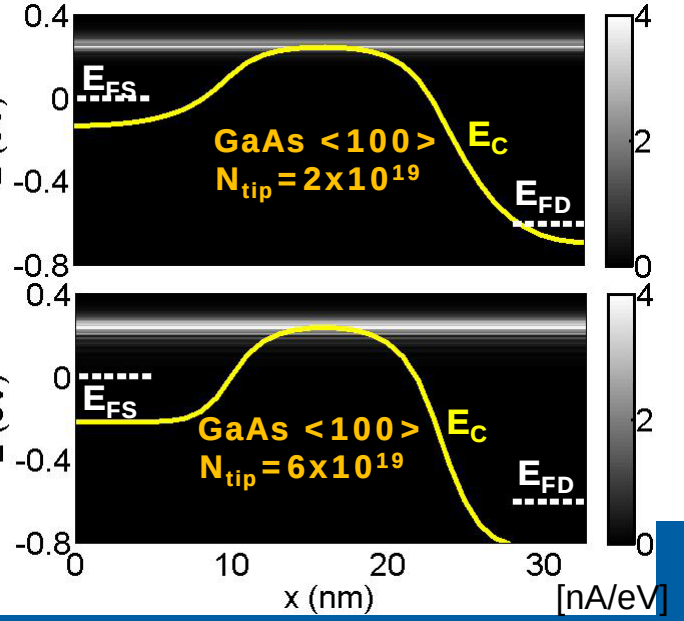

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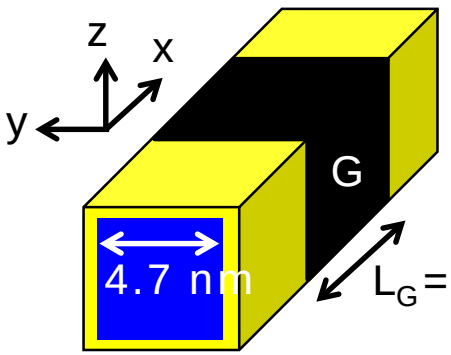
Optimizing Crystal Orientations

- Materials with multiple valleys (Γ, X, L): Band structure of quantum confined structures (e.g. NWs) may significantly depend on the **crystal orientation**
  - Example: Γ and L-valleys of **Ge NW nMOS**
  - Crystal orientation should be carefully chosen to optimize the band structure (e.g. **DOS** and **injection velocity**).



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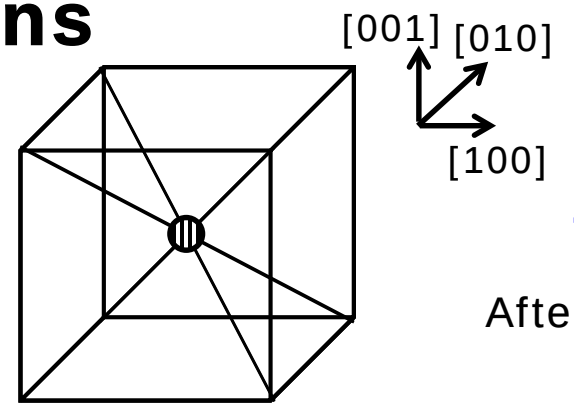
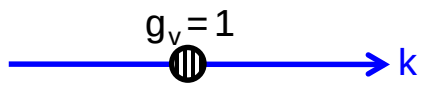
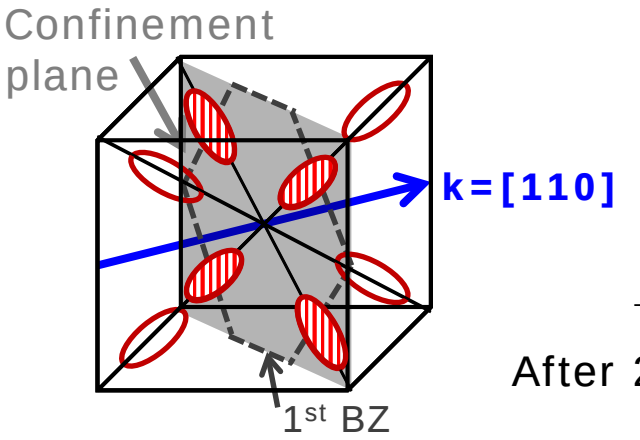
x	y	z	
[110]	[$\bar{1}$10]	[001]	"<110> NW"
[100]	[010]	[001]	"<100> NW"

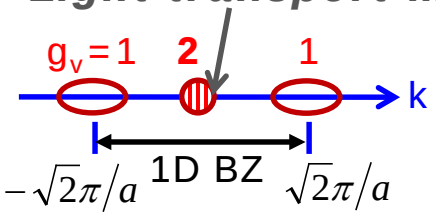




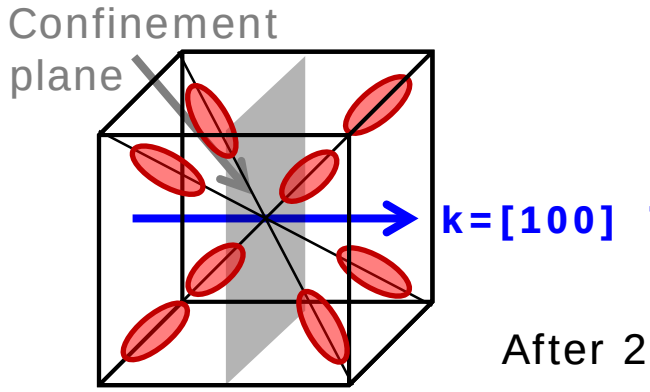
After 2D confinement (all cases)



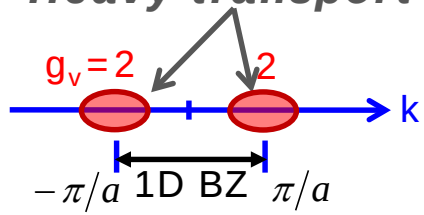
Light transport mass



After 2D confinement for **x=<110>**



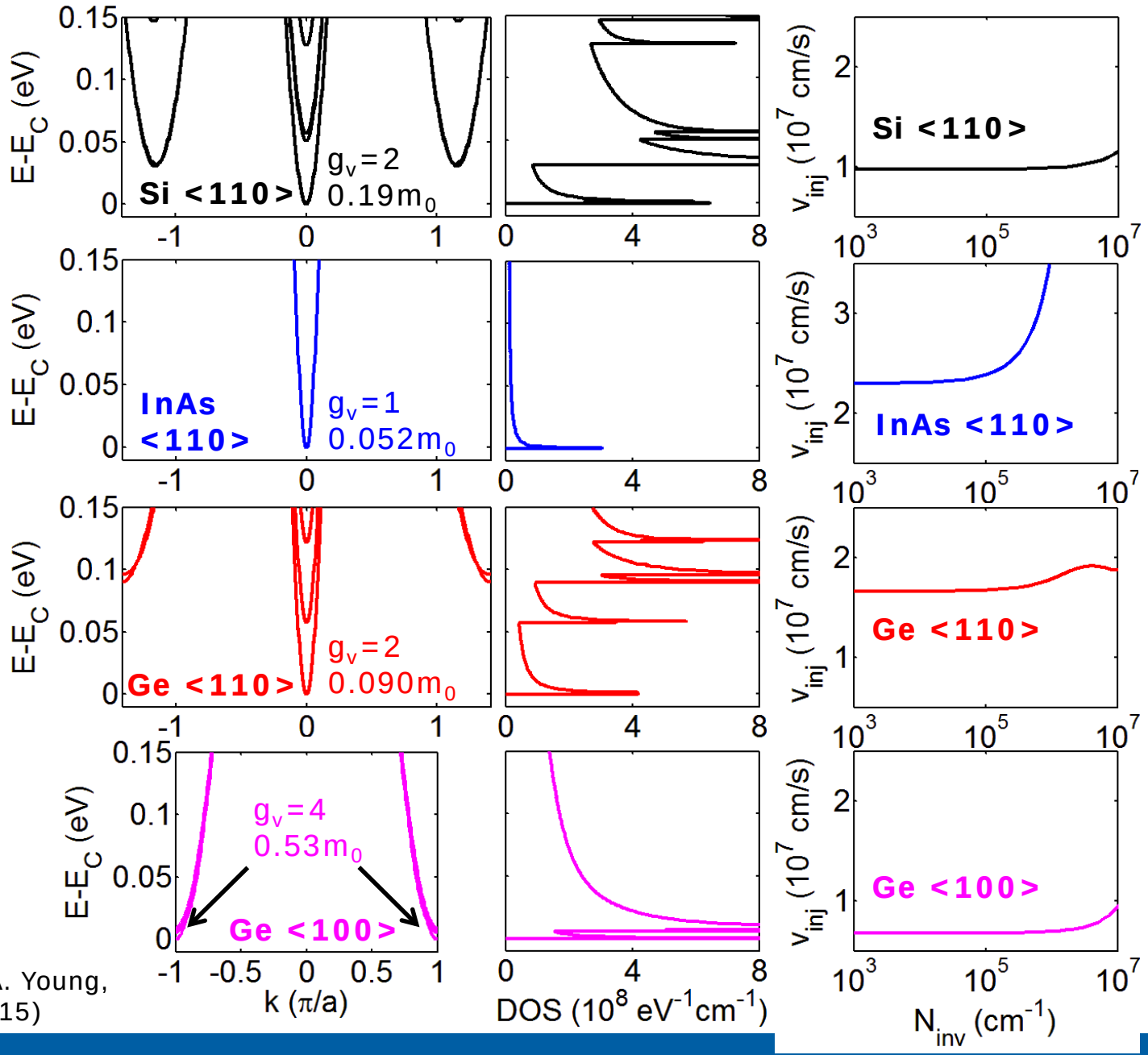
Heavy transport mass



After 2D confinement for **x=<100>**

Band Structures of NW nMOS

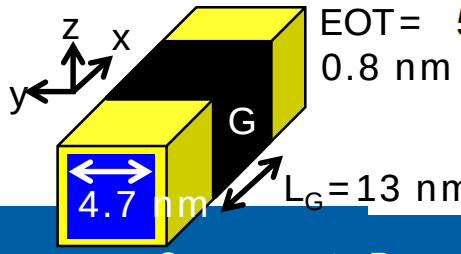
- **E-k**, density-of-states (**DOS**), injection velocity ($\mathbf{v_{inj}}$)
- InAs (Γ-valley only)
  - Weak orientation dependence
  - Light m* with g_v=1: v_{inj} is high, but DOS is low ("DOS bottleneck")
- **Ge <110> NW** gives optimum band structures
  - DOS improves (higher g_v) while v_{inj} remains high (light transport m*)
- Ge <100> NW gives even higher DOS, but v_{inj} degrades significantly (heavy transport m*).



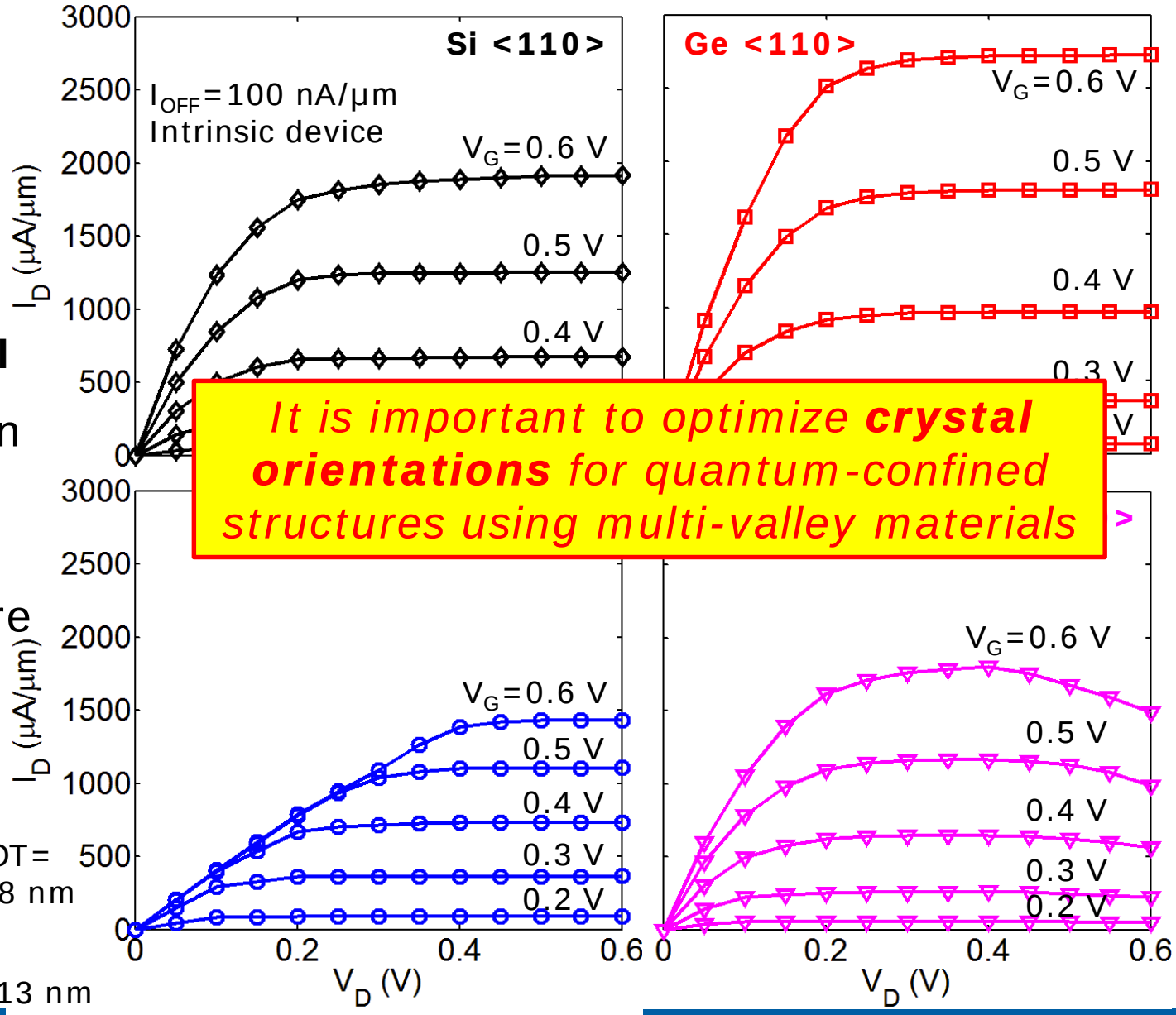
R. Kim, U. E. Avci, and I. A. Young, IEEE EDL **36**, 751-753 (2015)

I-V Simulation Results

- Atomistic self-consistent ballistic quantum transport simulation
  - $sp^3d^5s^*$ tight-binding model
  - Non-equilibrium Green's function (NEGF) method
  - **S/D tip optimized for each material**
- InAs gives ballistic currents lower than in Si ("DOS bottleneck")
- **Ge <110> NW** gives high ballistic current due to optimum band structure (improved DOS with still high v_{inj})
- Ge <100> NW gives ballistic current that are comparable to or lower than in Si (v_{inj} degradation).



R. Kim, U. E. Avci, and I. A. Young, IEEE EDL **36**, 751-753 (2015)



*It is important to optimize **crystal orientations** for quantum-confined structures using multi-valley materials*

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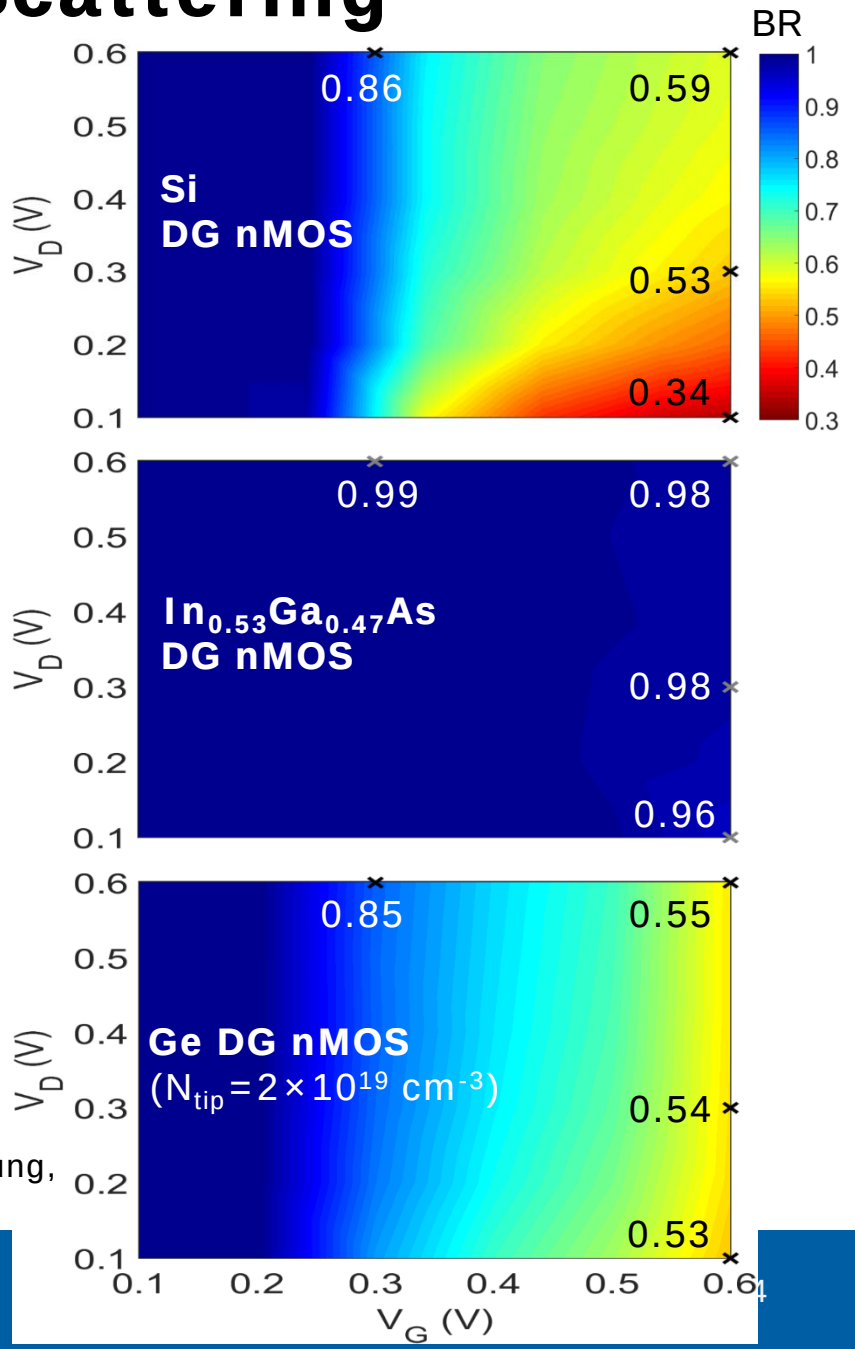
Carrier Transport Model: Ballistic vs. Scattering

- **Ballistic** transport model: Frequently used to estimate the **upper limit** of current drivability
- For the L_G of our interest (~13 nm), carrier scattering effect can be still significant.
- *Challenge*: For the scaled device, it is critical to consider **quantum transport effects** (e.g. tunneling) while it gives a **very high numerical cost** to include carrier scattering within the quantum simulation framework.
- **Our approach**: To capture both effects of quantum transport and carrier scattering, we use "**ballistic ratio**" as a correction factor to include scattering effects.
- Ballistic ratio (BR) ≡ I_{scatt} / I_{ball}
  - BR = 1: Ballistic limit
  - BR < 1: Current reduction due to scattering
  - I_{scatt} and I_{ball} are calculated by turning ON and OFF carrier scattering in **Monte Carlo** (MC) simulation

$$BR(V_G, V_D) = I_{scatt,MC}(V_G, V_D) / I_{ball,MC}(V_G, V_D)$$

R. Kim, U. E. Avci, and I. A. Young, IEEE JEDS **8**, 505-523 (2020)



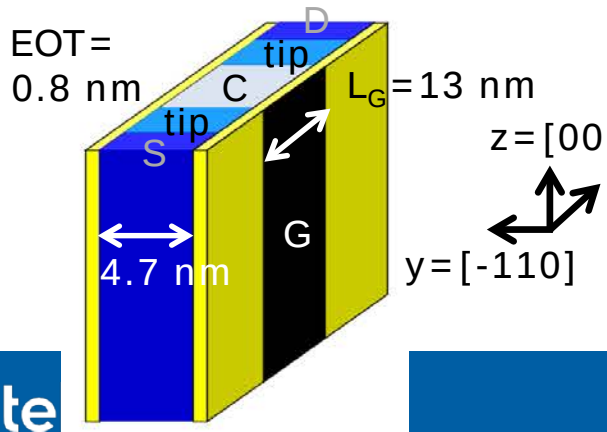
Carrier Transport Model: Ballistic vs. Scattering

- **Our "hybrid" approach** to capture both effects of quantum transport and carrier scattering:
  1) Extract "**ballistic ratio**" (BR) from full-band **MC simulation** considering relevant carrier scattering mechanisms

$$BR(V_G,V_D) = I_{scatt,MC}(V_G,V_D) / I_{ball,MC}(V_G,V_D)$$

  2) Apply the BR as **correction factors** to the **quantum ballistic** transport simulation results from atomistic NEGF

$$I_{scatt,QT}(V_G,V_D) = I_{ball,QT}(V_G,V_D) \times BR(V_G,V_D)$$



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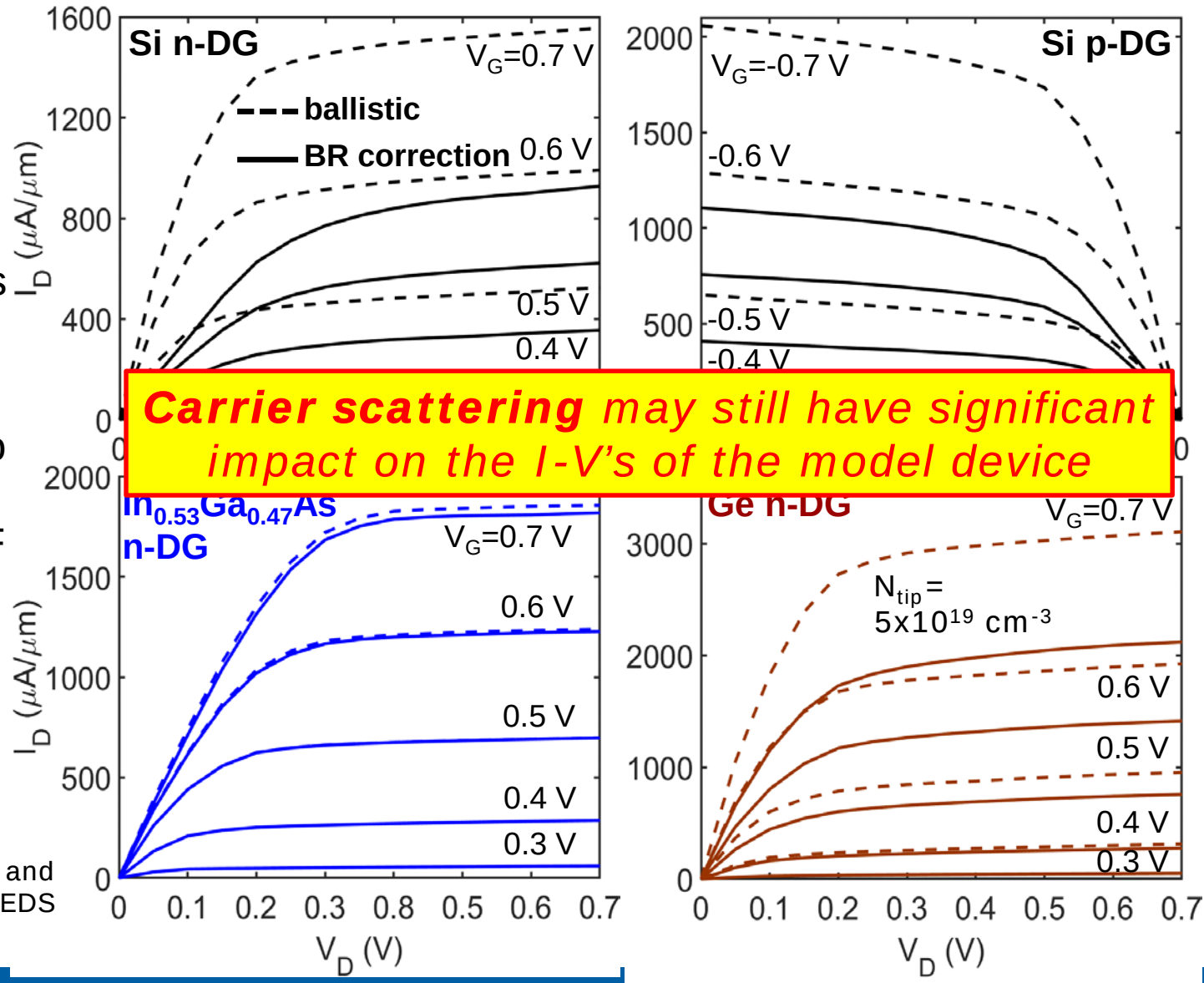

***Carrier scattering** may still have significant impact on the I-V's of the model device*

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CMOS Performance Metrics

- In addition to transistor I-V's, **CMOS circuit performance metrics** such as effective drive current ($\mathbf{I_{eff}}$), **capacitance**, switching energy ($\mathbf{CV^2}$), and switching delay ($\mathbf{CV/I}$) are also important.

$$I_{eff} = (I_H + I_L)/2 \qquad I_H = I_D(V_G = V_{DD}, V_D = V_{DD}/2) \qquad I_L = I_D(V_G = V_{DD}/2, V_D = V_{DD})$$

$$1/I_{eff,n+p} = 1/I_{eff,n} + 1/I_{eff,p}$$

$$C_{eff} = \frac{Q_G(V_G = V_{DD}, V_D = 0) - Q_G(V_G = 0, V_D = V_{DD})}{V_{DD}}$$ "Miller effect"

$$CV^2 = C_{load} V_{DD}^2$$

$$CV/I = C_{load} V_{DD} / I_{eff,n+p}$$

  - Device **parasitics**: S/D resistance (R_{SD}), Parasitic capacitance (C_{par})
  - Loading scenarios: "**gate**", "**wire**", or mixed loading (e.g. 50:50, 70:30)

CMOS combinations
(homogeneous and heterogeneous*)

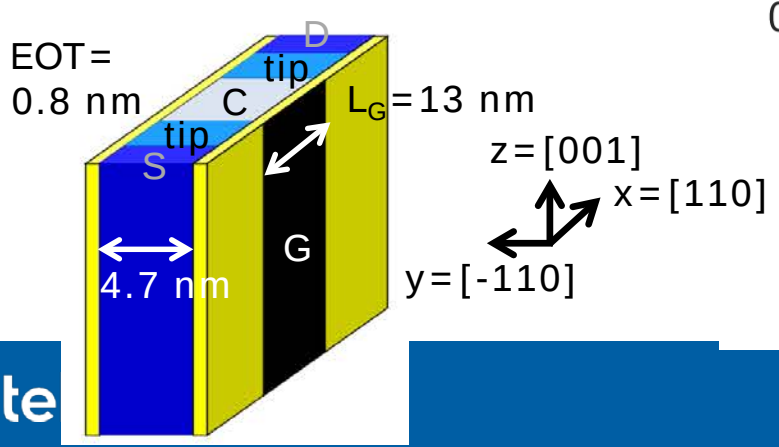
	nMOS	pMOS
Si CMOS	Si	Si
III-V hybrid CMOS	$In_{0.53}Ga_{0.47}As$	Si
	$In_{0.53}Ga_{0.47}As$	Ge
Ge hybrid CMOS	Si	Ge
Ge CMOS	Ge (low N_{tip})	Ge (low N_{tip})
	Ge (high N_{tip})	Ge (high N_{tip})

**A partial list – a comprehensive list of CMOS combinations discussed in our reference*

R. Kim, U. E. Avci, and I. A. Young, IEEE TED **62**, 713-721 (2015)
R. Kim, U. E. Avci, and I. A. Young, IEDM Tech. Dig., 34.1.1, Dec. 2015
R. Kim, U. E. Avci, and I. A. Young, IEEE JEDS **8**, 505-523 (2020)

Energy vs. Delay

- Gate capacitance loading
- Material-dependent trade-offs
  - Ge CMOS (low N_{tip}) gives the largest energy reduction for large delay (low freq) operation.
  - For small delay (high freq), III-V hybrid CMOS ($In_{0.53}Ga_{0.47}As$-Ge) gives the best performance.
- Trade-off also depends on the loading scenario



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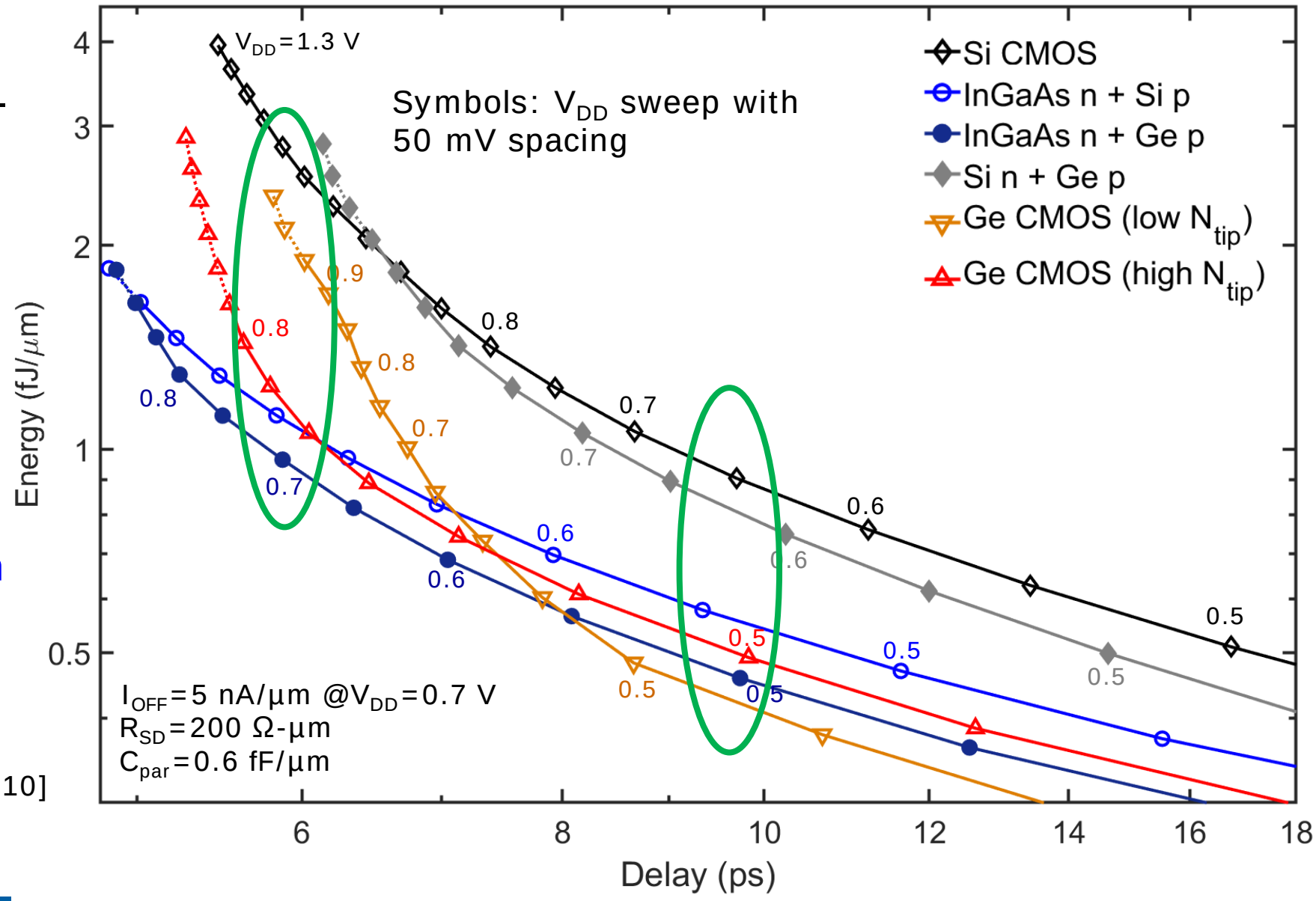

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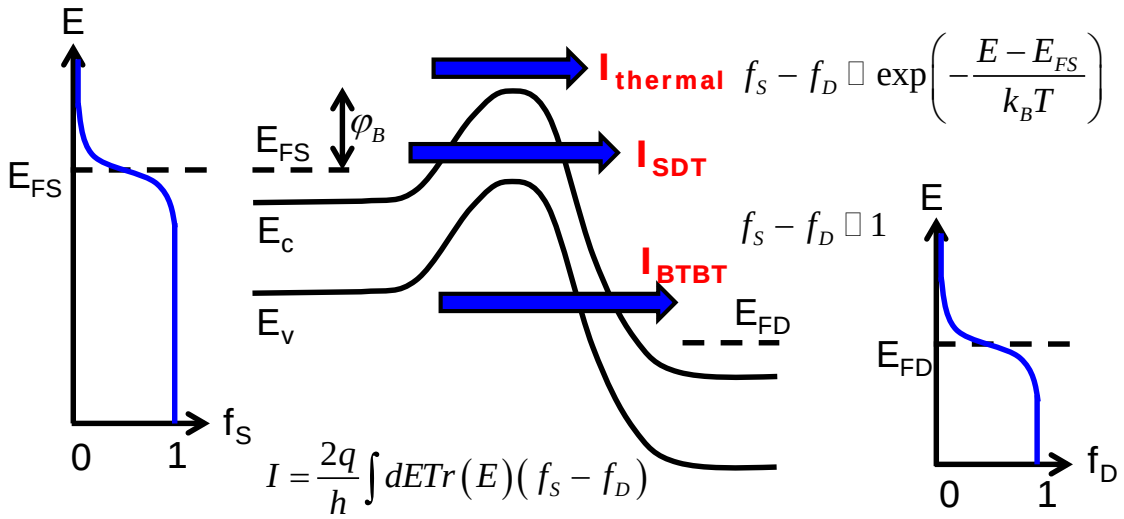
Temperature Effects

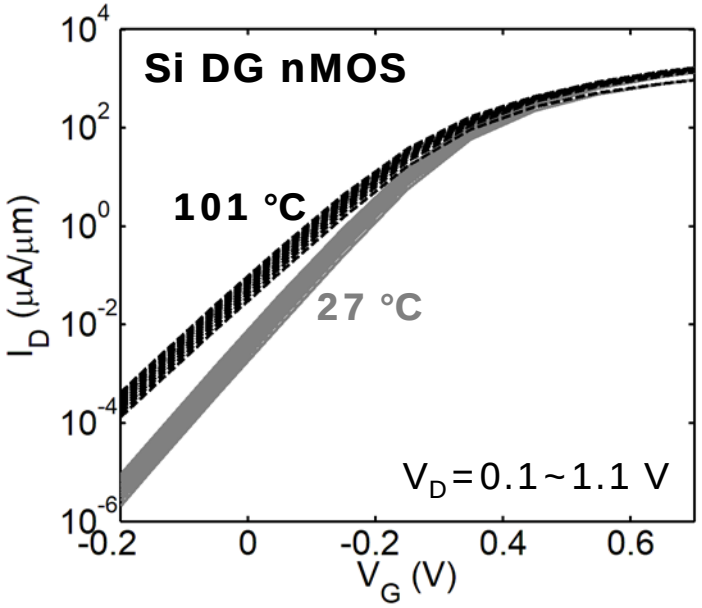
- Most of previous benchmarking studies in literatures assume room temperature (RT, 300 K, 27 °C)
- Actual operating T's of circuits: Much higher than RT
  - May have significant implications for CMOS benchmarking, especially for novel channel materials
- **T-dependence** of **thermionic** and **tunneling leakages**
  - Thermionic leakage ($I_{thermal}$): Very strong T-dependence
  - S-D (I_{SDT}) and band-to-band tunneling (I_{BTBT}): Weak T-dependence

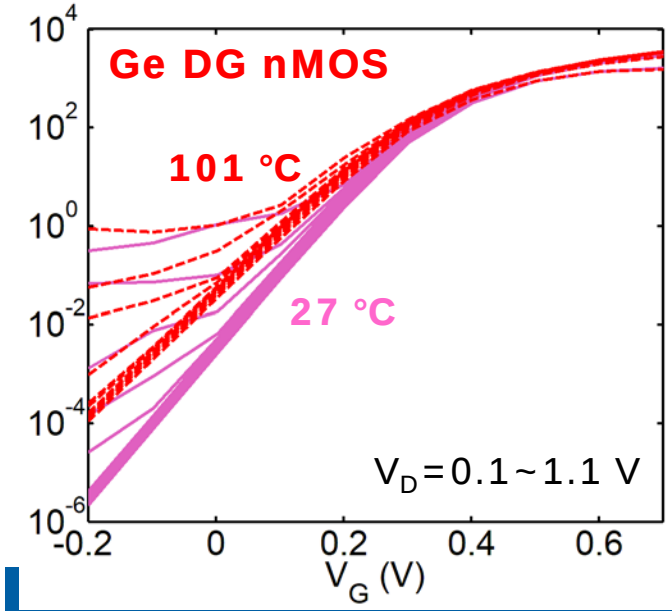
Application	Temperature
Mobile[a]	~60 °C
CPU[b]	100~120 °C
Automotive[c]	up to ~175 °C

a. G. Singla et al., *Proc. Design, Autom. Test Eur. Conf. Exhib.*, Mar. 2015, pp. 960–965.
b. J.-L. Tsai et al., *Proc. IEEE*, vol. 94, pp. 1502–1518, 2006
c. D. Cherniak et el., *Proc. IEEE RFIC*, Jun. 2017, pp. 57–60



R. Kim, U. E. Avci, and I. A. Young, IEEE EDL **41**, 1332-1335 (2020)

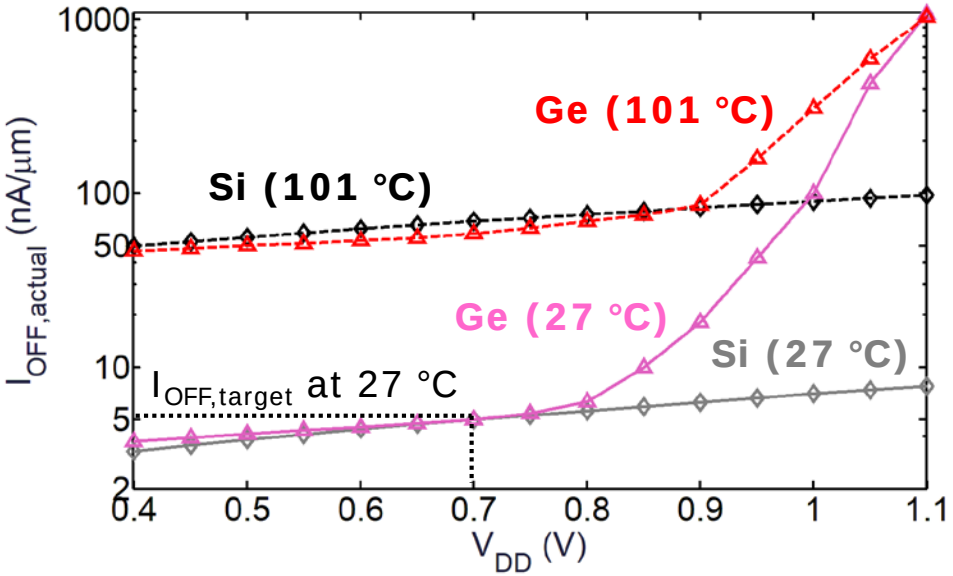


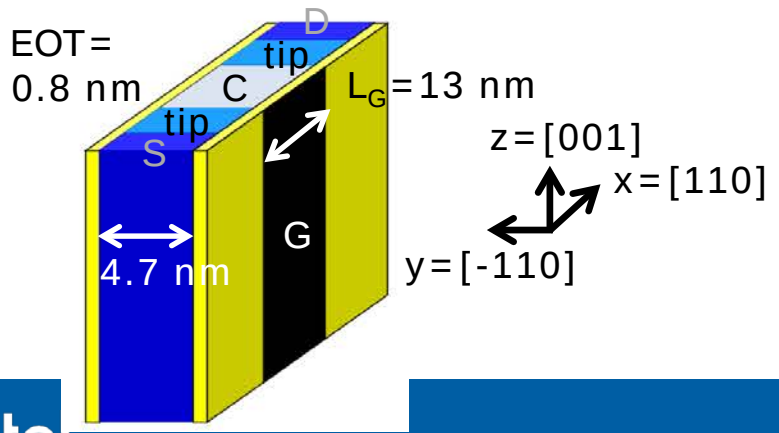


Temperature Effects

- $I_{OFF,actual}$: I_D at V_G=0 V, V_D=V_{DD}
- Si nMOS
  - $I_{OFF,actual}$ increases monotonically with V_{DD} (classical SCE)
  - $I_{OFF,actual}$ increases significantly with T (**$I_{thermal}$**)
- Ge nMOS
  - $I_{OFF,actual}$ first increases monotonically at low V_{DD}'s (classical SCE) but rapidly increases at high V_{DD}'s (**I_{BTBT}**)
  - $I_{OFF,actual}$ shows similar T-dependence as in Si at low V_{DD}'s (**$I_{thermal}$**) while the T-dependence becomes weaker at high V_{DD}'s (**I_{BTBT}**)

R. Kim, U. E. Avci, and I. A. Young, IEEE EDL **41**, 1332-1335 (2020)

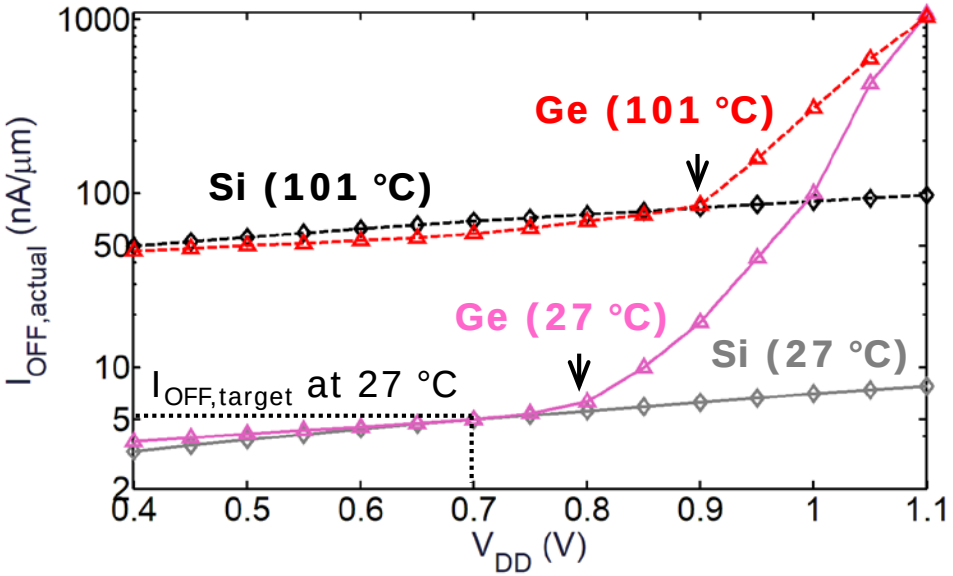


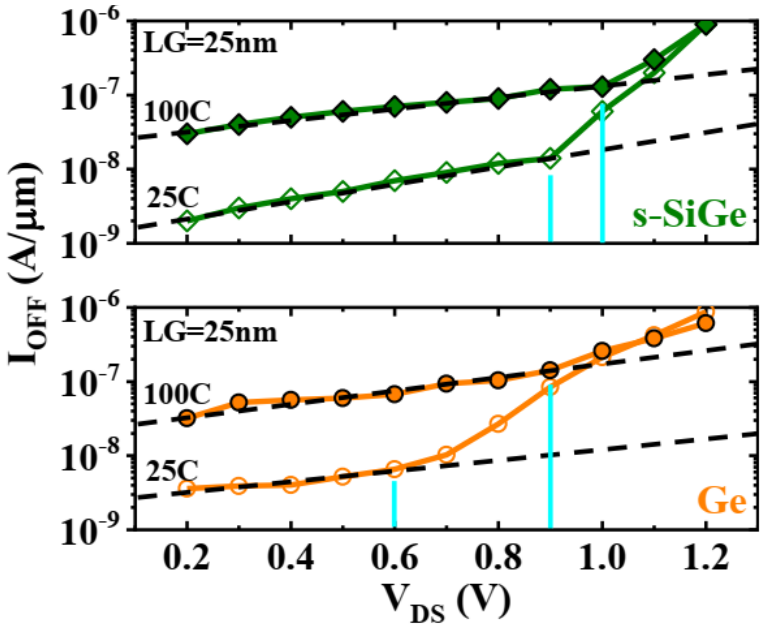


Temperature Effects

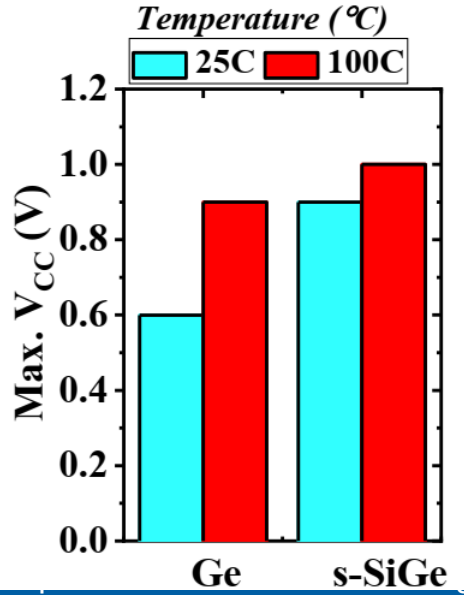
- A new metric: Maximum V_{DD} (**$V_{DD,max}$**)
  - Maximum V_{DD} where $I_{OFF,actual}$ of a device meets the $I_{OFF,actual}$ of the Si reference
  - Due to the different T-dependence of tunneling leakage, $V_{DD,max}$ of materials with light m^* and small E_g (e.g. InGaAs and Ge) increases at higher T.
- Confirmed by **experimental data** (SiGe and Ge pMOS)
  - *T-dependence of $I_{OFF,actual}$*
  - *Increase of $V_{DD,max}$ at high T*

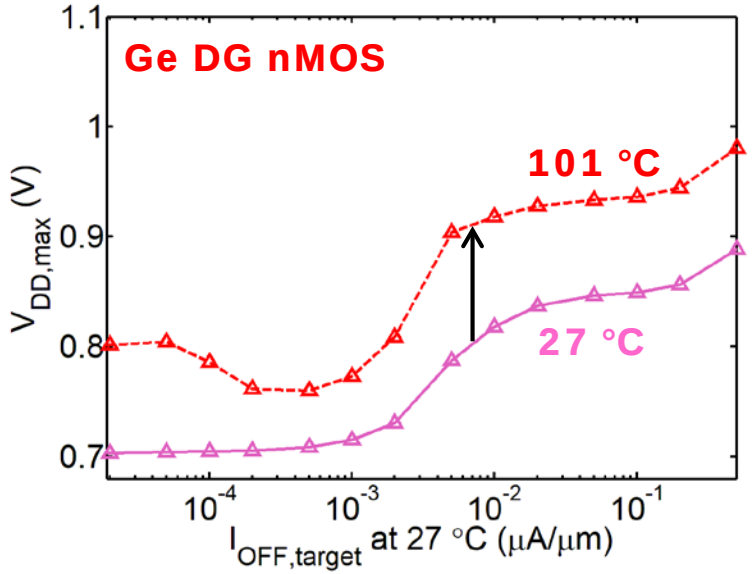
R. Kim, U. E. Avci, and I. A. Young, IEEE EDL **41**, 1332-1335 (2020)





A. Agrawal et al., in IEDM Tech. Dig., 2.2.1, Dec. 2020





Outline

- Model device
- Material-dependent device optimization
  - S/D tip design
  - Crystal orientation
- Carrier transport model
- Performance metrics
- Temperature effects
- Remaining challenges

Remaining Challenges

- While we have achieved significant benchmarking results for novel CMOS channel materials, there are still research gaps to be filled.

1) We used a “hybrid” approach by combining two different simulation tools (quantum ballistic + MC) to capture both effects of quantum transport and carrier scattering in a numerically manageable way.
   - A more **unified approach** may be developed to accurately include carrier scattering and quantum transport effects within a single, self-consistent simulation tool that is still **numerically tractable**.

2) While we considered some **circuit aspects** in our benchmarking (I_{eff}, CV^2, CV/I, operating T’s), more in-depth simulation may be done to analyze the material impact on the **layout**, **fabrication**, and **system-level performance** (“design-technology co-optimization”) to better help the material choice in future CMOS.
   - Novel CMOS channel materials (e.g. III-V’s and Ge) may promise performance boost for individual transistors, but they may also give **integration challenges** to Si-based technology.

Thank you for your attention!