

# Purdue ECE MN Area Research

Muhammad Ashraful Alam, Joerg Appenzeller, Zhihong Chen, Supriyo Datta, Sumeet Gupta,  
David Janes, Gerhard Klimeck, Mark Lundstrom, Dana Weinstein, Pramey Upadhyaya, Peide Ye

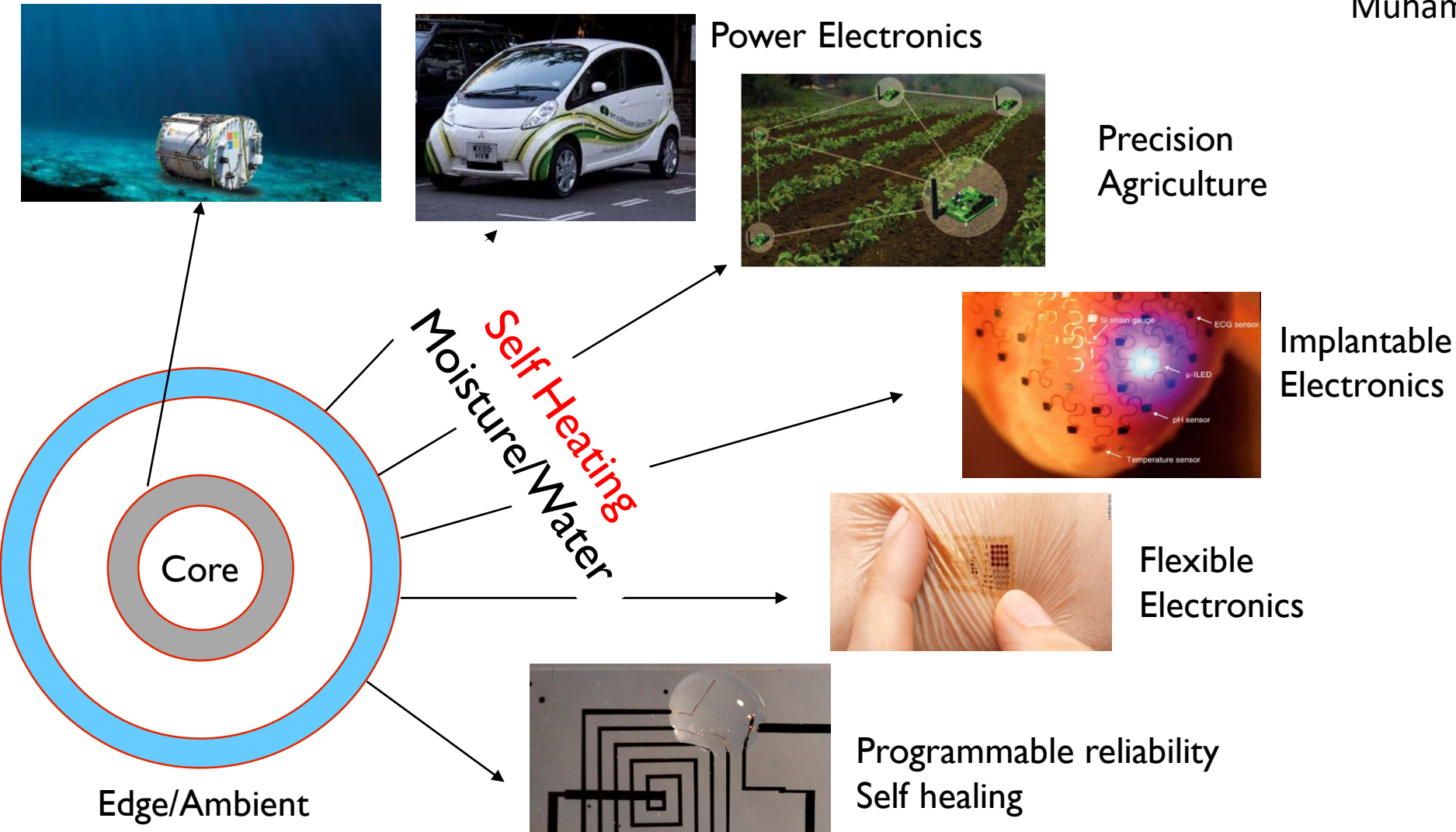
Microelectronics and Nanotechnology Area  
School of Electrical and Computer Engineering



# Reliability Physics of Classical and Emerging Electronic Devices (CEED)



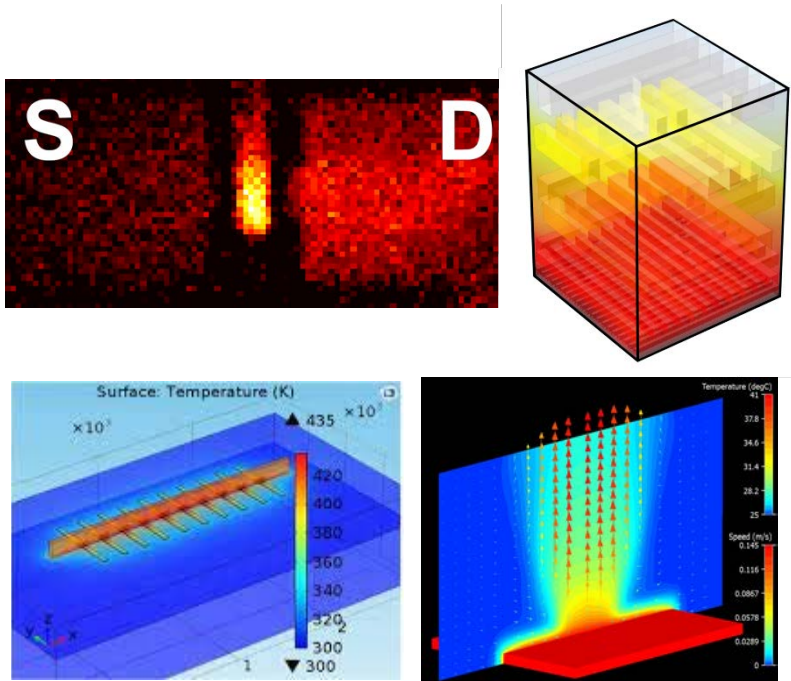
Muhammad A. Alam



# CEED: Challenges and Opportunities

## Integrated Circuits

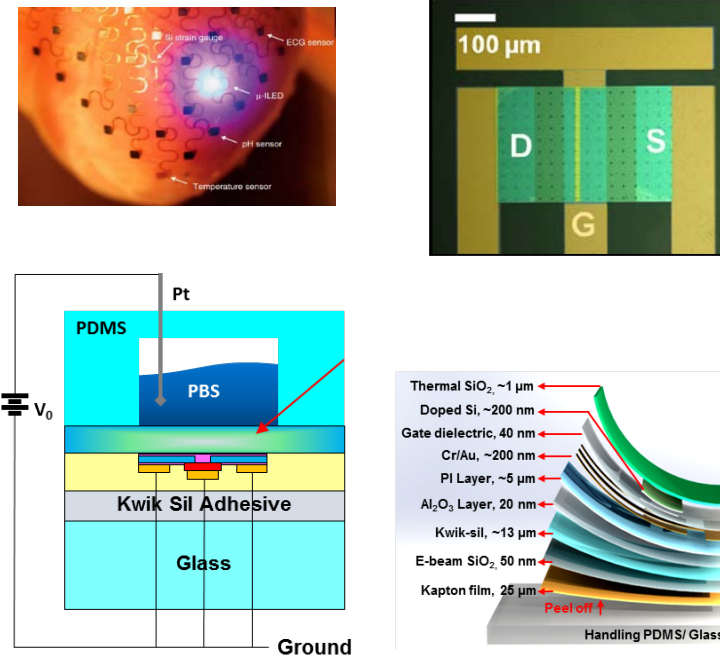
IC and Mission-specific Self-heating  
 FEOL/BEOL/Mold-compound interactions  
 Reliability as a design variable



IEEE TED 2017, 2018, 2020

## Biosensors

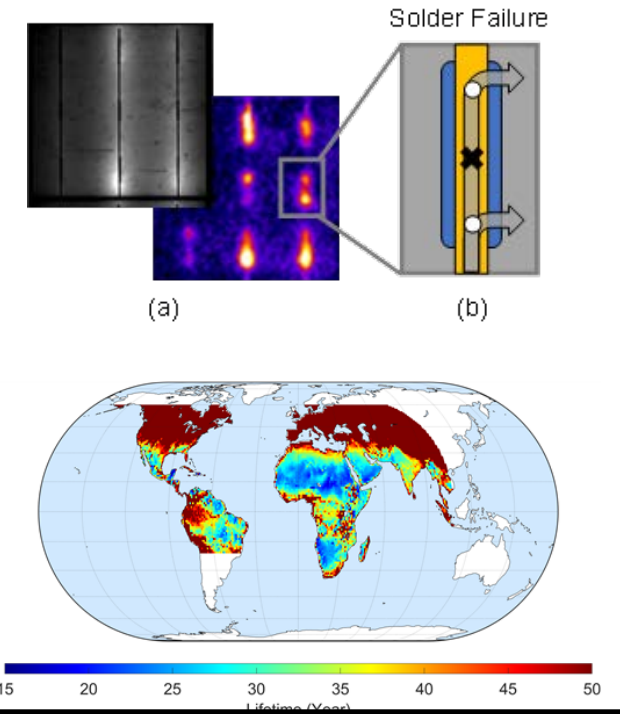
Calibration-drift in harsh/uncontrolled Environment; Next generation packaging, Reliable sensing in unreliable environment



IEEE TED 2020, PNAS 2019

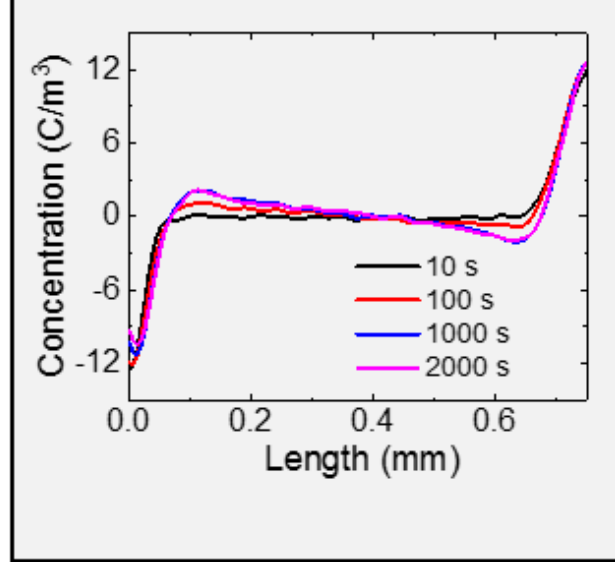
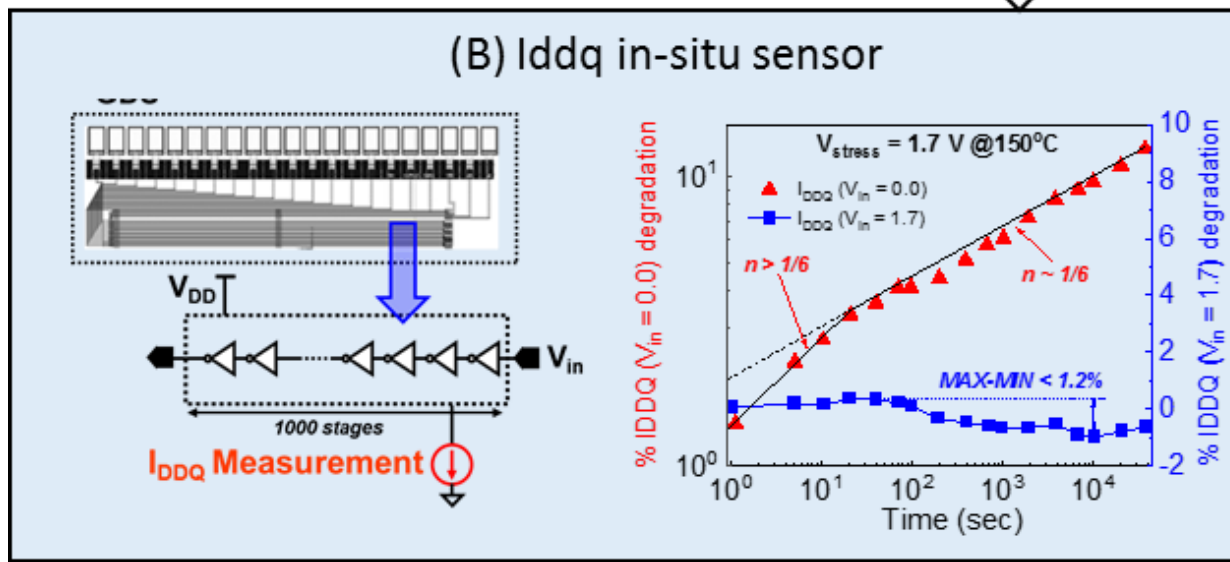
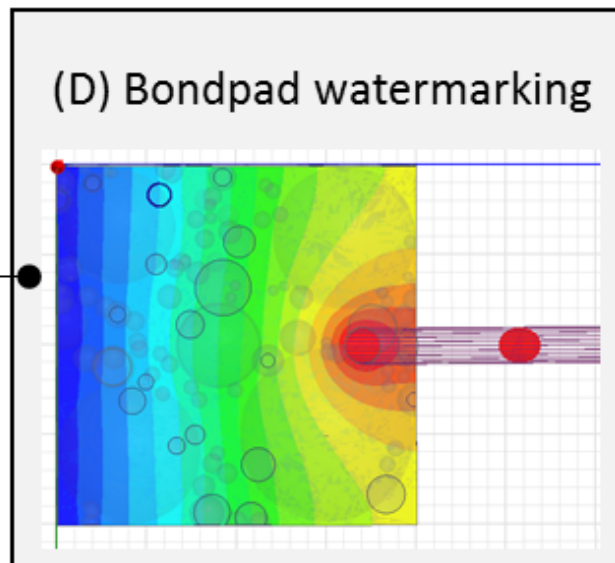
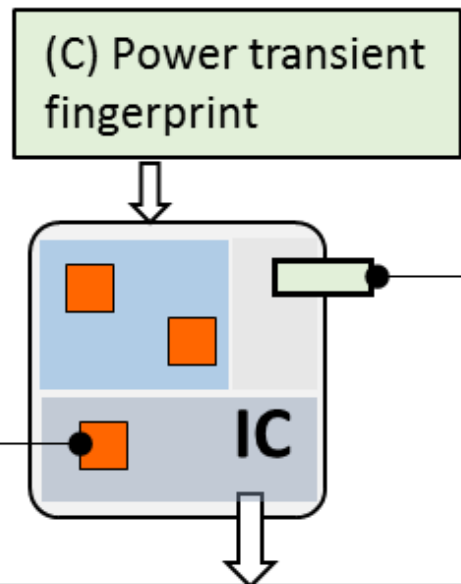
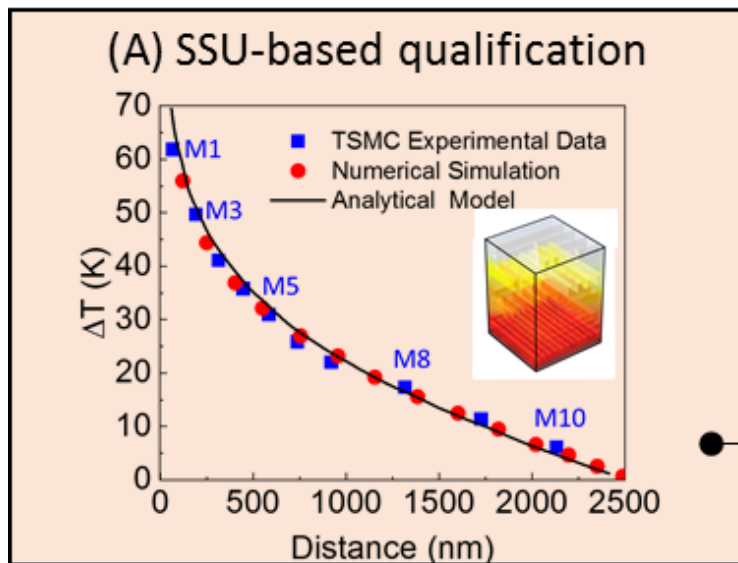
## Energy harvesters

Technology suitable for highly Variable weather conditions  
 Location-aware reliability



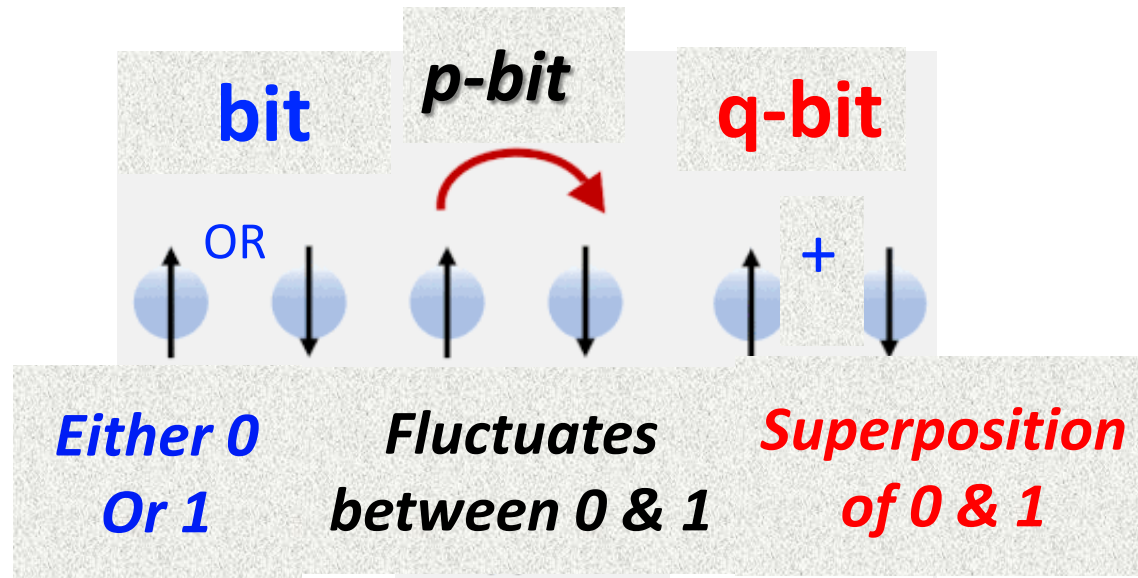
JPV 2019, Applied Energy 2021

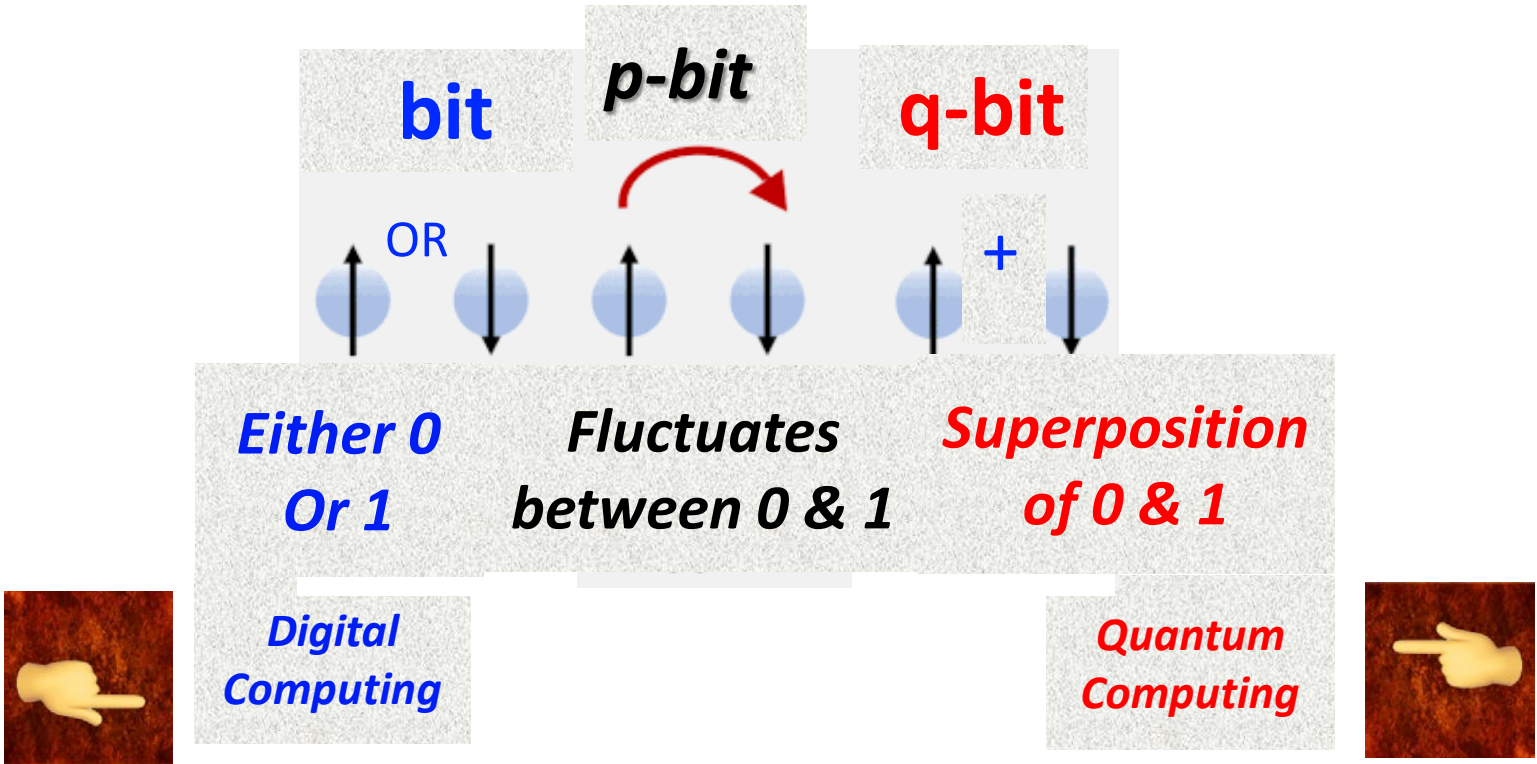
# “Intrinsic Odometers” for Secure Electronics

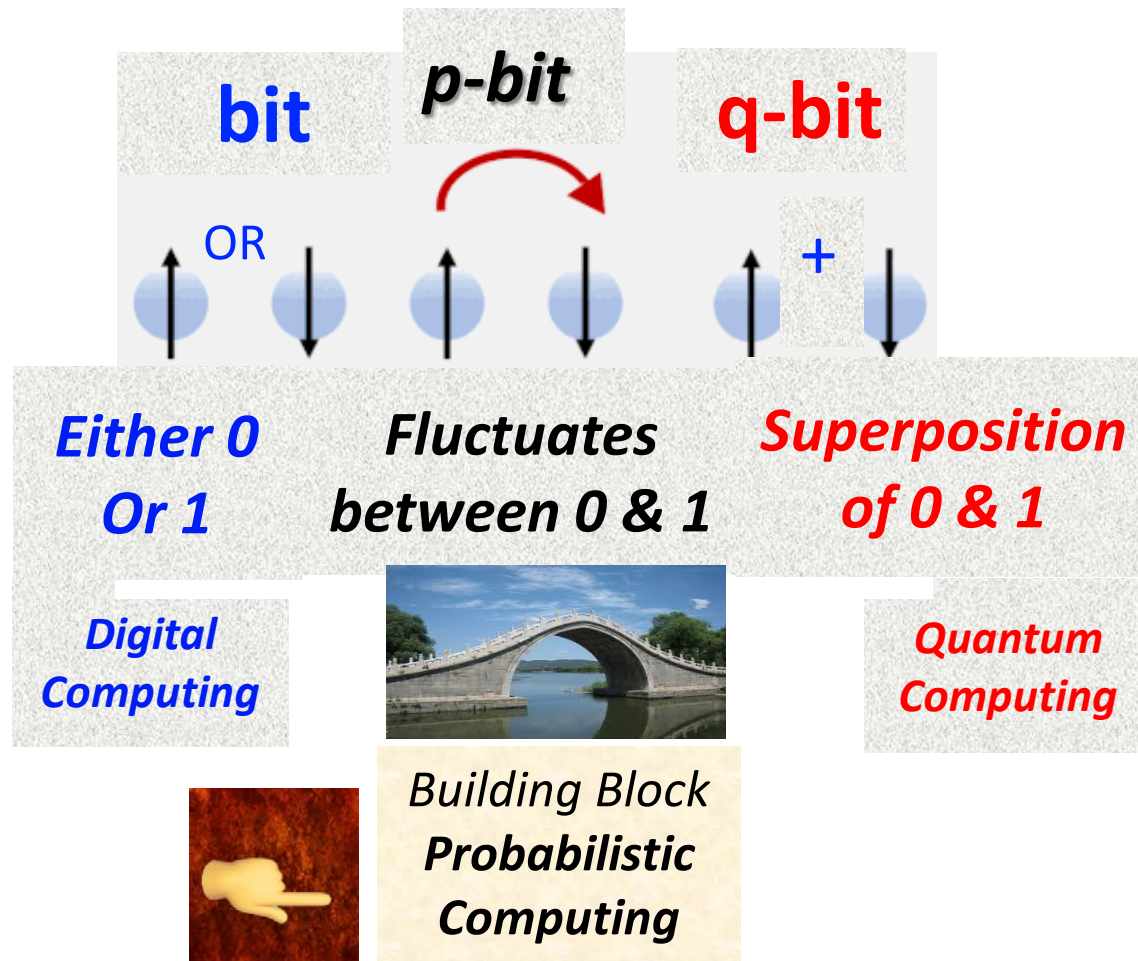


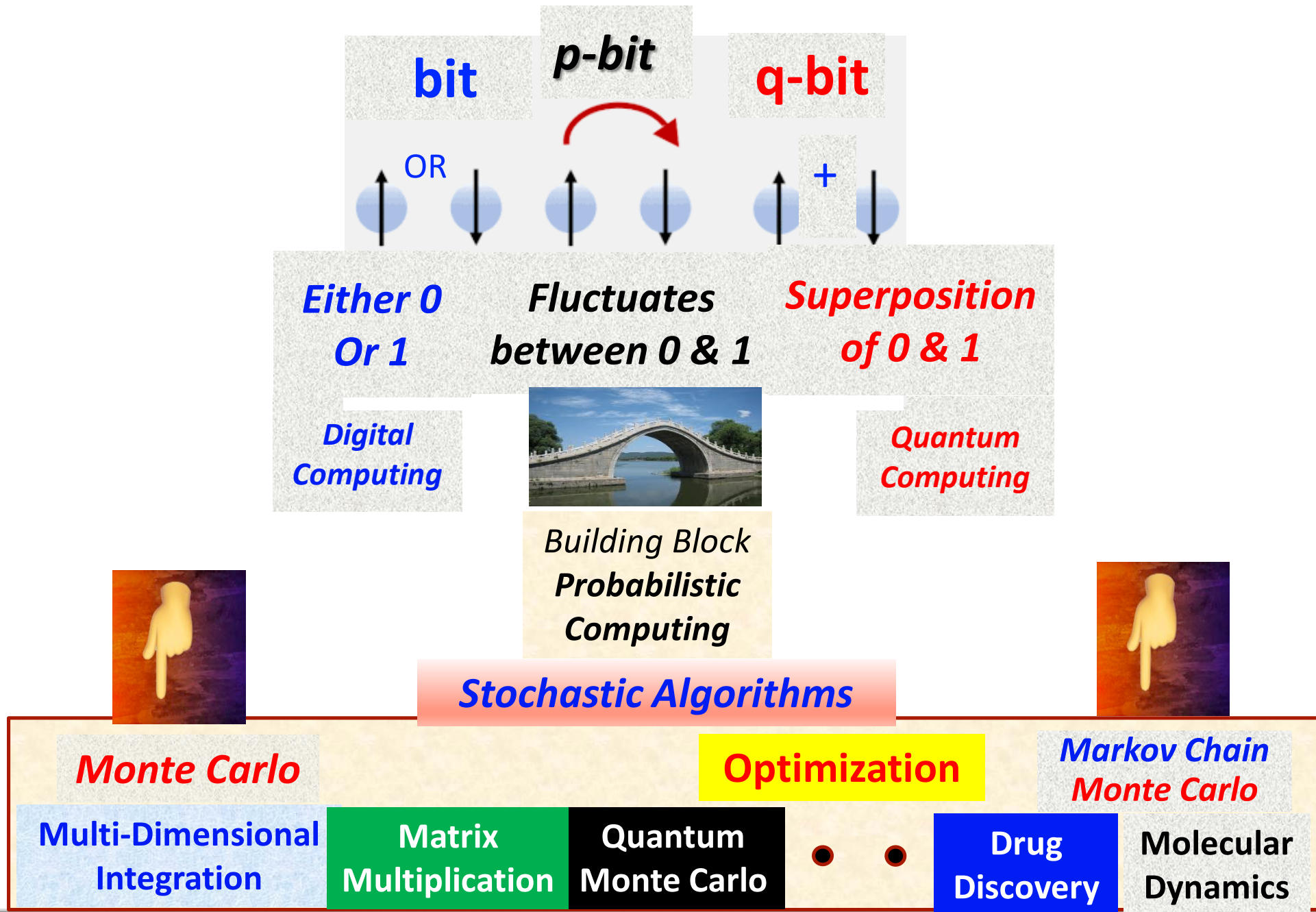


Supriyo Datta

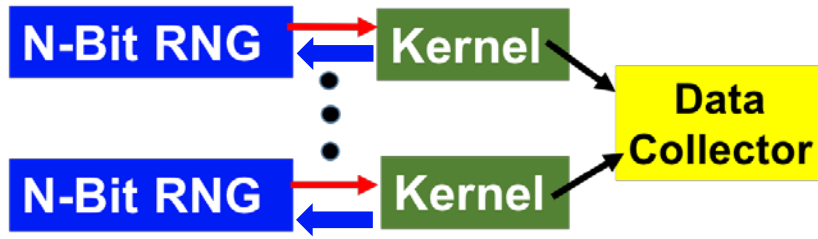








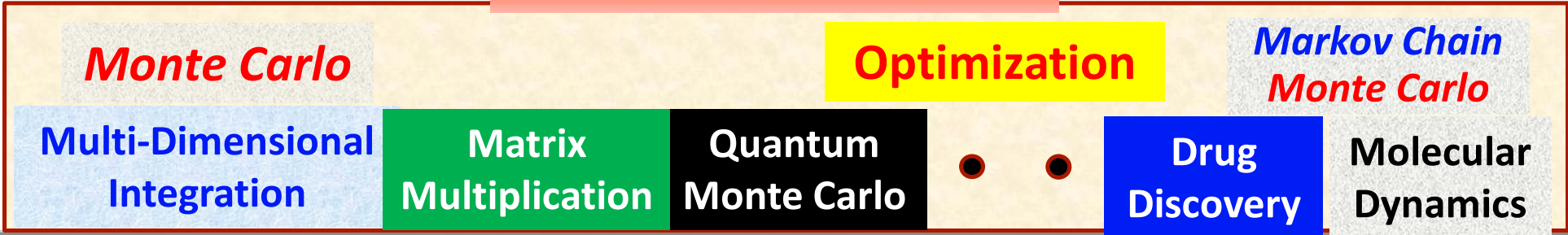


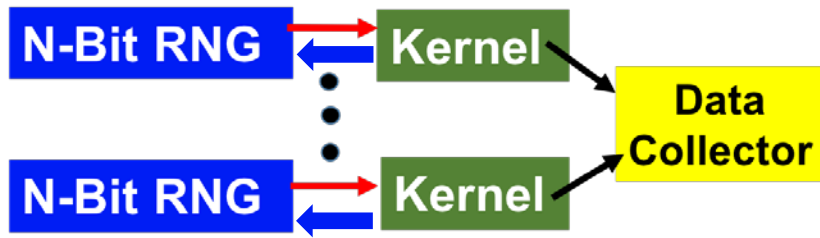


*Easy to parallelize*  
**"Architecture"**

*Building Block*  
**Probabilistic**  
**Computing**

*Stochastic Algorithms*





125 MHz  
FPGA  
aws

Available for public use at  
<https://www.purdue.edu/p-bit/>

IEEE Access 8, 157238 (2020)

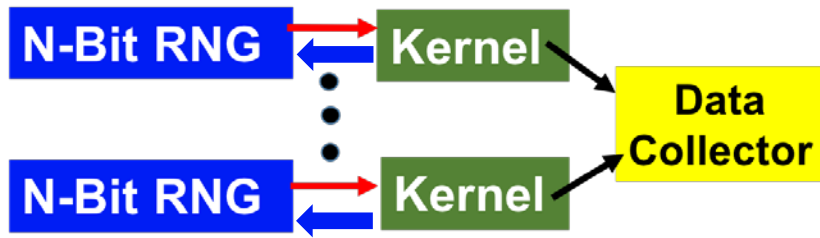


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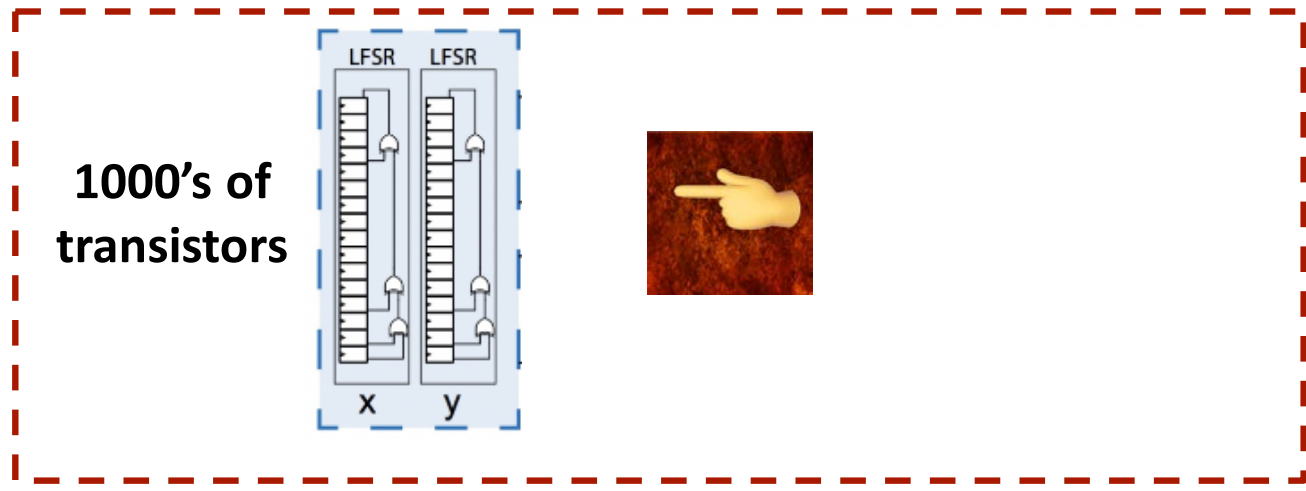
125 MHz  
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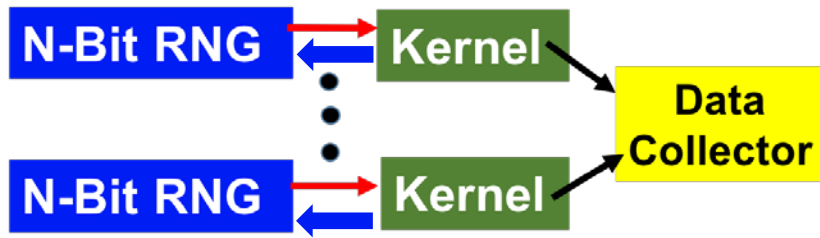
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IEEE Access 8, 157238 (2020)

*Easy to parallelize*  
**"Architecture"**

*Physics-Based  
Drop-in  
Replacement*





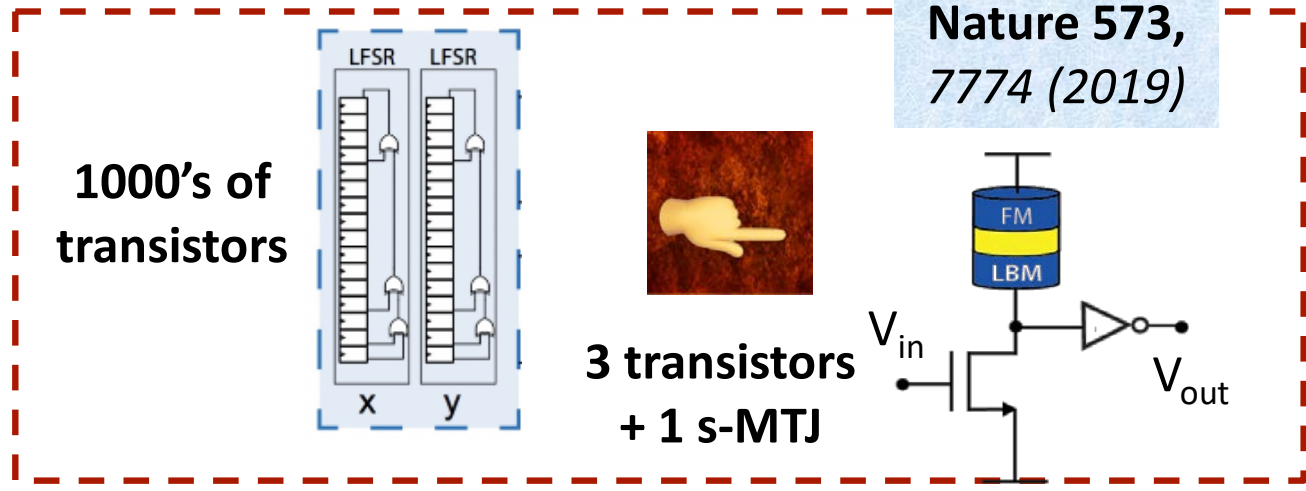
125 MHz  
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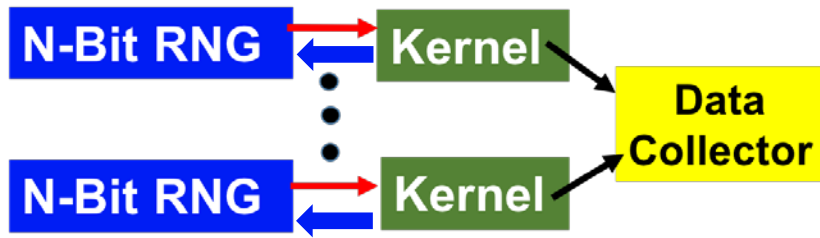
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IEEE Access 8, 157238 (2020)

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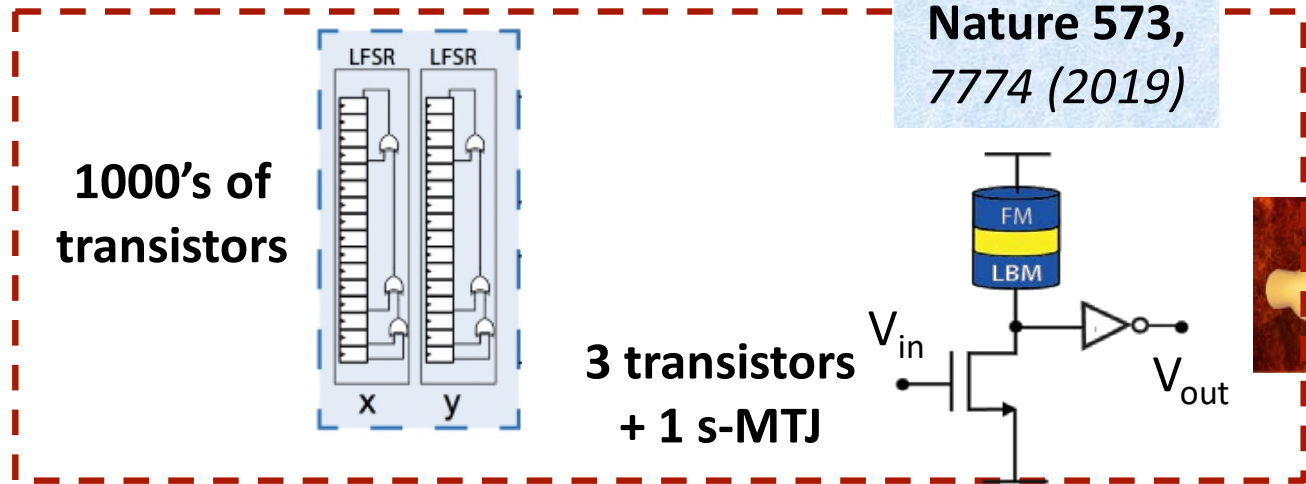
125 MHz  
FPGA  
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IEEE Access 8, 157238 (2020)

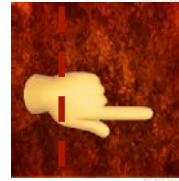
*Easy to parallelize*  
**"Architecture"**

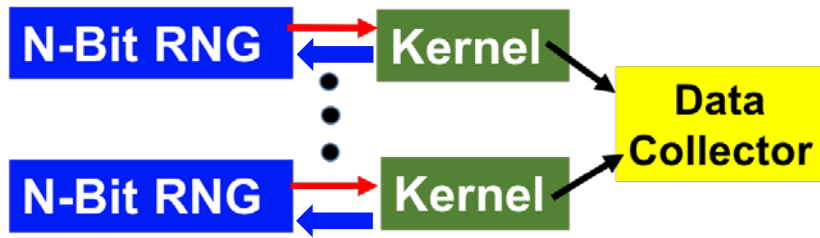
*Physics-Based*  
*Drop-in*  
*Replacement*



*Nanosecond*  
*fluctuations in*  
*resistance*

*Experimentally*  
*demonstrated*





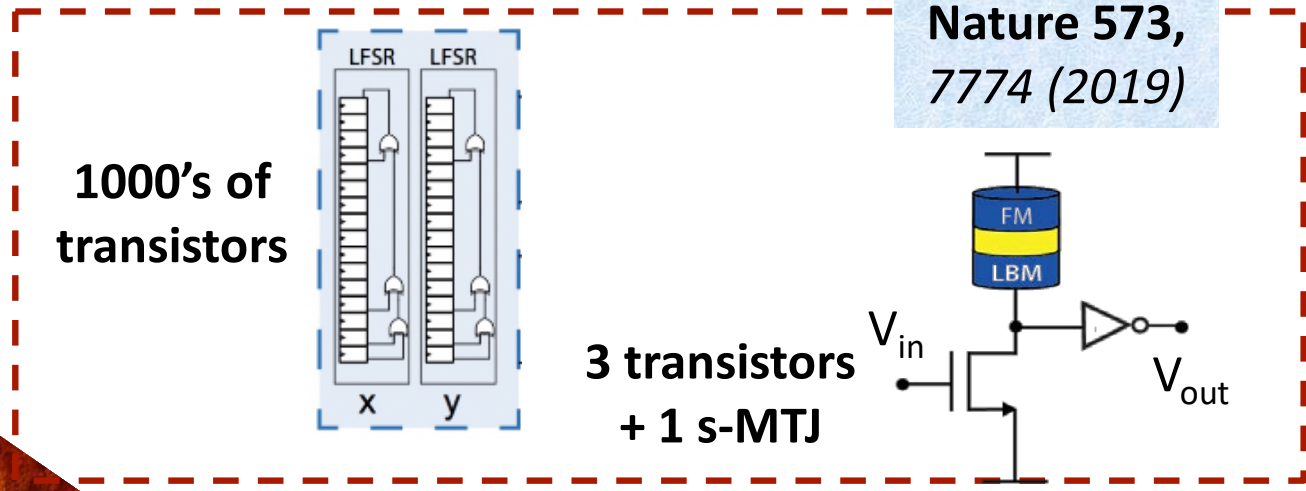
125 MHz  
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IEEE Access 8, 157238 (2020)

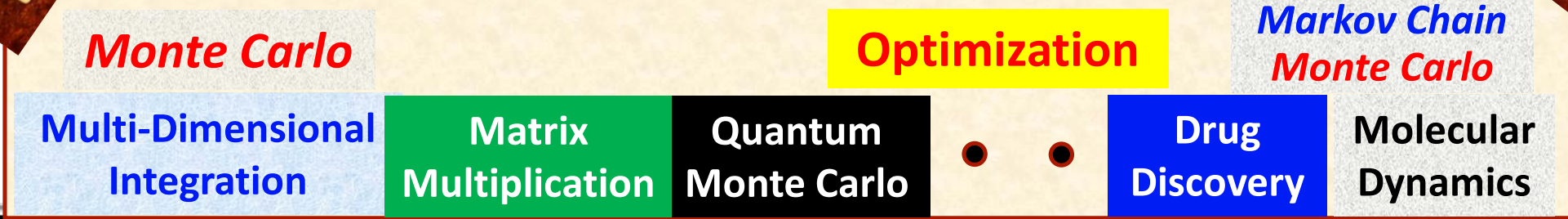
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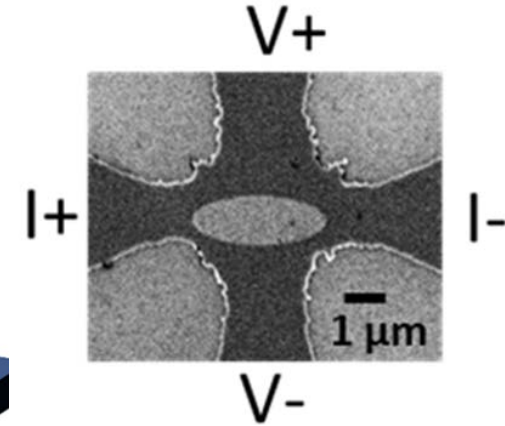
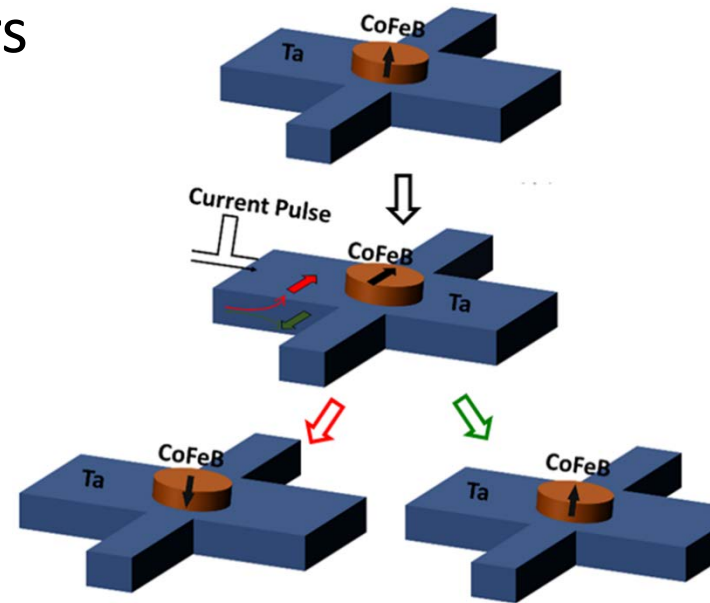
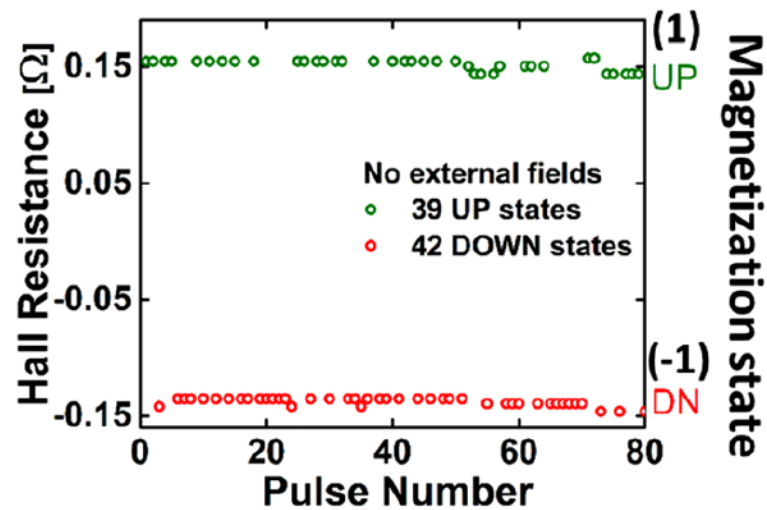
# Experimental work on p-bits and circuits



Joerg Appenzeller

## Tunable random number generators

1. Spin Orbit Torque (SOT) current pulse for hard axis initialization (*clock*)



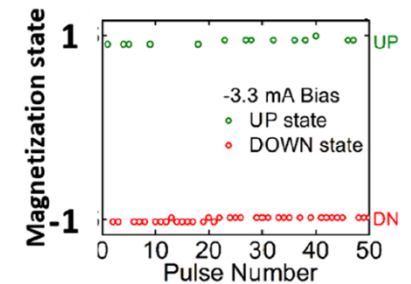
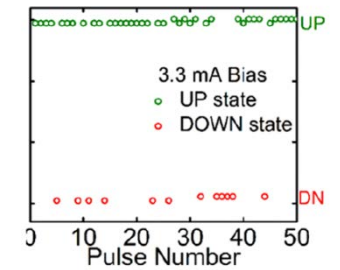
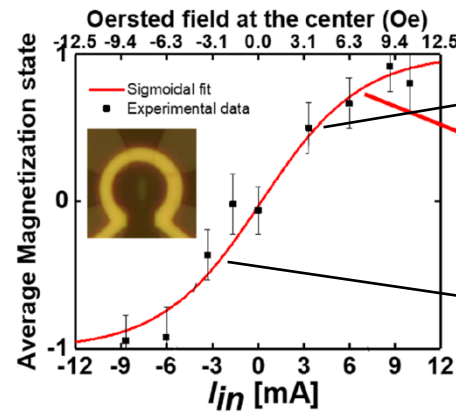
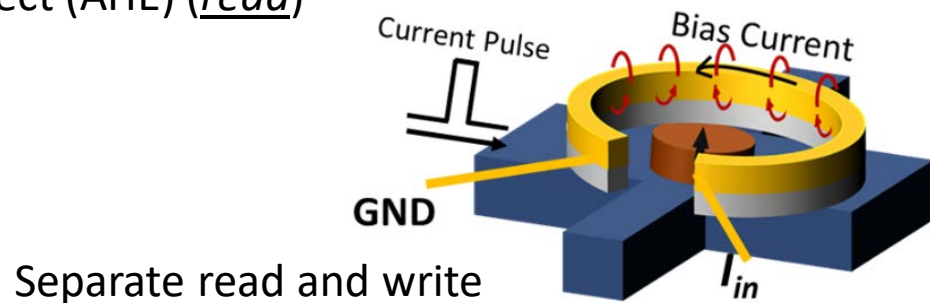
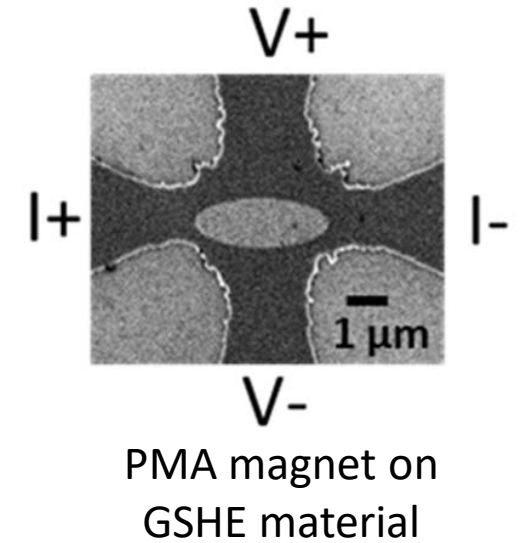
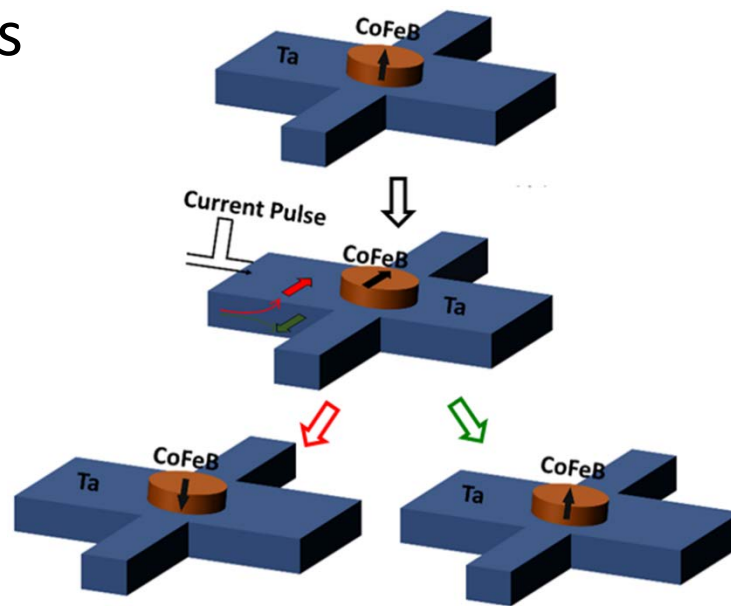
PMA magnet on GSHE material

For sufficiently large current pulses the magnet is found in its up and down state with a 50% / 50% probability!

# Experimental work on p-bits and circuits

## Tunable random number generators

1. Spin Orbit Torque (SOT) current pulse for hard axis initialization (*clock*)
2. Input current through Oersted ring (*write*)
3. Read out through Anomalous Hall Effect (AHE) (*read*)

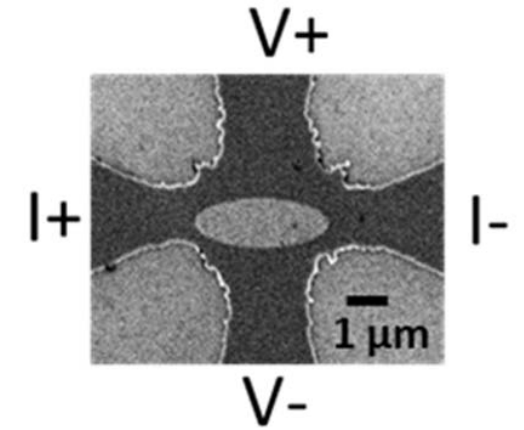
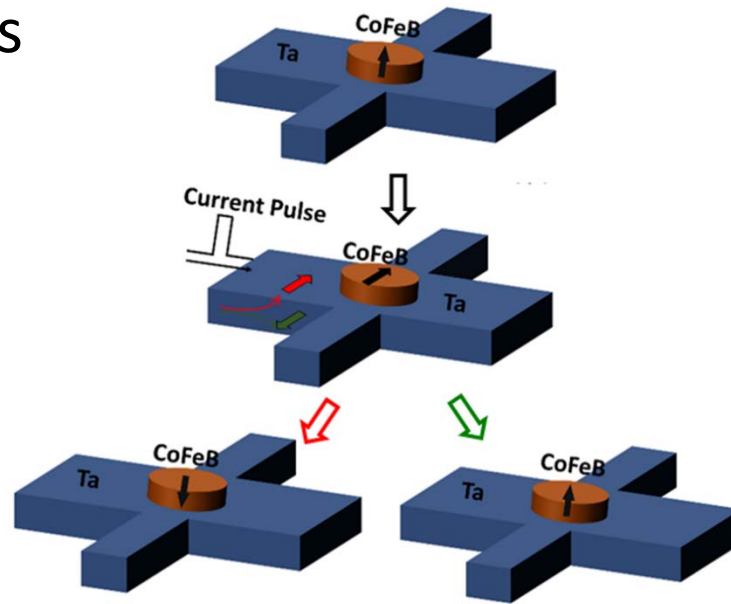




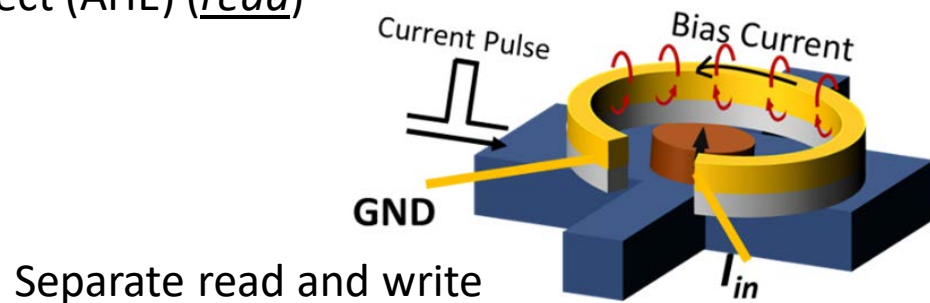
# Experimental work on p-bits and circuits

## Tunable random number generators

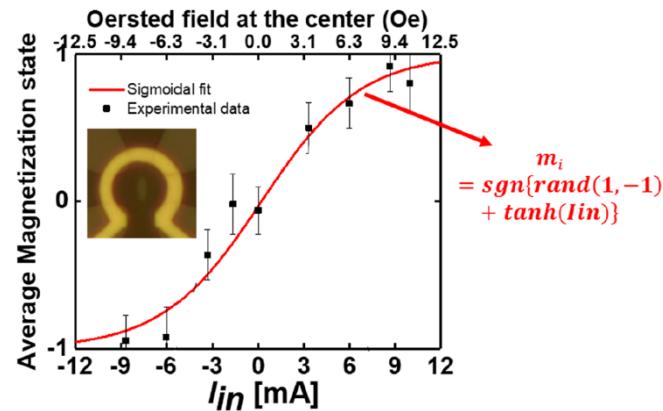
1. Spin Orbit Torque (SOT) current pulse for hard axis initialization (clock)
2. Input current through Oersted ring (write)
3. Read out through Anomalous Hall Effect (AHE) (read)



PMA magnet on GSHE material



Separate read and write

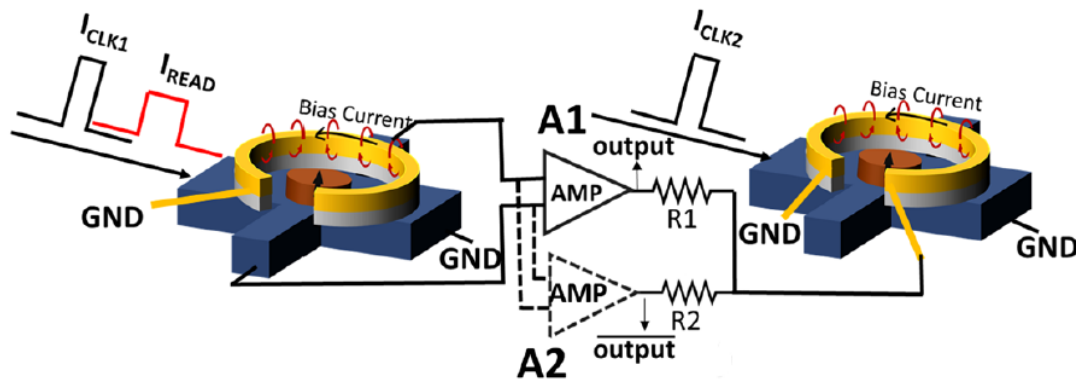


Demonstration of an all-electrical p-bit with field generating metal ring!

# Experimental work on p-bits and circuits

## Correlations in connected p-circuits

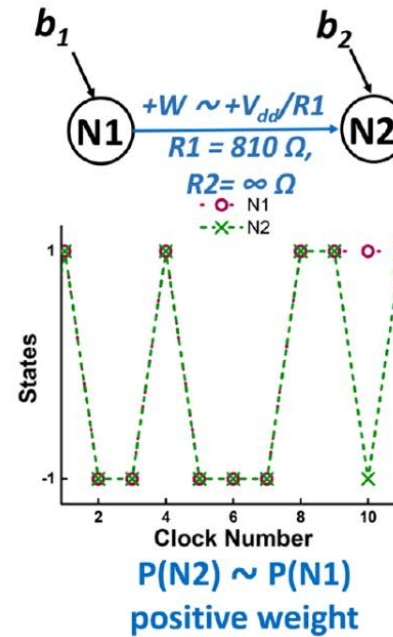
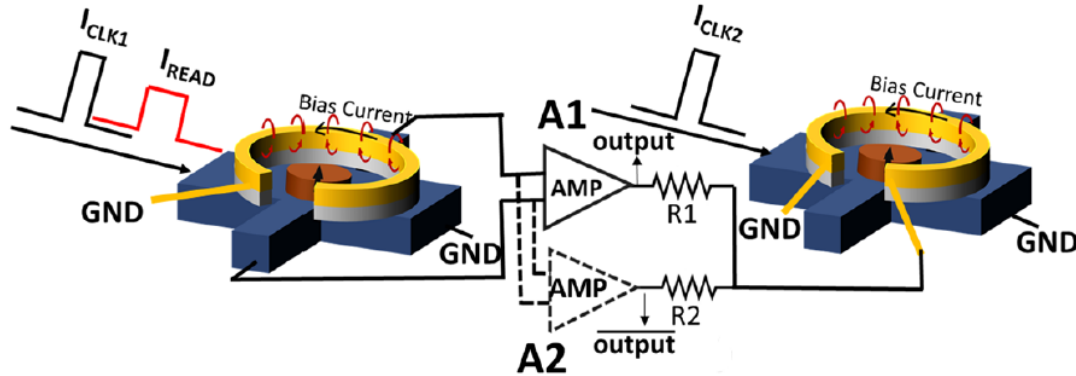
- Each node exhibits a sigmoidal activation function
- Nodes are connected through resistors R1 and R2, allowing for different weights of the interconnect
- During measurement devices are clocked, an input pulse is provided, and the state of the two magnet nodes N1 and N2 are read by AHE



# Experimental work on p-bits and circuits

## Correlations in connected p-circuits

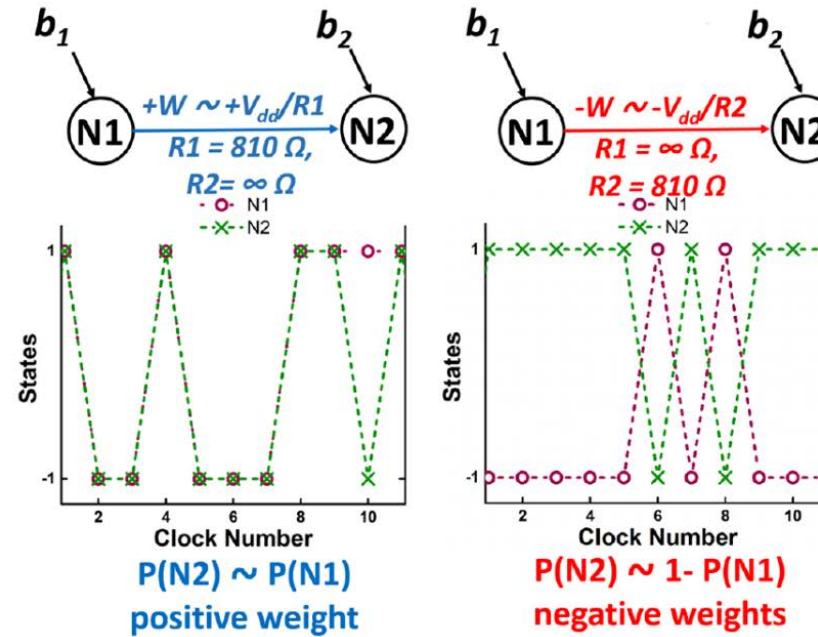
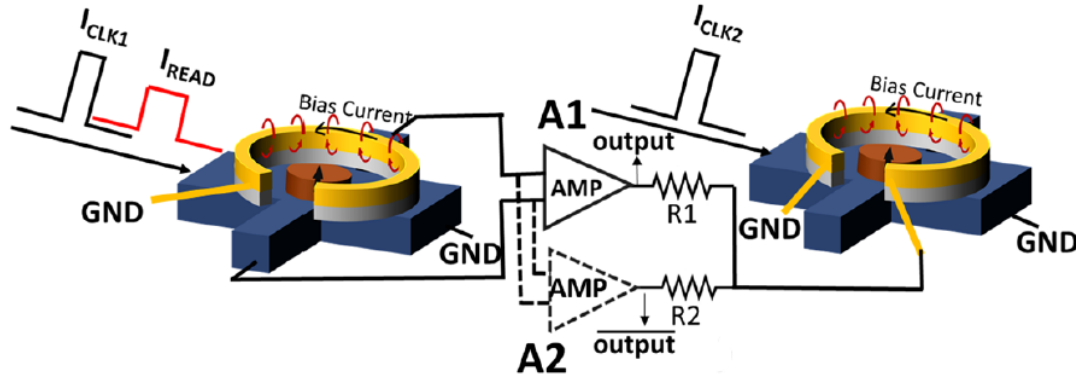
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# Experimental work on p-bits and circuits

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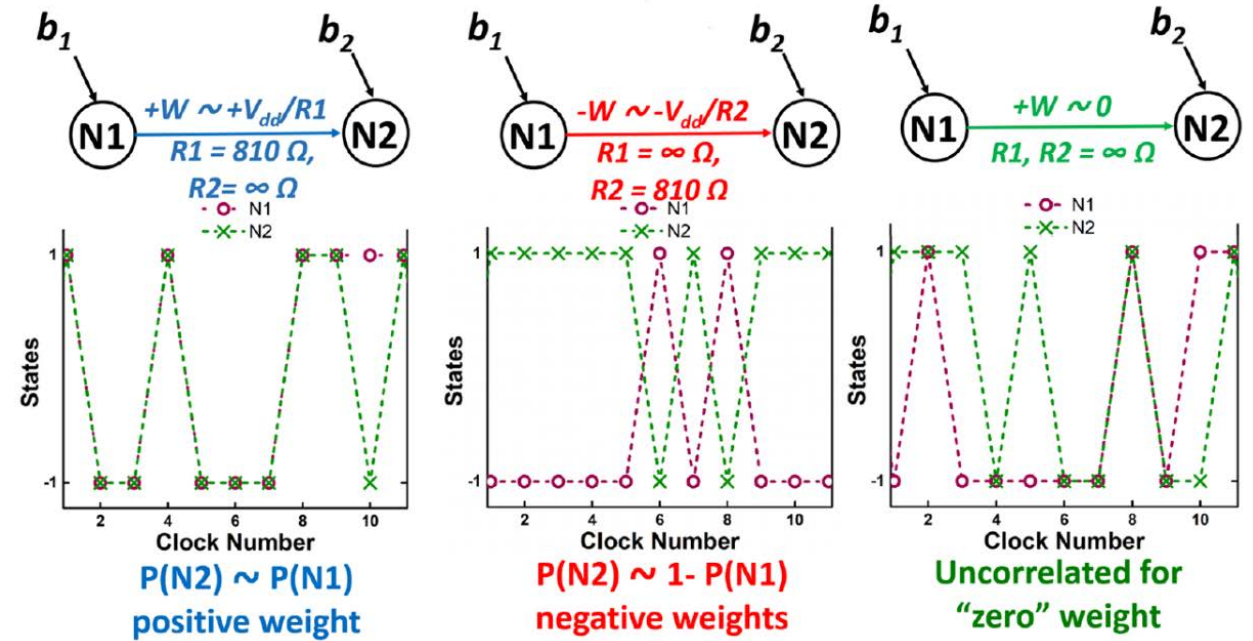
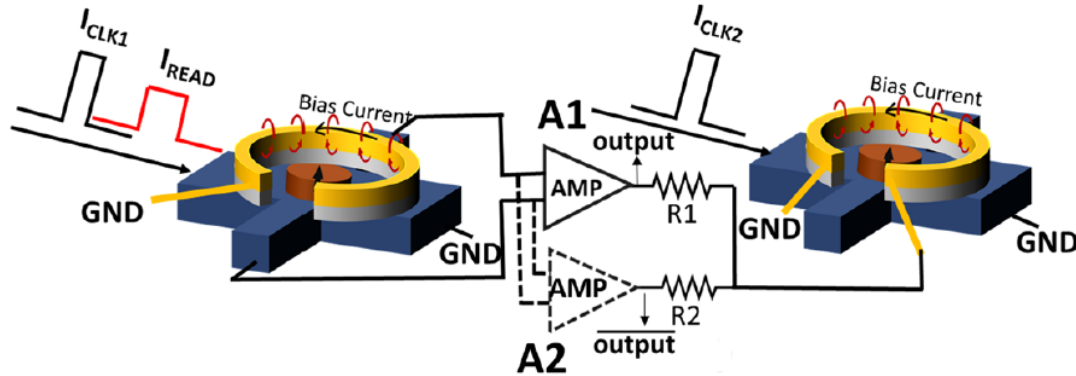
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# Experimental work on p-bits and circuits

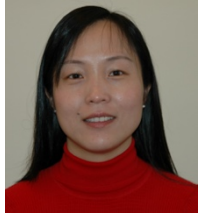
## Correlations in connected p-circuits

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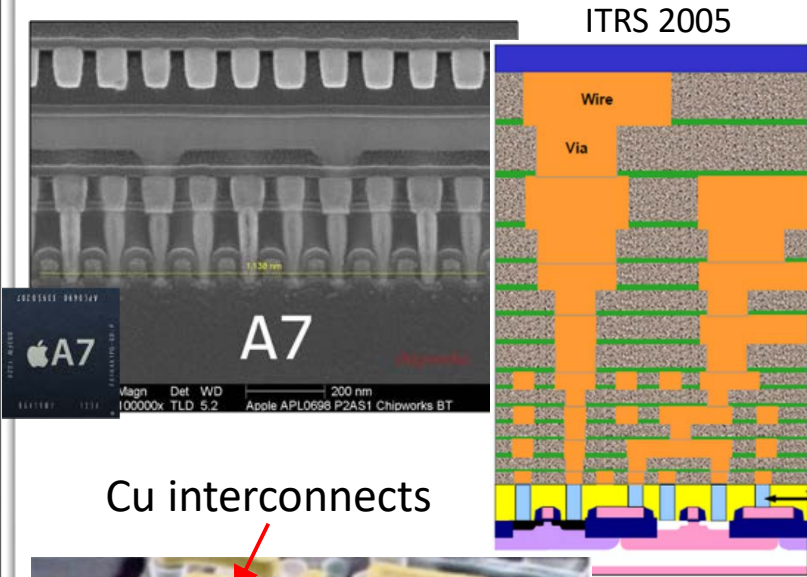


Demonstration of a weighted 2 p-bit circuit!

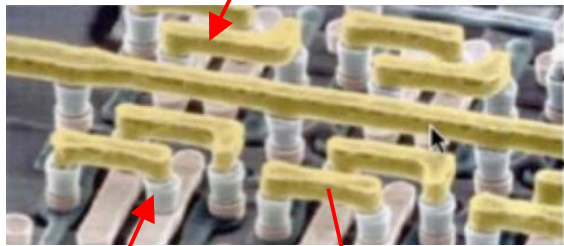
# 2D Materials for BEOL Interconnect Technologies



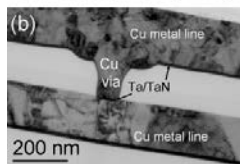
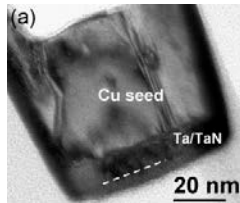
Zhihong Chen



Cu interconnects

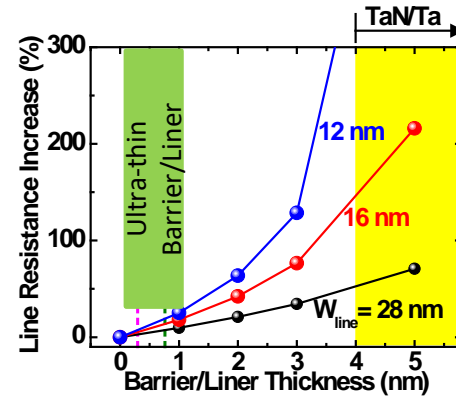
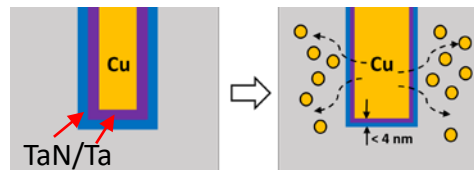


via



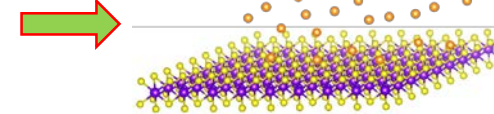
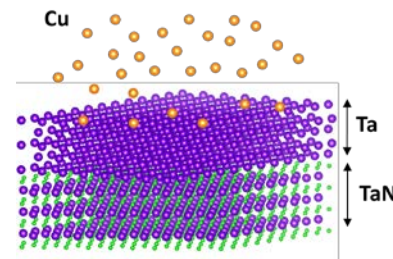
Mat. Sci. Semi. Proc, **27**, 860 (2014)

Diffusion Barrier/Liner Bilayer (TaN/Ta)

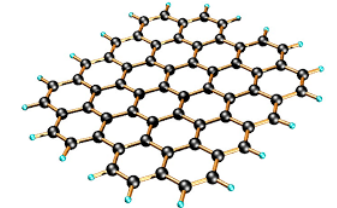
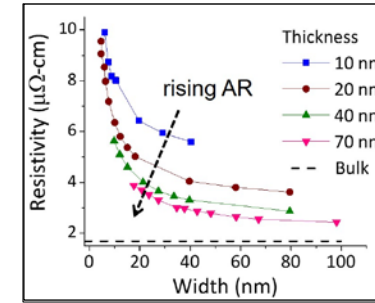
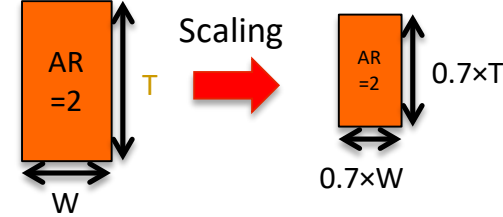


- Conventional barrier/liner > 4nm
- Increasing Cu resistivity at scaled dimensions

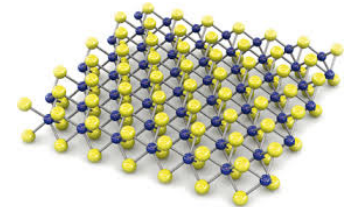
Line resistance  $\uparrow$  electromigration  $\uparrow$  Joule heating  $\uparrow$



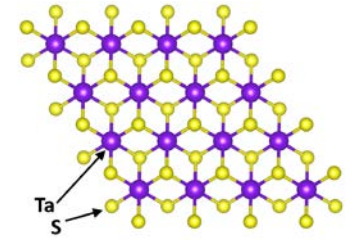
Atomically thin 2D materials as diffusion barrier, liner and capping layer



Graphene

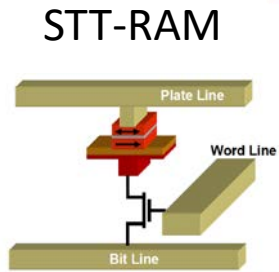
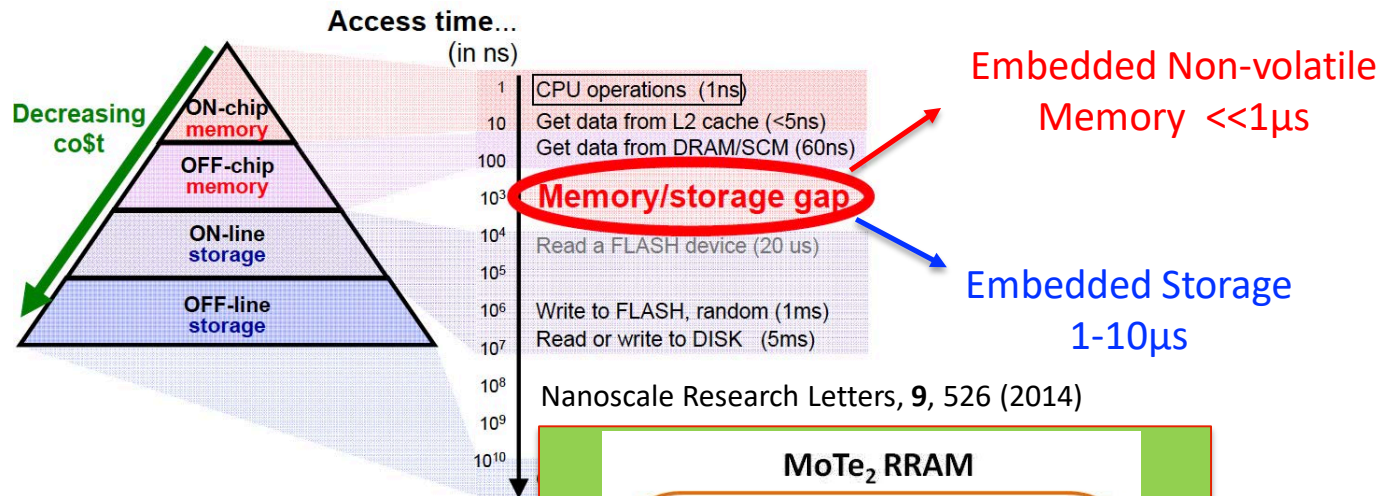


MoS<sub>2</sub>

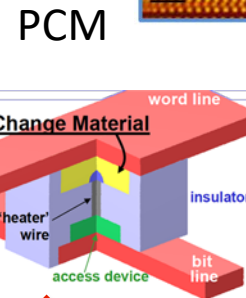
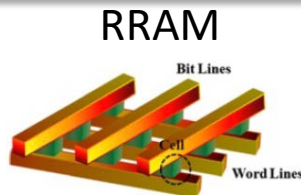
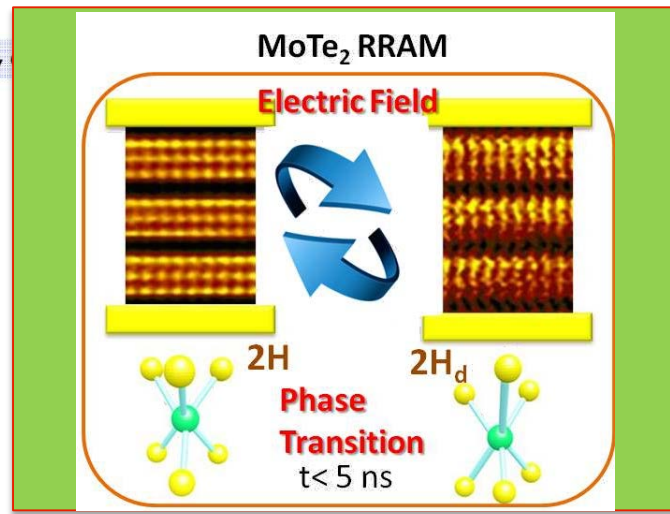


TaS<sub>2</sub>

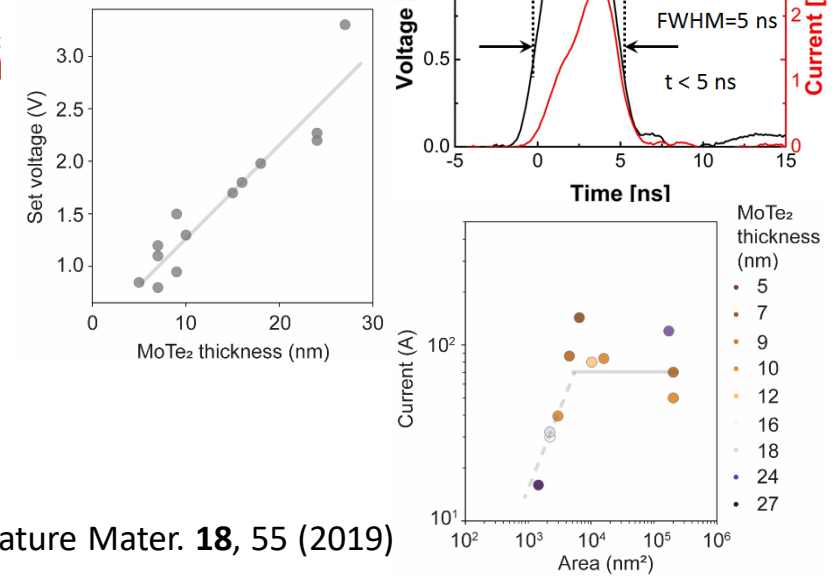
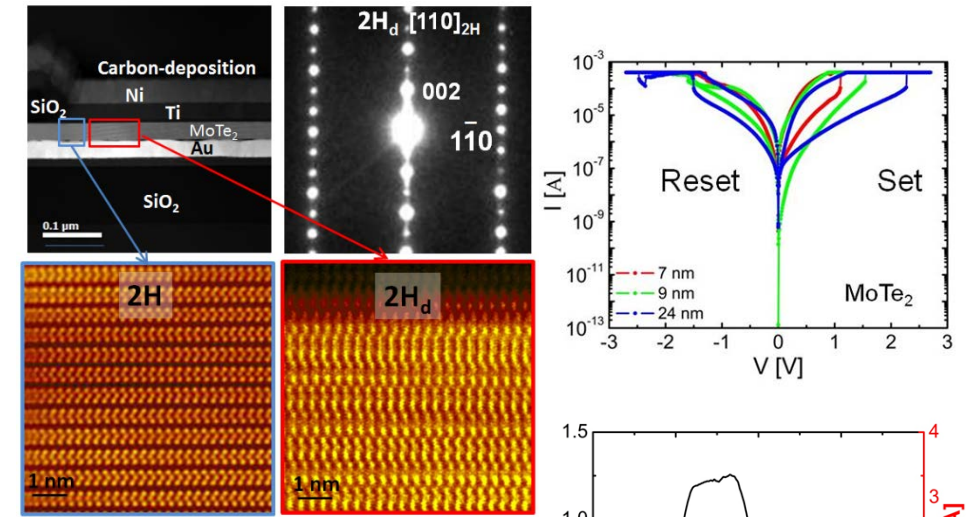
# 2D Materials for High-speed Non-volatile Memory



Higher Density



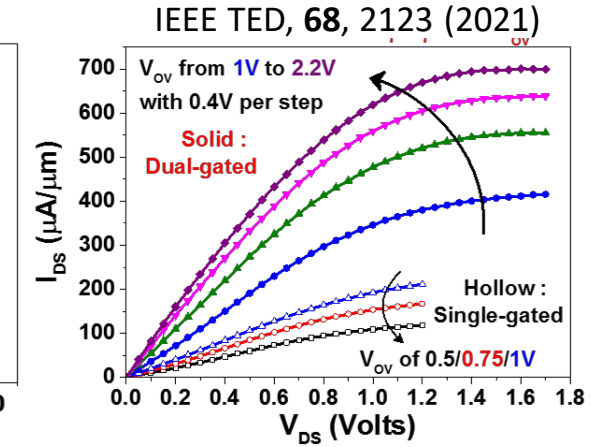
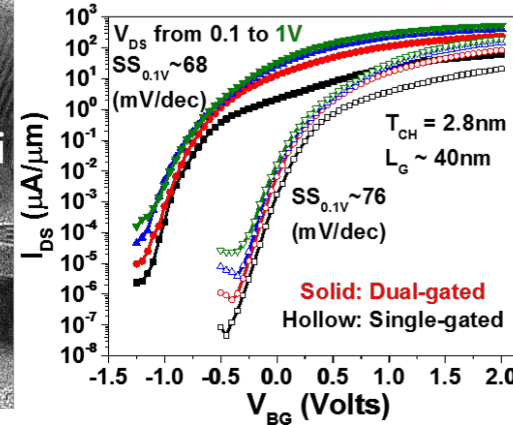
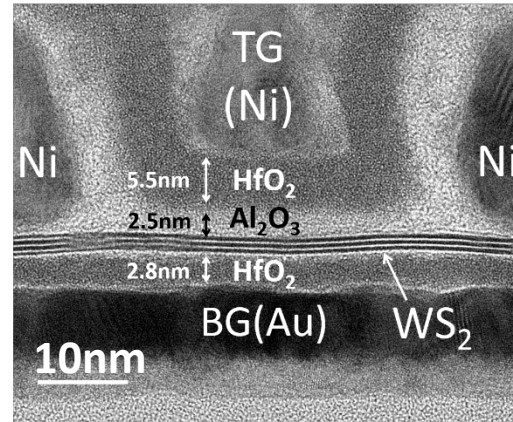
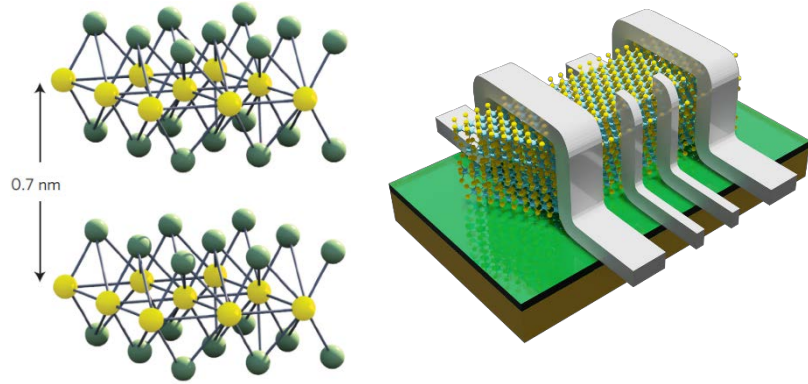
Faster



Nature Mater. 18, 55 (2019)

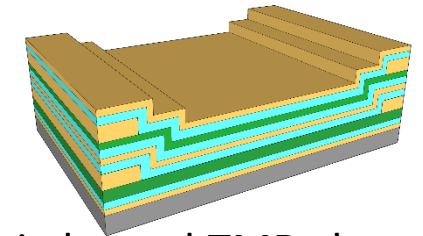
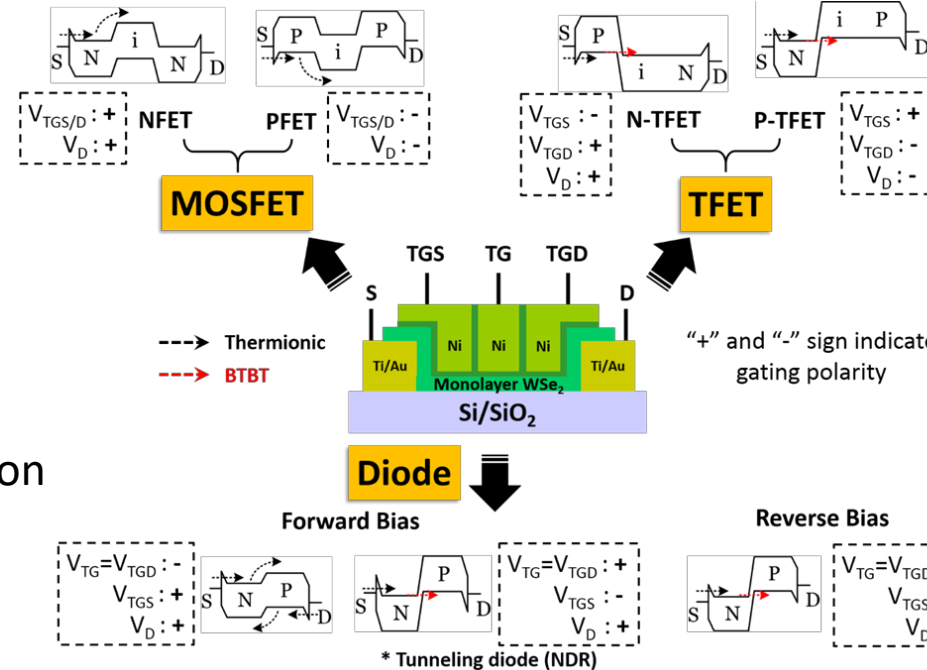
Electric field induced phase change in 2D materials for high speed, low energy, non-volatile memory – combined RRAM+PCM

# 2D TMD Materials for Beyond CMOS Applications

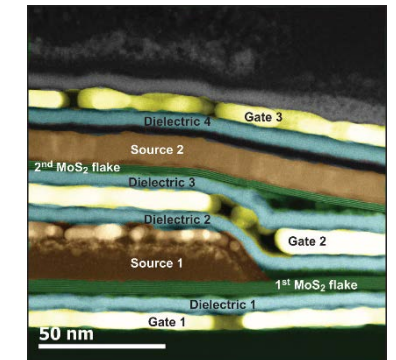


- Ultra-thin body for aggressive scaling
- Comparable field-effect mobility
- Thickness-dependent  $E_g$  from 1-2 eV
- Access of both electron and hole injection

Small 15, 1902770 (2019)



Multi-channel TMD sheet FETs



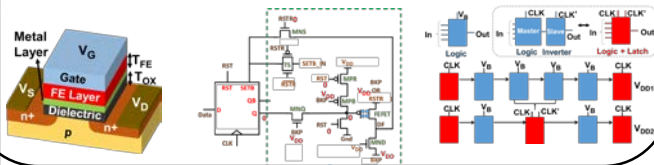
Demonstrations of 2D TMD based MOSFETs, Tunneling FETs, reconfigurable FETs, and 3D integration of multi-channel FETs



# Research Overview – Sumeet Gupta

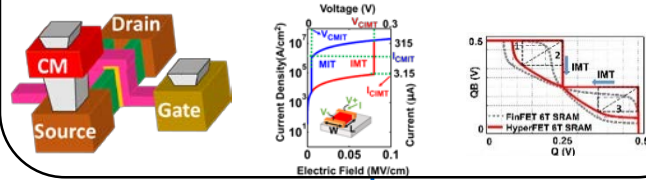
## Ferroelectric FETs

- Non-volatile memories
- Logic-Memory Reconfigurability
- Non-volatile Computing
- In-Memory Computing



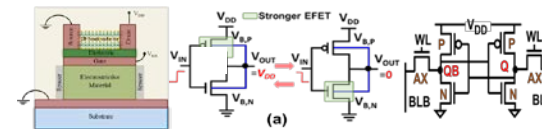
## Correlated-Material Enhanced Electronics

- Phase FETs: Steep Switching Devices
- Logic and SRAM Design
- Selectors for Cross-point Memories



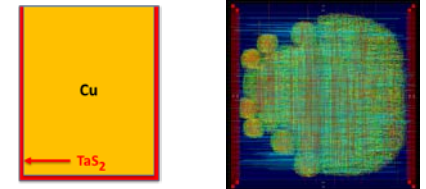
## Piezoelectric FETs

- Logic based on steep switching FETs
- Non-volatile memories
- In-memory computing



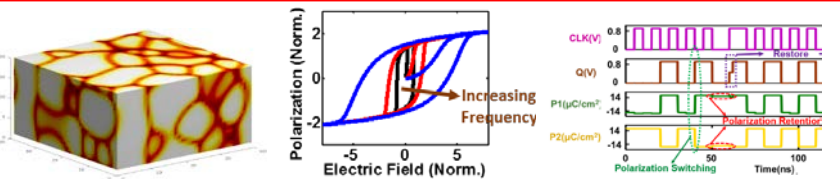
## TMD based Electronics

- Interconnects
- Logic and Memory Design



## Modeling and Simulation

- Phase field and Compact model for Ferroelectrics and FEFETs
- Models for spin devices
- SPICE model for correlated materials and HyperFETs
- Models for PeFETs and TMD FETs



## Device-Circuit Co-design of Charge-Based Technologies

Future Ultra-Low Power Computing Platforms

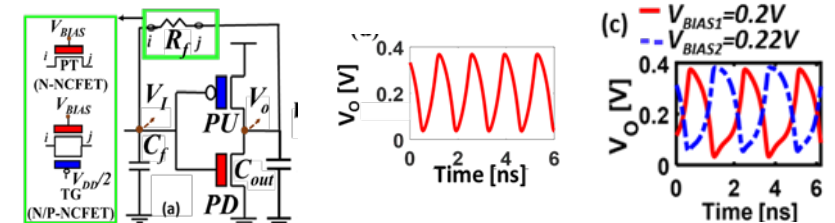
Modeling

Non-Boolean

Spin-based Memories and Logic

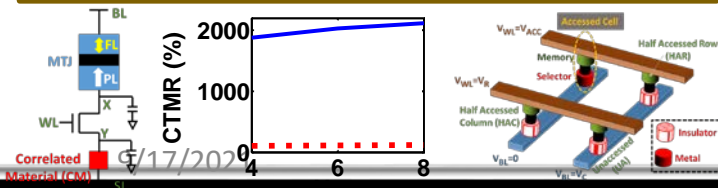
## Associative Computing

- FEFET based Coupled Oscillators
- Applications in pattern matching, graph coloring



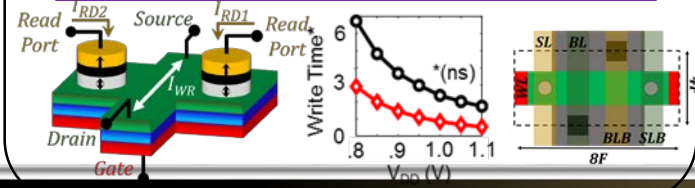
## Correlated Materials Enhanced Spintronics

- MRAMs
- Sense Amplifiers
- Cross-point Architectures



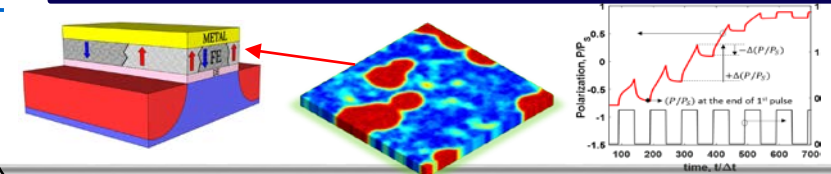
## TMD based Spintronics

- Valley coupled Spintronics using TMD
- Single-Ended/Differential Memories
- Non-volatile Flip-Flops



## Neuromorphic Computing

- FEFET based Bio-Plausible Neurons and Synapses
- New adaptive learning mechanisms enabled by FEFET based neuro-mimetic devices



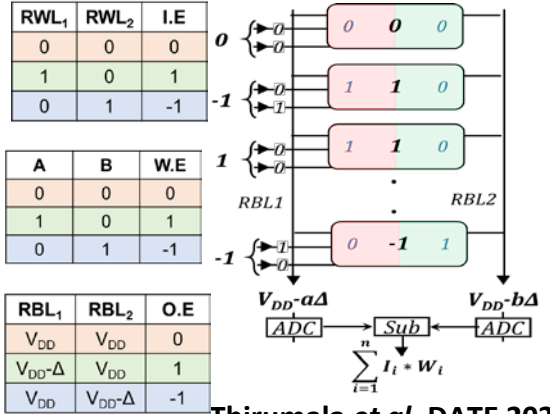
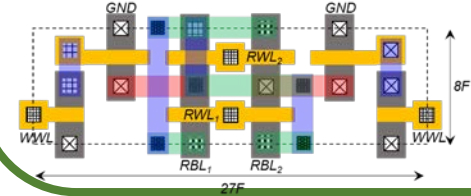
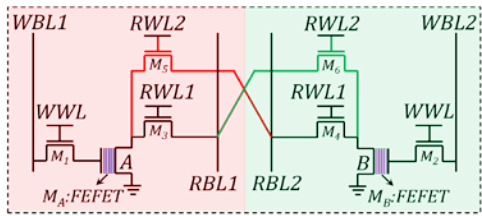
# FeFETs: Modeling and Device-Circuit Co-Design



Deep Neural Network Architectures (A. Raghunathan)

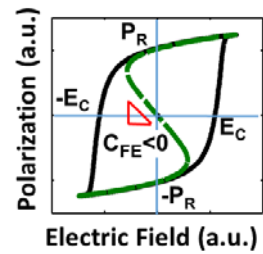
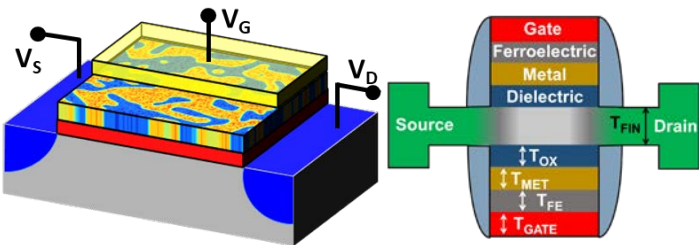
## Ultra-Low Precision Compute-Enabled Memories

Cross-coupled Cells for Signed Low Precision In-Memory Computation



Thirumala *et al*, DATE 2020  
Jain *et al*, TVLSI 2020

## Ferroelectric Transistors (FEFET) Design



## Phase Field Model based Simulation Framework

FEFET Variation Models

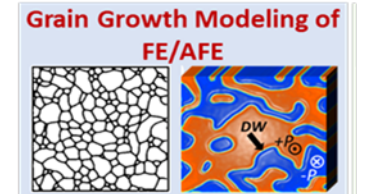
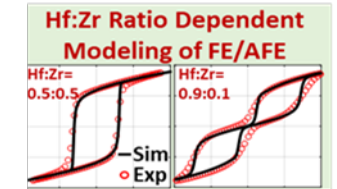
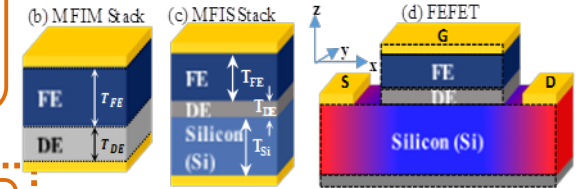
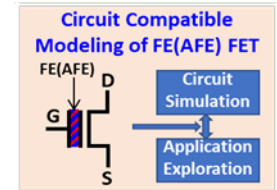
Circuit-Compatible Model

Landau Ginzburg Devonshire (LGD) Eq.

Poisson's Eq.

Charge/Current Eq.

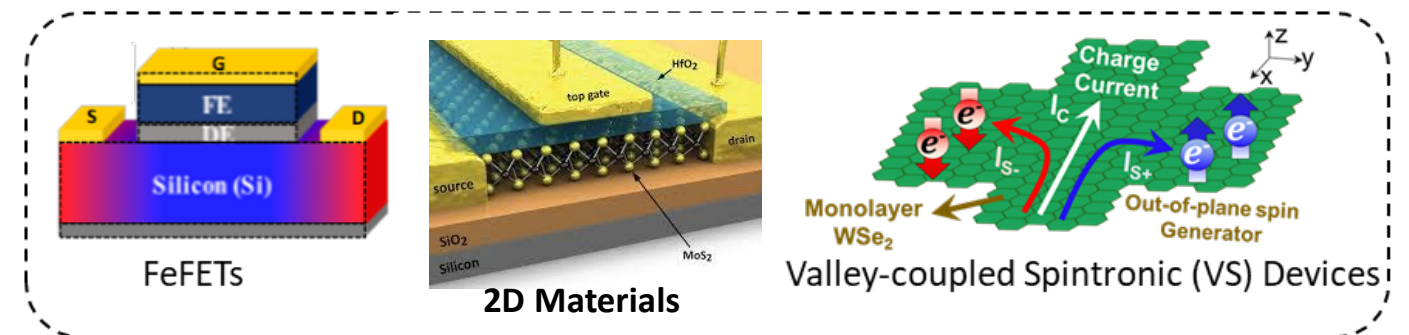
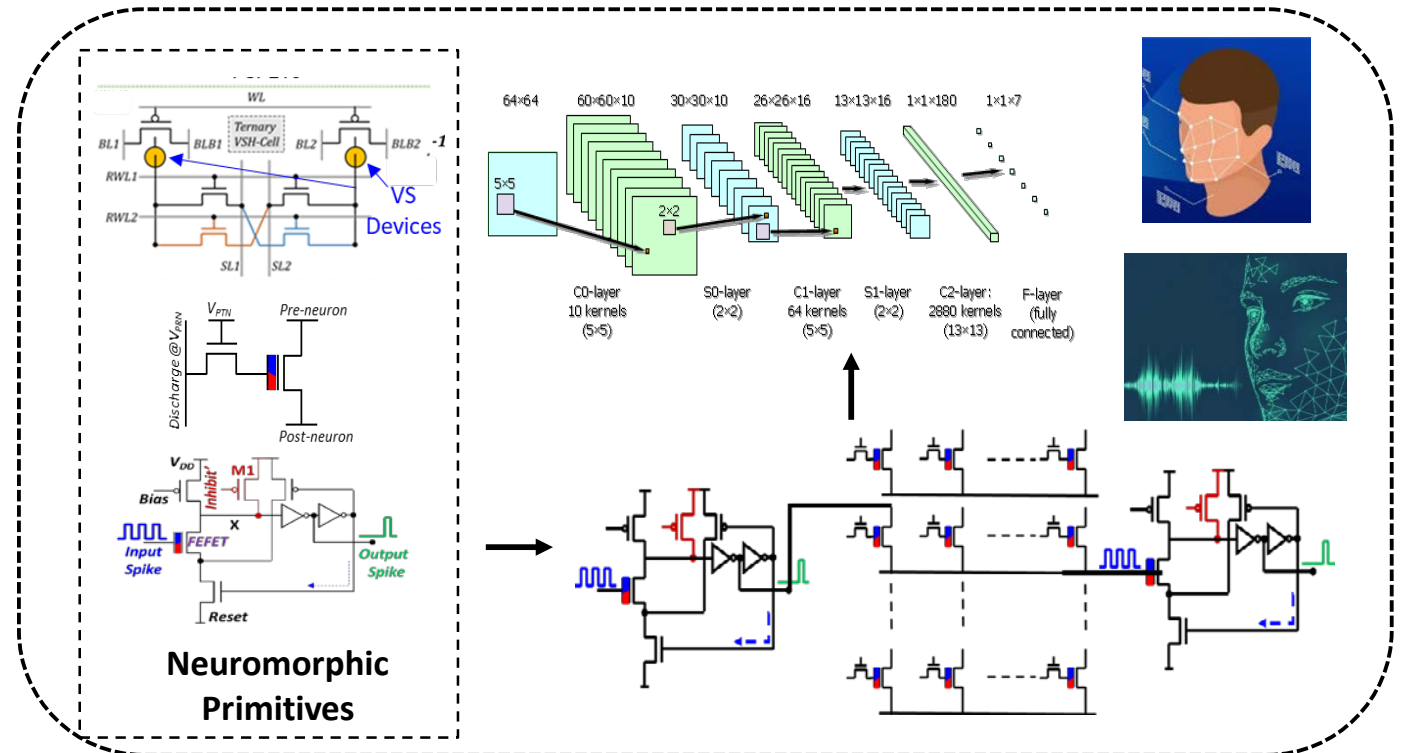
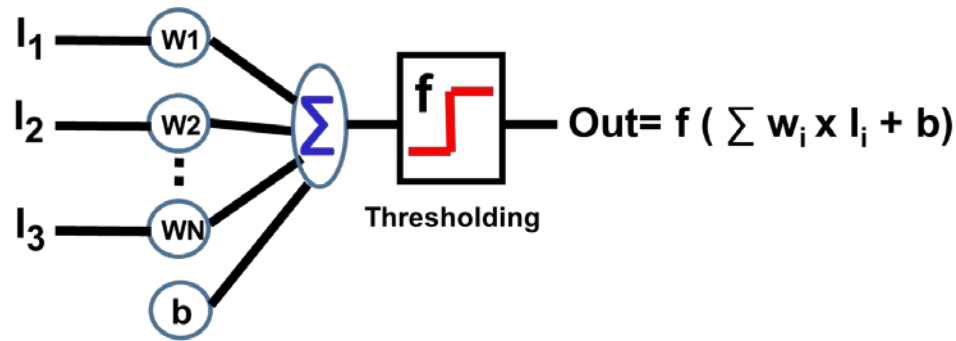
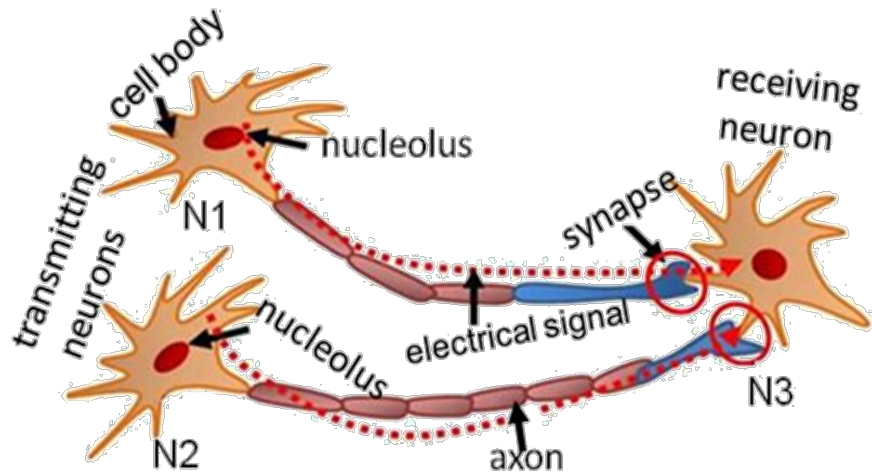
Saha *et al*, APL 2019  
Saha *et al*, Scientific Reports 2020  
Saha *et al*, IEDM 2020



Calibration with Experiments from collaborators (Ye, Datta)

# Future Research Directions

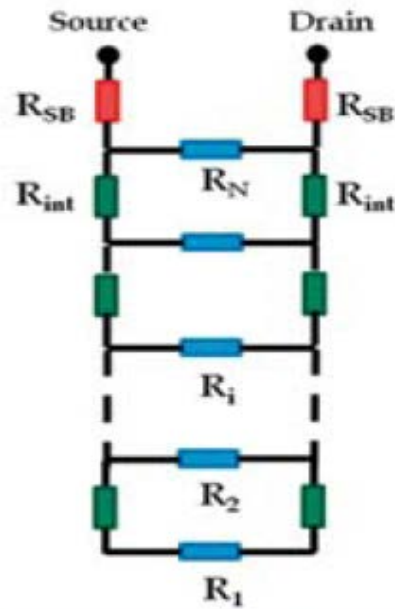
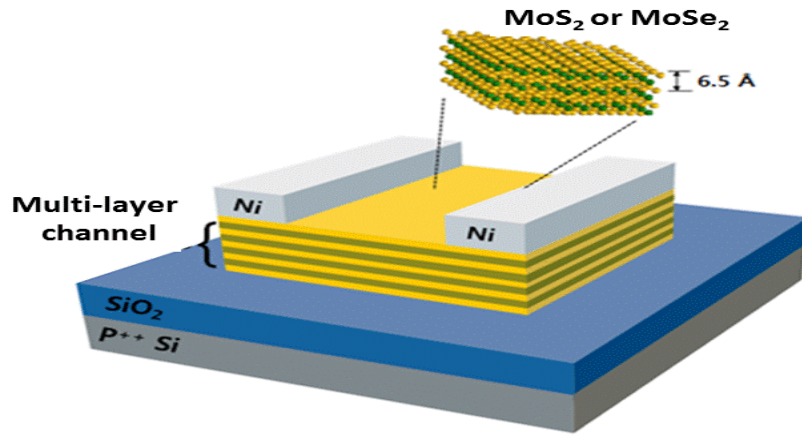
## Heterogenous Integration of Neuro-mimetic Technologies for Secure and Low Power Edge AI



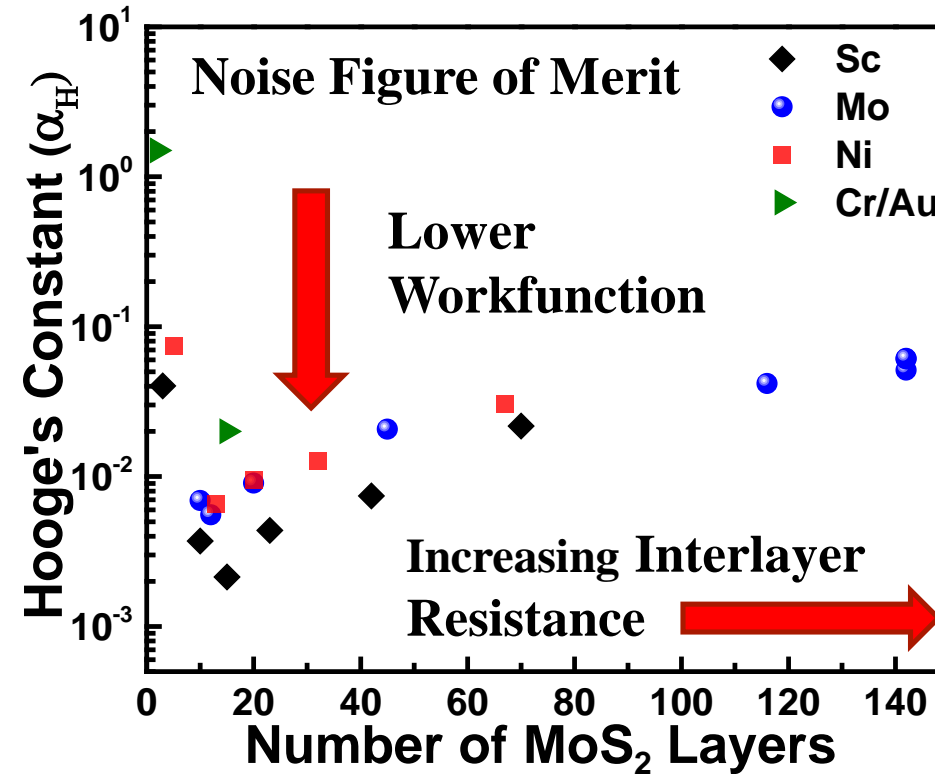
# Mobility and 1/f Noise in 1-D and 2D FETs



David Janes



Back Gate



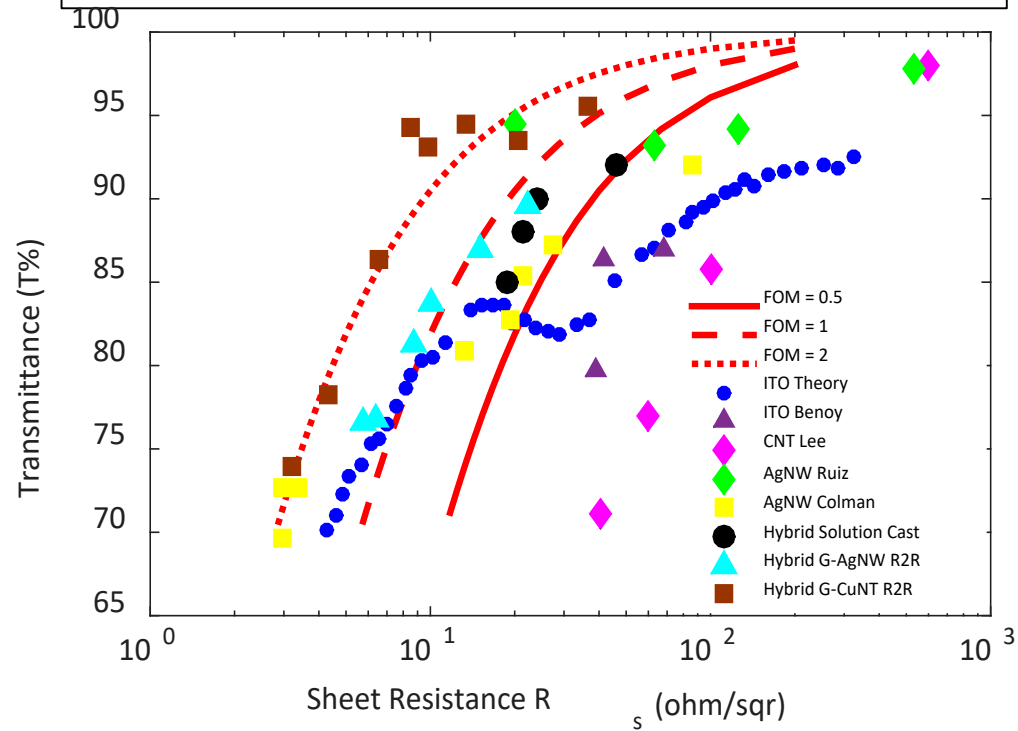
- Physically-based model of channel, interlayer resistance and contact (extending mobility approach of Appenzeller, et al)
- Understand optimal materials, channel thickness, contact

➤ Collaborators: S. Das, *Kansas State*, J. Appenzeller, *Purdue*, C. J. Delker, C. T. Harris, and B. Swartzentruber, *Sandia*

# Nanostructured Transparent Conductors and Templated Self-Assembly of Photonic Materials

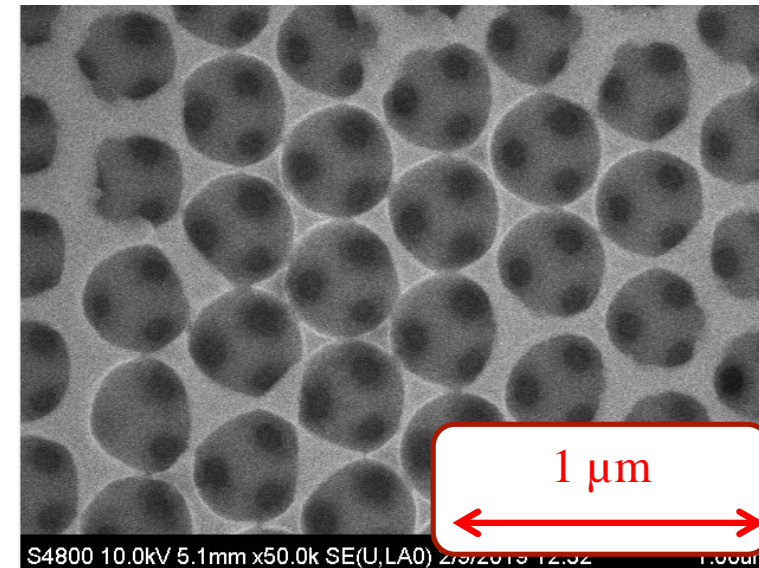
Transparent Conductors:

- 1D/2D Hybrids
- Low Resistance, High Transmittance



Nanostructured templates:

- Electrodeposition (metals, semicond.)
- Laser Annealing



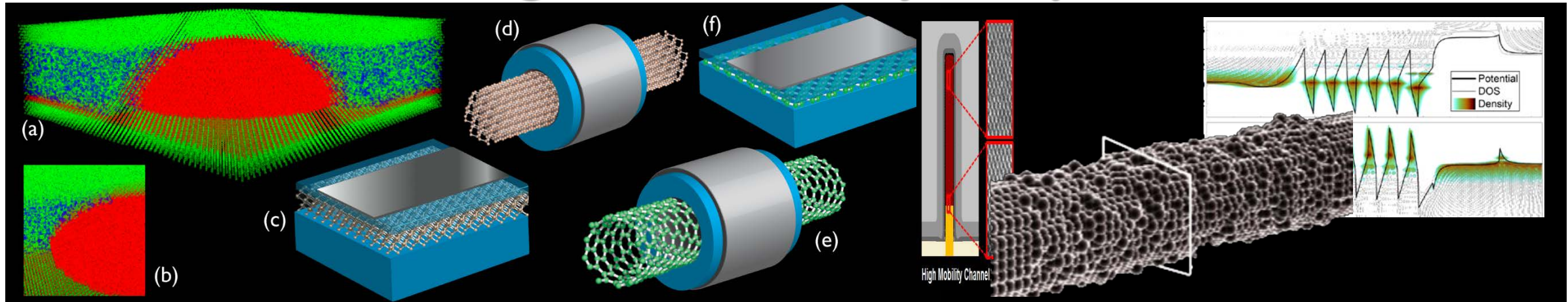
InSb Inverse Opal Structure

➤ Collaborators: M.A. Alam, A. Kildeshev, D. Warsinger, A. Marconnet, *Purdue*



# Nano Electronic Modeling – NEMO

## Multi-Scale Modeling Framework Beyond Specific Devices



### Available NEMO5 Capabilities:

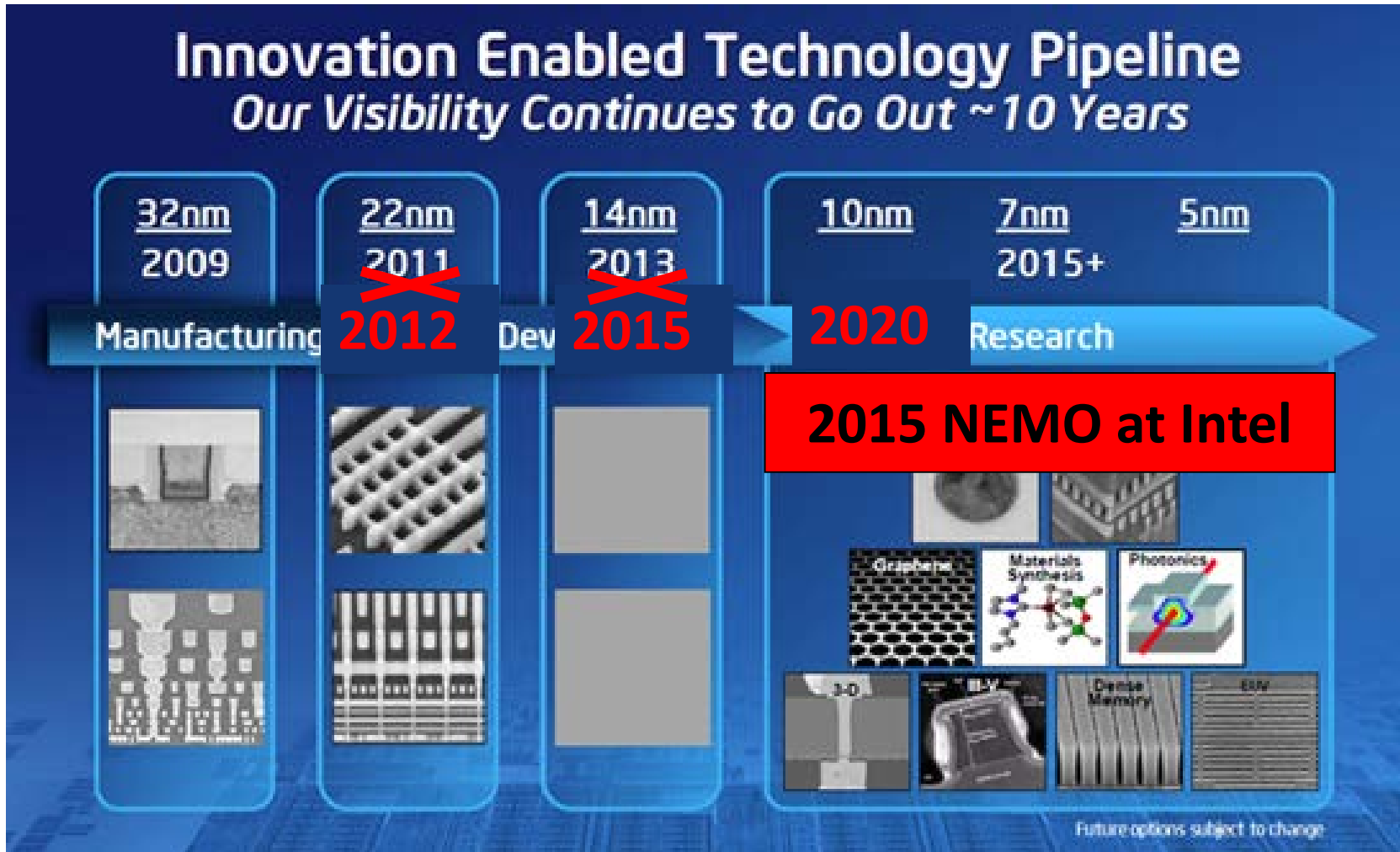
- 3D, 2D, 1D geometries -Atomic representation
- Realistically extended device sizes
- Nanowires, mosFET, tunnelFETs, quantum dots
- All semiconductors & metals: SiGe, III-V, 2D
- Roughness, impurities, alloys
- 50 Million atom structures
- Material science-MD structure input

### Quantitative agreement w /Experiments:

- nanowires, 2D materials, InGaAs FETs
- million-atom InGaAs/GaAs optical quantum dots
- Single atom transistor design of P in Si
- Ultra-scaled – 4 atom wide, 1 atom nanowires
- LEDs
- Bulk Phonon dispersions,
- Thermal transport at nm-scale

**A new and unique toolset that cannot (yet) be bought elsewhere**

# Moore's Law - 2009 Intel Road Map



nm Node	22	14	10	7	5
Node atoms	176	122	80	56	40
Electrons	160-190	64-80	30-38	18-23	11-15

- Intel Adoption of NEMO:
- 2009 initial engagement
  - 2012-2017 co-development
  - 2015 Intel buys a dedicated supercomputer to run NEMO
  - 2019 Intel announces NEMO integration at IEDM
  - 2015-2020 NEMO helps design 2 transistor generations
  - 2018 - SILVACO licenses NEMO first industrial customers

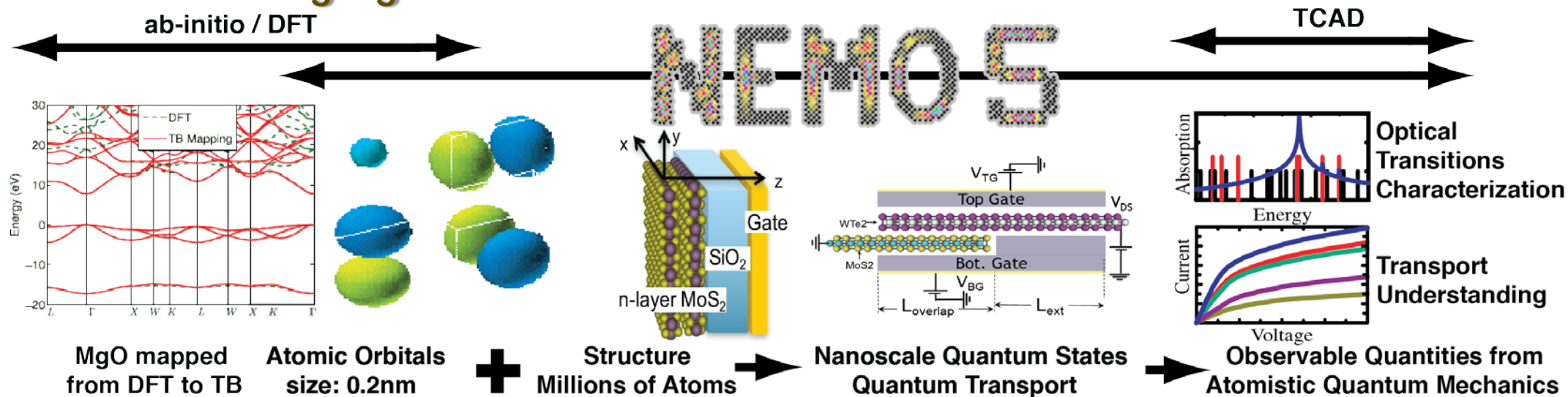
nature  
nanotechnology

## A single-atom transistor

Martin Fuechsle<sup>1</sup>, Jill A. Miwa<sup>1</sup>, Suddhasatta Mahapatra<sup>1</sup>,  
 Oliver Warschkow<sup>1</sup>, Lloyd C. L. Hollenberg<sup>3</sup>, Gerhard Klimek<sup>1</sup>

The ability to control matter at the atomic scale and build

# Bridging the Scales - From Ab-Initio to Realistic Devices



## Goal:

- Device performance with realistic extent, heterostructures, fields, etc. for many materials

## Problems:

- TCAD does not contain any real material physics
- Need ab-initio to explore new material properties
  - Ab-initio cannot model non-equilibrium.
  - Heterostructures are step functions!
  - Infinite waves needed to resolve a step!
- Need a local basis

## Atom Position Approach:

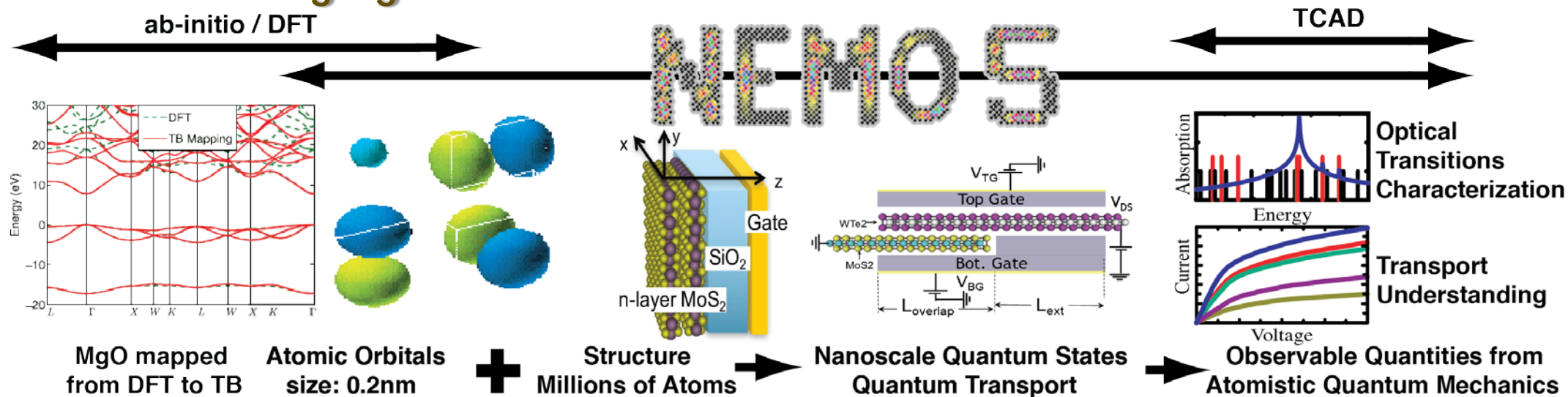
- Valence Force Fields
- Molecular Dynamics
- Ab-initio

## Electronic Structure Approach:

- Ab-initio - bulk or small ideal superlattices
- Map ab-initio to tight binding
  - Local atomic basis
  - Transferrable parameters



# Bridging the Scales - From Ab-Initio to Realistic Devices



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## Atom Position Approach:

- Valence Force Fields
- Molecular Dynamics
- Ab-initio

## Electronic Structure Approach:

- Ab-initio - bulk or small ideal superlattices

**New virtual tool for qualitative and quantitative exploration.**  
**Qualitatively like the introduction of physical MBE or ALD tools.**  
**A new and unique toolset that cannot (yet) be bought elsewhere.**

# nanoHUB in a nutshell: translating traditional research to **new paradigms** in publishing, computing, research, & education

What ?

- > 685 nano-Apps in the cloud
- > 6,511 lectures and tutorials
- > 170 courses => MOOC

Largest global nano-facility

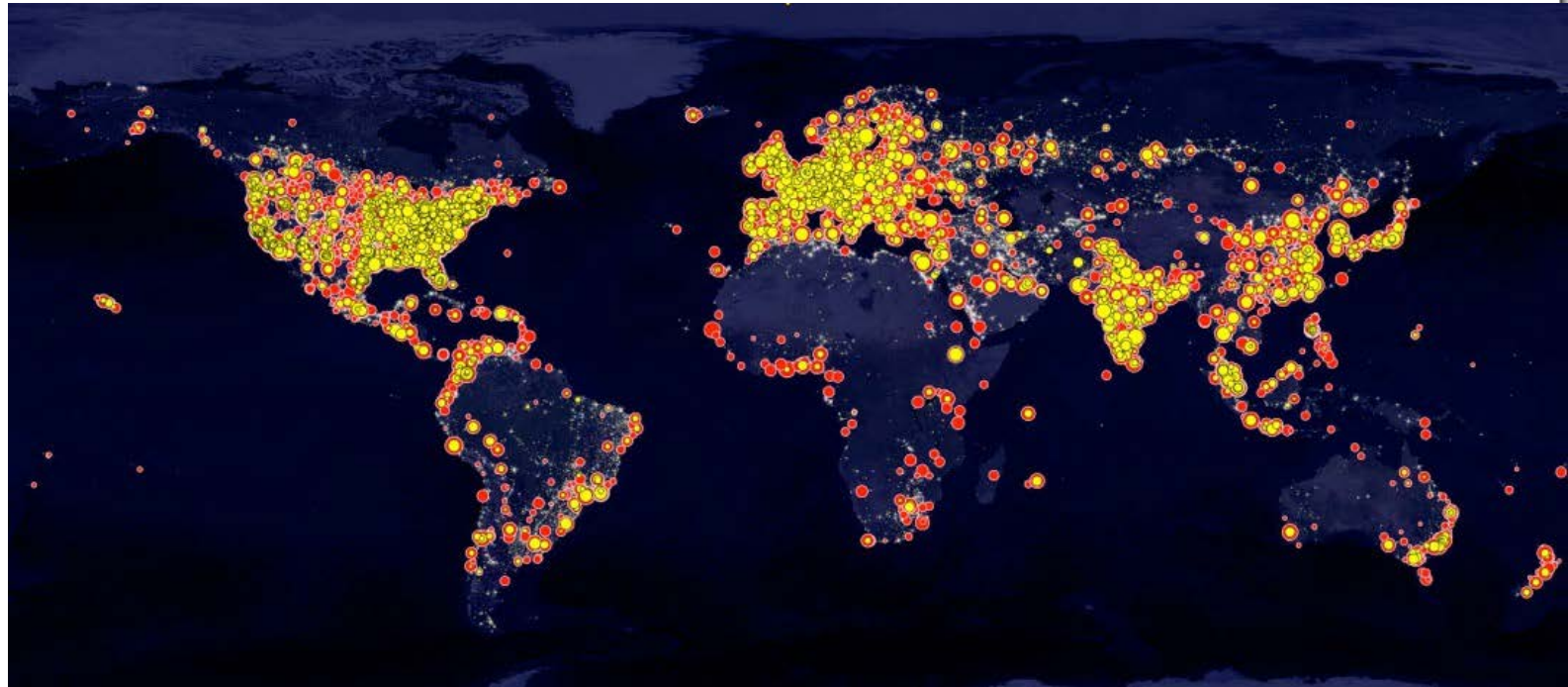
Cyberinfrastructure

24/7 operation with 99.4% uptime

Who?

- > 1.8 million users annually
- > 2,440 contributors
- 172 countries

- Faculty
- Students
- Industry practitioners



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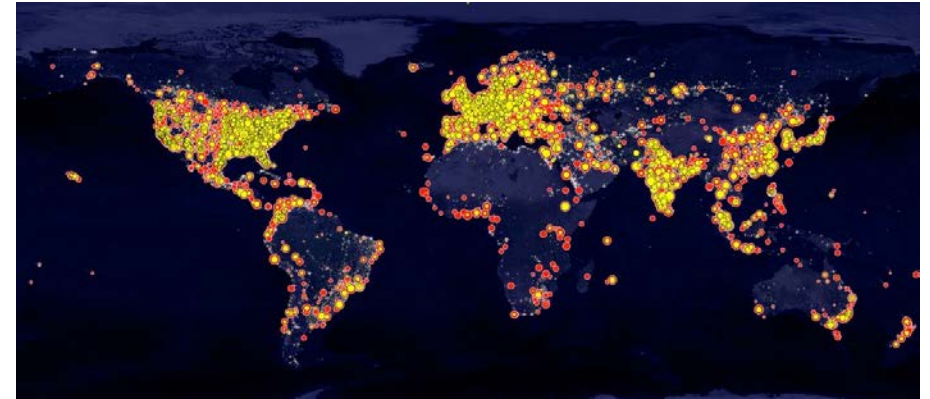
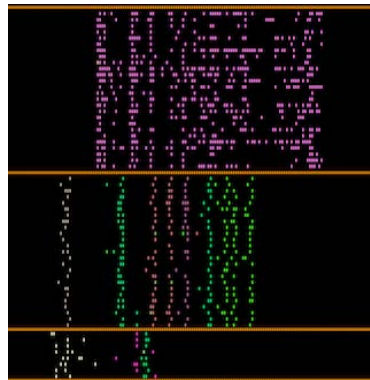
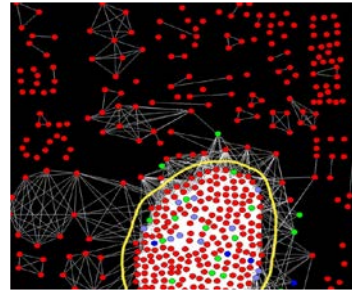
24/7 operation with 99.4% uptime

Who?

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- Students
- Industry practitioners

**Fundamental changes in approach or underlying assumptions**



Research Impact:

- nanoHUB tools now listed in

**WEB OF SCIENCE** **Google Scholar**

- > 2,507 papers cite nanoHUB
- > 54,300 secondary citations
- h-index of 105

Educational Impact

- >89,730 students use tools in classrooms, >3,840 classes, 185 institutions
- Rapid curriculum change <6 months adoption rate

Next up: Prof. XYZ

# HybridMEMS



Dana Weinstein

## Vision:

Develop MEMS RF devices, transducers, and sensors in low-barrier-to-entry technology platforms for adaptive wireless communication, timing, and IoT applications. |

## Focus:

- MEMS-IC resonators, oscillators, and filters in UHF through Ka band frequencies
- III-V programmable RF and mm-Wave components
- Lithium Niobate gain, switchable, tunable devices
- Recent: Phase change and phase transition MEMS
- Recent: Ultrasonic transducers for biomedical applications and IoT

everythingrf.com

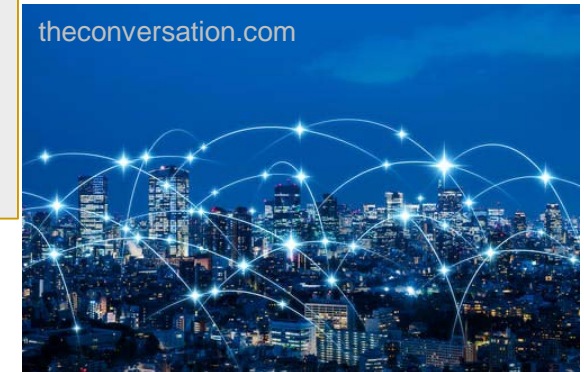


- Automotive applications, sensors
- 5G/6G communication
- mm-Wave imaging
- THz spectroscopy
- IoT / Smart infrastructure
- Neuromorphic computation
- Quantum computing above 4K



Qinteq

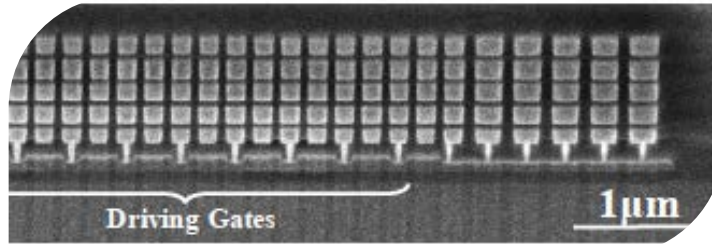
theconversation.com



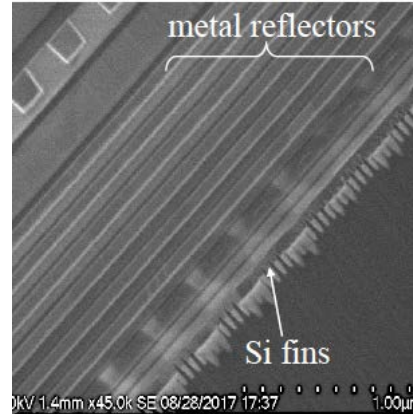
# HybridMEMS – Research Focus

## CMOS MEMS resonators and physical sensors

Seamless integration of electromechanical structures in standard CMOS technology. No post-processing or packaging required.



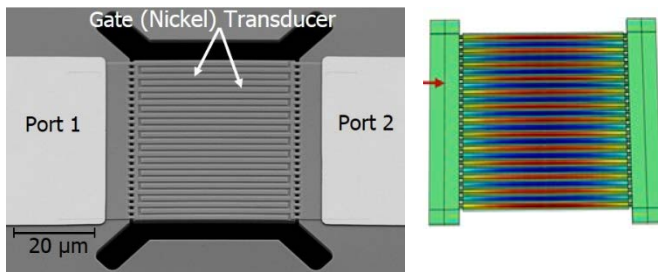
3 GHz SOI FET resonators  
Q>13000 (Global Foundries 32nm SOI)



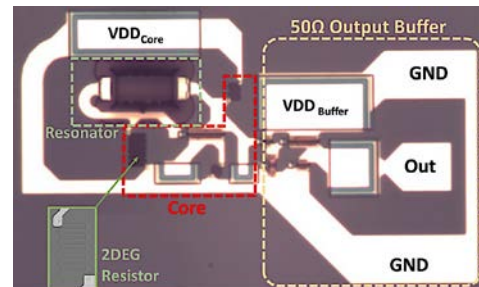
30+ GHz FinFET resonators  
Q>1000 (GF 14LPP)

## GaN MMIC-MEMS

GaN MEMS in monolithic microwave ICs (MMIC) leveraging HEMTs and 2D electron gas (2DEG) for high Q, high frequency RF components with programmable functionality



Lamb mode GaN resonators  
Q = 8327. f = 1.87 GHz

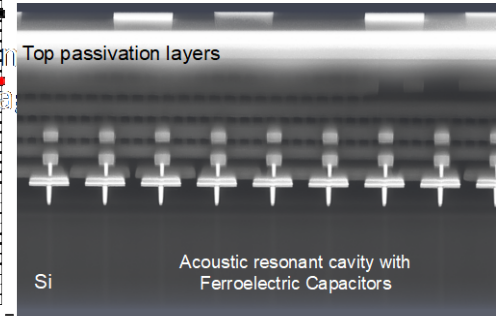
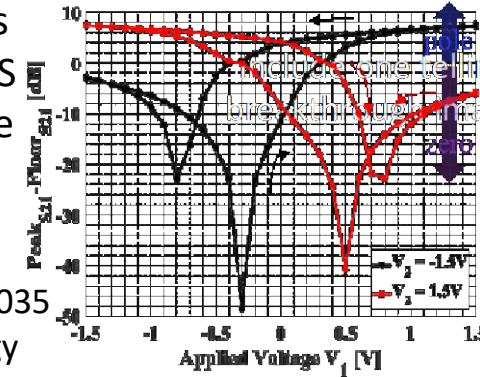


GaN MEMS oscillators and filters in MMIC technology

## Ferroelectric Transducers

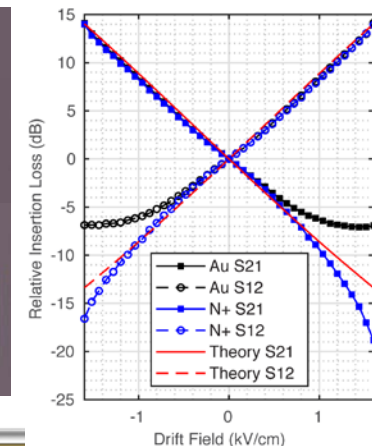
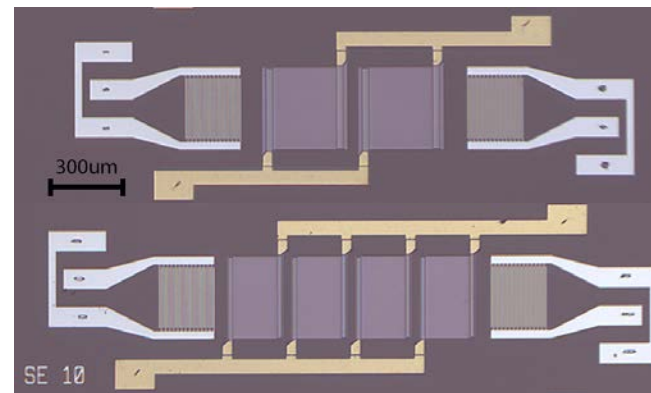
- Need for larger electromechanical coupling in CMOS-MEMS. Ferroelectrics are piezoelectric and can improve drive/sense efficiency by 100-1000x over capacitive transducers.
- Opportunities beyond CMOS for switchable 5G/6G filters

700 MHz resonators in TI E035 FeRAM technology



## Acoustoelectric

Non-reciprocal amplification of acoustic waves for applications in RF circulators, isolators, and correlators.



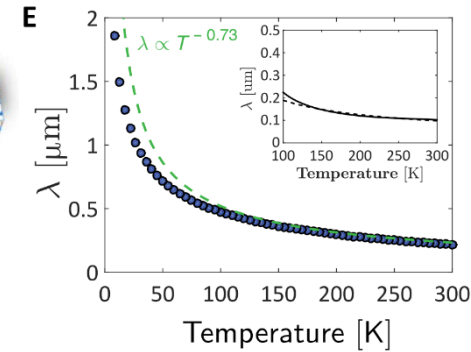
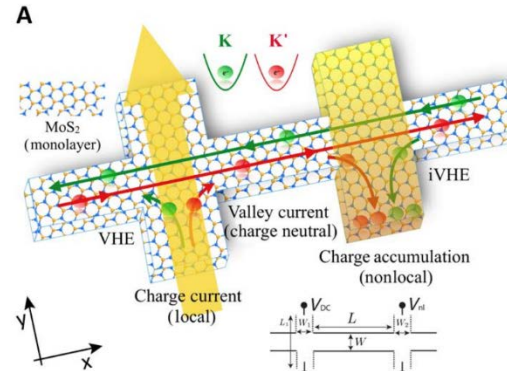
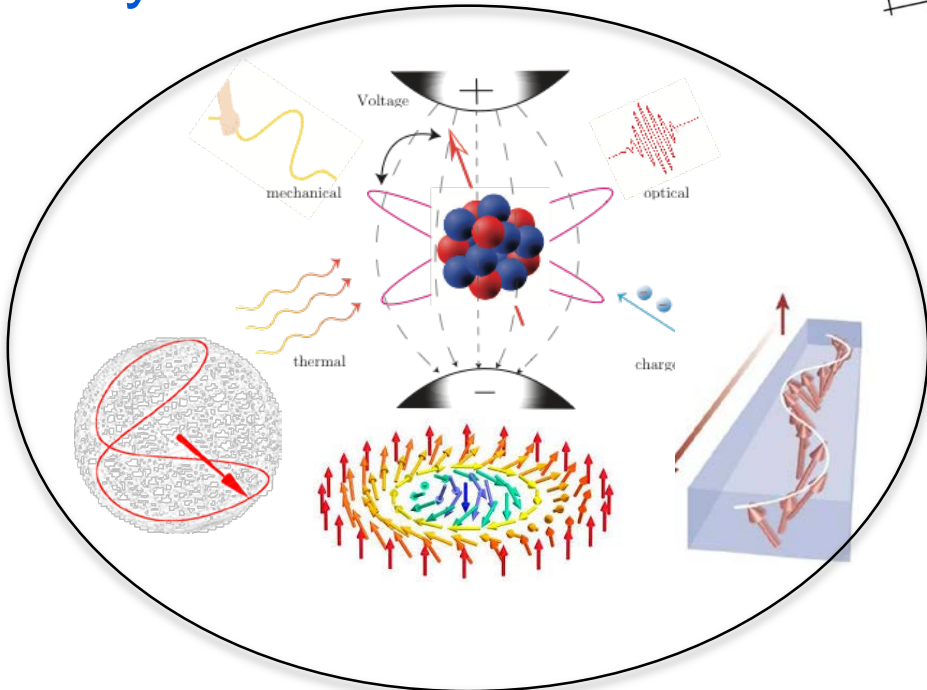
InGaAs/LN AE transmission lines with record-breaking terminal gain and non-reciprocity

# Novel Physics for Next-generation Microelectronics

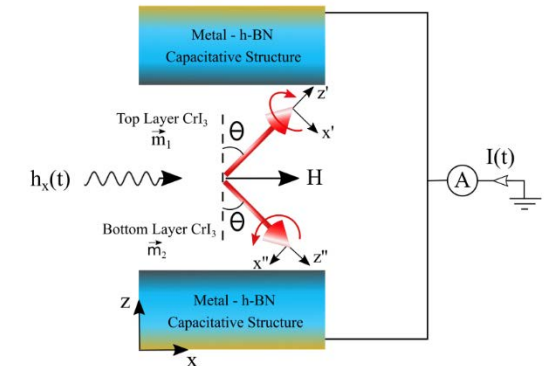


Pramey Upadhyaya

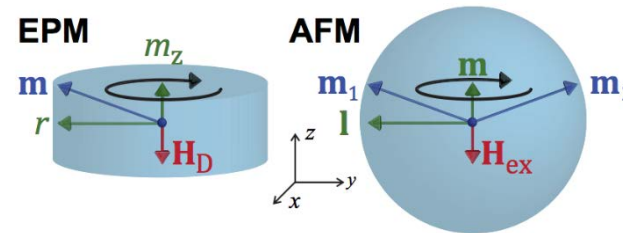
Memory, Computing & Sensing  
 Energy-efficient, compact, tunable dynamical systems



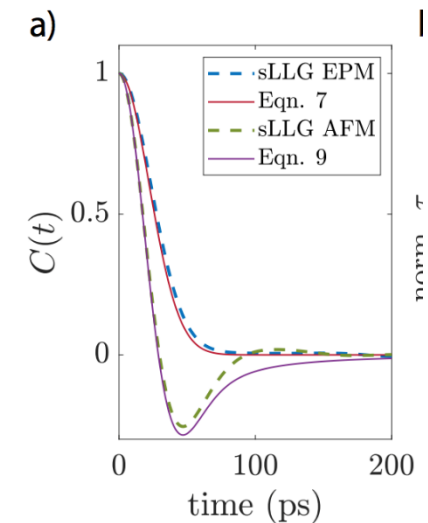
Chen/PU collab. **Sci. Adv.** (2019)



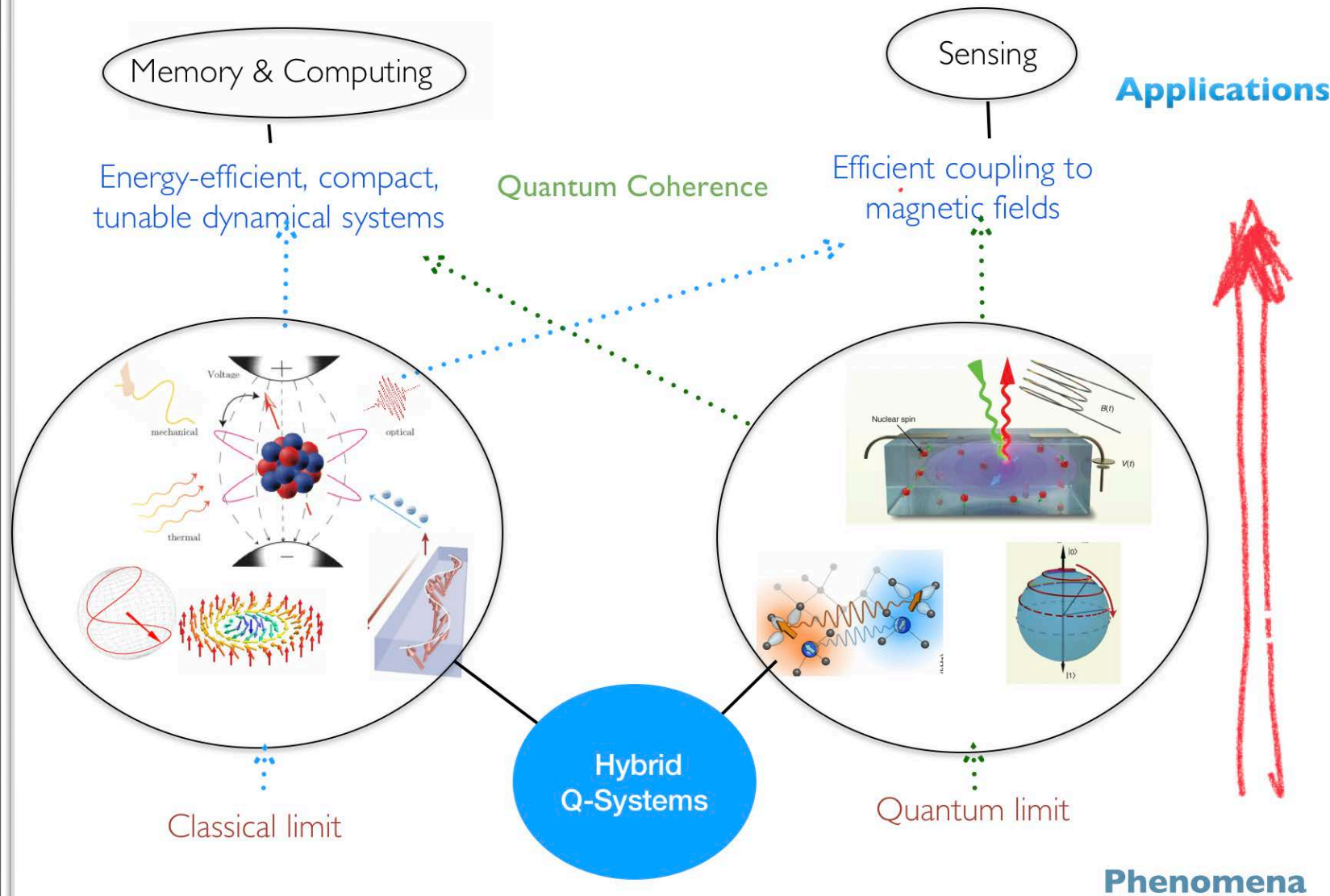
2d magnet, THz detector  
**PRB** (2019)



Sub ns P-bits  
 Datta/PU collab. **PR Applied** (2019)



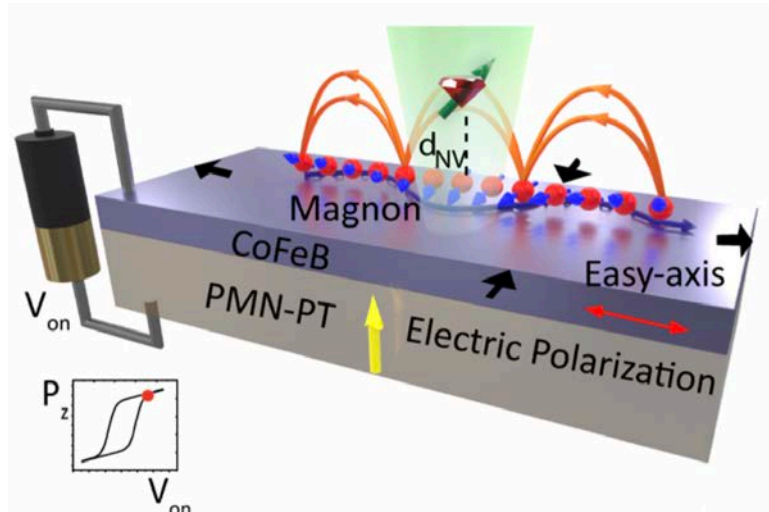
# Hybrid Quantum-Nano Systems for Microelectronics



Motivation:

1. *Quantum* for advancing next-generation *classical* microelectronic platforms
2. *Classical* for advancing next-generation *Quantum* platforms

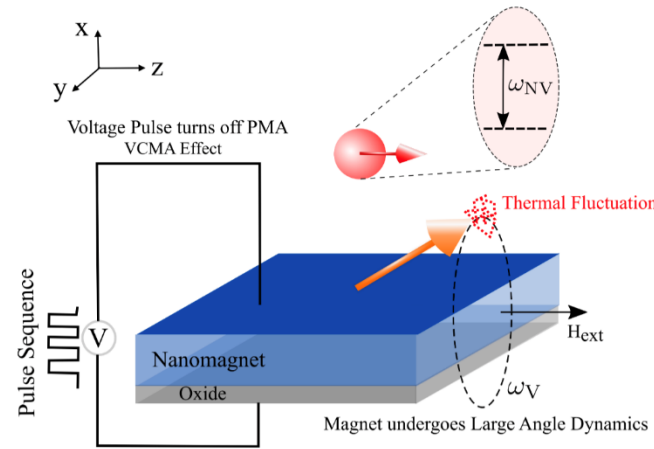
# Hybrid Quantum-Nano Systems for Microelectronics: Examples & Possibilities



E-field Q-sensors (with Appenzeller/Chen/Shalaev):  
arXiv:2012.01497 (2020)

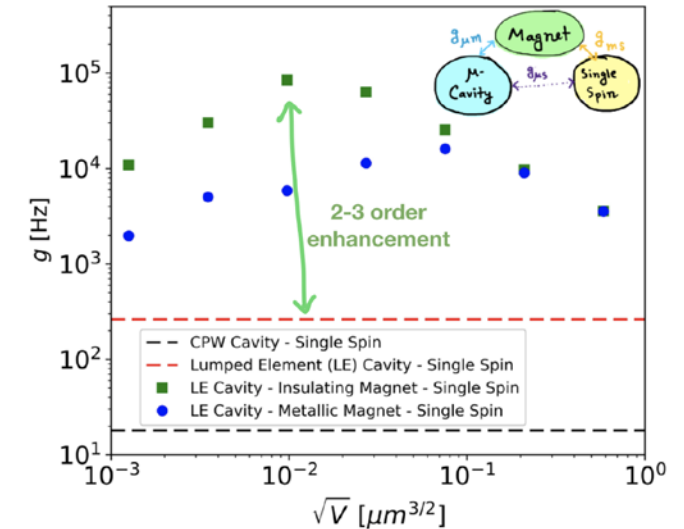
*Quantum for classical* microelectronics

Nanoscale, GHz-bandwidth, noninvasive,  
ambient Q-sensors for electromagnetic  
fields and materials



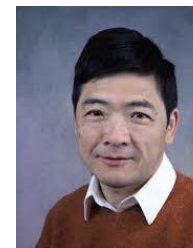
*Classical for quantum* platforms

Control fields and transducers for scalable  
Quantum systems

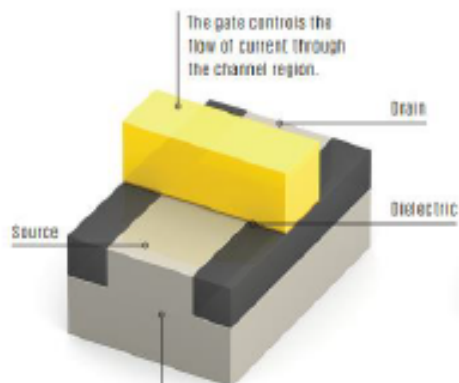




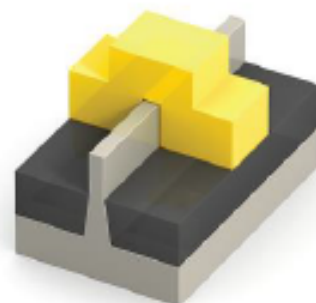
# Nanosheet devices could be the final evolutionary step for Moore's Law. (The Last Silicon Transistor, IEEE Spectrum 2019)



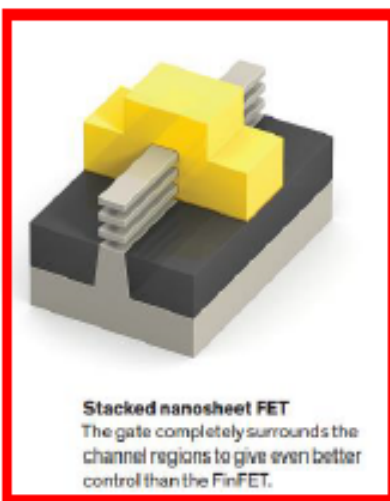
Peide Ye



**Planar FET**  
Up until about 2011, planar transistors were the best devices available.



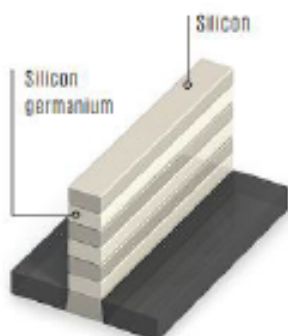
**FinFET**  
Surrounding the channel region on three sides with the gate gives better control and prevents current leakage.



**Stacked nanosheet FET**  
The gate completely surrounds the channel regions to give even better control than the FinFET.

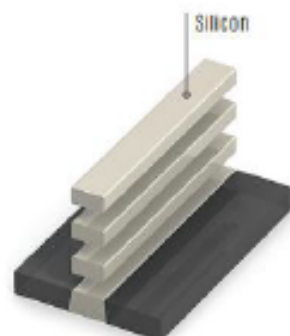
## 2D Opportunity?

- Junctionless FET
- No doping need?
- Accumulation-type

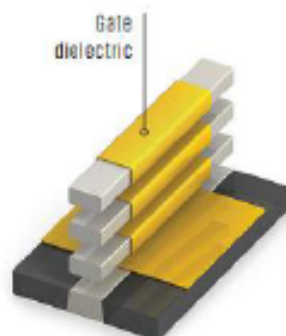


A superlattice of silicon and silicon germanium are grown atop the silicon substrate.

Si/Ge selective etching

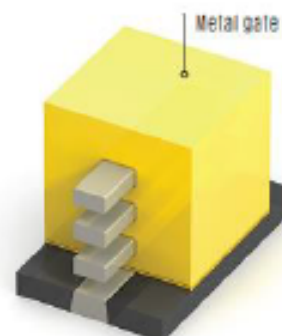


A chemical that etches away silicon germanium reveals the silicon channel regions.



Atomic layer deposition builds a thin layer of dielectric on the silicon channels, including on the underside.

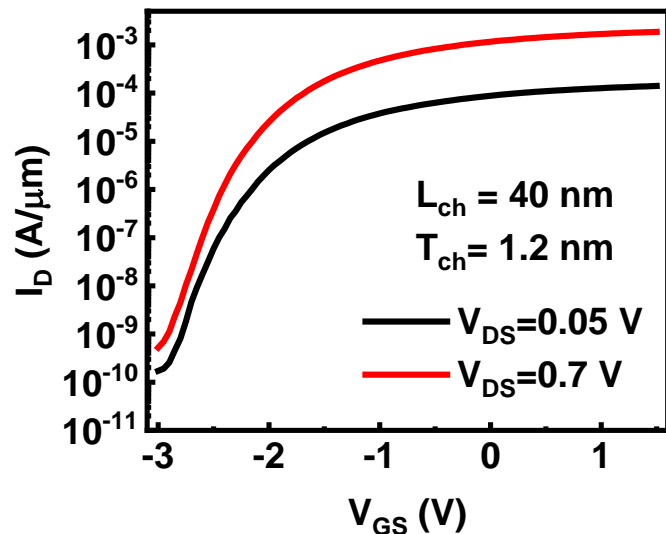
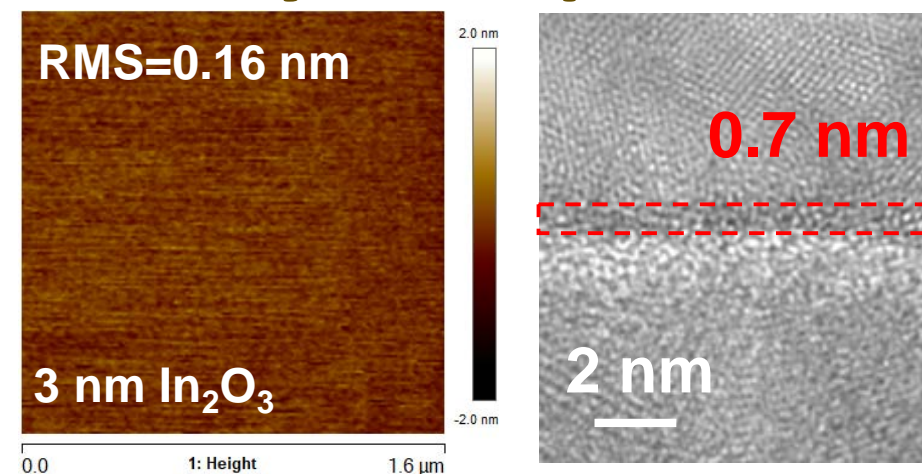
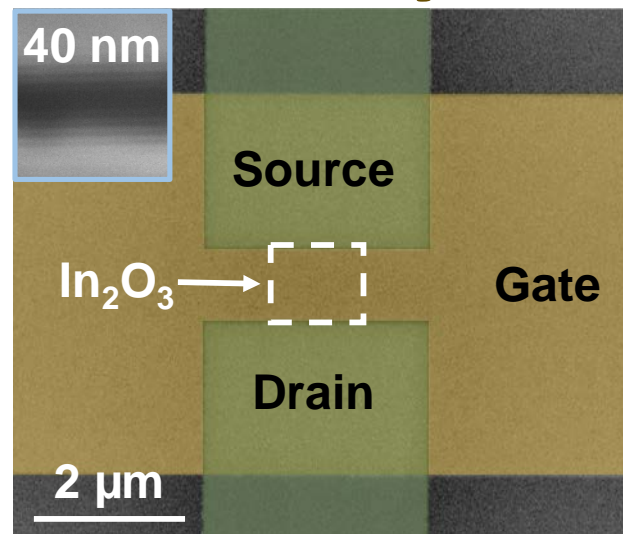
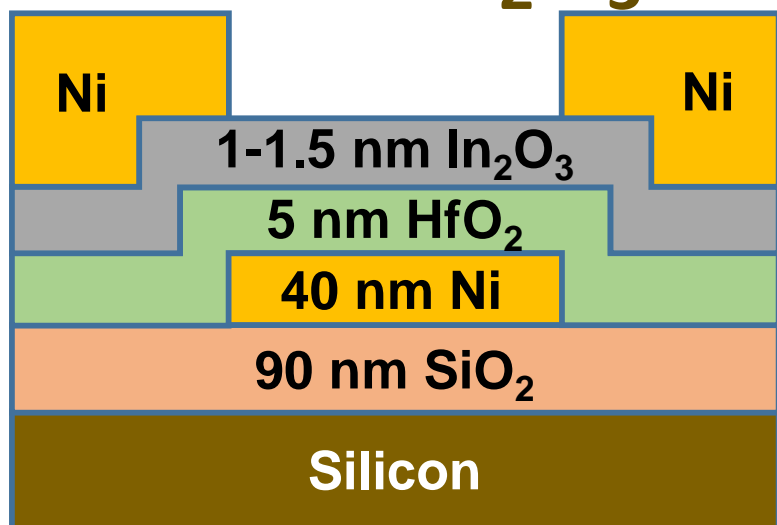
ALD high-K dielectric



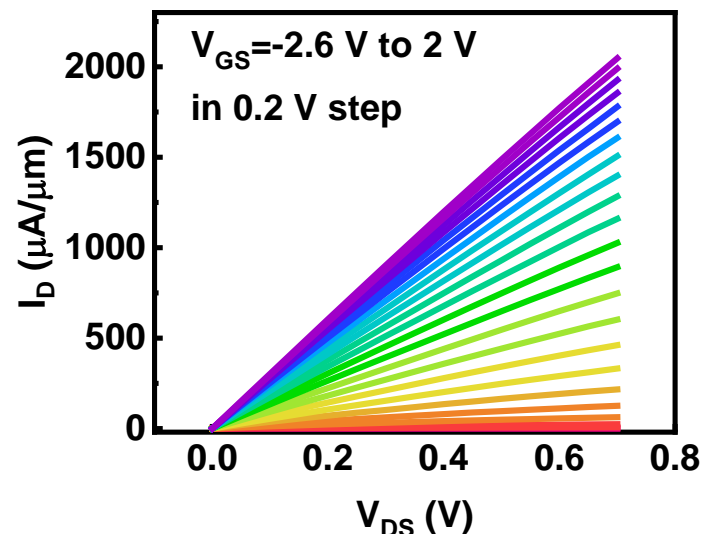
Atomic layer deposition builds the metal gate so that it completely surrounds the channel regions.

Atomic-Scale Ultra Precision Control for Future Ultra Efficient Microelectronics

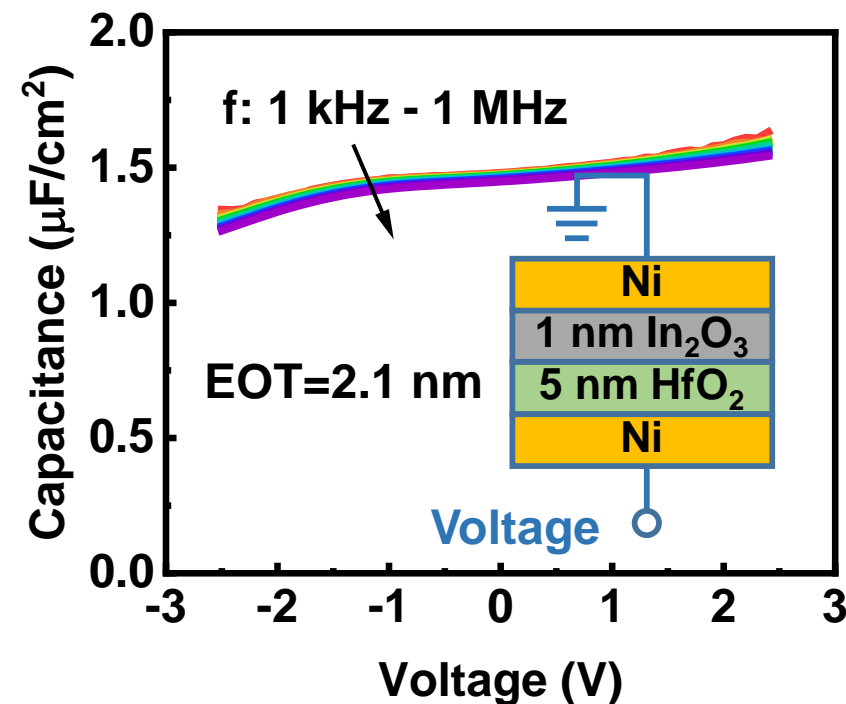
# Ultrathin $\text{In}_2\text{O}_3$ Transistors by Atomic Layer Deposition



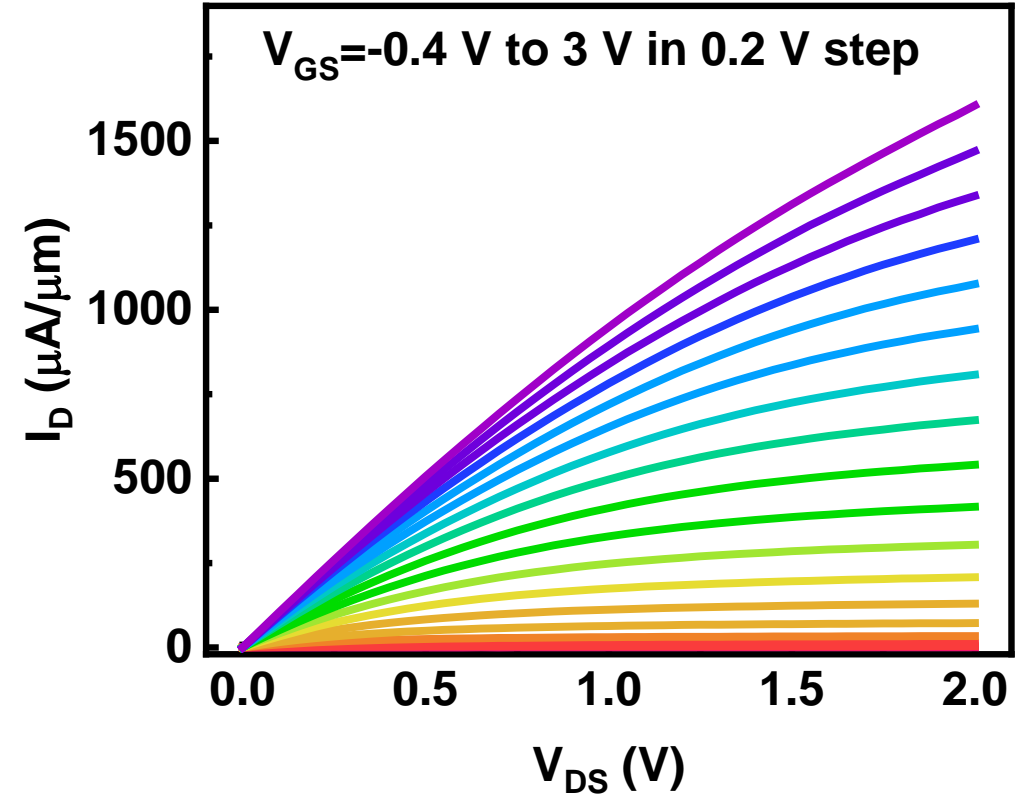
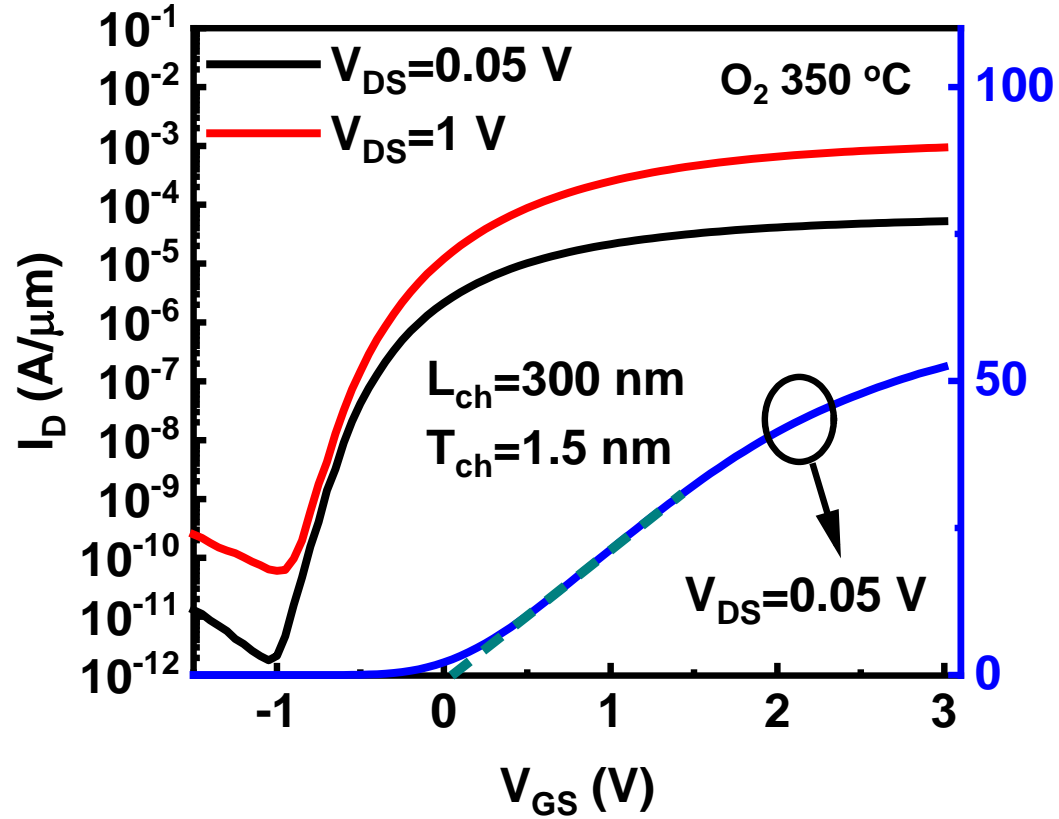
M. Si et al., IEEE EDL, 2020.  
M. Si et al., Nano Lett., 2020.



A. Charnas et al., APL, 2021.  
M. Si et al., IEEE TED, 2021.

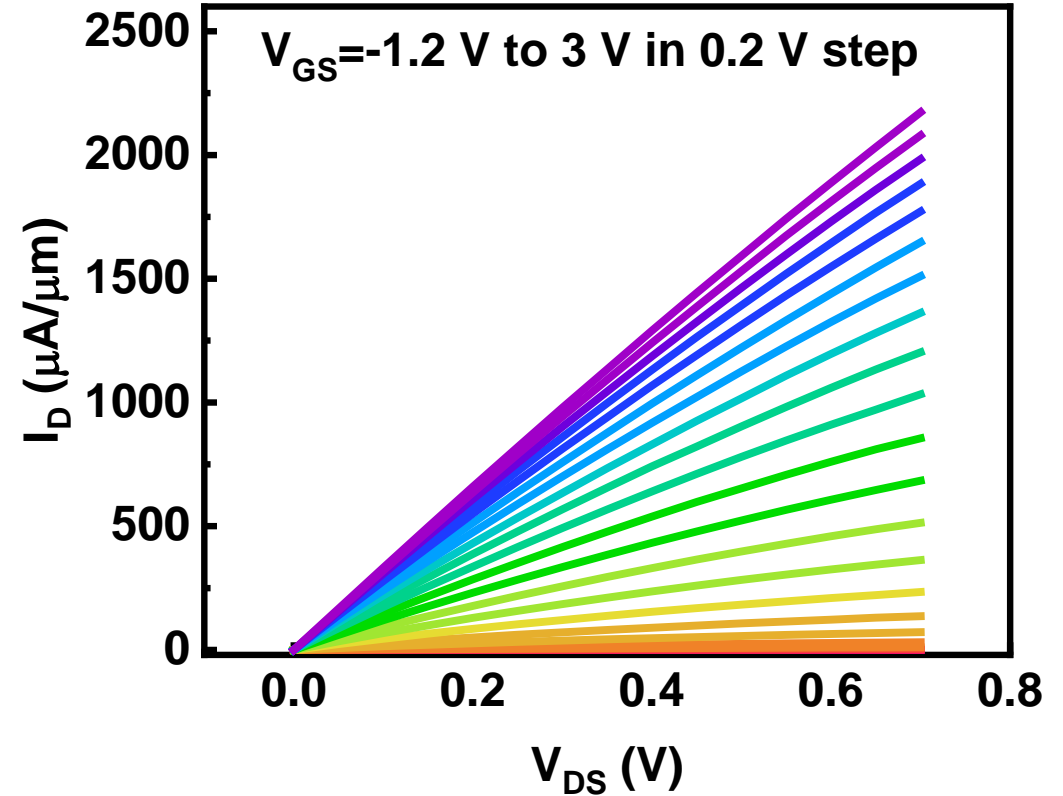
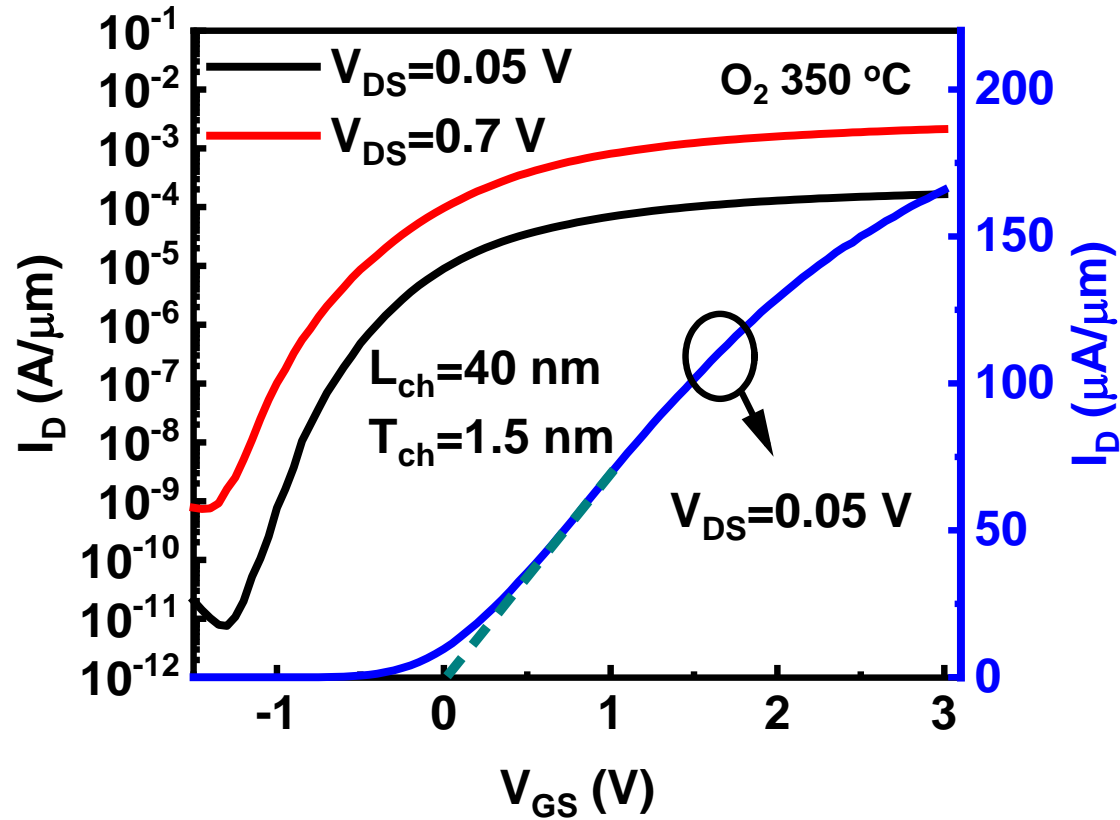


# High-Performance Device by O<sub>2</sub> Annealing



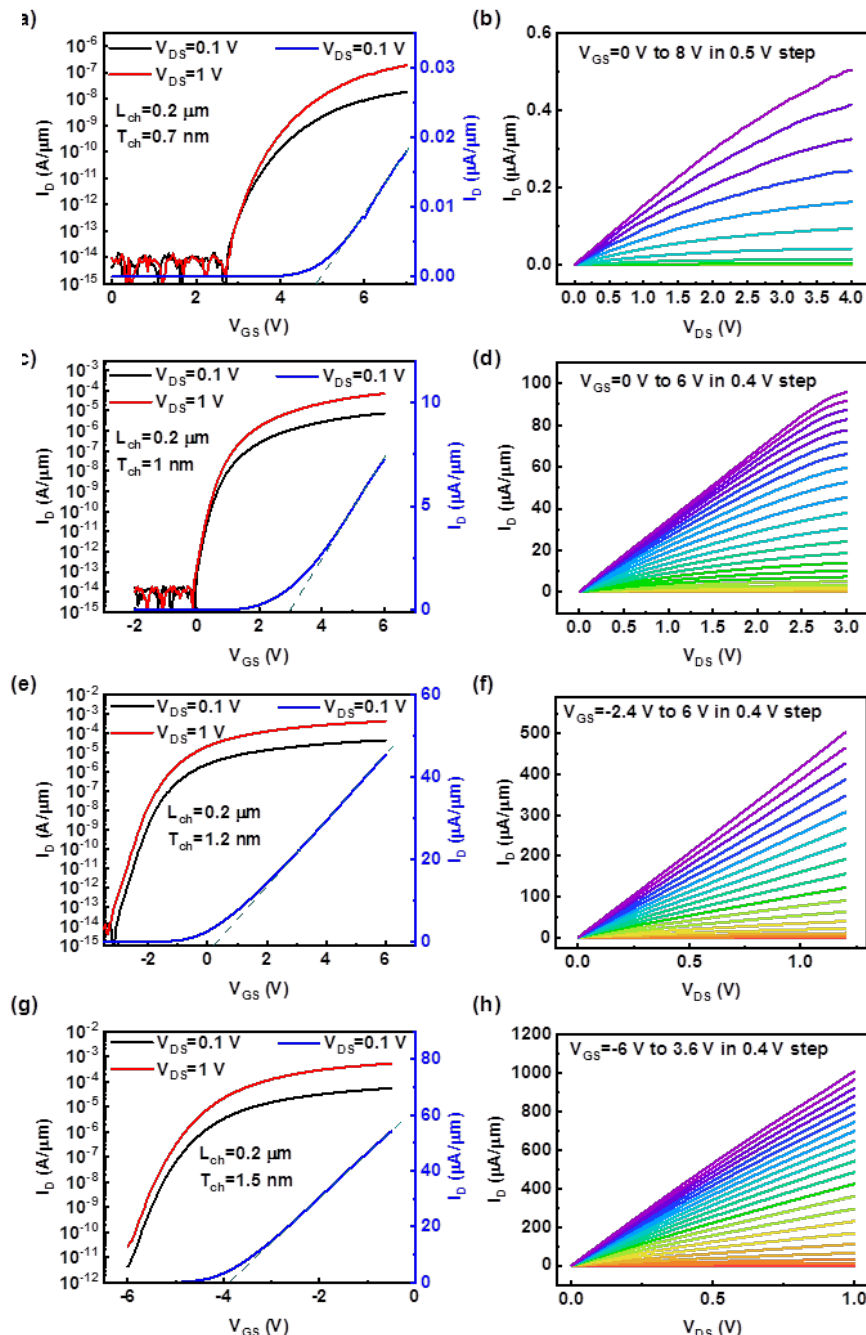
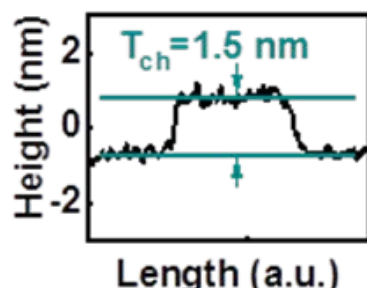
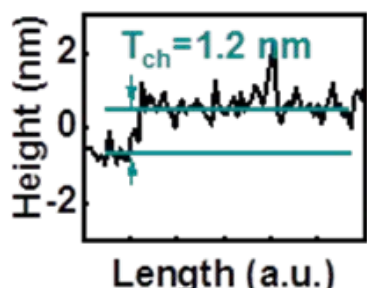
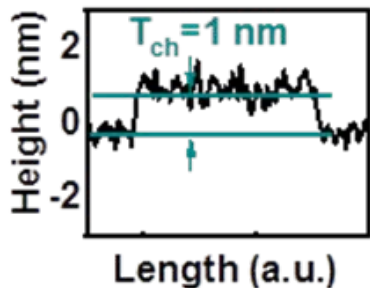
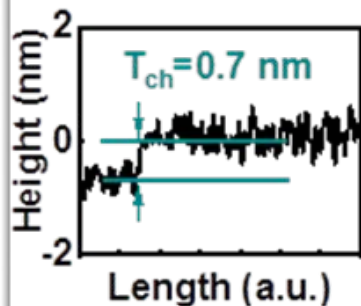
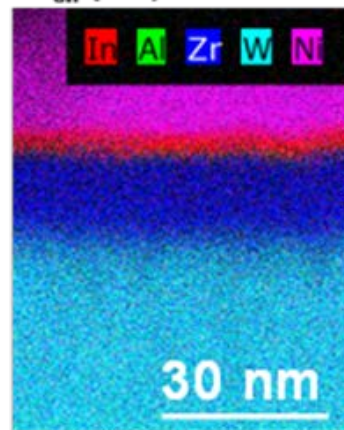
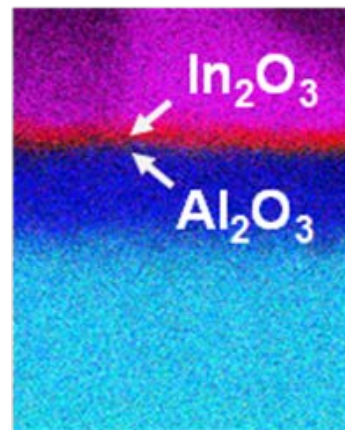
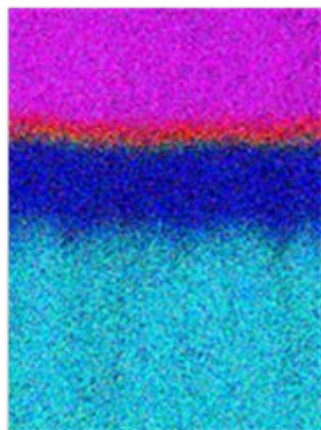
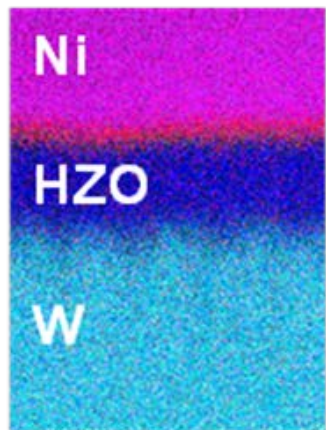
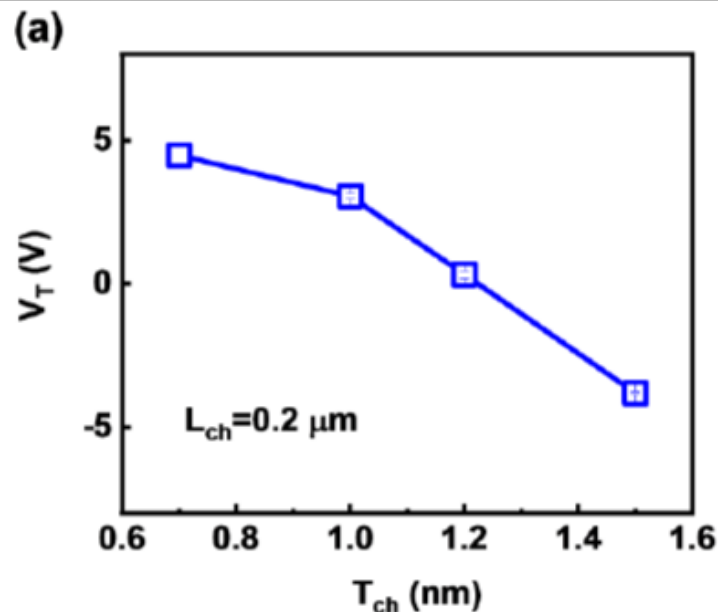
□ Long channel device showing drain saturation.

# High-Performance Device by O<sub>2</sub> Annealing



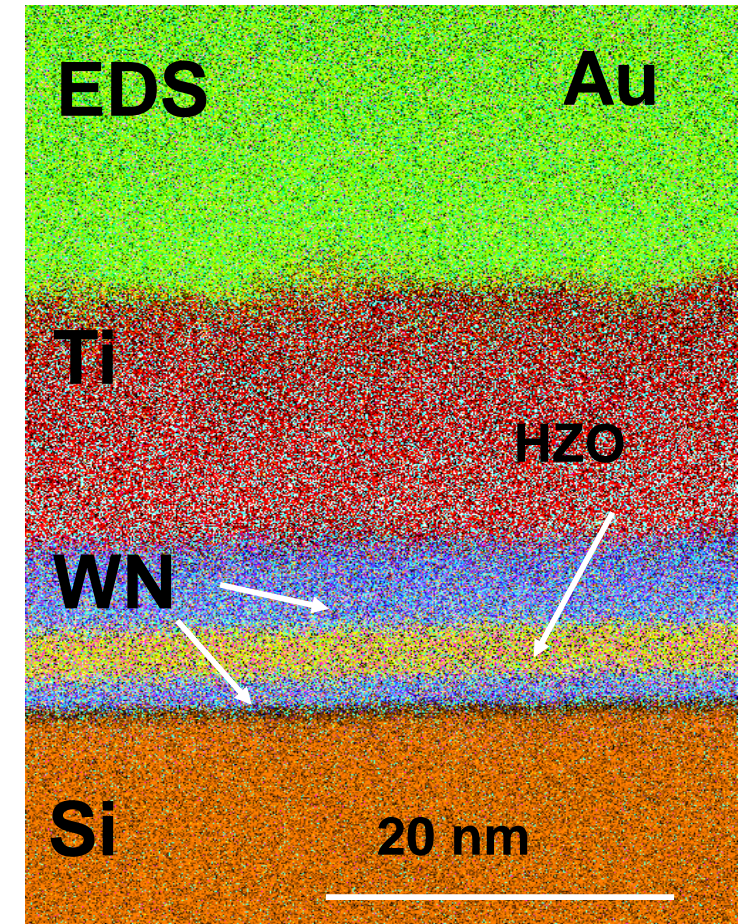
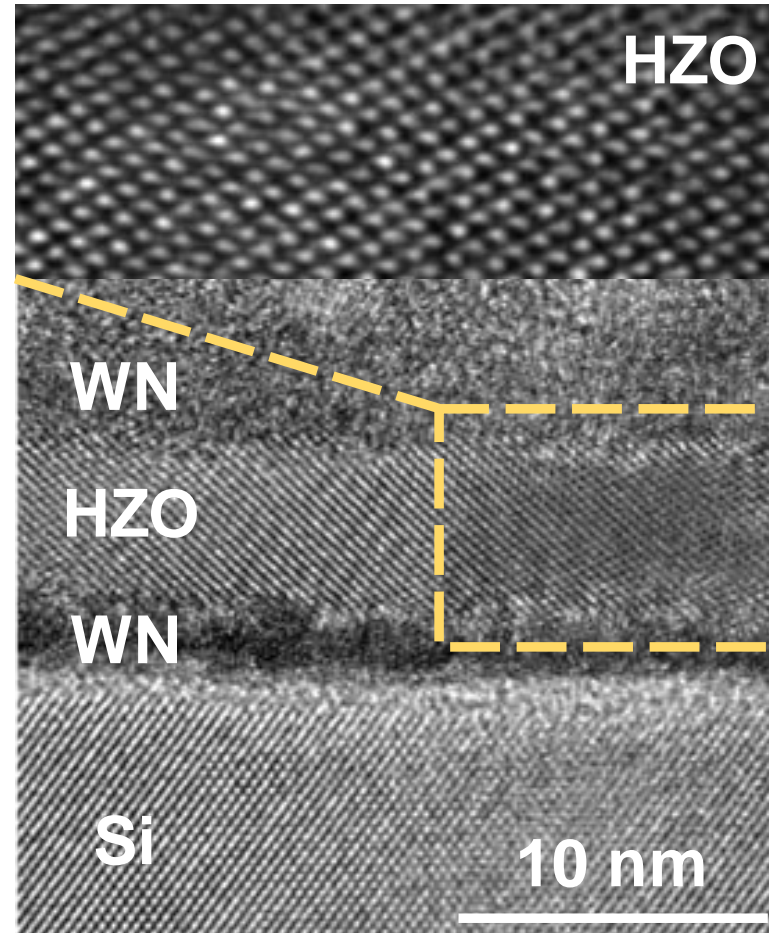
□ On-current  $> 2$  A/mm with enhancement-mode operation.

Threshold voltage ( $V_T$ ) is controlled by the channel thickness at 0.1nm level (1 ALD cycle)



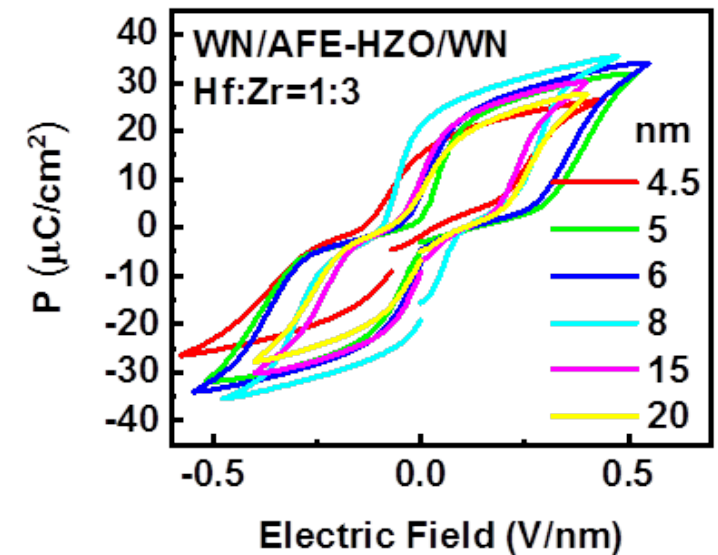
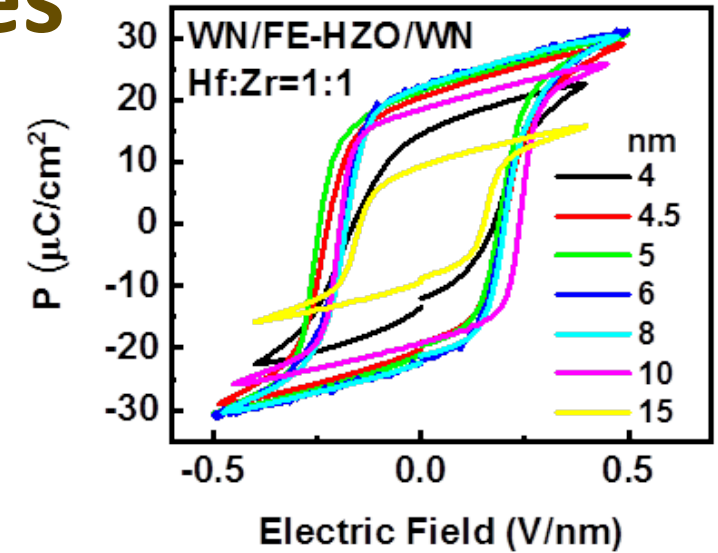
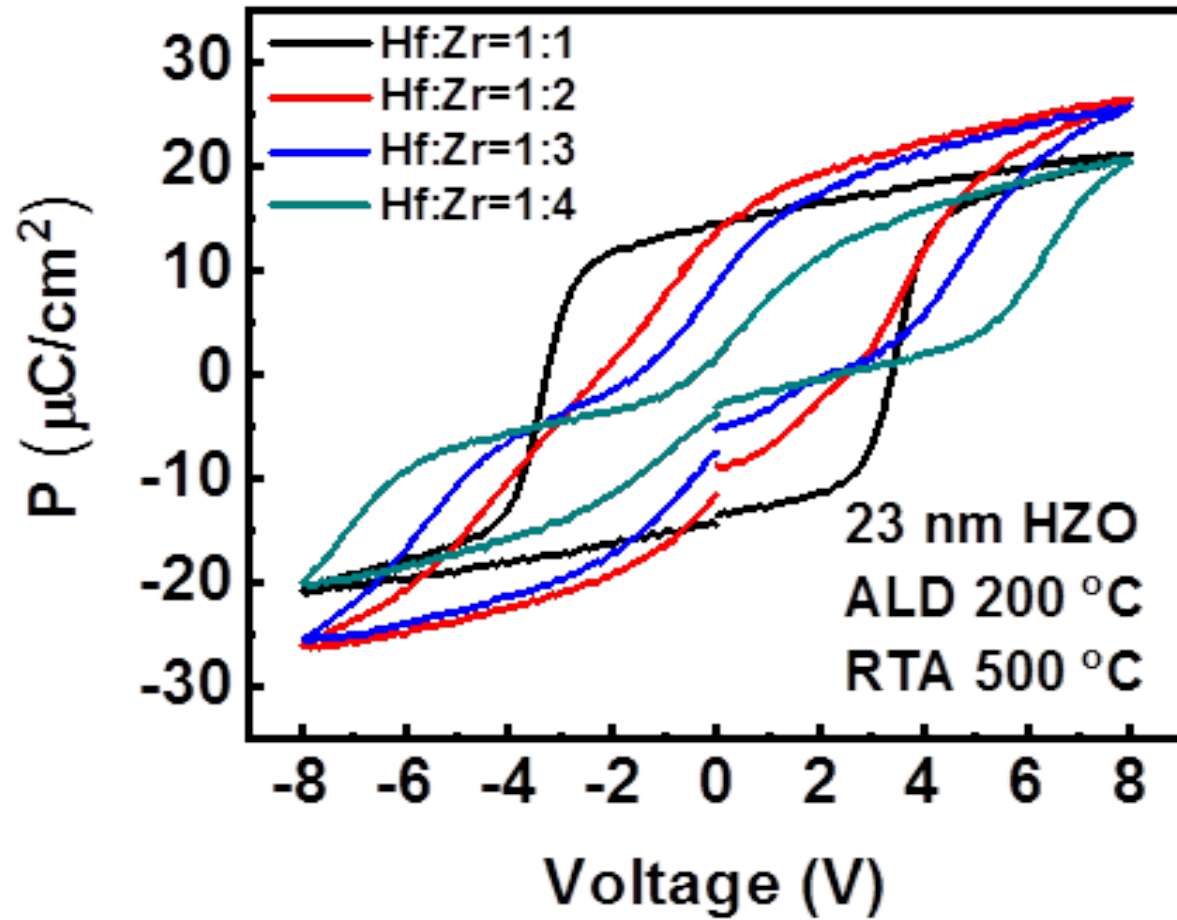
# Atomic Layer Deposition of Ferroelectric and Anti-ferroelectric HfZrO<sub>2</sub>

- Solvent Cleaning
- ALD WN
  - BTBMW, NH<sub>3</sub>
  - 400 °C
- ALD HZO
  - TDMAHf, TDMAZr, H<sub>2</sub>O
  - 200 °C
  - Hf:Zr=1:1 (FE)
  - Hf:Zr=1:3 (AFE)
- ALD WN
- RTA 500 °C in N<sub>2</sub> for 1 min
- Ti/Au Evaporation
- CF<sub>4</sub>/Ar Dry Etching

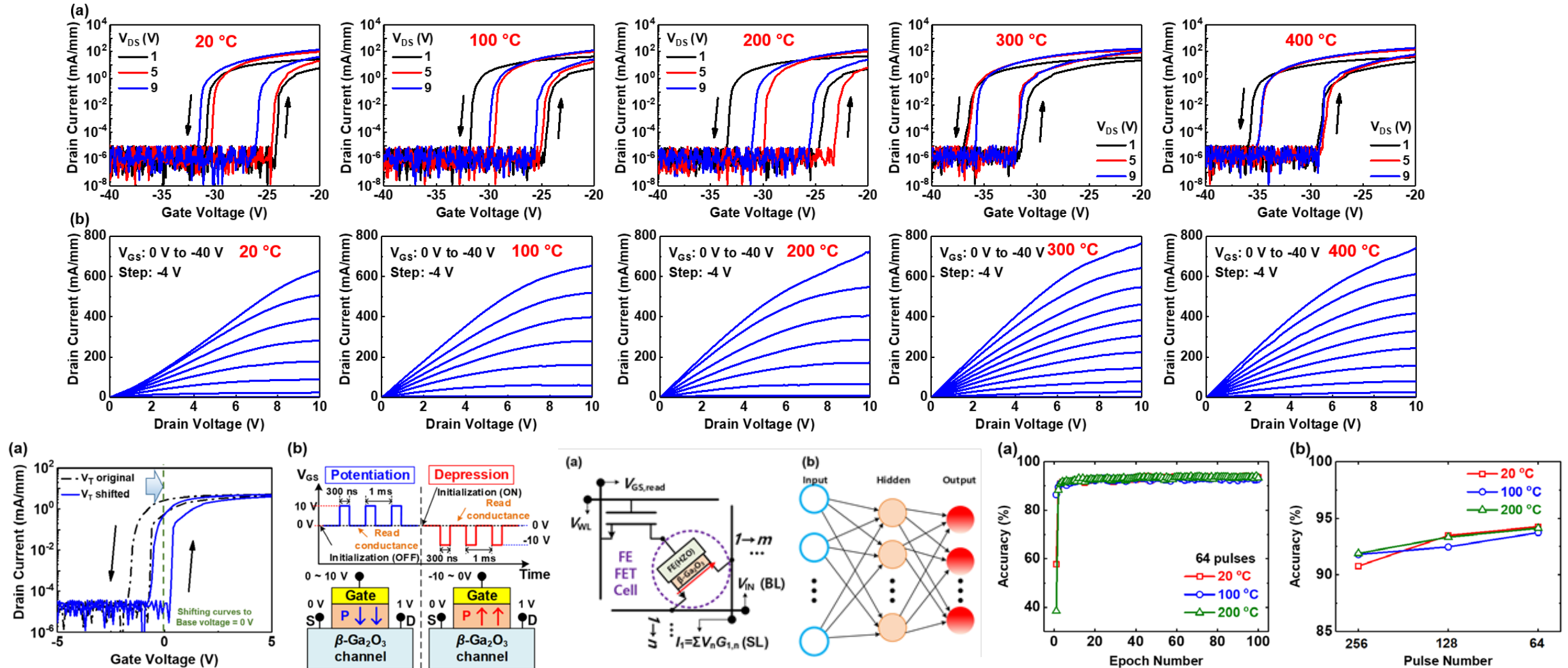


X. Lyu et al., VLSI, 2019

# Ferroelectric vs. Anti-ferroelectric Controlled by Atomic Layer Cycles



# First Experimental Demonstration of Robust HZO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Ferroelectric Field-Effect Transistors as **Synaptic Devices** for Artificial Intelligence Applications in a **High Temperature Environment**



J. Noh et al. IEEE TED 2021.



# New Era Electronics

“This new electronics lives close to the frontiers of science, and requires a high level of technical competence. It grows by the development of new products. It is characterized by the transistor and other solid state electronic devices.”

-- Frederick Terman, 1960.



Mark Lundstrom

## ***21<sup>st</sup> Century Electronics:***

- driven by applications
- inspired by new science
- enabled by new materials/heterogeneous integration
- accomplished by people with the right stuff

## ***SCALE +***

***Lecture Notes on New Era Electronics  
(World Scientific Publishing Company)***



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*Thank you!*