Nanoelectronics and the Future of Microelectronics

Mark Lundstrom
Electrical and Computer Engineering
Purdue University, West Lafayette, IN
August 22, 2002

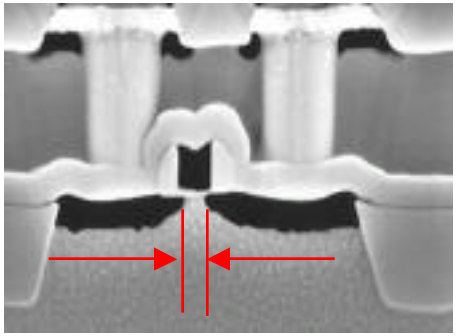
1. Introduction
2. Challenges in Silicon Technology
3. Beyond the MOSFET: Molecular FETs?
4. Beyond FETs?
5. Conclusions

1. Introduction

Objectives:

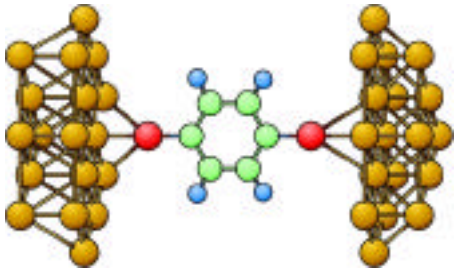
1) Use theory and computation to <u>understand</u> small electronic devices and to <u>explore</u> the most promising paths for the next 2-3 decades.

2) <u>Educate</u> students and professionals in new ways of treating small electronics devices.



10 nm scale MOSFETs

"The important thing in science is not so much to obtain new facts as to discover new ways of thinking about them."
-William Bragg



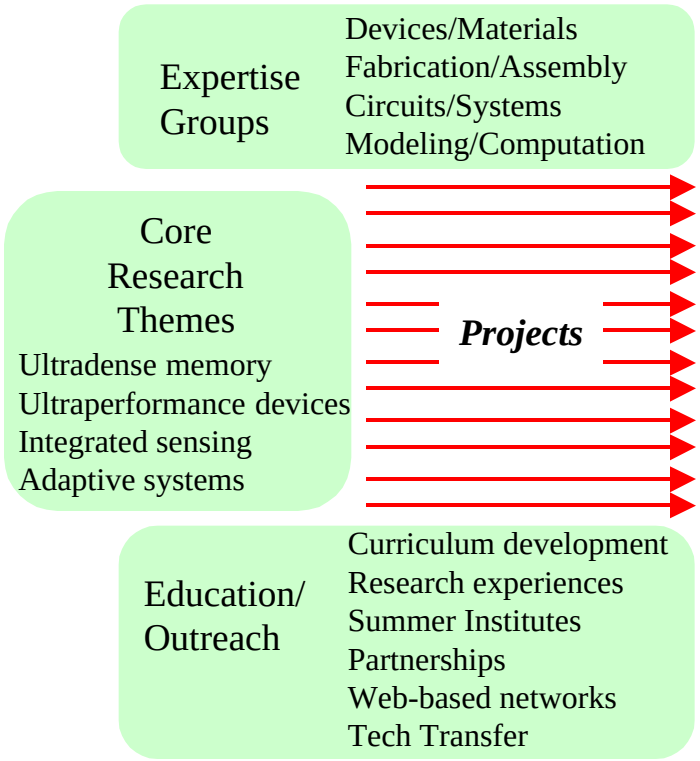
molecular electronics?

NASA URETI: Nanoelectronics and Computing

Purdue University, Northwestern,Florida, Cornell, UCSD, Yale

Mission:

To lay a foundation for a new class of heterogeneous terascale systems with the intelligence, adaptability, and fault tolerance necessary for future NASA missions

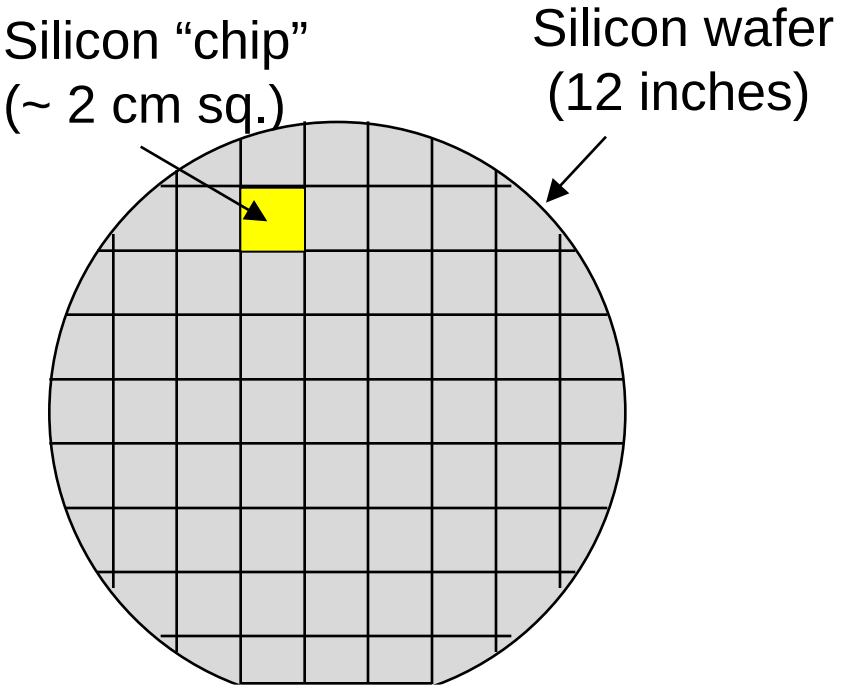


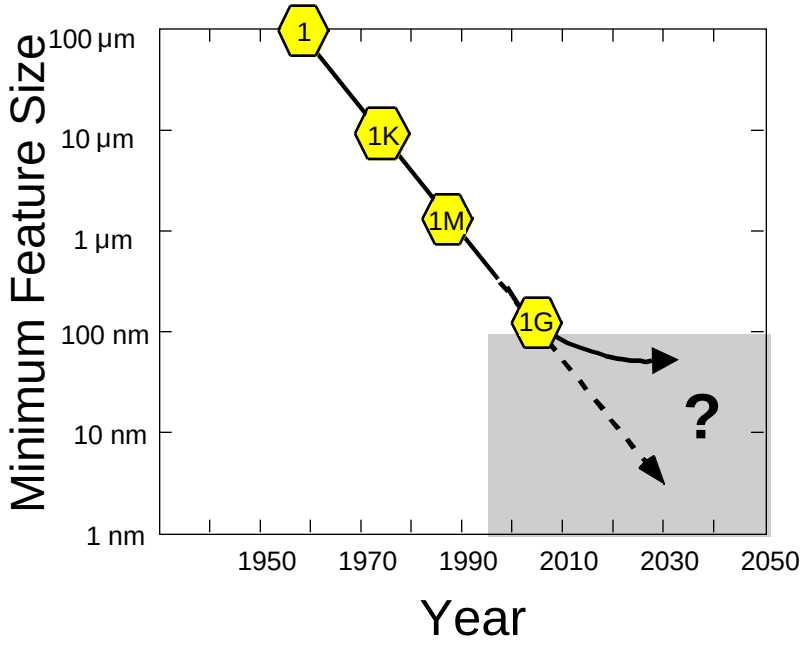
"towards *integrated nanosystems*"

Nanoelectronics and the Future of Microelectronics

1. Introduction
2. Challenges in Silicon Technology
3. Beyond the MOSFET: Molecular FETs?
4. Beyond FETs?
5. Conclusions

2. Challenges in Silicon Technology…..





Currently: >200M transistors/chip

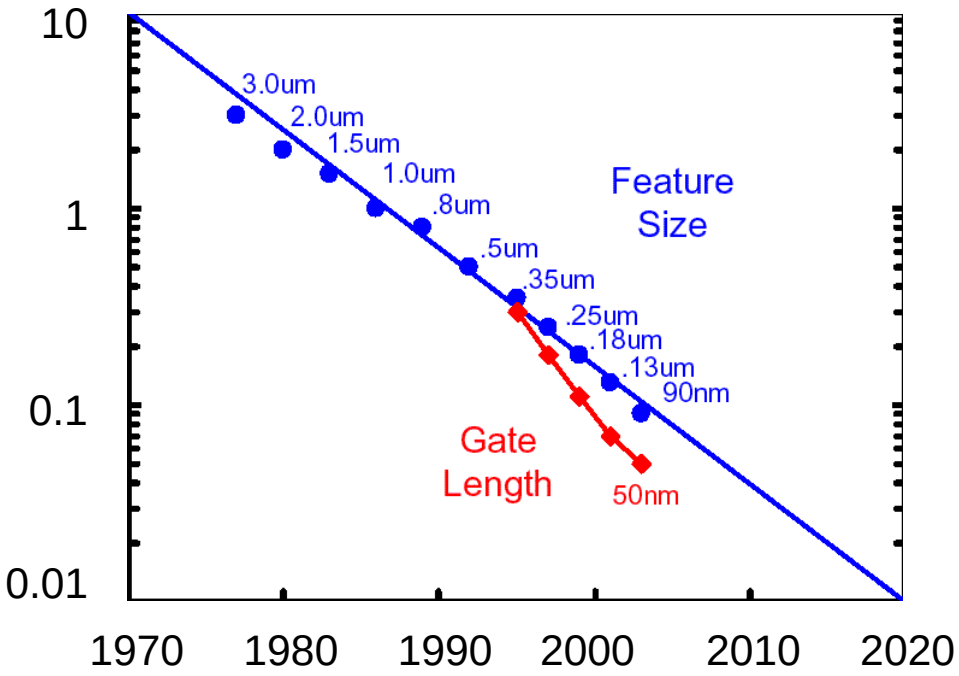
2016: ~10B transistors/chip

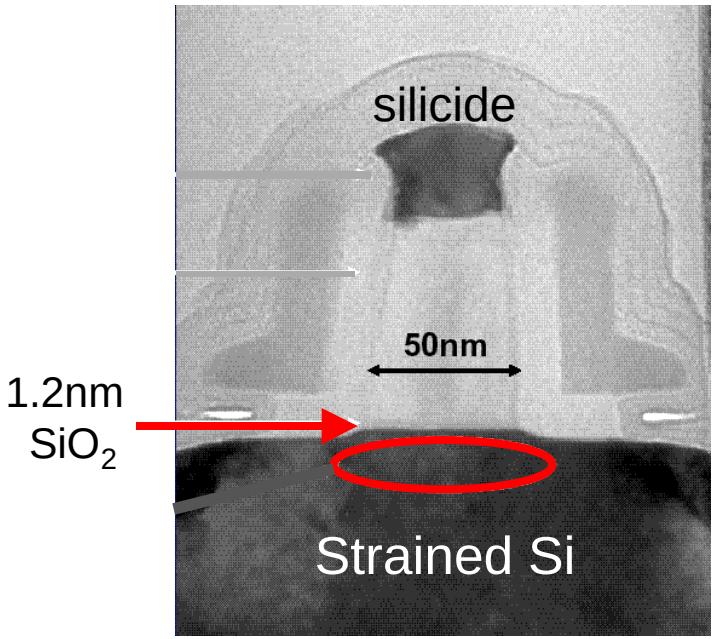
Technology generation

$L \rightarrow L/\sqrt{2}$

Cost per function drops 25% / yr

Intel: August 2002





www.intel.com/research/silicon/90nm_press_briefing-technical.htm

2. Challenges in Silicon Technology…..

- fundamental limits
- materials limits
- device limits
- circuit and system limits
- practical limits

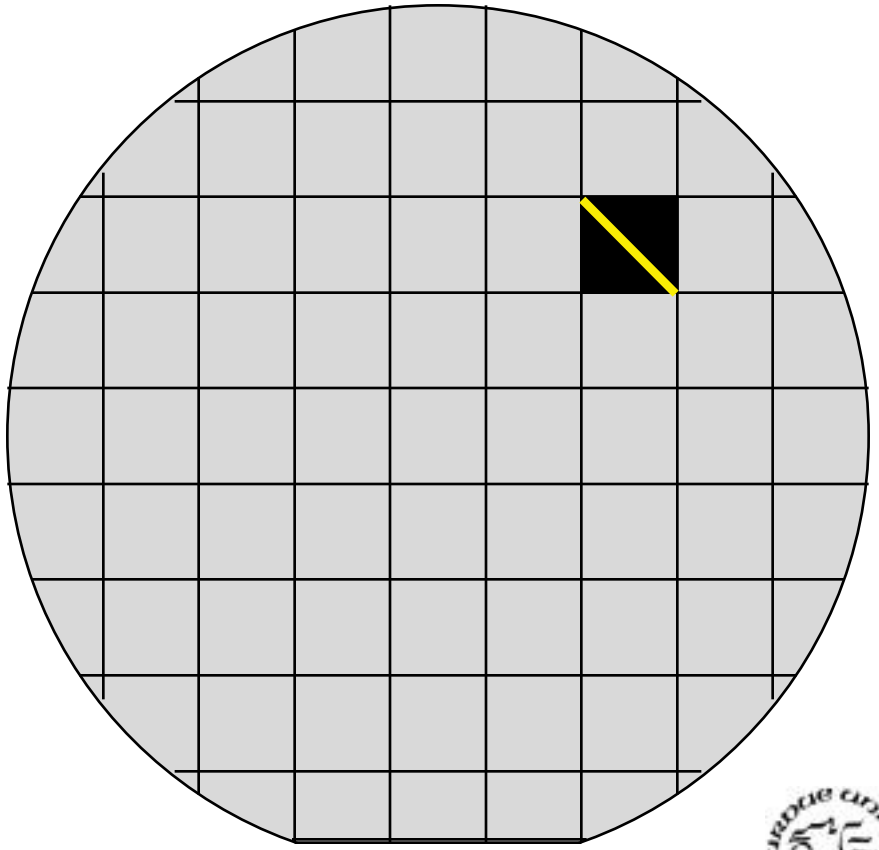
J.D. Meindl, et al., *Science*, **293**, 2044, 2001

- thermodynamics
- quantum mechanics
- **electromagnetics**

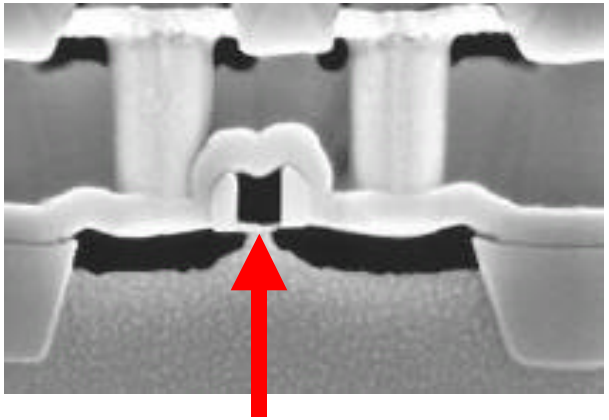
$$\tau > \ell / c \approx 200\,\text{ps}$$

In practice:

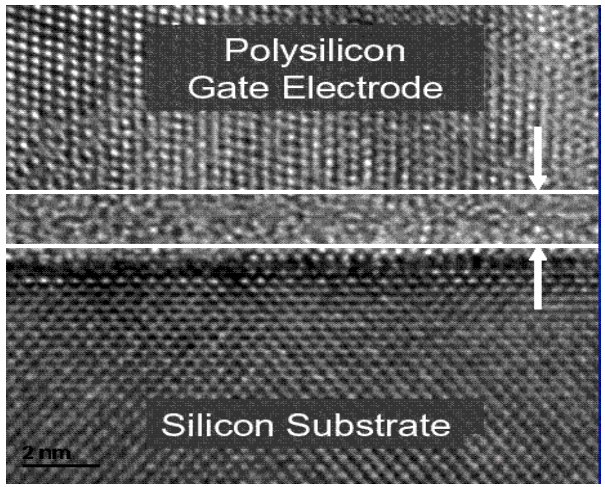
$$\tau \approx r_{\text{int}} c_{\text{int}} \sim \ell^2$$



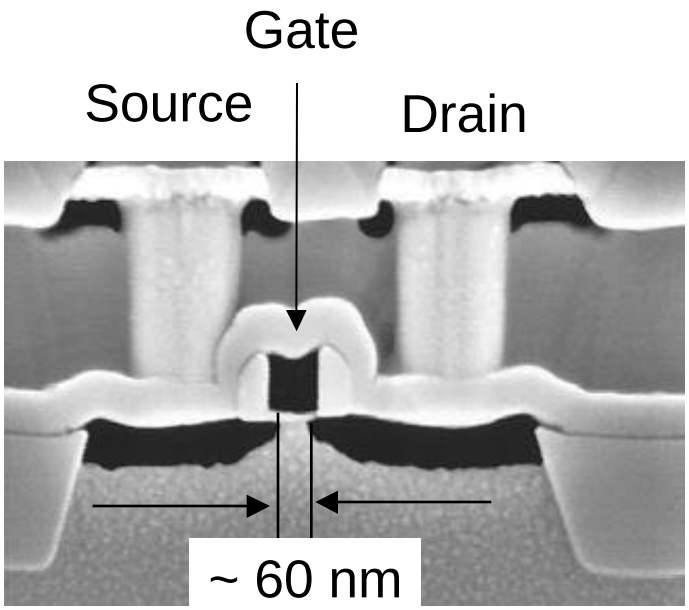
- silicon
- metal interconnects
- interlevel dielectrics
- **gate dielectric**



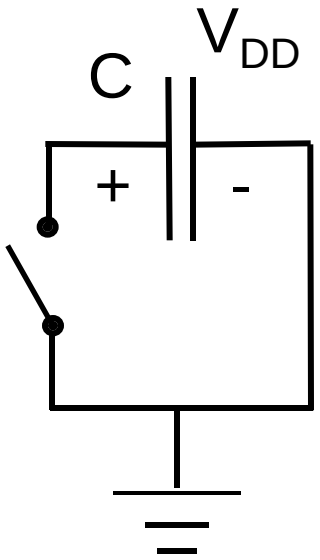
1.2 nm



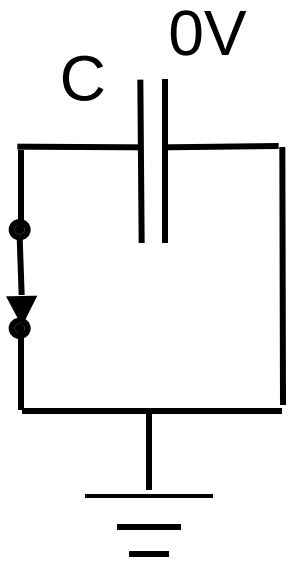
Min thickness?



off-current

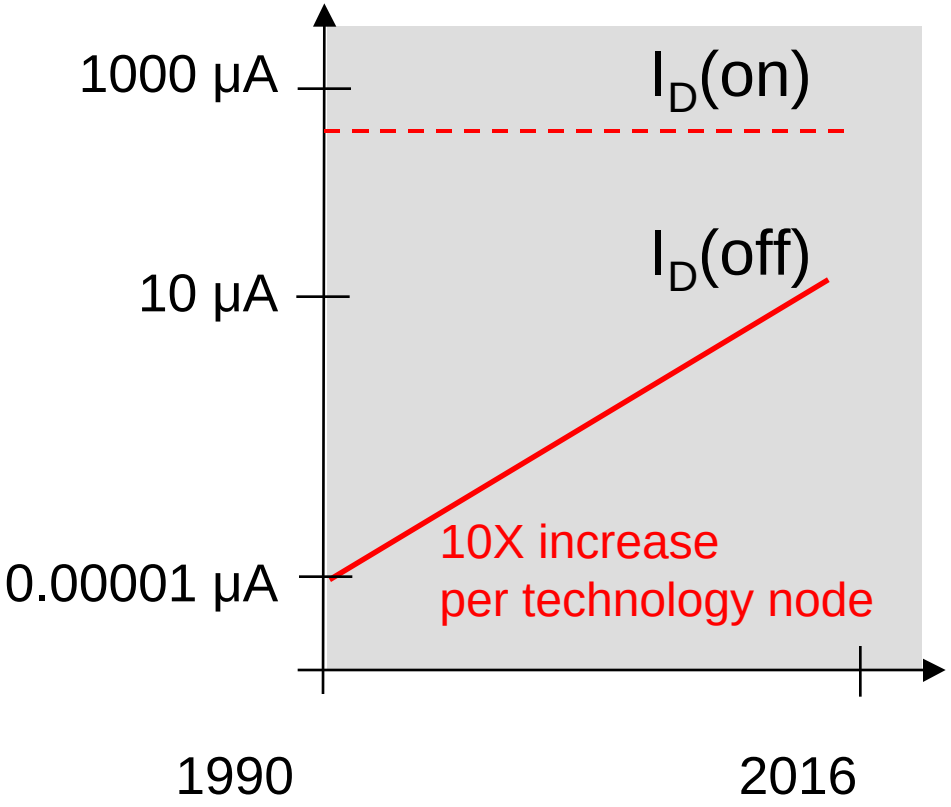


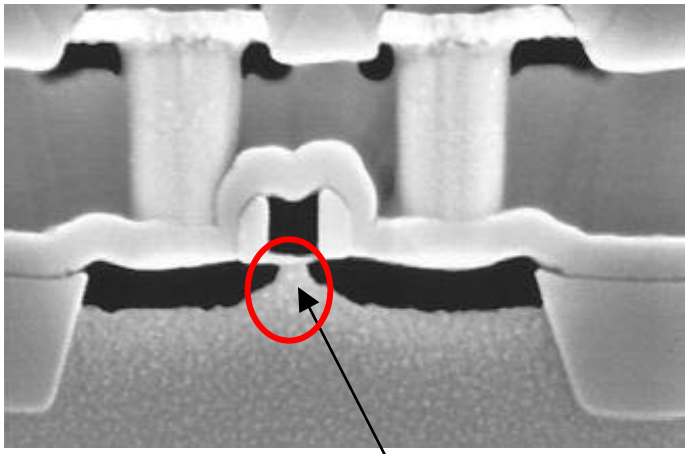
on-current



power: $f C V_{DD}^2$

2. Challenges in Silicon Technology….. *device leakage and fluctuations*

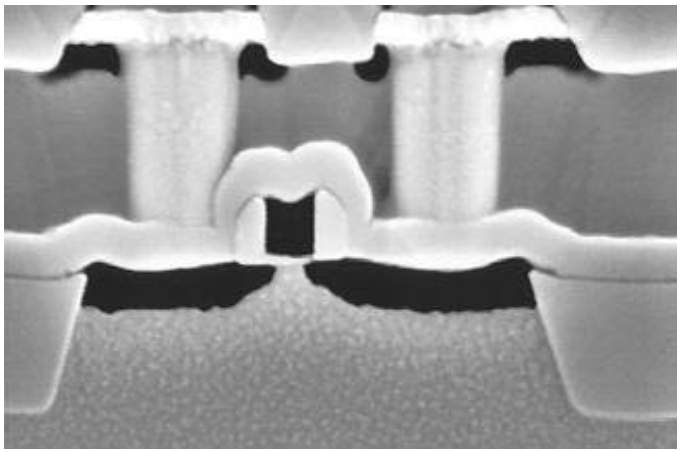


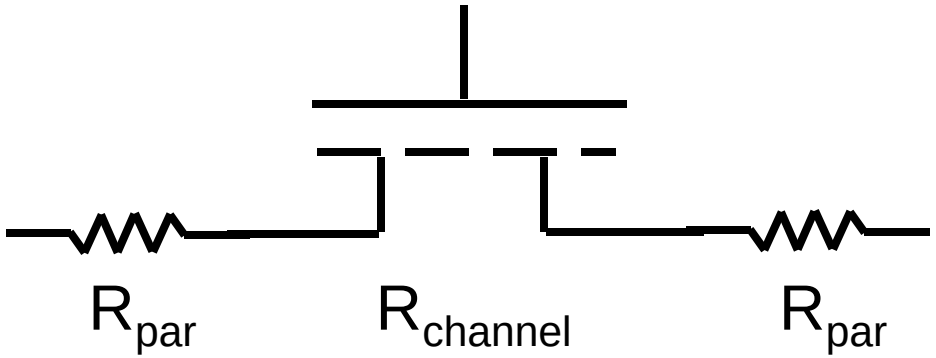


$$\Delta V_T \quad \frac{1}{\sqrt{N}}$$

2. Challenges in Silicon Technology…..

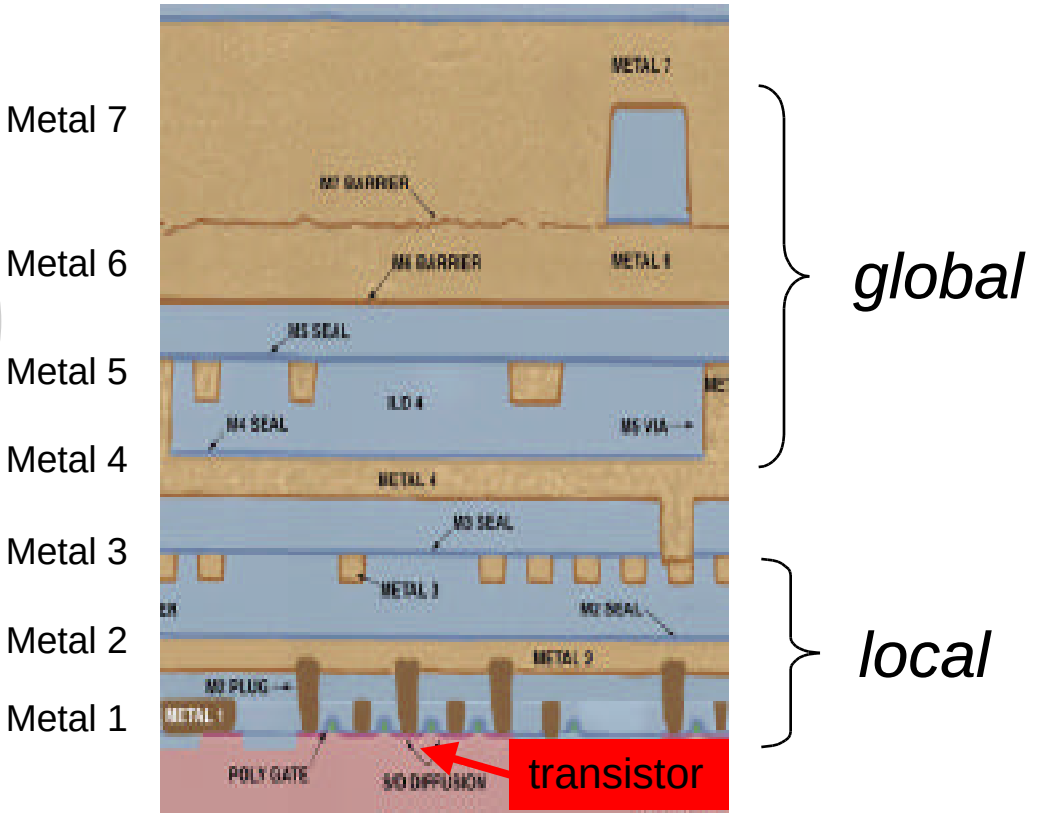
Device contacts



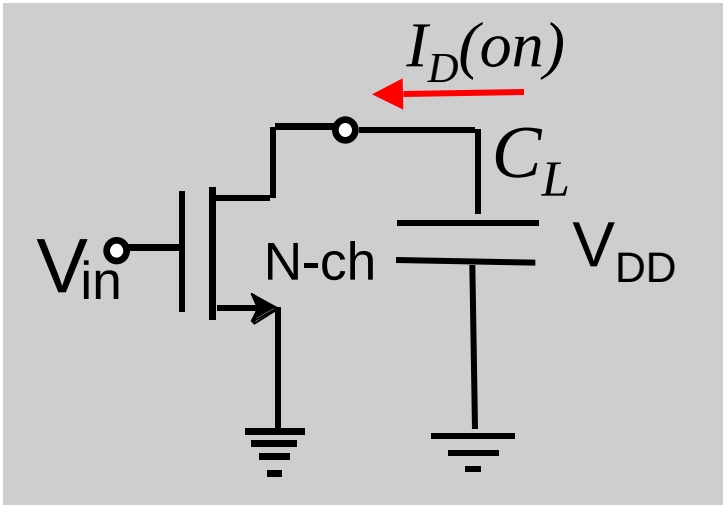


$$R_{parasitic} < 0.20 \times R_{channel}$$

- **Speed**
- **Power**


Metal 7
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
global
local
transistor
Silicon wafer

local



device:

$$t_t = \frac{L}{\upsilon} \approx 0.1\text{ps} = \frac{1}{1.6\,\text{THz}}$$

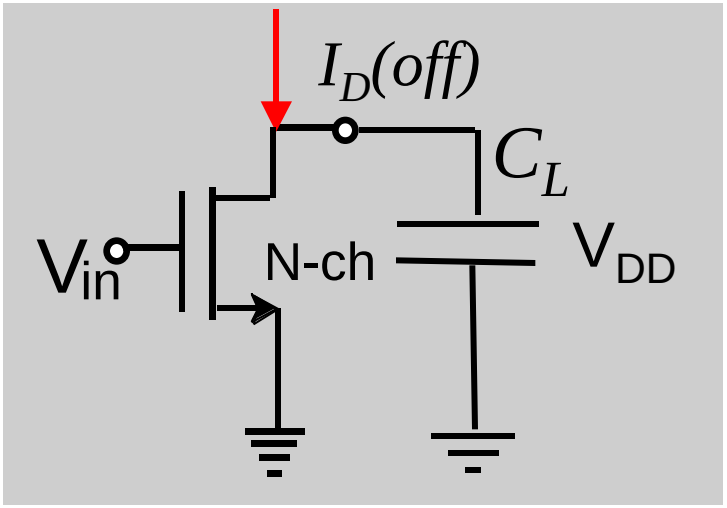
circuit:

$$\tau = \frac{C_L V_{DD}}{I_D(on)}$$

system:

$$\tau_{global} \approx r_{\text{int}} c_{\text{int}} \sim \ell^2$$

static power



$P_{off} = I_D(off)V_{DD}$

$I_D(off) \approx 10\,\mu A/\mu m$

$\approx 1\,kW$

10^{10} transistors/chip

dynamic power

$$f C V_{DD}^2$$

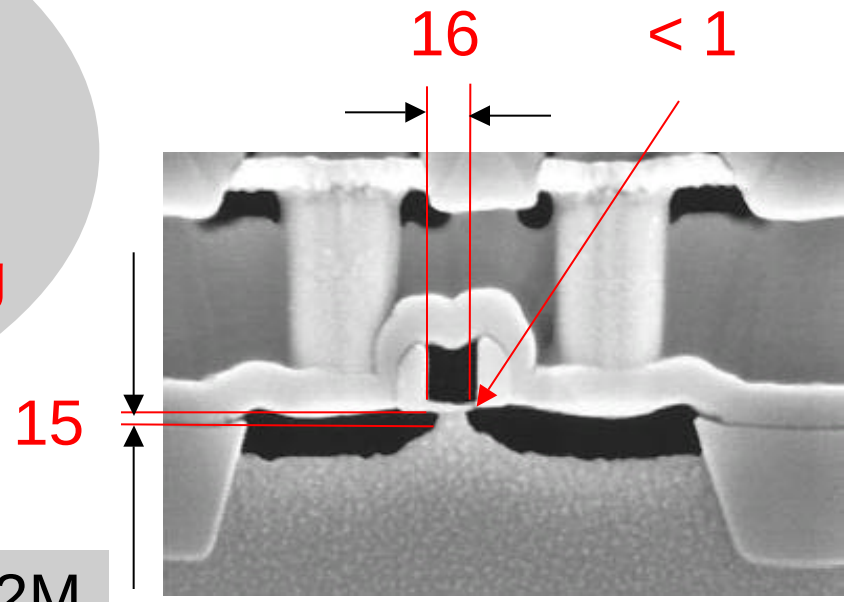
End-of-the-Roadmap silicon chips will operate 5 orders of magnitude from the fundamental limits for two main reasons:

1) Global interconnect delays

2) The need for a relatively high power supply voltage of ~ 0.5V

J.D. Meindl, et al., “Limits on Silicon Nanoelectronics for Terascale Integration,” *Science*, **293**, 2044, 2001

- lithography
- etching
- doping, etc.
- **atomic scale manufacturing**



2016 MOSFET

All dimensions in units of the Silicon lattice constant, 5.4Å

1967 Cost of a Silicon Fab:	$ 2M
2002 Cost of a Silicon Fab:	~ $ 3B
2015 Cost of a Silicon Fab:	~$100B

Selected 2001 ITRS "Grand Challenges"

- MOSFET on/off ratio
- power management
- noise management
- global interconnects (cost of communication)
- next generation lithography
- process control
- cost-effective manufacturing
- decreasing reliability
- error tolerant design
- design productivity (system complexity)

www.itrs.net

2. Challenges in Silicon Technology…..

"After four decades of rapid advances in … silicon semiconductor technology, a systematic assessment of its hierarchy of physical limits reveals an enormous remaining potential to advance from the current multi-billion transistor chips to the multi-trillion transistor range of terascale integration."

"This potential represents more than a three decade increase in the number of transistors per chip…"

"Fundamental physical limits….are virtually impenetrable barriers to future advanced of TSI."

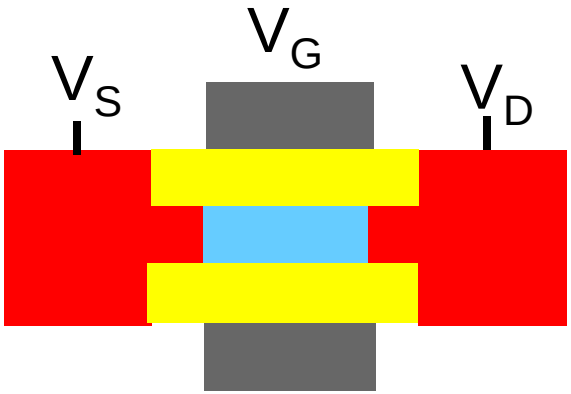
J.D. Meindl, et al., "Limits on Silicon Nanoelectronics for Terascale Integration," *Science*, **293**, 2044, 2001

Nanoelectronics and the Future of Microelectronics

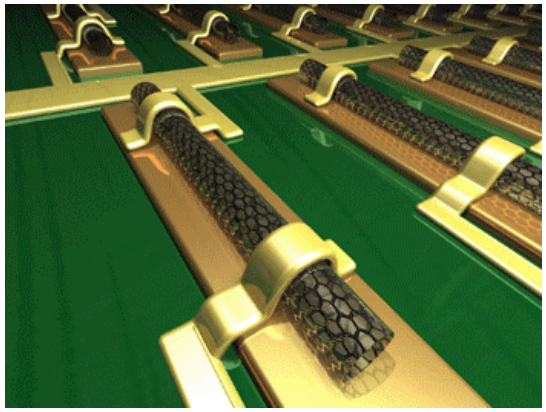
1. Introduction
2. Challenges in Silicon Technology
3. Beyond the MOSFET: Molecular FETs?
4. Beyond FETs?
5. Conclusions

3. Beyond the Si MOSFET.....

1) MOSFET

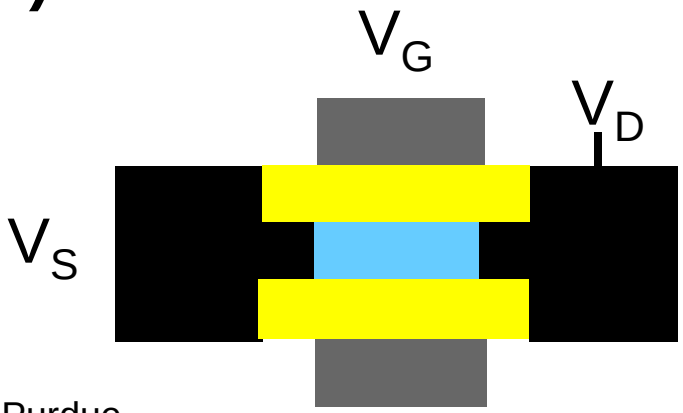


3) CNTFET

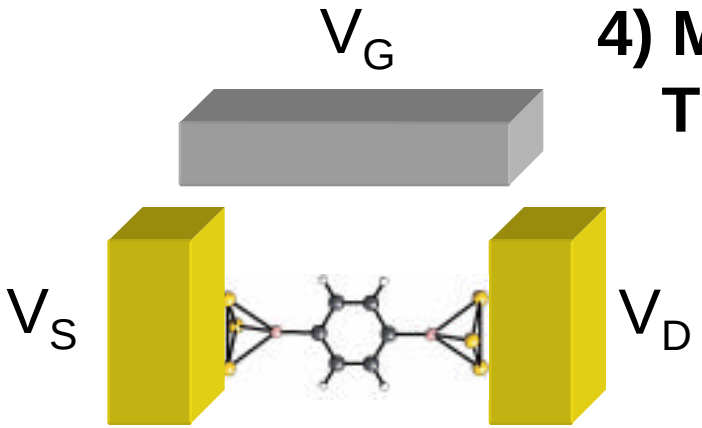


Bachtold, et al., Science, Nov. 2001

2) SBFET

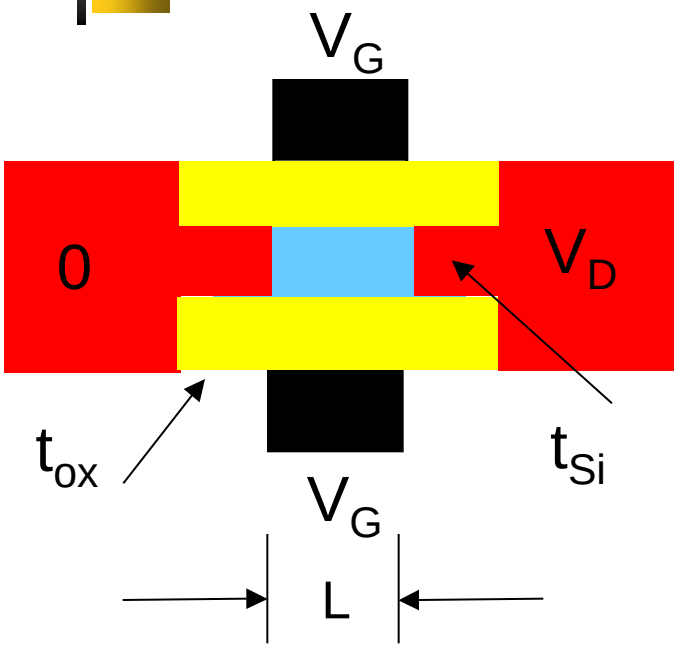


4) Molecular Transistors?

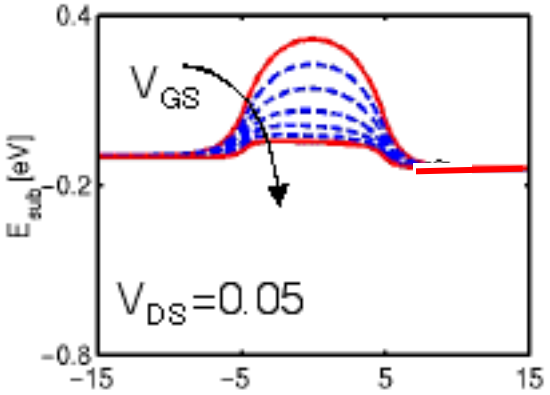


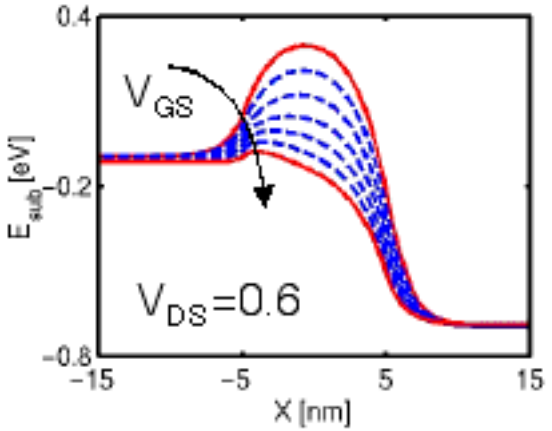
3. Beyond the Si MOSFET.....

The Double Gate MOSFET



electron energy = -q x voltage

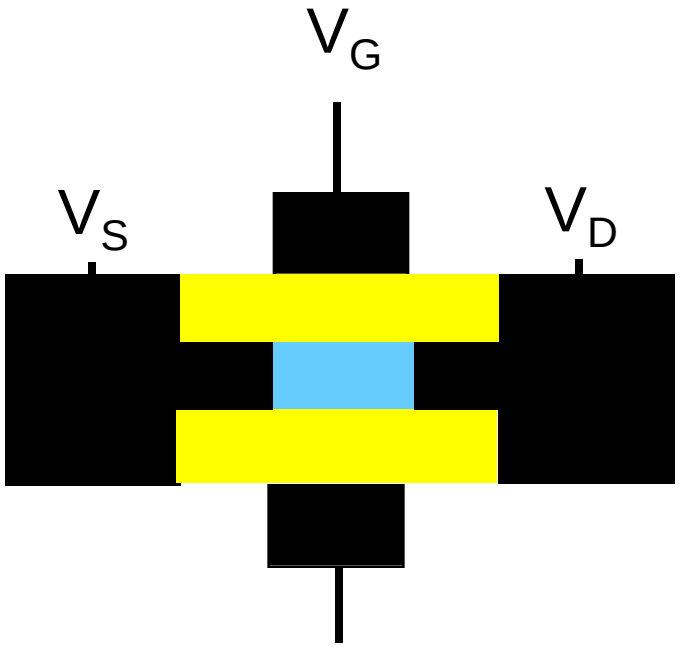




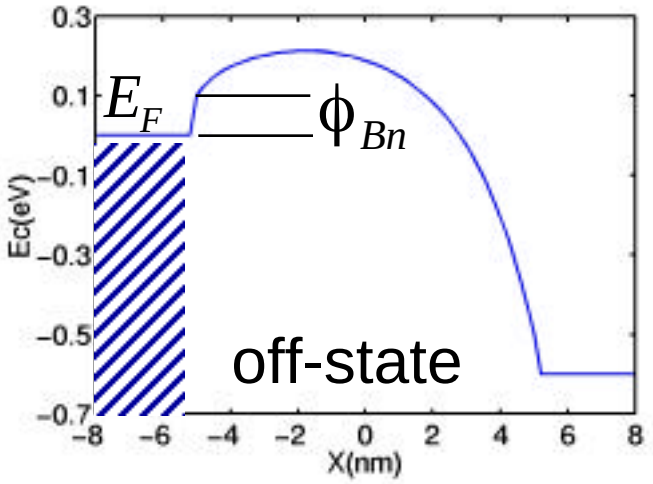
+ good scaling
+ good sub-threshold swing
+ high drive current
- manufacturability
- design

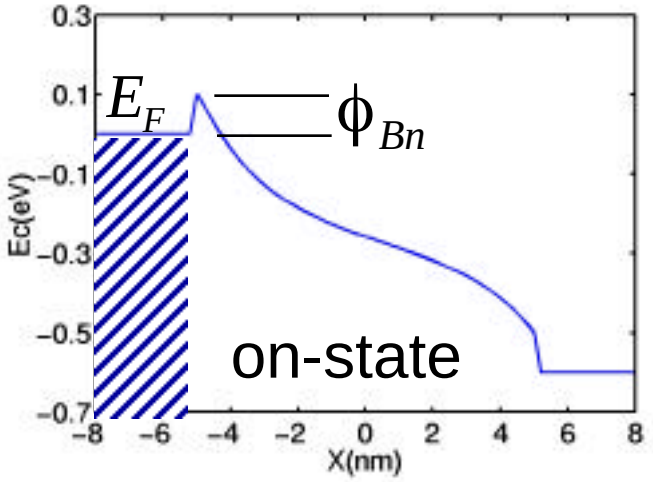
gate-modulated Q

The Schottky barrier MOSFET

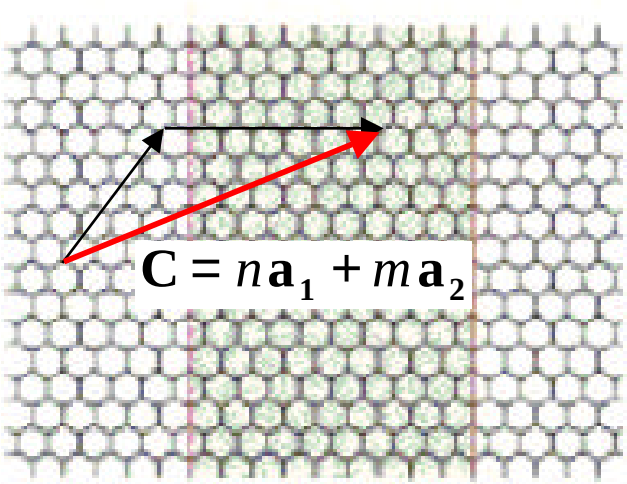


gate-modulated T

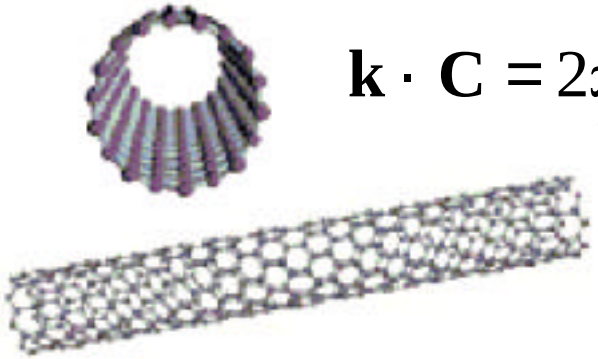




graphene



(n, m) carbon nanotube

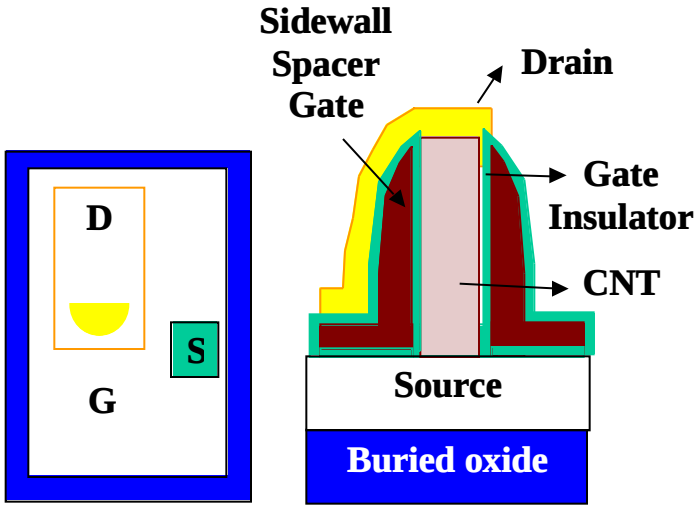


$$\mathbf{k} \cdot \mathbf{C} = 2\pi q$$

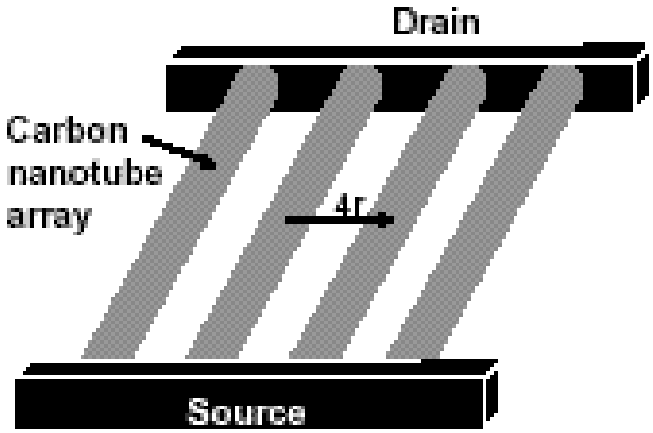
"chirality"

- metalic: (n-m) = multiple of 3
- semiconducting: E_G ~ 0.7 eV/D(nm)

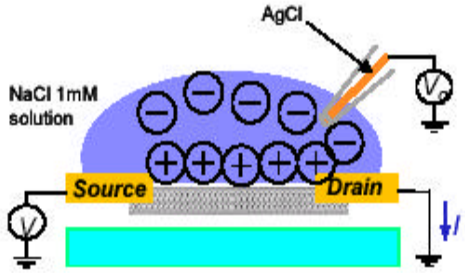
coaxial geometry

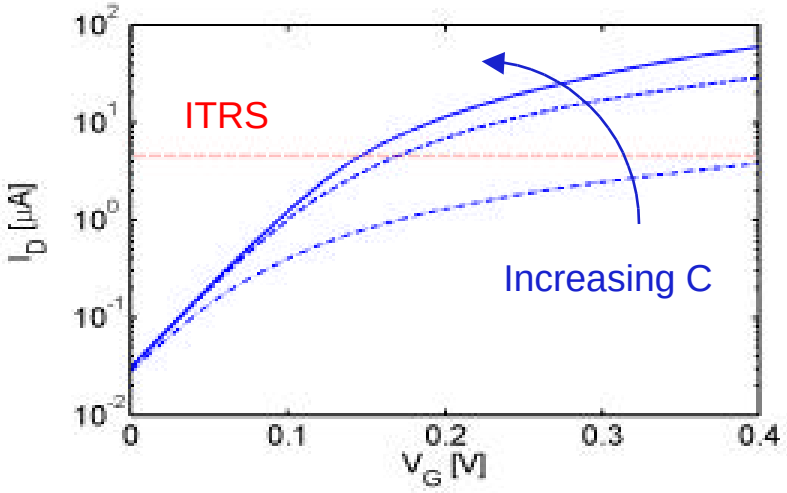


planar geometry CNTFET



3. Beyond the Si MOSFET..... *the CNTFET*





I_{on} ~ 10 μA
at V_{DD}~1V

μ(max) ~ 2,000-20,000 cm²/ V-s

D = 3 nm
T_{ins} = 10nm SiO_2
T_{ins} = 3nm HfO_2
T_{ins} = water gate

McEuen group, to be published.

The ultimate FET?

near-ballistic transport

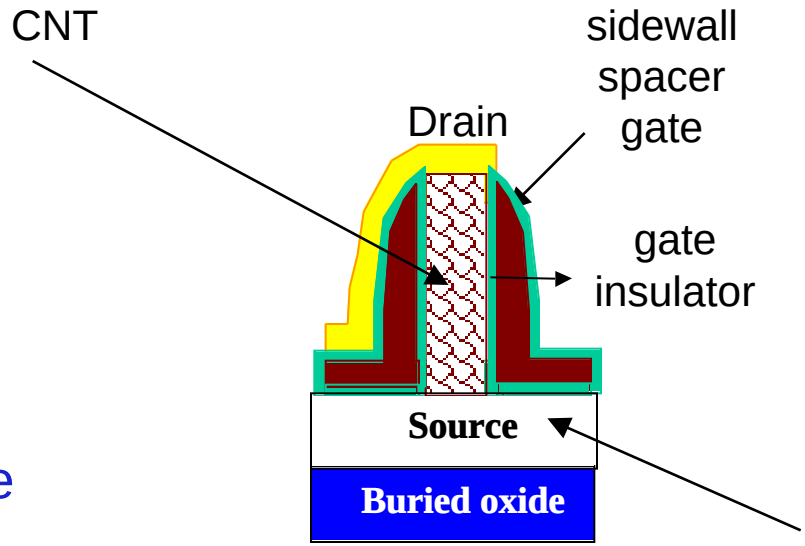
high velocity bandstructure

high on-current (perhaps 3 nA/nm)

high on/off ratio

low voltage

good device-device control



cylindrical geometry for electrostatics

no surface states to accommodate hi-K

C_Q limited operation

negative SB contact?

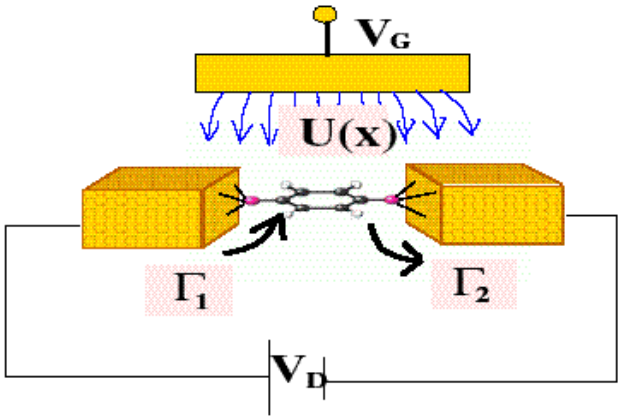
$R_{series} \sim 0$

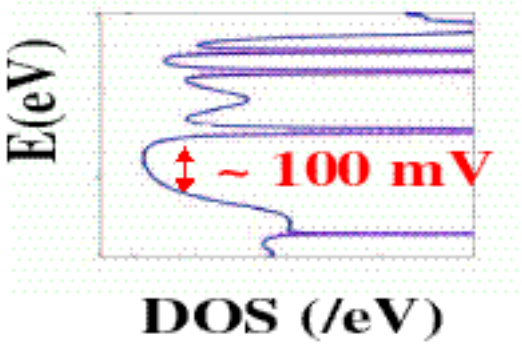
small footprint

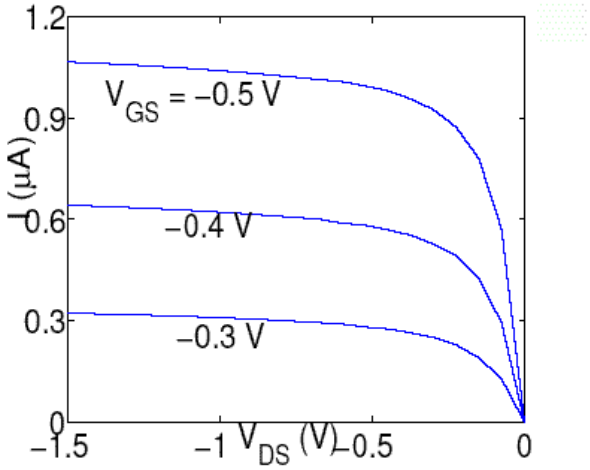
growth, assembly, manufacturing?

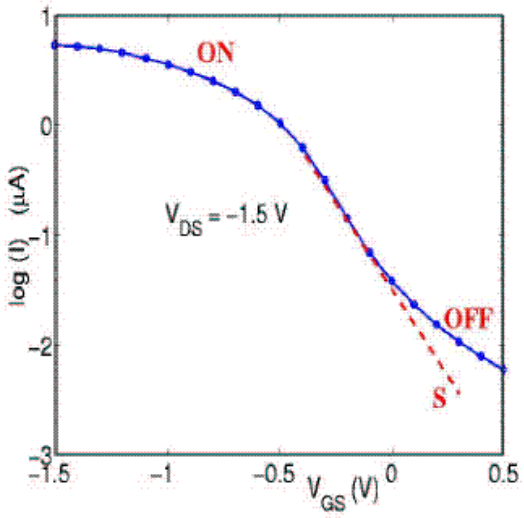
3. Beyond the Si MOSFET.....

SAMFETs ?









L≈ 1 nm

t_{ox} << L

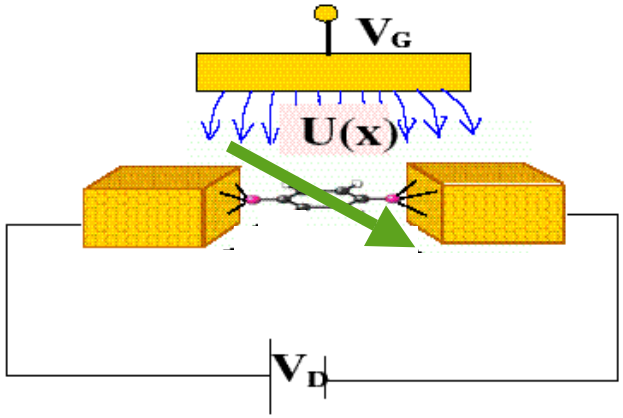
t_{ox} ≈ 1-2Å !!

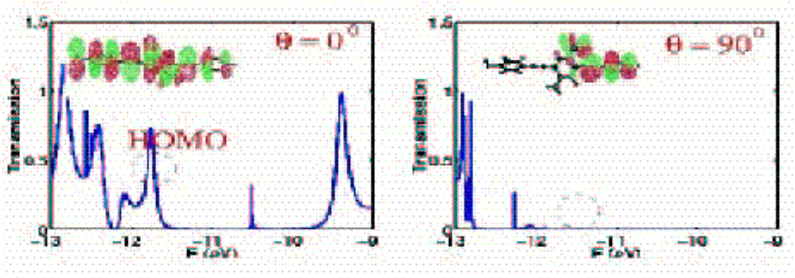
S ≈ 100 mV/dec

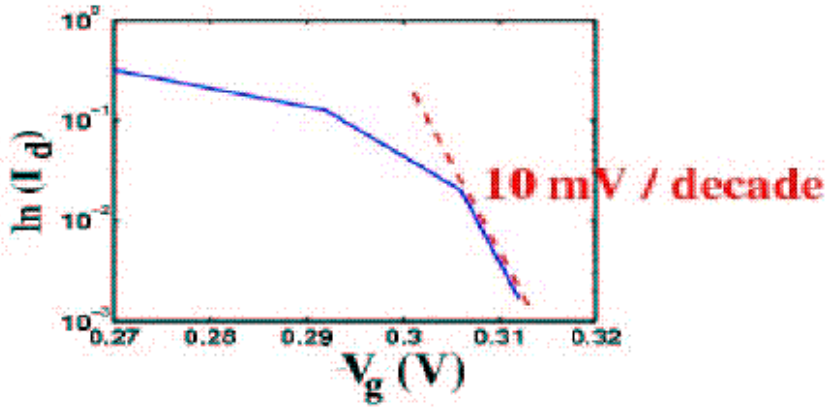
P. Damle, et al.

3. Beyond the Si MOSFET.....

SAMFETs ?







gate-modulated conformation?

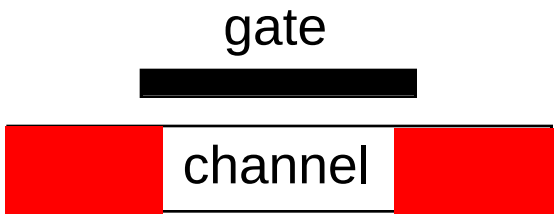
t_{ox} = 1nm

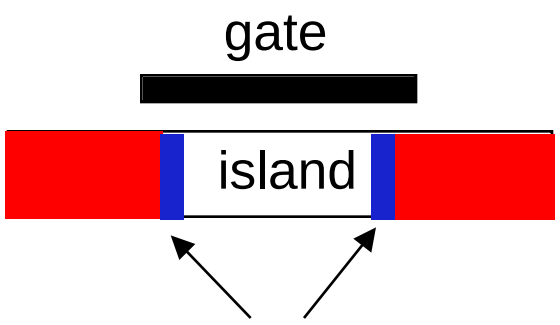
S. Datta, A. Ghosh, P. Damle, T. Rakshit

Nanoelectronics and the Future of Microelectronics?

1. Introduction
2. Challenges in Silicon Technology
3. Beyond the MOSFET: Molecular FETs?
4. Beyond FETs?
5. Conclusions

Single electron transistors





2016: L=9nm, W=18nm

V_{DD} = 0.4V, V_T = ~0.2V

T_{ox} = 1 nm

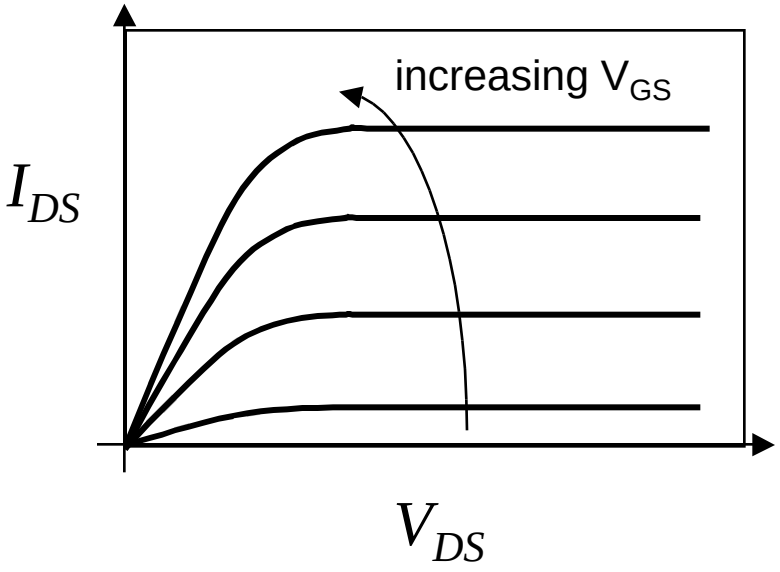
$q/C >> k_B T/q$

~6 *electrons*

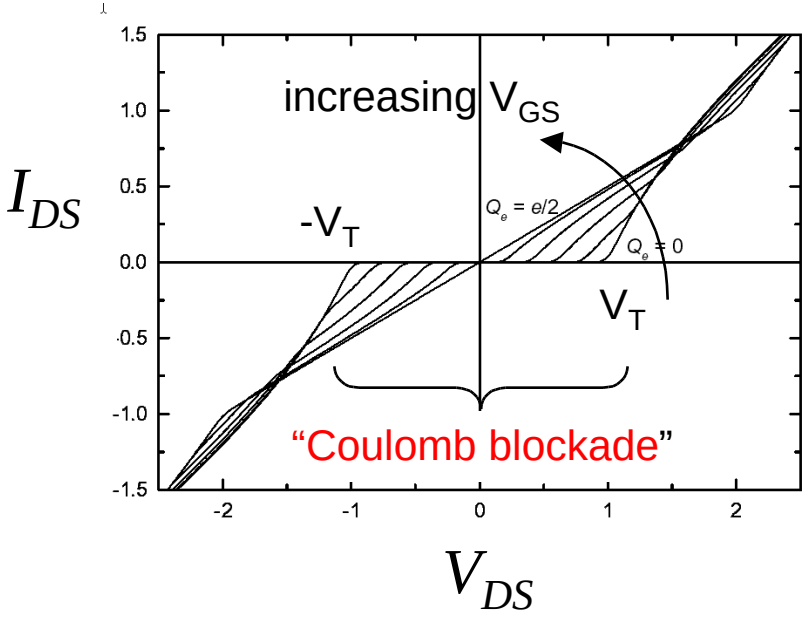
for 300K operation
Dia ~ 1 nm
(C ~ 0.1aF)

4. Beyond FETs.....

Small MOSFET

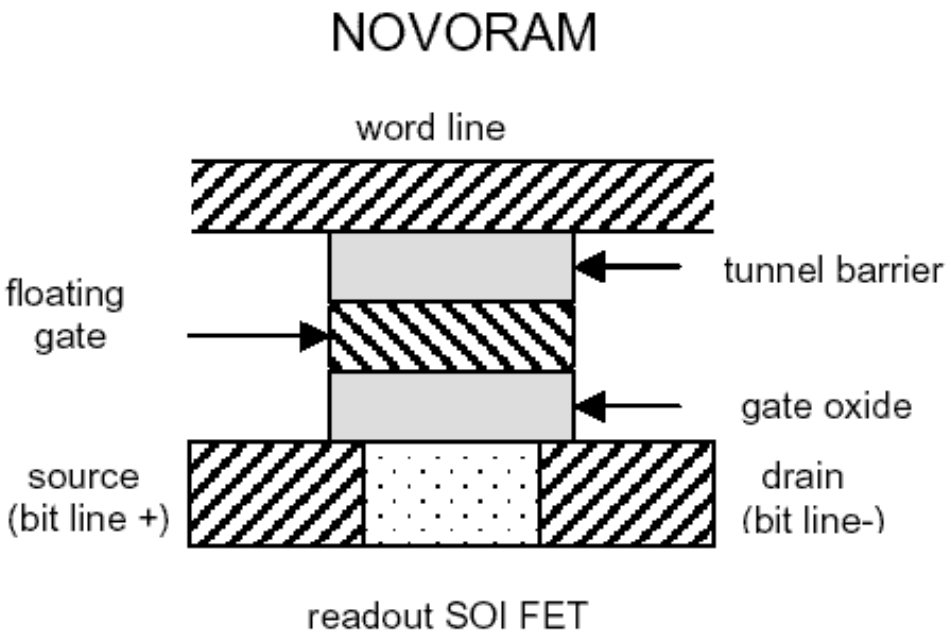


Single Electron Transistor



From K. Likharev, to appear 2002

SET / MOSFET memories?



Cell size = $8F^2$

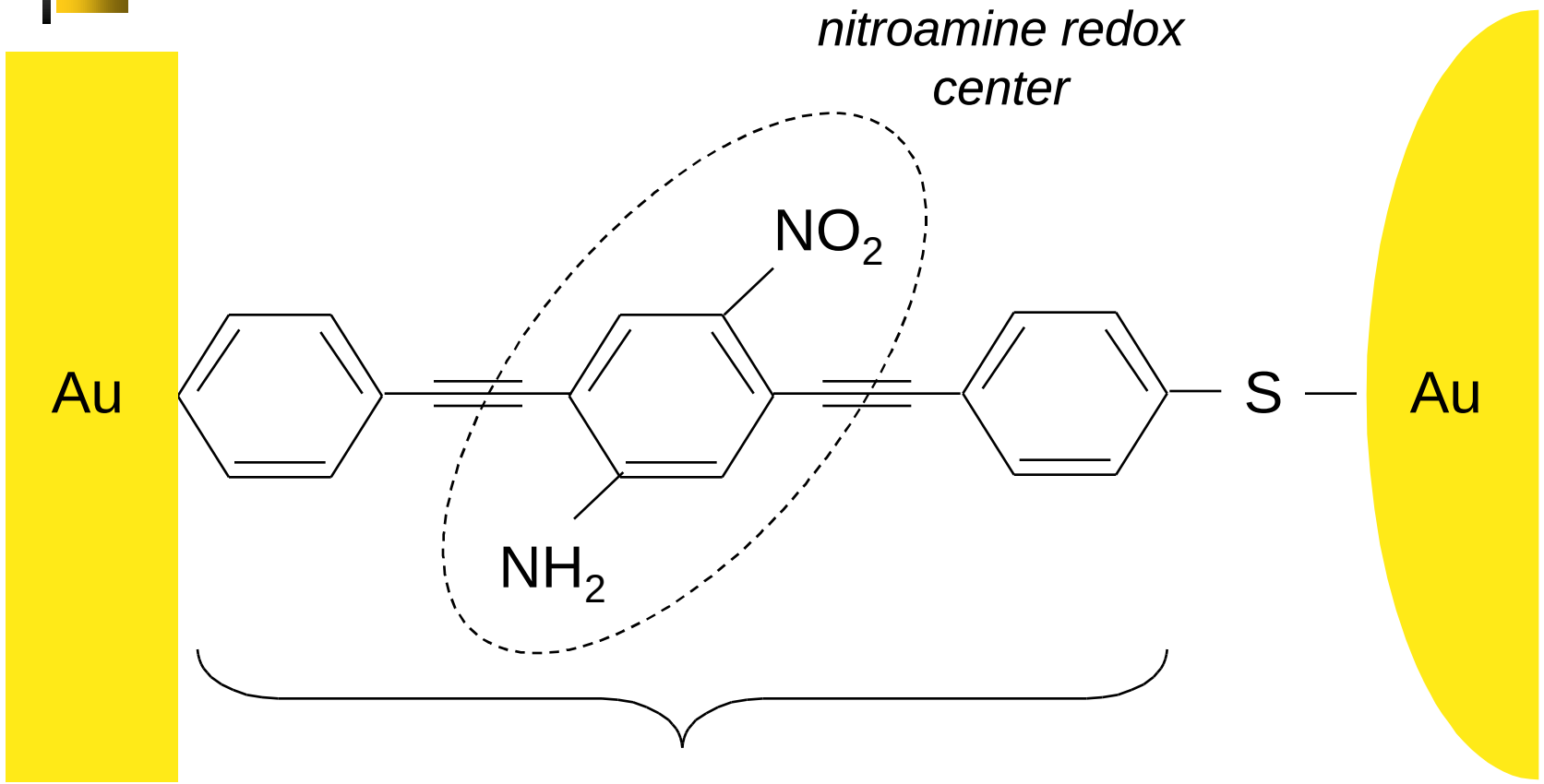
$F_{min} \approx 2$ nm

-->

> 10^{12} bits/cm^2

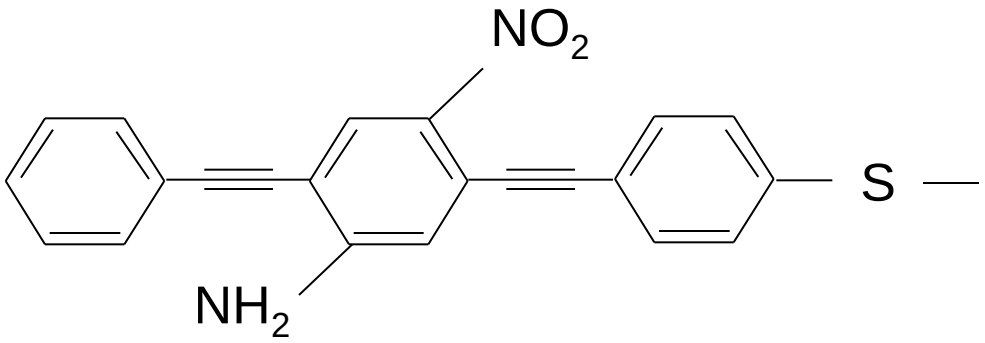
From K. Likharev, to appear 2002

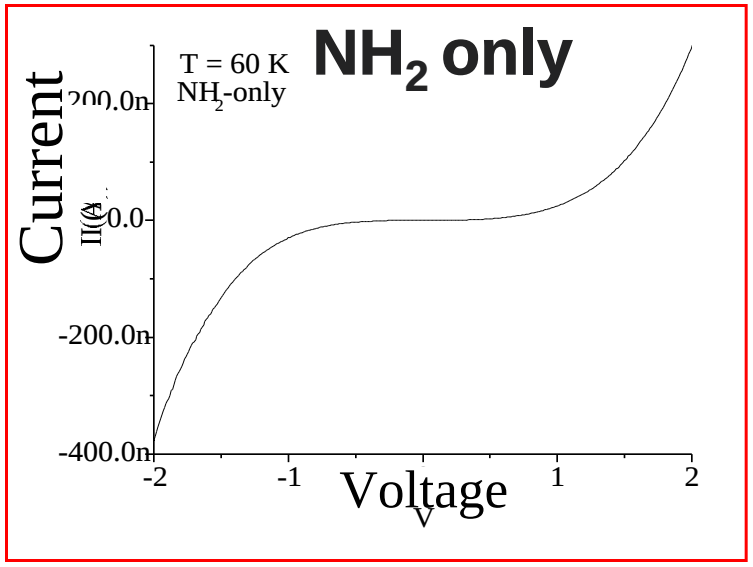
4. Beyond FETs.....

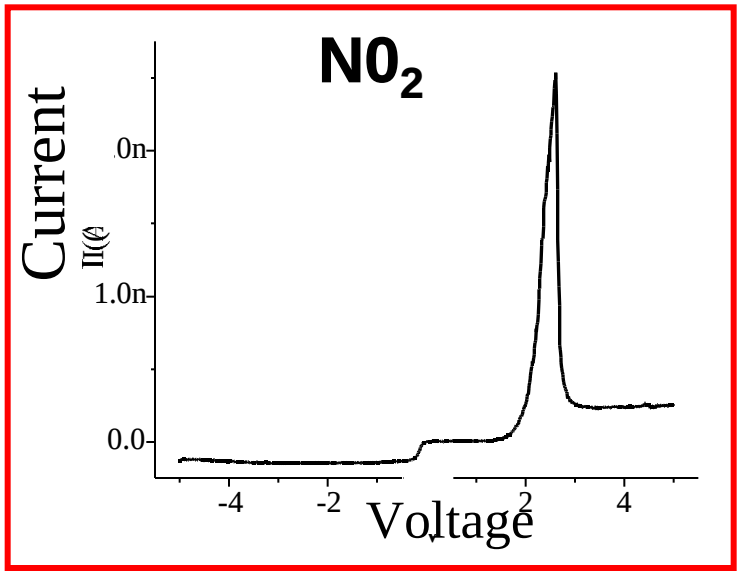


Reed (Yale) and Taur (Rice)

4. Beyond FETs.....



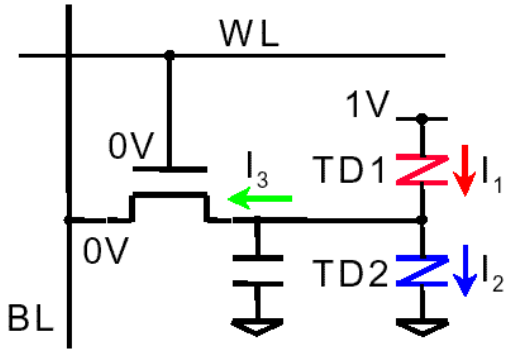


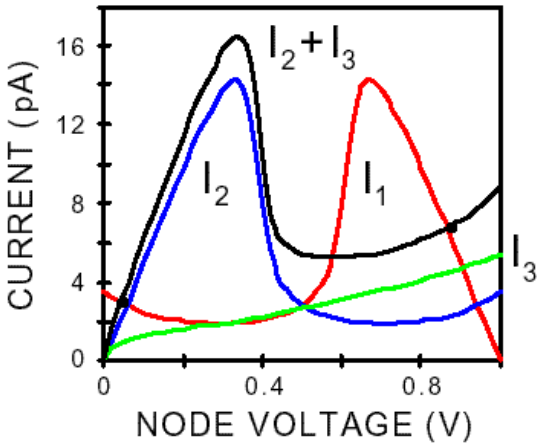


J. Chen, *et al*., Yale

CMOS/TD SRAM

- memory
- latches
- registers
- A/D converters
- multiplexers
- clock generators
- etc.





+ *increase speed*
+ *lower power*
+ *reduce size*

+ *20X reduction in power (DRAM)*

+ *50% reduction in size (SRAM)*

A. Sebaugh, et al. 1998 IEDM Tech. Digest

Nanoelectronics and the Future of Microelectronics

1. Introduction
2. Challenges in Silicon Technology
3. Beyond the MOSFET: Molecular FETs?
4. Beyond FETs?
5. Conclusions

5. Conclusions

- The science of molecular electronics is rapidly advancing.
- This is a creative time for device invention.
- Silicon technology continues to beat Moore's Law.

How do we make progress towards integrated nanoelectronic systems?

5. Conclusions

End-of-the Roadmap MOSFETs

- low on-current at low V_{DS}
- high off-current
- large device to device variations
- low reliability and yield
- device footprint hard to scale

The characteristics of nano-MOSFETs will be similar to those of the alternatives being explored.

5. Conclusions

Selected 2001 ITRS Design Challenges

- communication centric design (network-oriented paradigms)
- design robustness (fault tolerance)
- system power consumption (on-chip parallelism, re-configurability)
- integration of heterogeneous technologies (for sensing, actuation, possibly computation)

www.itrs.net

5. Conclusions

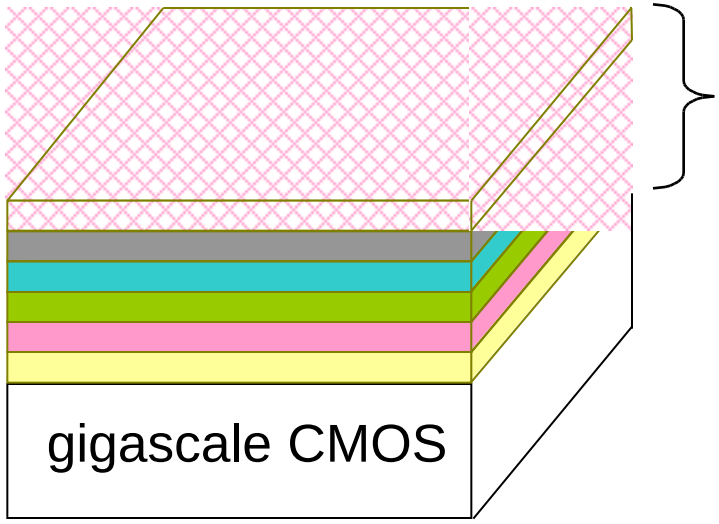
Characteristics of future nanocomputer architectures

- extremely localized interconnect
- homogeneous arrays to support heterogeneous processing
- parallelism at multiple levels
- dynamic re-configurability and fault tolerance

Beckett and Jennings., “Towards Nanocomputer Architecture,” *ACSAC ‘2002..*

5. Conclusions

3D heterogeneous systems



1) add functionality to a Si SOC:

- bio-inspired perceptualization
- sensors
- optoelectronics
- …

2) improve a Si SOC:

- ultra-dense nonvolatile memory
- cooling (active/passive)
- low-cost manufacturing
- …

Integrated Nanoelectronic Systems: A 10 Year Vision

1) develop the science base
2) explore transistors and novel devices
3) growth and assembly…

…guided by system issues

identify promising approaches

develop science and engineering base for prototype integrated nanosystems

Year 1 Year 5 Year 10

5. Conclusions

-circuit / system design

"The best way to predict the future is to invent it."
-Alan Kay

-nano / molecular science
-device invention