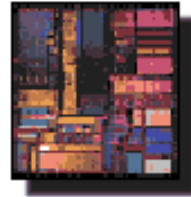# Digital Systems Design Automation
Unit 1: Course Introduction and Overview
## Lecture 1.3: Course Overview

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Outline

1.1 Moore's Law

1.2 Design Complexity and need for EDA

1.3 Course Overview

1.4 Taxonomy of integrated circuits

1.5 Levels of abstraction in IC design

1.6 A quick tour of logic level design automation

Focus of this course

- How to <u>automatically</u> design and analyze digital VLSI circuits at the <u>logic</u> level (gates & flip-flops)
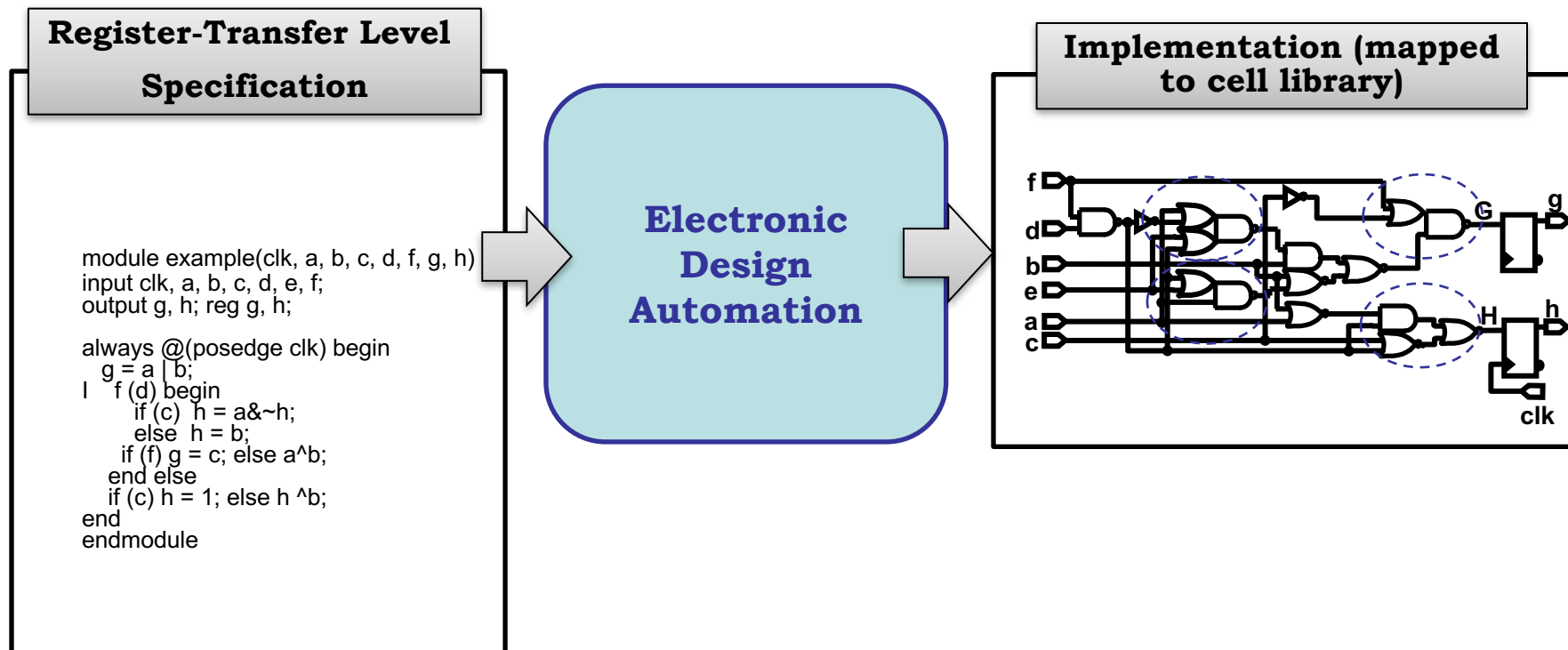
Focus of this course

- Foundations of logic-level EDA tools
  - Computational techniques and algorithms used
- This is <u>NOT</u>
  - A course on how to design VLSI circuits (although prior knowledge of design using EDA tools would help)
  - A course on Verilog or VHDL
  - A training course on how to use commercial EDA tools

Required Background

- Digital logic design
  - Basic undergraduate course (Purdue ECE 270 or equivalent)
- Programming (C/C++)
  - Write correct programs of few 1000s of lines without assistance
  - Compile and run programs downloaded from the Internet with moderate documentation
  - Study existing code and get a basic understanding of how it works
- Basic data structures and algorithms
  - Purdue ECE 368 / 608 or equivalent
- Experience using EDA tools (desirable, not necessary)

Course Outline

- **Introduction**
- **Advanced Boolean Algebra**
  - Re-cap of basics and advanced concepts
- **Two-level minimization of combinational circuits**
  - Review of Quine-McCluskey method
  - Exact and heuristic algorithms (Espresso)
- **Multi-level logic synthesis**
  - Technology-independent optimizations
  - Technology mapping
- **Sequential logic optimization**
  - Finite State Machine (FSM) minimization, retiming, regular expressions and FSMs
- **Logic verification**
  - Boolean Satisfiability (SAT)
  - Canonical Boolean representations - Binary Decision Diagrams (BDDs)
- **Timing Analysis**
  - Longest true path, path sensitization criteria, algorithms for computing true delay, statistical timing analysis
- **Power Analysis and Optimization**
  - Gate-level power estimation, technology mapping for low power, automatic clock gating and power management
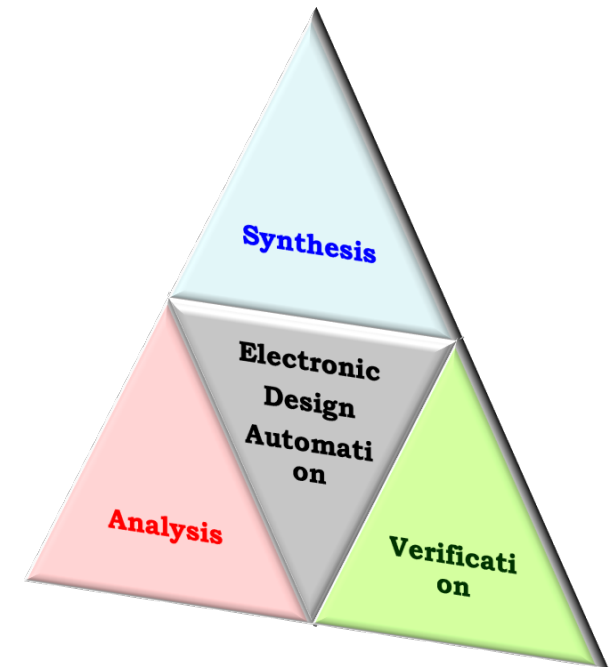
Logistics

- Office hours: Tuesday, Thursday 10:30-11:30AM
- Course material, announcements, homework submissions using Brightspace or hardcopy
- Assistant: Camille Hamelman
  - Office: MSEE 330
  - Email: camillea@purdue.edu
- Travel: I may have to miss a few classes due to work-related travel
  - Will schedule makeup classes and/or provide video lectures

References

- **Recommended reference books**
  1. Synthesis and Optimization of Digital Circuits, Giovanni De Micheli, McGraw-Hill, Jan. 1994, ISBN-10: 0070163332 (available on Brightspace)
  2. Logic Synthesis and Verification Algorithms, Gary D. Hachtel and Fabio Somenzi, Springer, Feb. 2006, ISBN-10: 0387310045.
  3. Logic Synthesis, Srinivas Devadas, Abhijit Ghosh, Kurt Keutzer, McGraw-Hill, June 1994, ISBN-10: 0070165009
  4. Introduction to Algorithms, Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, Clifford Stein, MIT Press, Sep. 2001, ISBN-10: 0262032937
- **Additional papers and reference material will be posted on Blackboard or handed out as needed**

References

- Conferences and Journals
  - Design Automation Conference – www.dac.com
  - International Conference on Computer-Aided Design – www.iccad.com
  - Design, Automation, and Test Europe – www.date-conference.com
  - Asia South-Pacific Design Automation Conference – www.aspdac.com
  - IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems – http://tcad.polito.it
  - ACM Transactions on Design Automation of Electronic Systems - http://todaes.acm.org/
- Trade magazines and websites
  - Electronic Engineering Times (EE Times) – www.eetimes.com
  - Electronic Design News (EDN) - www.edn.com
  - EDACafe - www.edacafe.com
  - EDA Consortium - www.edac.org
- Leading EDA companies
  - Synopsys – www.synopsys.com
  - Cadence – www.cadence.com
  - Mentor Graphics – www.mentor.com

Course Grading

- Homeworks: 30%
- Midterm: 25%
- Class participation: 5%
- Project: 40%

- Late submission policy: -10% per day

Reading for next two classes

- Review Boolean algebra (your favorite book)
  - Digital Design: Principles & Practices, 4th Ed., John F. Wakerly, Prentice Hall, 2005
  - Purdue ECE270 course material
    - *Module 2: Boolean Algebra and Combinational Logic Circuits*
- De Micheli – Ch 1 (Introduction)

    OR

- Hachtel & Somenzi – Ch. 1 (Introduction)

Did You Know?

- The integrated circuit was first conceived by Geoffrey W. A. Dummer (British Ministry of Defense) and published on May 7th, 1952. He unsuccessfully attempted to build such a circuit in 1956.

- The IC was first realized by Jack Kilby (Texas Instruments) and Robert Noyce (Fairchild Semiconductor) around the same time.

- Kilby built a working prototype by Sept. 1958, and TI filed a patent on Feb. 6th, 1959

- Robert Noyce came up with his idea for an integrated circuit ~6 months after Kilby. His invention solved the problem of interconnecting the components by adding a metal layer

- Knowing that TI had already filed a patent on something similar, Fairchild wrote out a highly detailed application, hoping that it wouldn't infringe on TI 's similar device.

- All that detail paid off. On April 25, 1961, the patent office awarded the first patent for an integrated circuit to Robert Noyce while Kilby's application was still being analyzed. Today, both men are acknowledged as having independently conceived of the idea.

- Noyce went on to be a co-founder of Intel.

- Kilby was jointly awarded the Nobel Prize in Physics in 2000.

Source: nobelprize.org, pbs.org

Geoffrey Dummer

Jack Kilby

Robert Noyce