Thermal Transport in Layered Materials, Devices, and Systems

A. Gabourie, A. Sood, E. Yalon, Ç. Köroğlu, M. Chen, M. Muñoz Rojo, S. Vaziri, S. Suryavanshi, E. Pop

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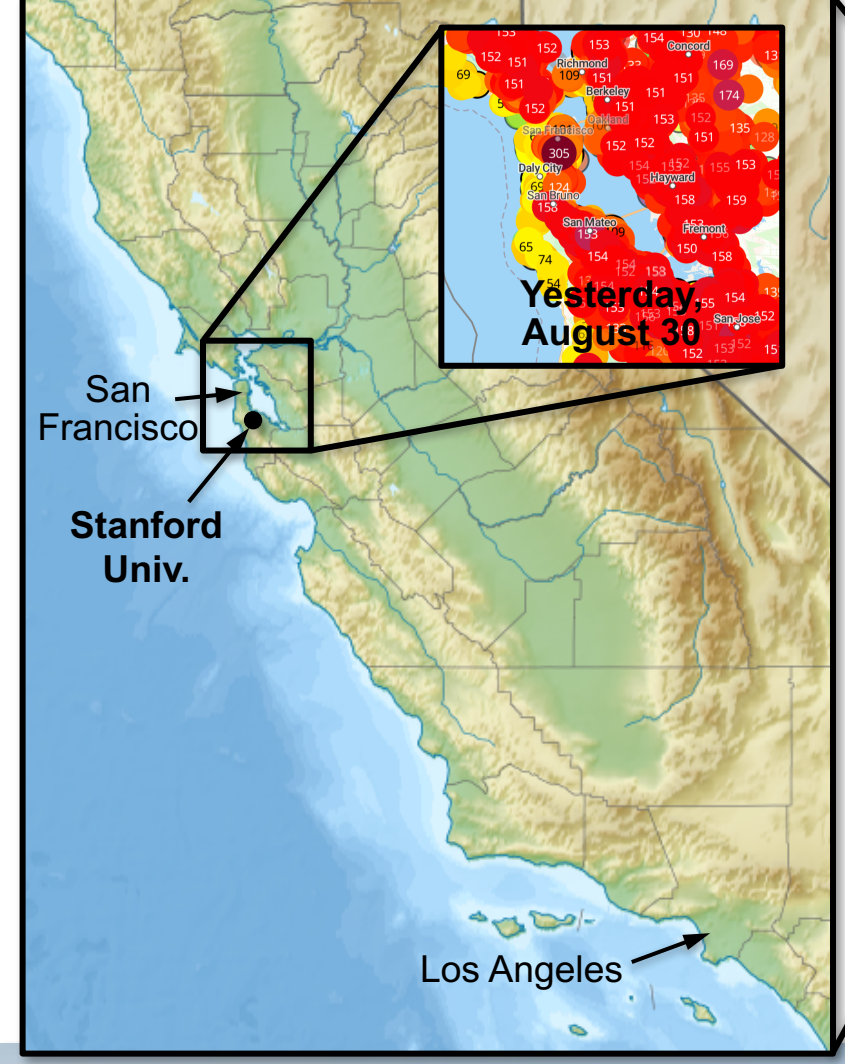
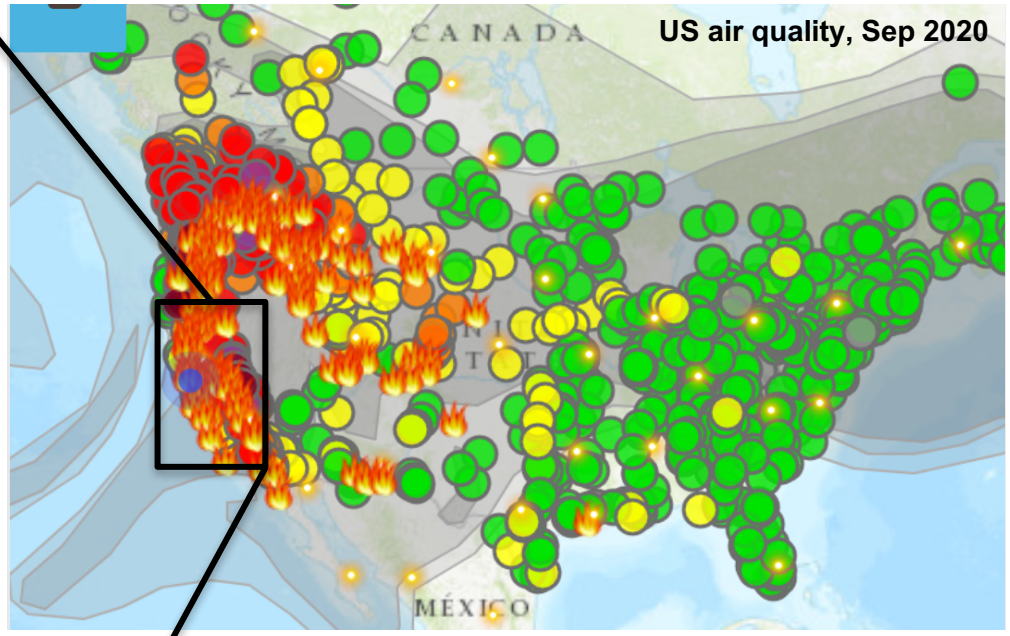
SLAC, SystemX Alliance, Precourt Institute for Energy, Stanford University

http://poplab.stanford.edu
http://2d.stanford.edu
@profericpop


Yesterday,
August 30
San Francisco
Stanford Univ.
Los Angeles


US air quality, Sep 2020
CANADA
MÉXICO


Golden Gate, Sep 2020

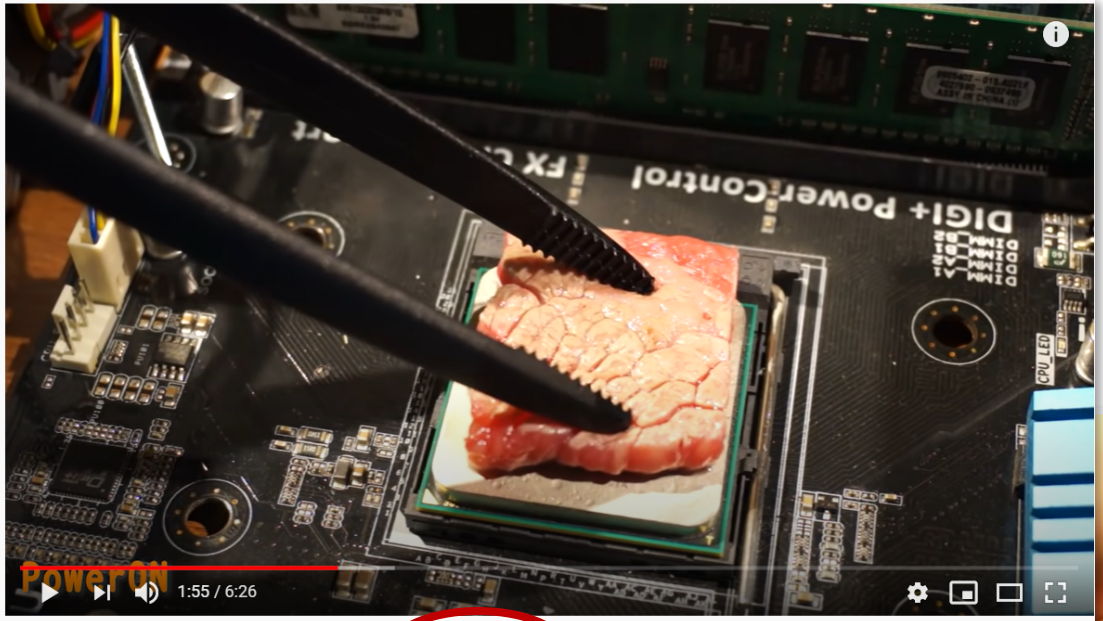

San Francisco, Sep 2020


Stanford, not during the apocalypse

Outline

- **Energy problems in electronics**
- 2D materials for 3D integration
- Fundamental thermal properties of 2D materials
- Devices & systems with 2D and layered materials
- Acknowledgements

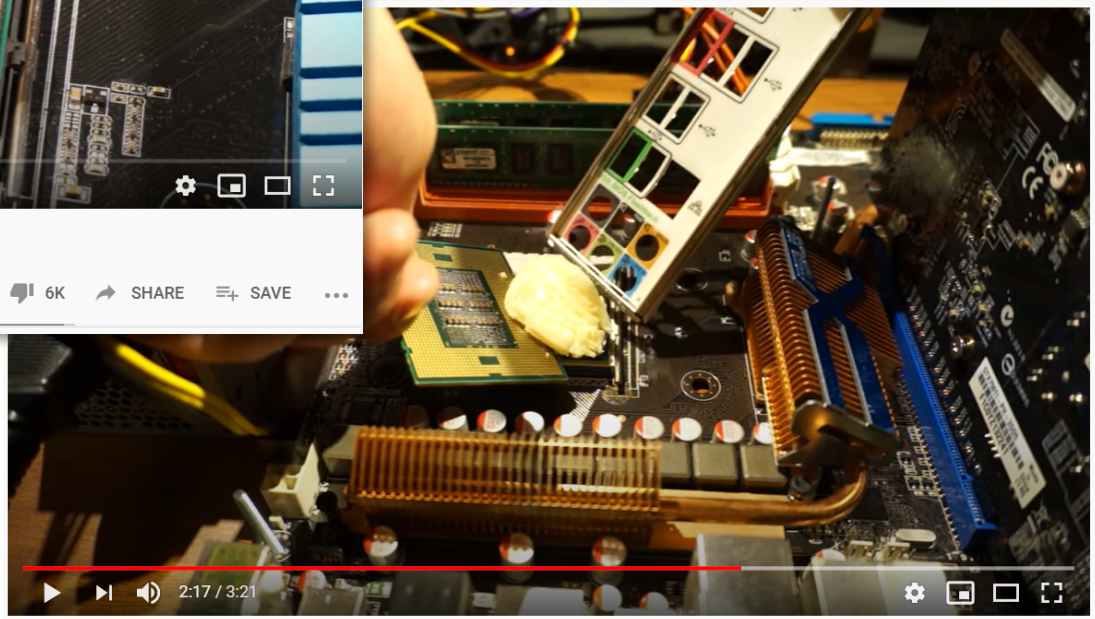
Electronics Use (and Waste) Much Power



CPUで焼肉してみた！ BBQ on AMD CPU (Meatsink)

2,615,425 views • Mar 1, 2020

103K 6K SHARE SAVE



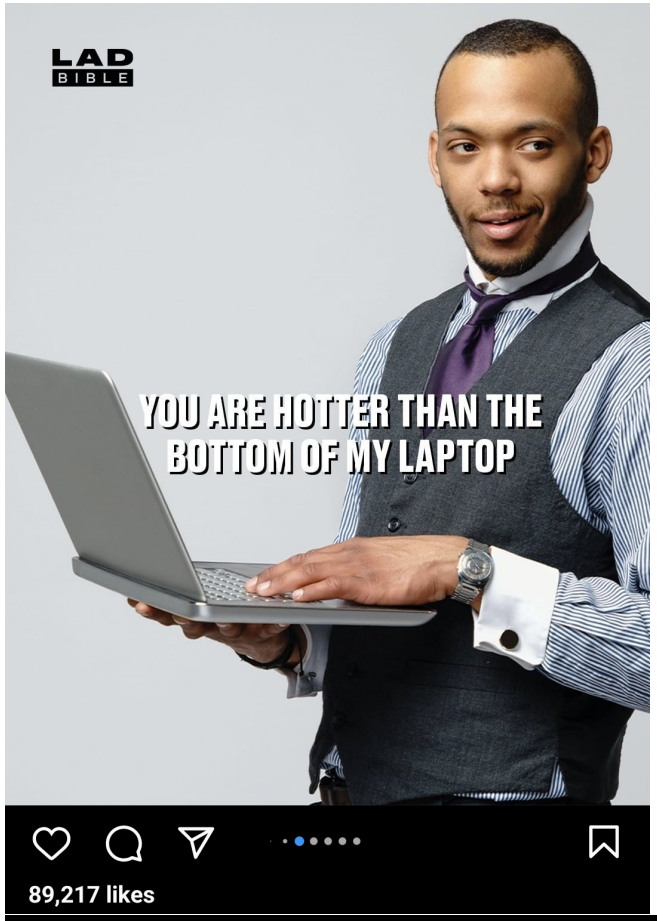
Cooking Pancake on AMD CPU!! CPUでホットケーキを作ってみた！

27,705 views • Mar 14, 2020

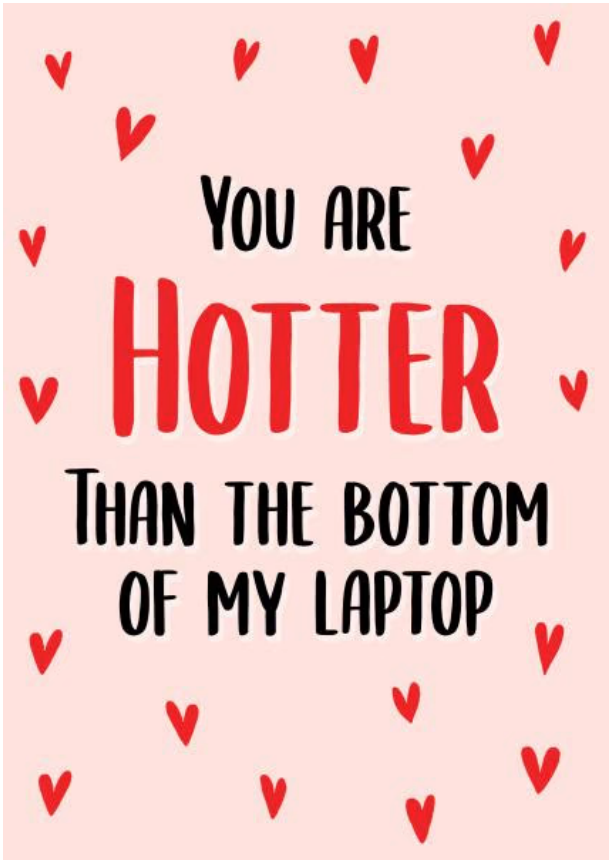
924 35 SHARE SAVE

https://www.youtube.com/c/MerryNightmare7710

Electronics Use (and Waste) Much Power

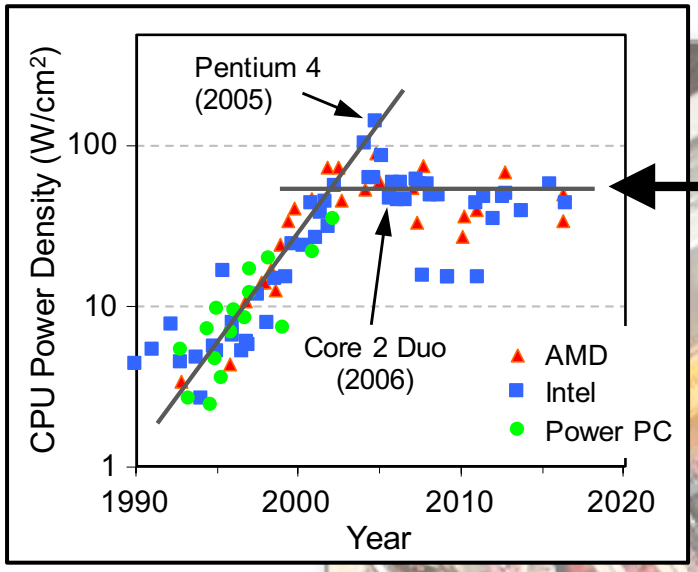


These are the most cringe-worthy chat up lines submitted and voted for by Brits on Thortful.com, with “You are hotter than the bottom of my laptop” taking the top spot as the cheesiest of them all.



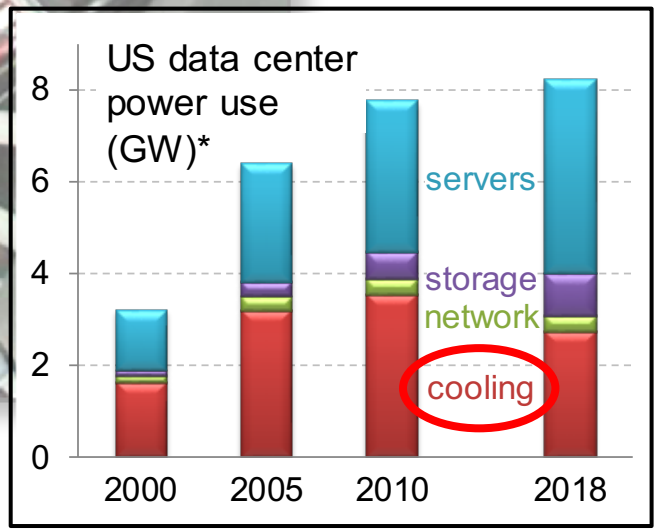
Electronics Use (and Waste) Much Power

E. Pop, *Nano Research* 3, 147 (2010)
Energy in Electronics, EE 323



Electronics, limited by power & heat since 2005!

Koomey (2008)
Shehabi et al. (2018)



Calibrating: 1 GW ~ 1 nuclear power plant
12 GW ~ all electricity used by Argentina

*World-Wide about 24 GW

Electronics Use (and Waste) Much Power

Excess Heat = High Cooling Costs

How did we get here?

Moore's Law

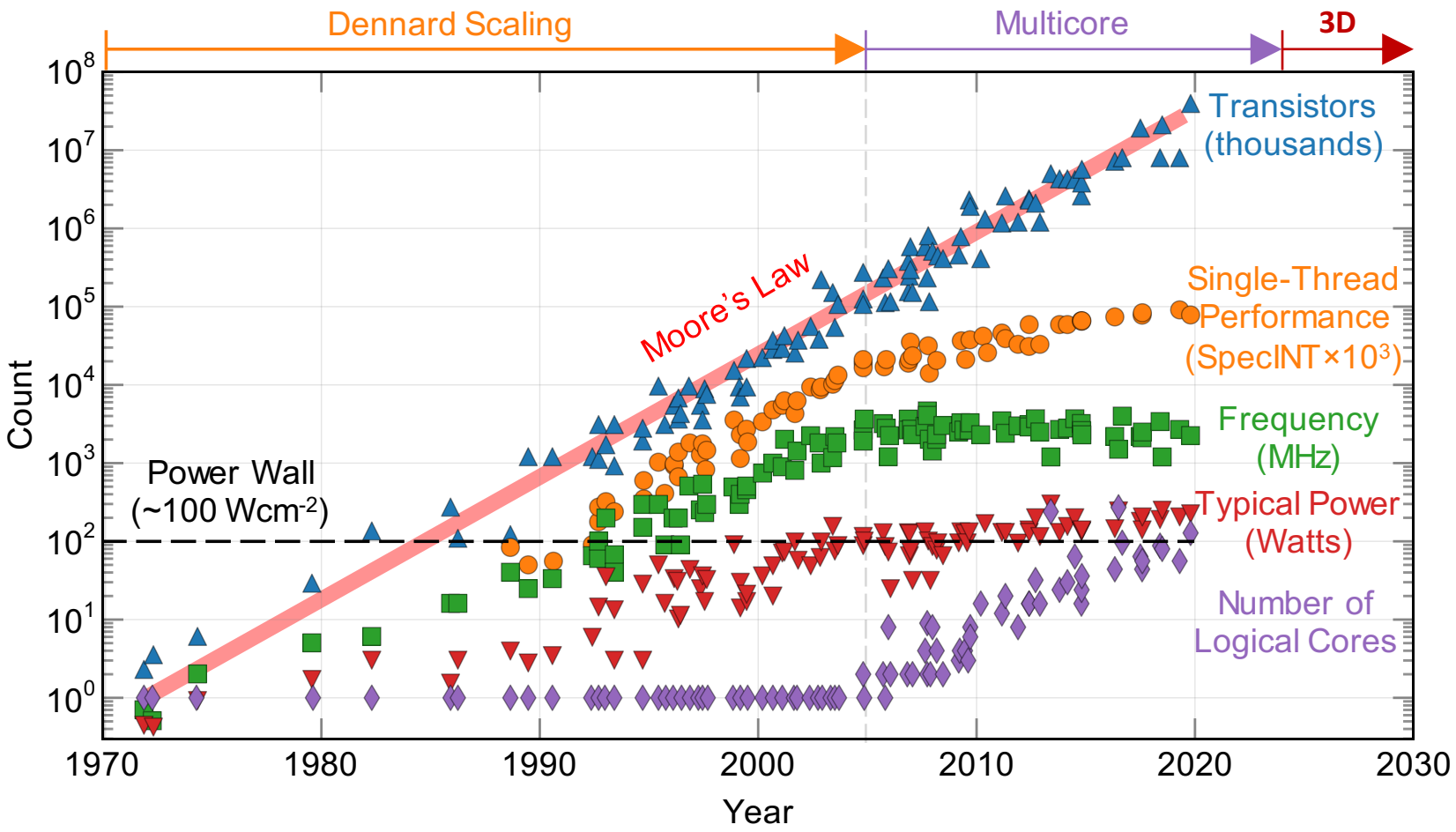


Figure by Alex Gabourie (Pop Lab). Original data collected by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten. Data from 2010 through 2019 collected by K. Rupp.

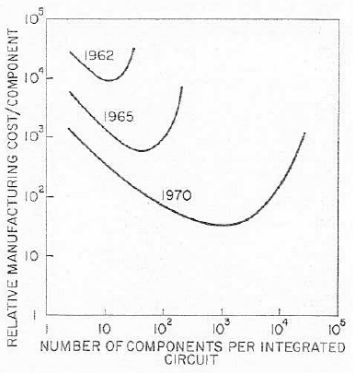
Moore's Law vs. Dennard's Law

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

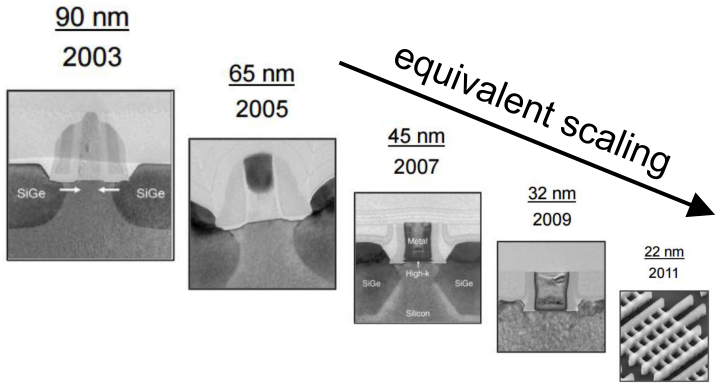
Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.



Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions

ROBERT H. DENNARD, MEMBER, IEEE, FRITZ H. GAENSSLEN, HWA-NIEN YU, MEMBER, IEEE, V. LEO RIDEOUT, MEMBER, IEEE, ERNEST BASSOUS, AND ANDRE R. LEBLANC, MEMBER, IEEE

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1



Moore: complexity vs. cost

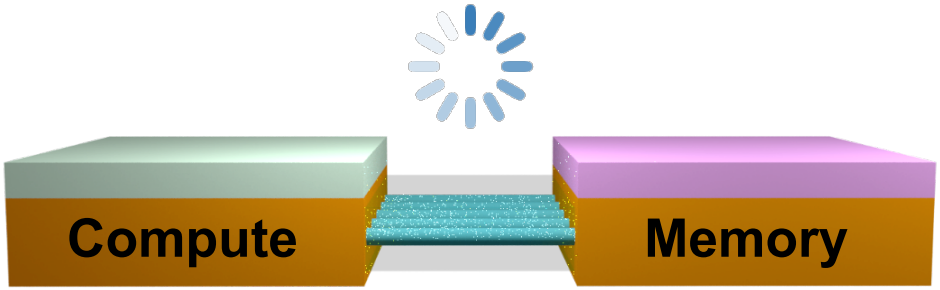
not ending, going 3D…

Dennard: geometric scaling

~ ending at atom-scale

The Problem with Computing Today

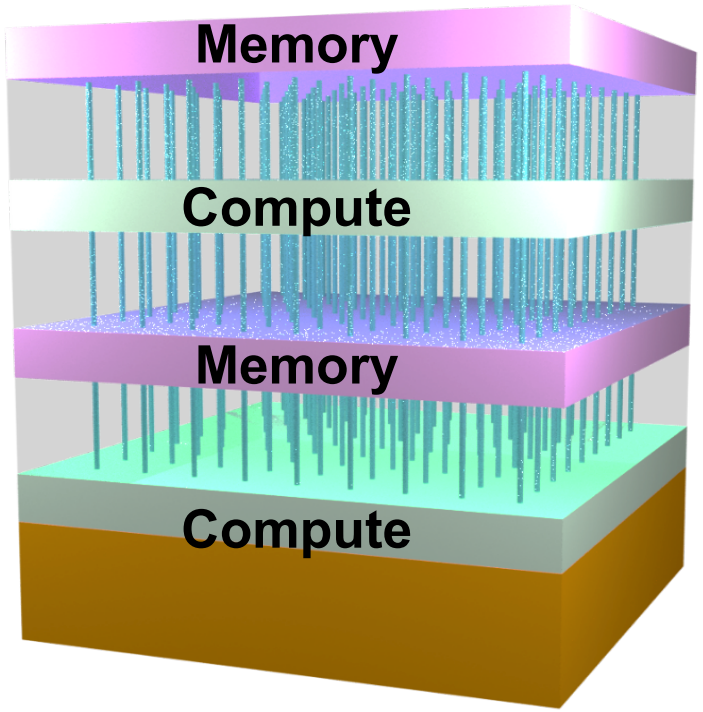
M. Aly, […], K. Goodson, C. Kozyrakis, E. Pop, J. Rabaey, C. Re, H.-S.P. Wong, S. Mitra, *IEEE Computer* (2015)



Today: Separate compute & memory chips

Very energy inefficient

Also today: data centers ~10 GW and personal tech >15 GW in US*



graphics courtesy C.-H. Wang

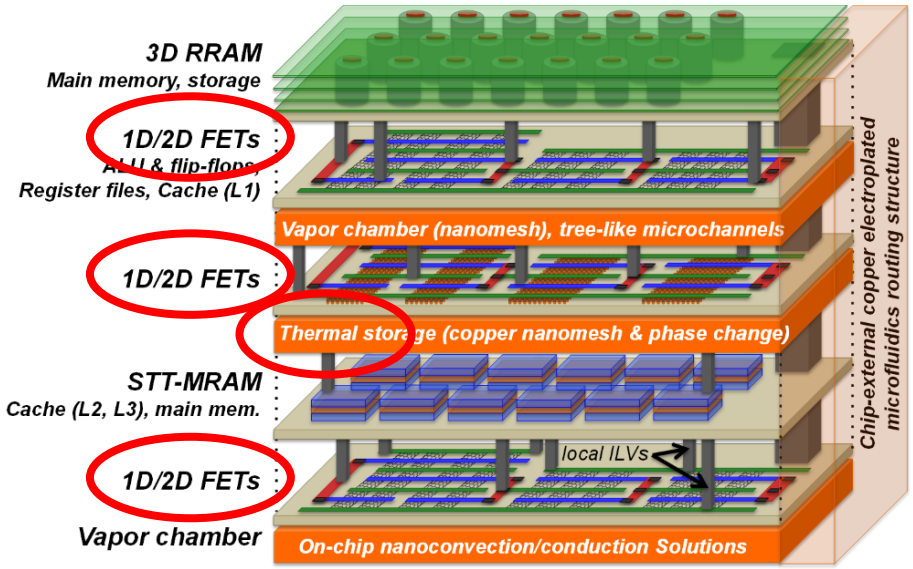
Future: 3D integrated logic and memory

10 to 1000x more energy-efficient

* N. Jones, *Nature* 561, 163 (2018)

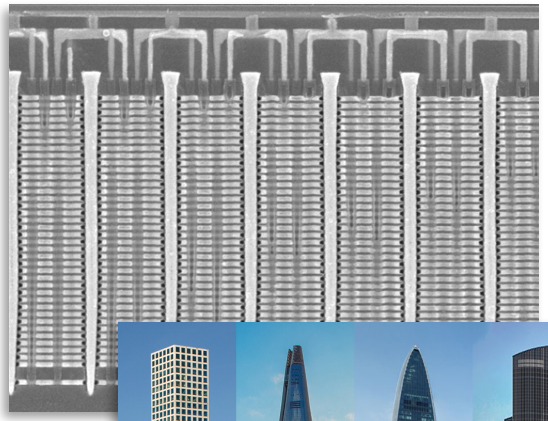
3D Is Driving our 2D and Thermal Work

- **Can some new materials replace silicon in 3D?**
- Short answer: NOT replace, BUT **complement 3D heterogeneous integration**



M. Aly et al., *IEEE Computer* **48**, 24 (2015)

32-layer vertical Flash memory



~200 layers today

- Silicon-CMOS compatibility is required
- For back-end of the line (BEOL) this usually means **< 500 °C for < 2 hours**

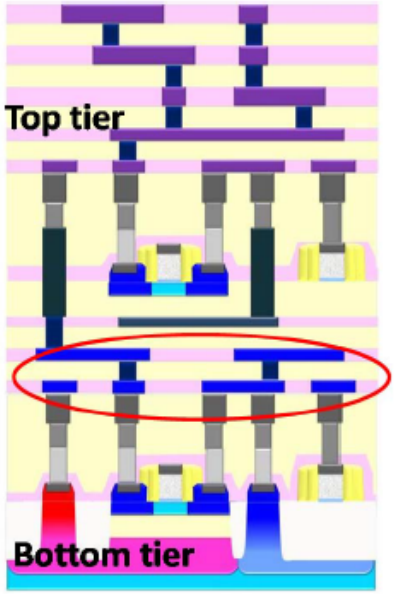
Historical Sidenote: 3D at Stanford in 1982

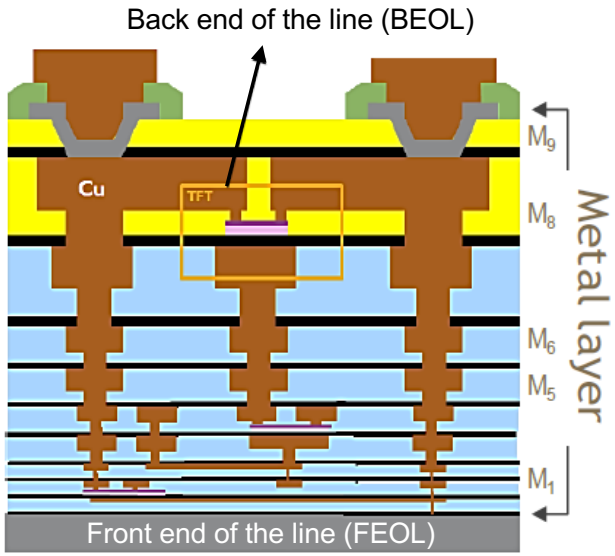

CIS Newsletter

Center for Integrated Systems ☆ ☆ ☆ Stanford University ☆ ☆ ☆ Stanford, California U.S.A.

- 3D "high-rise" electronics pursued at least since early 1980s
- Why didn't this work?
  - Laser-crystallized amorphous silicon
  - Silicon scaled just fine below 1 μm

In 3D, Thermal Properties Are Very Important





courtesy: IMEC

- **High power density** → FEOL cooking BEOL, logic cooking memory, …
- 3D integration → many **interfaces** and (usually) **low-*K**** dielectrics
- Performance (I_{on}) degrades with ↑T... leakage (I_{off}) and reliability ~exp(T)

*Low-k (permittivity) and low-κ (thermal conductivity)

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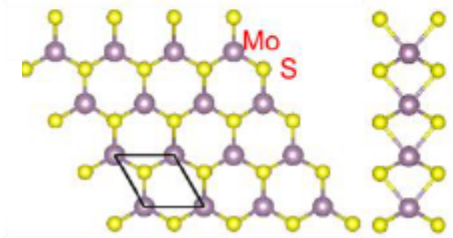
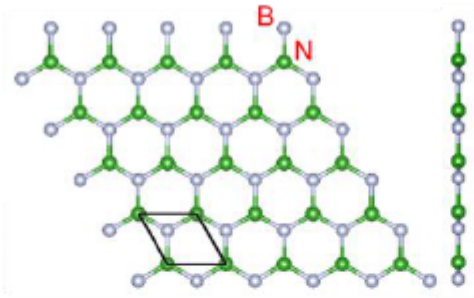
What Are 2-Dimensional (2D) Materials?

Transition Metal Dichalcogenides (TMDs like MoS_2)



~6 Å

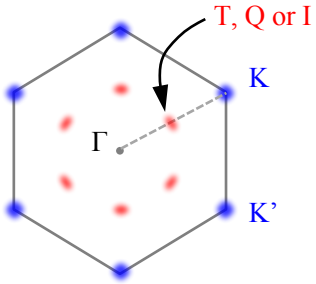
Hexagonal Boron Nitride (insulator)



- **One-to-three atom thick** materials… metals, insulators, **semiconductors**
- Practical band gaps (~2 eV) + electron & hole mobilities ~ 100 $cm^2V^{-1}s^{-1}$ in atomically thin semiconductors, better than silicon in sub-1 nm thin films
- Van der Waals bonds → **heterogeneous integration** w/out lattice matching (possible at low-temperature)

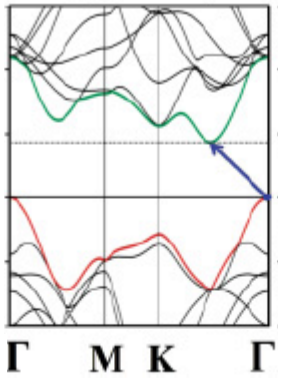
Ex: Electron & Phonon Bands of 2D MoS_2

Electrons:

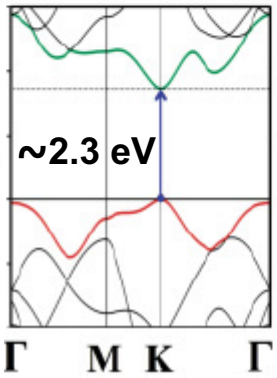


K = 2x degenerate
Q = 6x degenerate (along T line)

bulk MoS_2 (indirect gap)

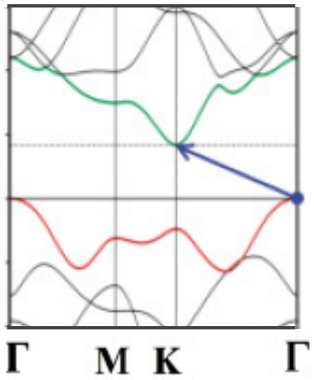


1L MoS_2 (direct gap)



optical gap (1.8 eV) includes exciton effect

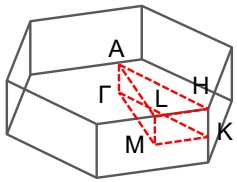
1L MoS_2 (tensile strain)

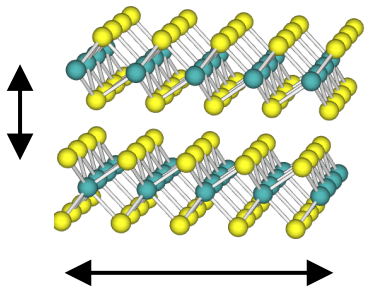


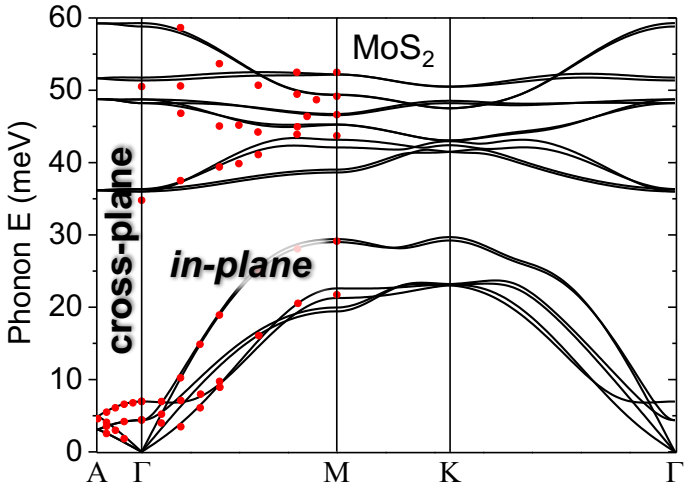
(less is known about strain)

Yun, Phys. Rev. B (2012)

Phonons:



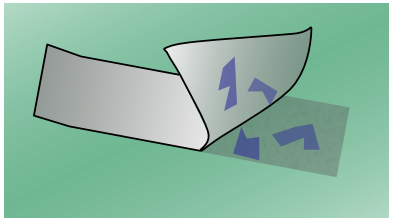




Very anisotropic!

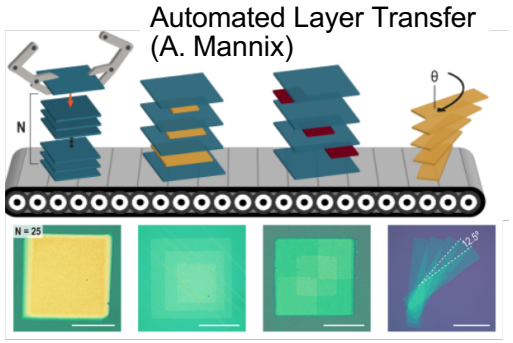
Huge Advances in 2D Synthesis

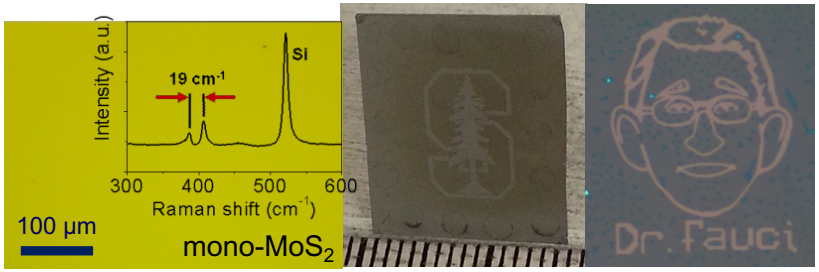
Then:



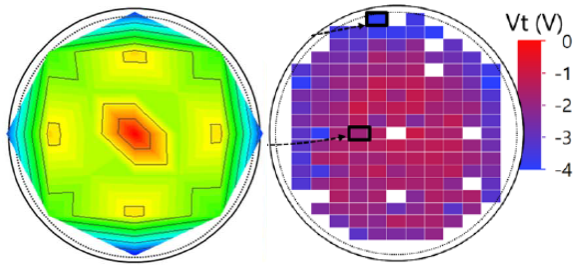
random ~10 μm pieces (2004)

Now:



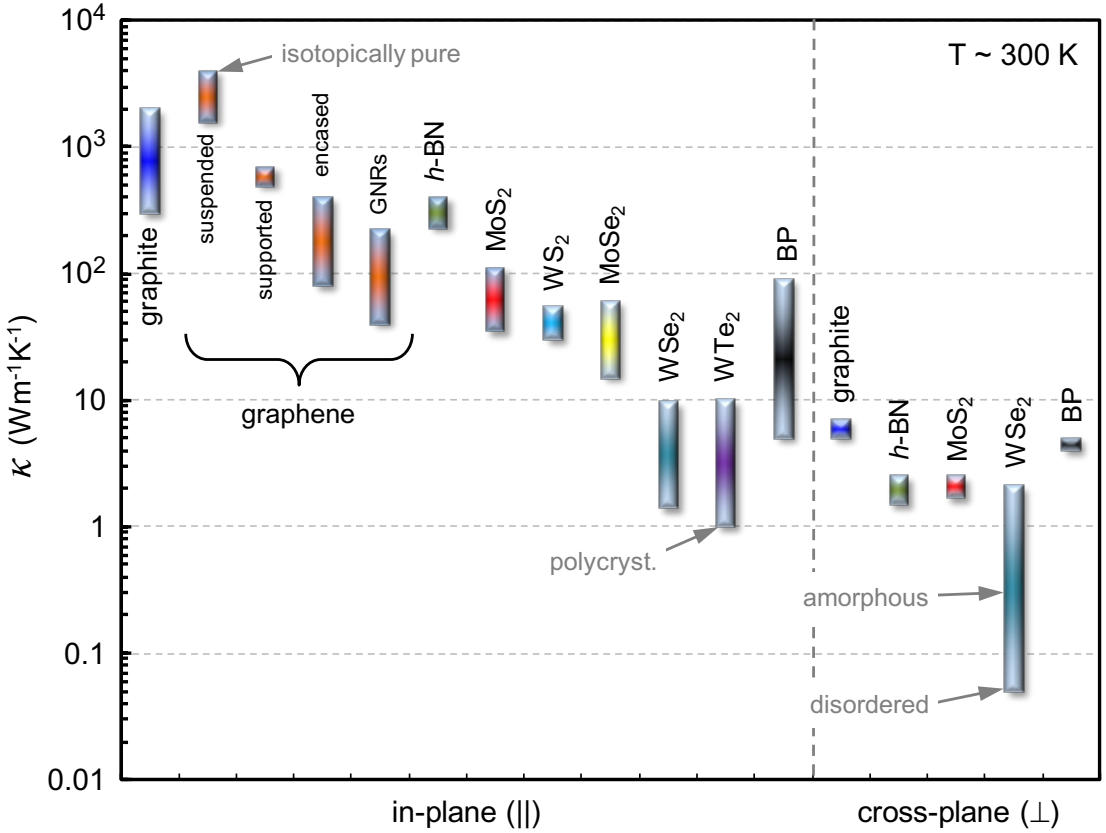


25-100 mm CVD/CVT growth at Stanford



300 mm wafer scale at IMEC

Thermal Properties of 2D Materials



$$Q'' = -\kappa \nabla T$$

heat flux

thermal conductivity

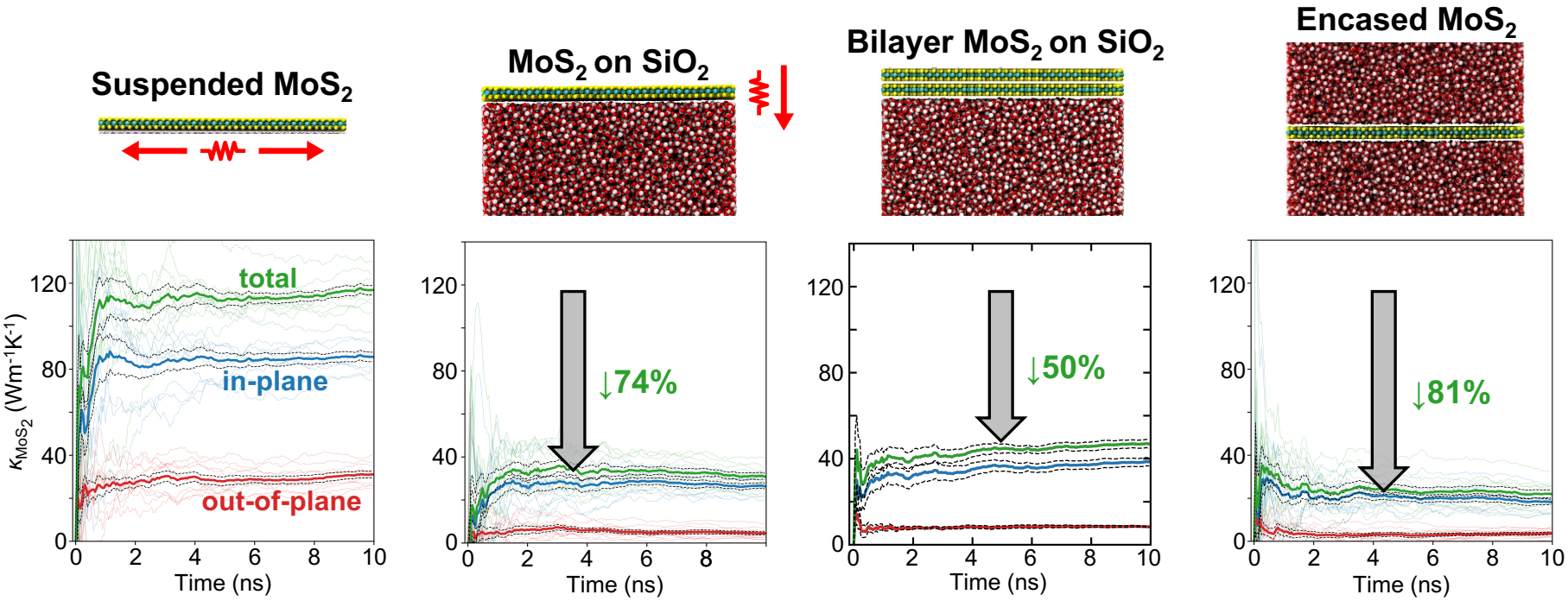
T gradient

- **Huge thermal anisotropy** of 2D materials: in-plane $\kappa_{||}$ >> cross-plane $\kappa_{\perp}$
- Can thermal anisotropy be leveraged for **heat blocking and spreading**?
- Thermal properties must be understood in both **3D systems and devices**

* E. Pop, V. Varshney, A. Roy, *MRS Bull.* 37, 1273 (2012); Figure courtesy Z. Li and A. Gabourie (Pop Lab)

Thermal κ of MoS_2 on SiO_2 Decreases

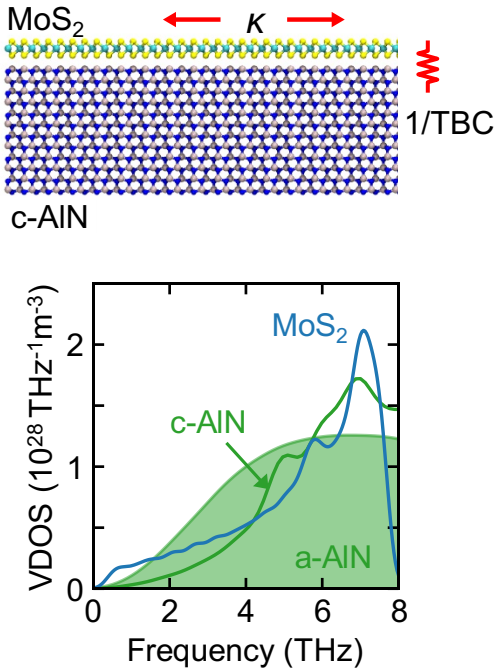
A. Gabourie, S. Suryavanshi, A.B. Farimani, E. Pop, *2D Materials,* **8**, 011001 (2021)

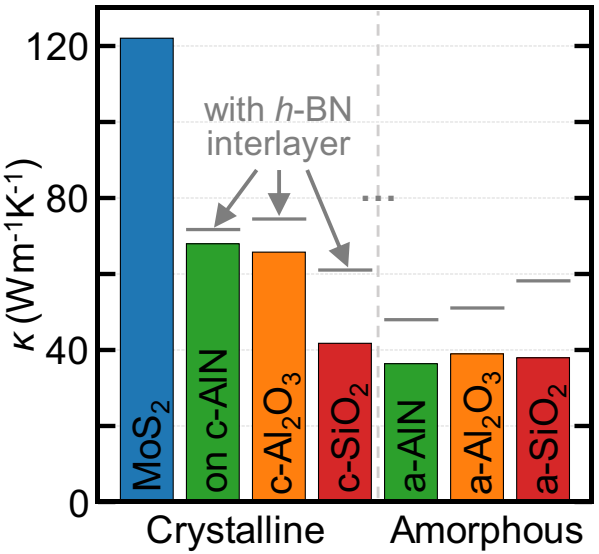


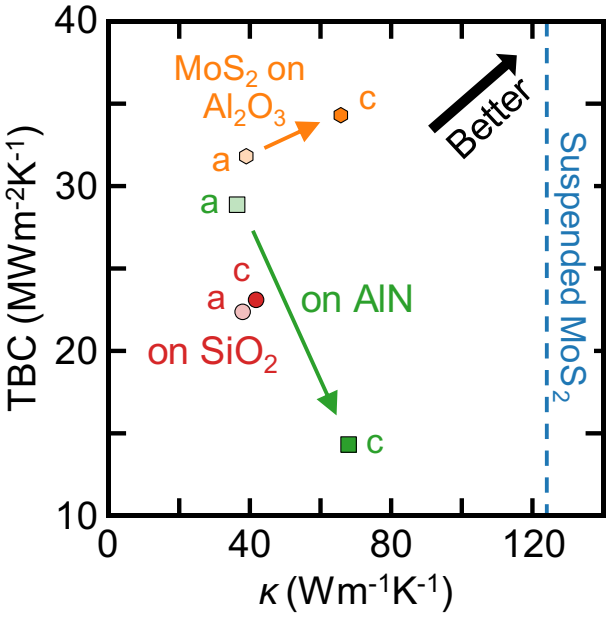
- Suspended, isolated MoS_2 thermal κ is comparable to κ of doped silicon
- SiO_2-**supported or encased** MoS_2 thermal κ **decreases** 50 to 80%
- Why? Scattering with **remote phonons** (but less for bilayers)
- This is important for sub-150 nm transistors (heat flow to contacts)

Thermal κ of MoS_2 on Other Substrates

A. Gabourie, Ç. Köroğlu, E. Pop, *J. Appl. Phys.* 131, 195103 (2022)



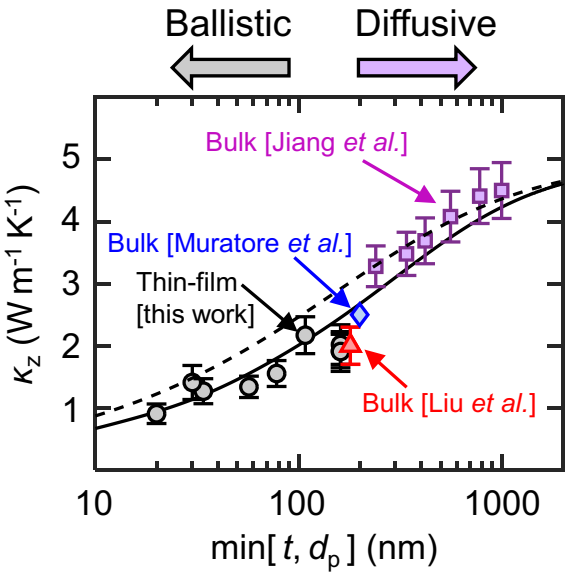


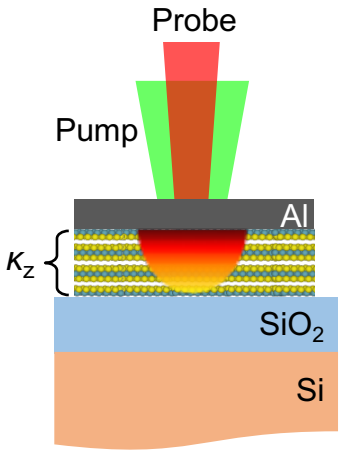


- Thermal κ of MoS_2 **best preserved on c-AlN, c-Al_2O_3, or *h*-BN**
- Why? Long-wavelength vibrational density of states (< 2 THz)
- Thermal boundary conductance **(TBC) scales differently** → tuning?

Cross-Plane Thermal κ_z of MoS_2

A. Sood, F. Xiong, S. Chen, […], D. Donadio, K. Goodson, E. Pop, *Nano Lett.* **19**, 2434 (2019)

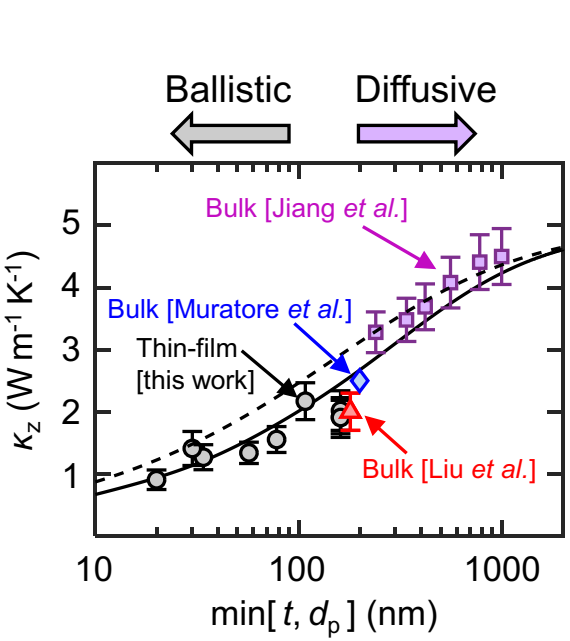


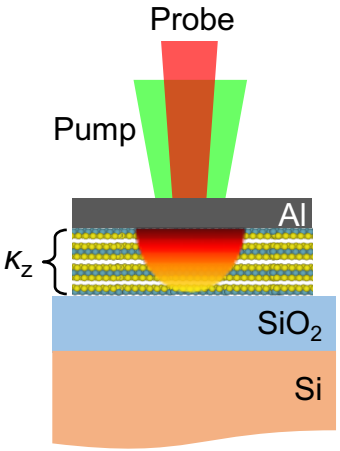


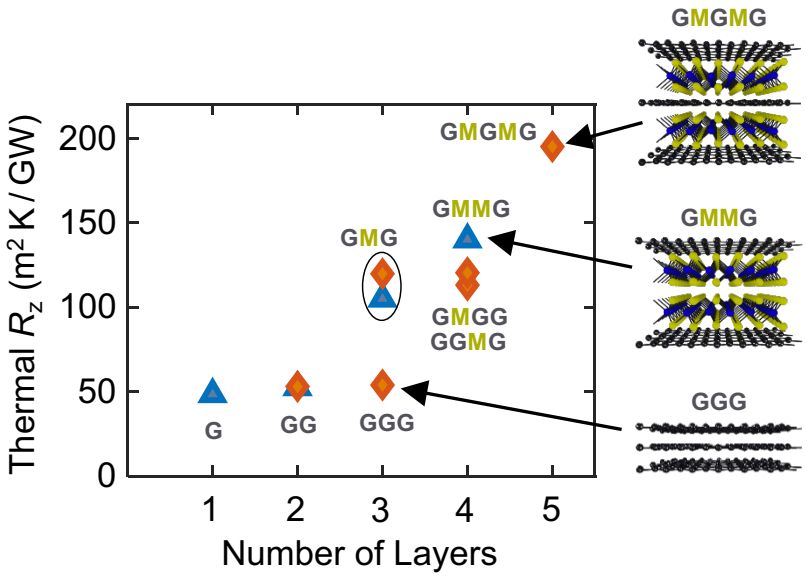
- Cross-plane **thermal κ_z scales with thickness, *t*** (ballistic to diffusive)
- Phonon mean free paths MFP > 200 nm carry ~50% of the heat

Cross-Plane Thermal κ_z of MoS_2

A. Sood, F. Xiong, S. Chen, […], D. Donadio, K. Goodson, E. Pop, *Nano Lett.* **19**, 2434 (2019)
A. Sood, C. Sievers, […], D. Donadio, K. Goodson, E. Pop, *ACS Nano* **15**, 19503 (2021)







- Cross-plane **thermal κ_z scales with thickness, *t*** (ballistic to diffusive)
- Phonon mean free paths MFP > 200 nm carry ~50% of the heat
- Thermal κ_z **lower for Graphene-MoS_2 superlattices** (e.g. **GMGMG**)

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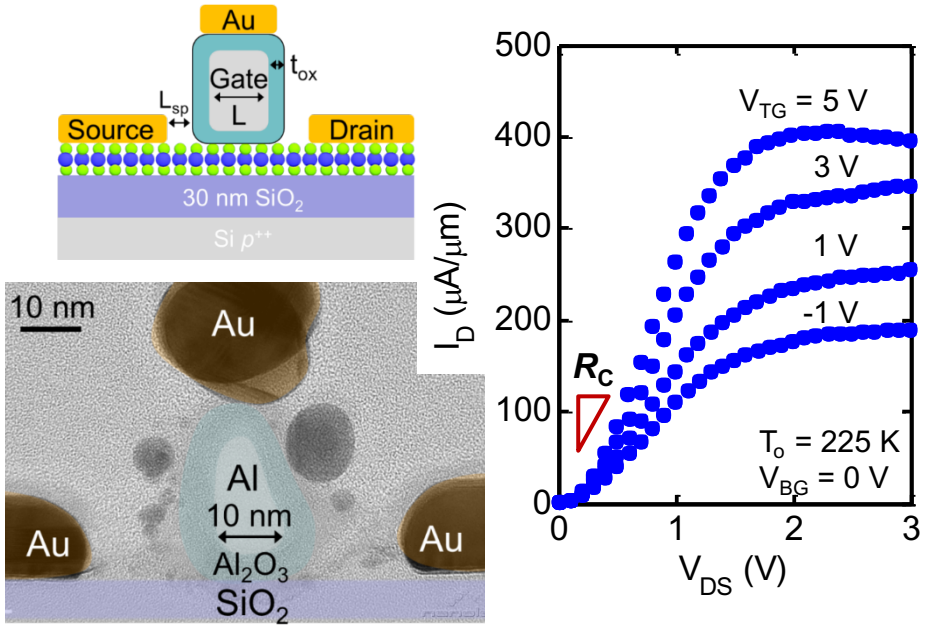
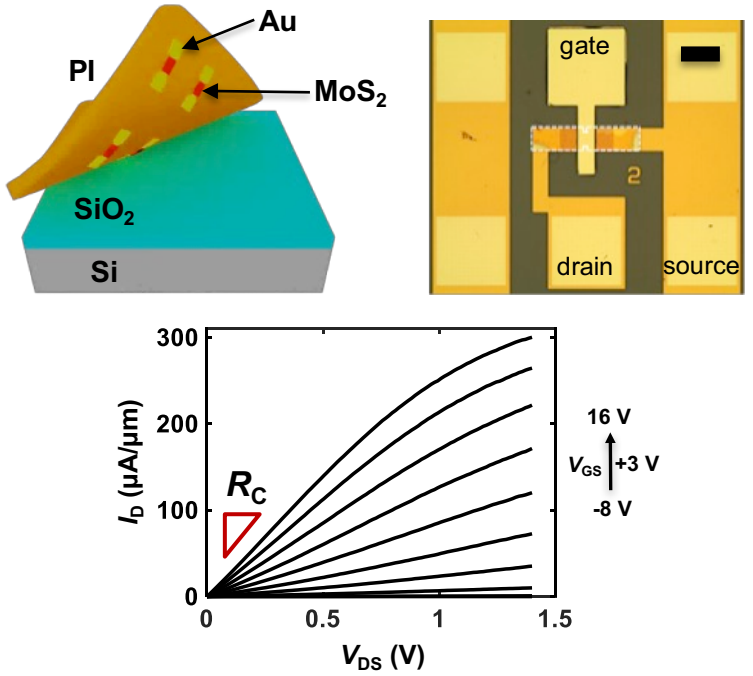
- **Acknowledgements**

Wanted: 2D Transistors for 3D Integration

C. English, K. Smithe, R.L. Xu, E. Pop, *IEDM* (2016)



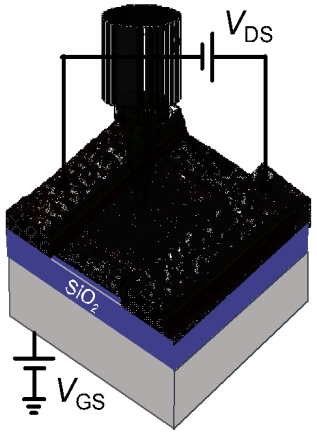
A. Daus, S. Vaziri, […], E. Pop, *Nature Elec.* **4**, 495 (2021)

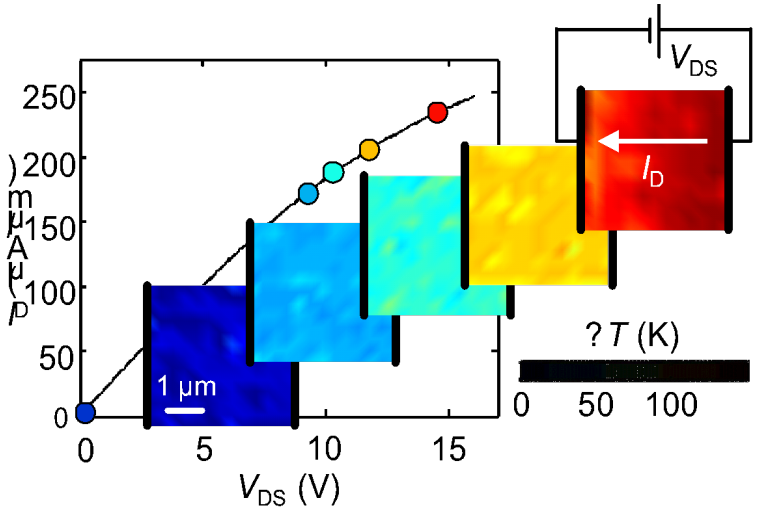


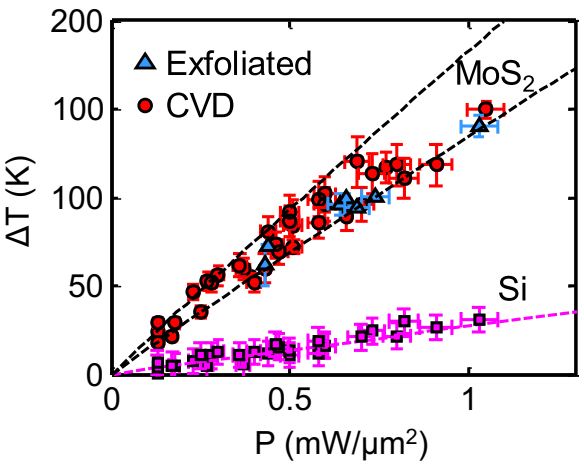
- 10 nm-scale MoS_2 transistors **on rigid SiO_2/silicon**
- Then-record $I_D \approx 400$ μA/μm
- 100 nm-scale MoS_2 transistors **on flexible polyimide (PI)**
- Record $I_D \approx 300$ to 470 μA/μm
- Limited by **contact resistance (R_C)**, **gate stack**, and **self-heating**

Energy Dissipation in MoS_2 Transistors

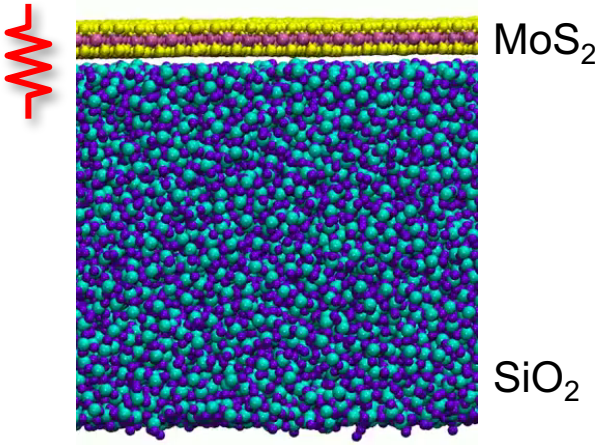
E. Yalon, C. McClellan, K. Smithe, R.L. Xu, M. Munoz Rojo, S. Suryavanshi […] E. Pop, *Nano Letters* **17**, 3429 (2017)
E. Yalon, Ö.B. Aslan, K. Smithe, C. McClellan, S. Suryavanshi, […], E. Pop, *ACS Appl. Mater. Interfaces* **9**, 43013 (2017)







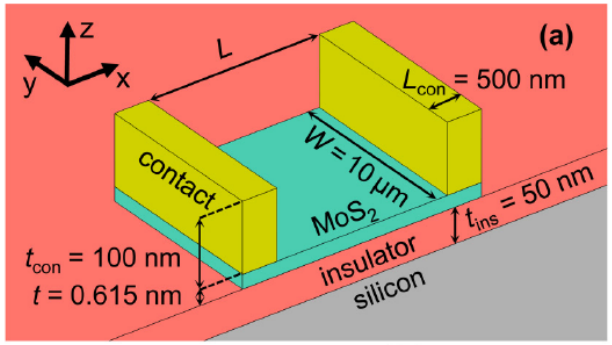
- **First measurement** of power dissipation in large MoS_2 transistors (Raman and SThM)
- They get hot **(>200°C)** during operation!
- Why? Poor **thermal boundary conductance** (TBC) of MoS_2-SiO_2 van der Waals interface

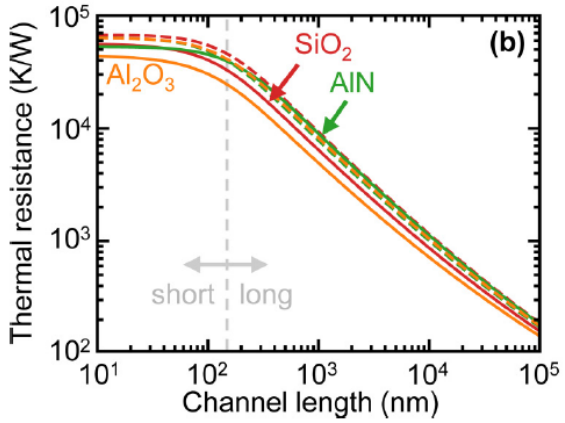


work of Alex Gabourie

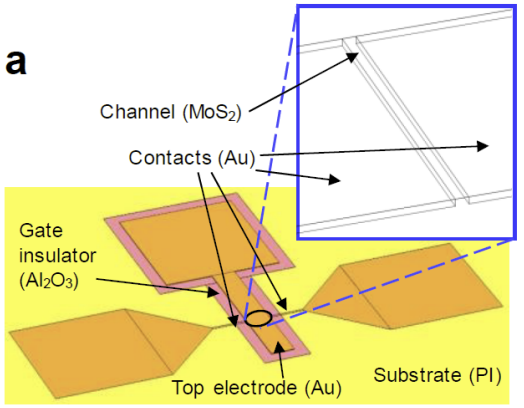
Where Does the Heat Go in Transistors?

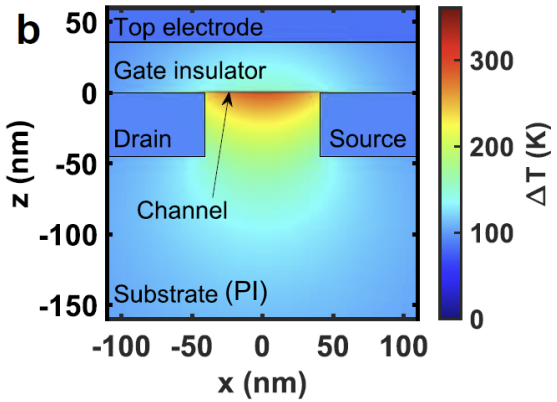
A. Gabourie, Ç. Köroğlu, E. Pop, *J. Appl. Phys.* **131**, 195103 (2022)





A. Daus, S. Vaziri, […], E. Pop, *Nature Elec.* **4**, 495 (2021)





Back-gated 2D transistors:

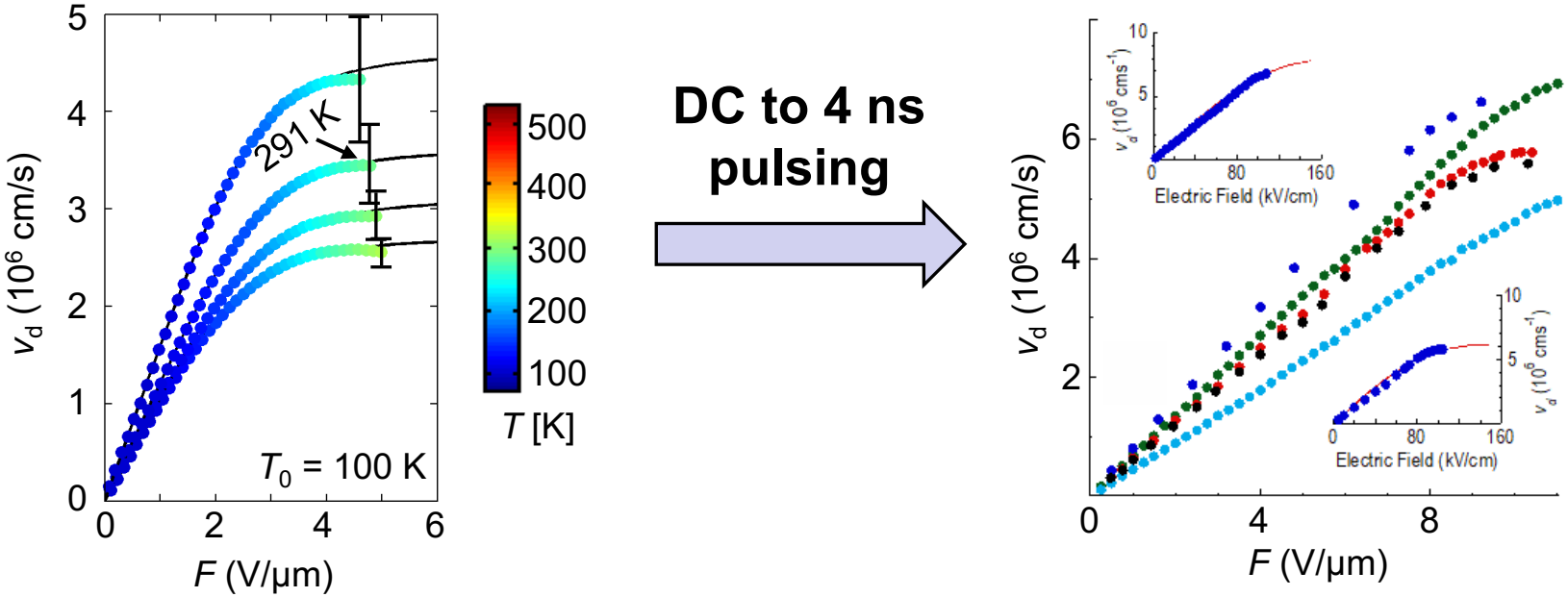
- L > 150 nm, heat flows **to substrate**
- L < 150 nm, heat flows **to contacts**

Dual-gated transistors or on plastics:

- It's complicated
- Ex: heat flow **into gate**, **then** contacts

Can Pulsing Eliminate Self-Heating?

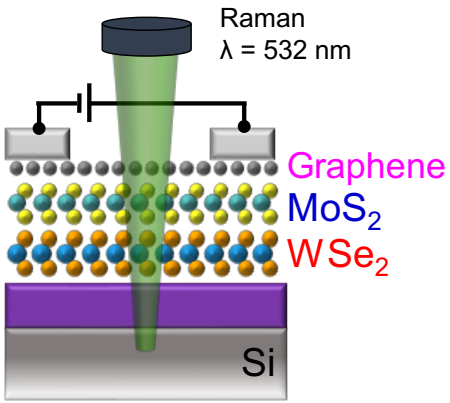
K. Smithe, C. English, S. Suryavanshi, E. Pop, *Nano Letters* **18**, 4516 (2018)
J. Nathawat, K. Smithe, C. English, […], E. Pop, J. Bird, *Phys. Rev. Mater.* **4**, 014002 (2020)

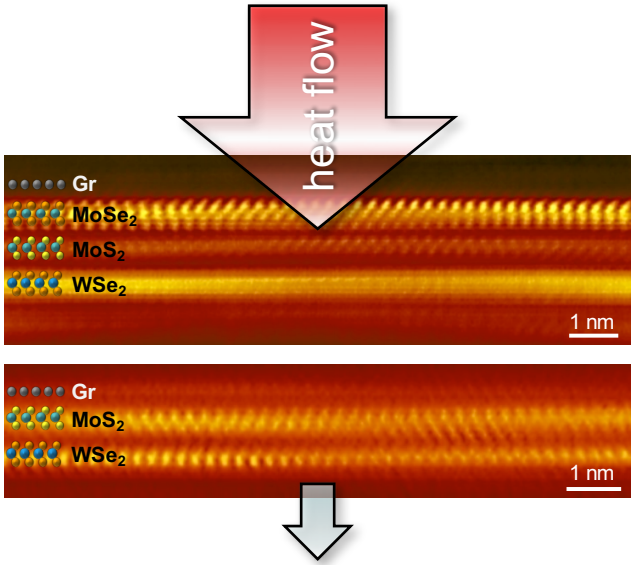


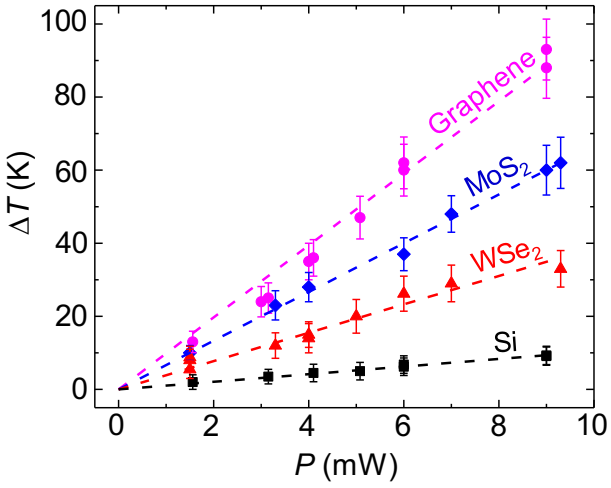
- High current in MoS_2 → Joule heating limits saturation velocity v_{sat} and I_D
- **Ultra-fast pulsed** measurements (< 4 ns) below thermal and (most) charge trapping time constants reduce self-heating
- v_{sat} from 3.4 x 10^6 cm/s to **6 x 10^6 cm/s** → I_D can be **~ 1 mA/μm**
  (with n ~ 10^{13} cm^{-2})

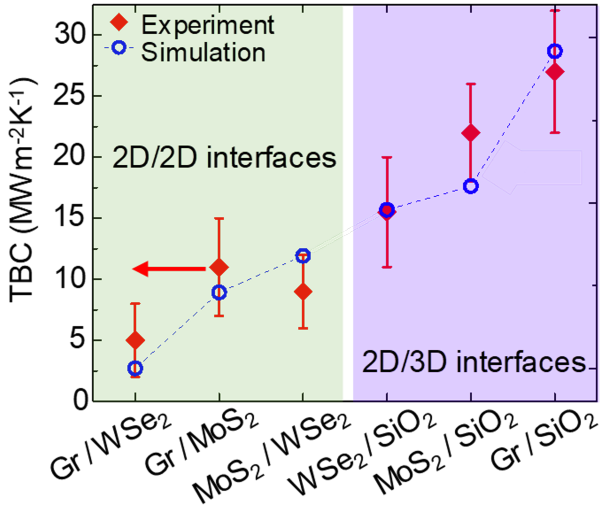
Very Large Cross-Plane Thermal Resistance

S. Vaziri, E. Yalon, M. Munoz Rojo, S. Suryavanshi, C. McClellan, […] E. Pop, *Science Adv.* **5**, eaax1325 (2019)







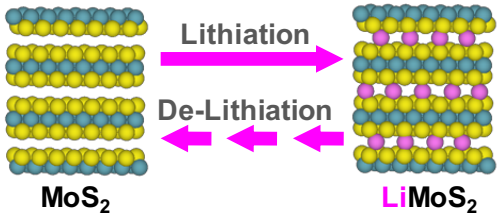


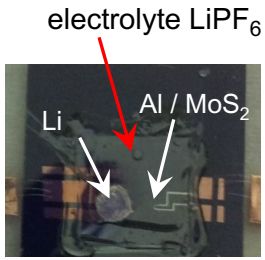
- What if we have multiple, stacked 2D materials?
- Atomic **mass & phonon mismatch** b/w layers
- Raman thermometry with **atomic layer precision**
- Effective thermal $\kappa_{\perp}$ ~ 0.01 $Wm^{-1}K^{-1}$ (< air)

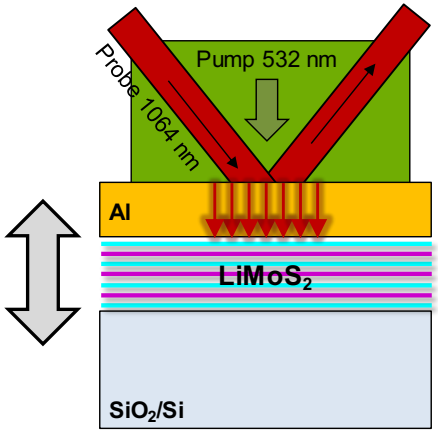
Unusual Application: Thermal Transistor #1

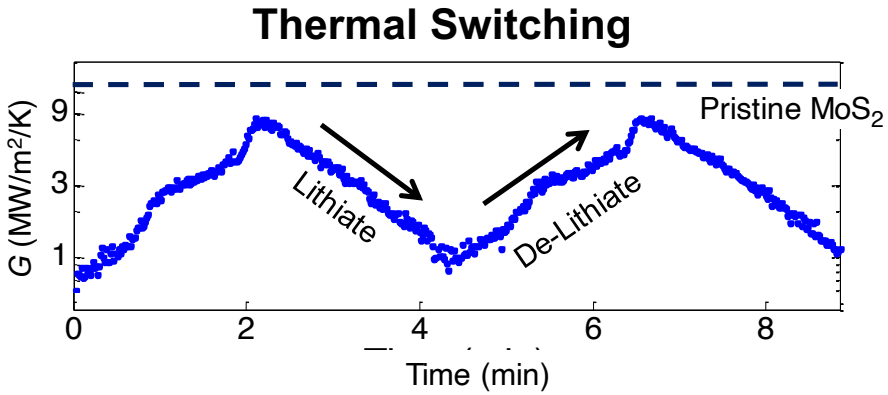
A. Sood, F. Xiong, […], D. Donadio, Y. Cui, E. Pop, K Goodson, *Nature. Comm.* **9**, 4510 (2018)

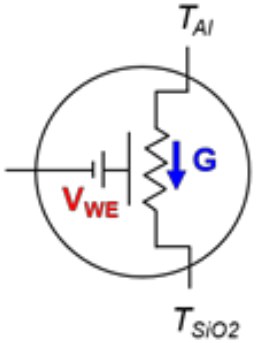
- Use reversible **Li intercalation in MoS_2**
- **Switch heat flow by ~10x** as a thermal transistor → control *T* transients

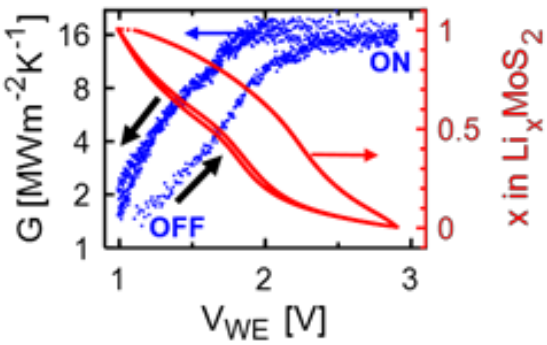










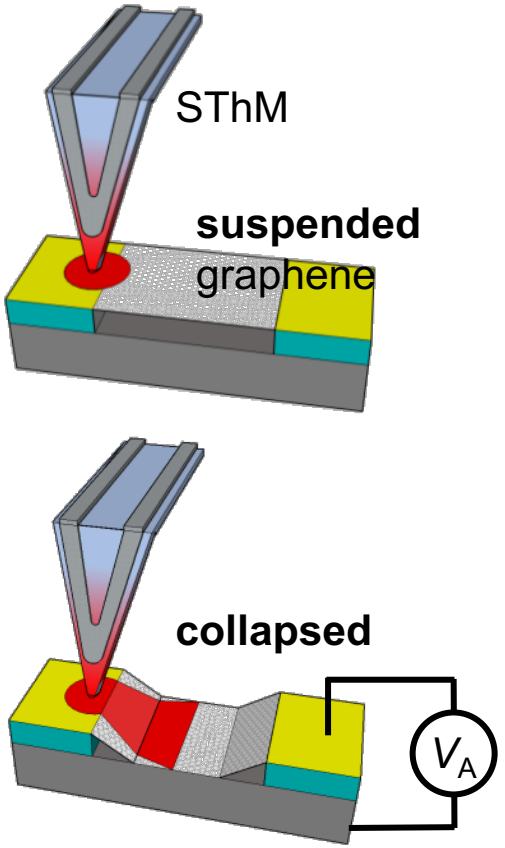


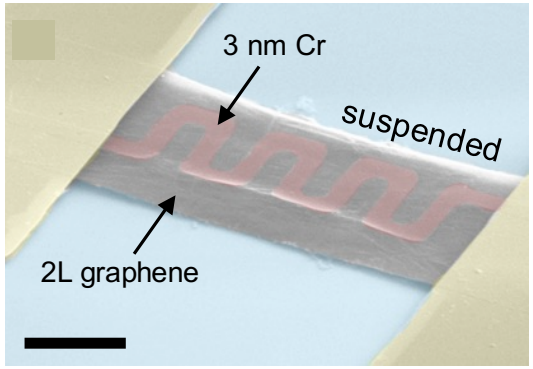
Thermal Transistor On/Off ~10 (meas.)

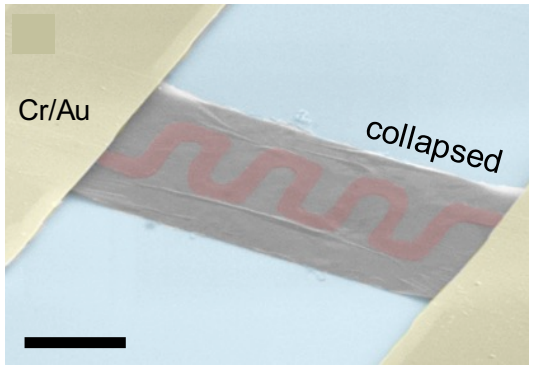
Unusual Application: Thermal Transistor #2

M.E. Chen, M. Muñoz Rojo, F. Lian, J. Koeln, […], A.G. Alleyne, K.E. Goodson, E. Pop, *2D Materials* **8**, 035055 (2021)

- Use switching of **suspended graphene membrane**
- **Much faster thermal switch** (~ns) but lower thermal on/off ratio





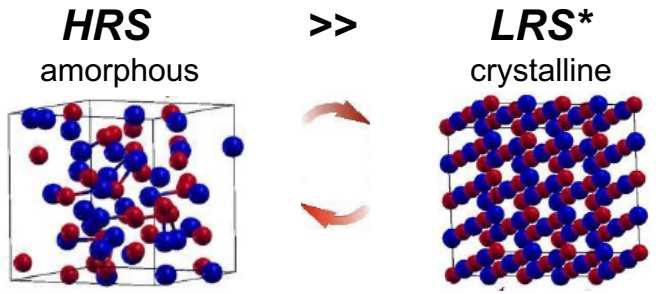


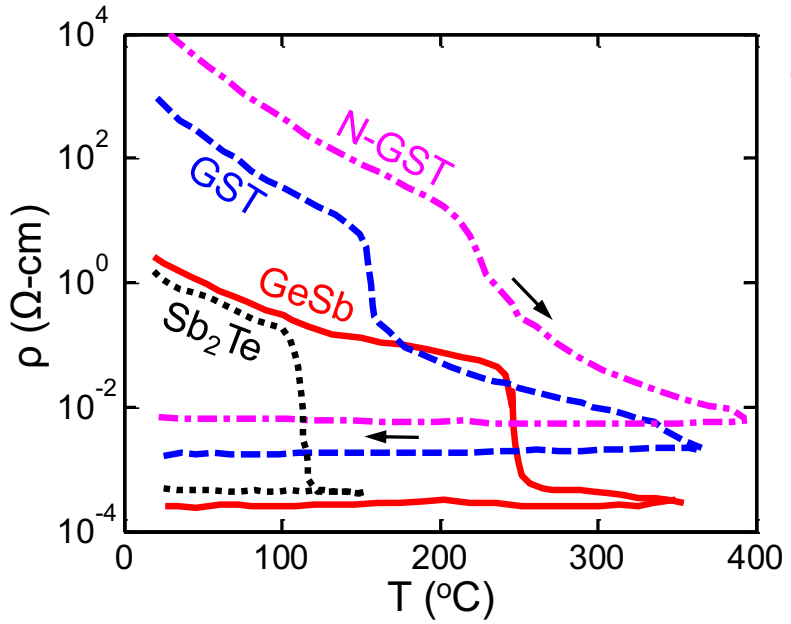
Thermal Transistor On/Off ~ 1.3 (meas.)
up to 2 (theo.)

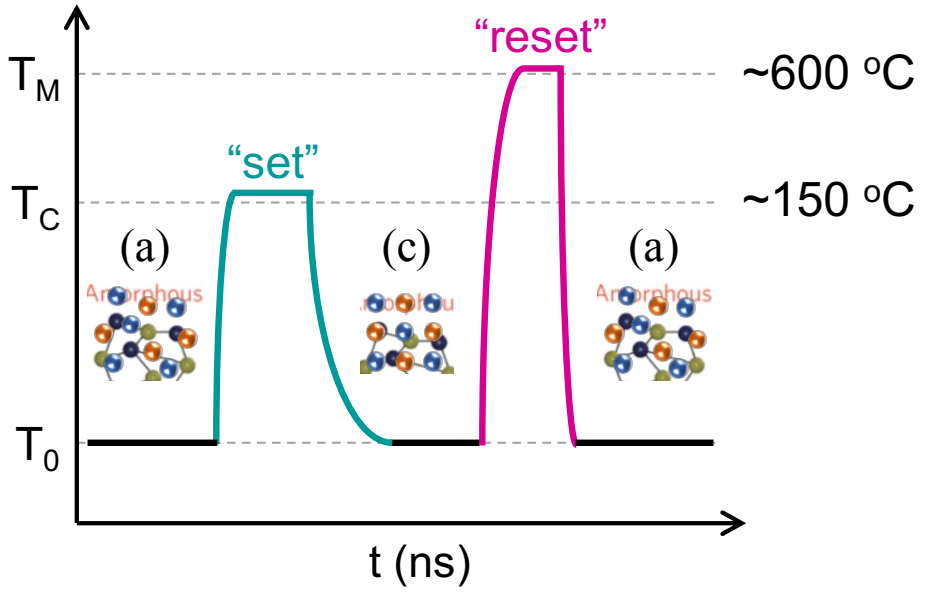
Applications to Phase-Change Memory

F. Xiong, A.D. Liao, D. Estrada, E. Pop, *Science* **332**, 568 (2011)

- Chalcogenides e.g. $Ge_2Sb_2Te_5$ (GST)
- Large resistance change (HRS/LRS)
- Multi-levels for neuromorphic applications
- Reversible phase change induced by **Joule heating (pulsed V or I)**





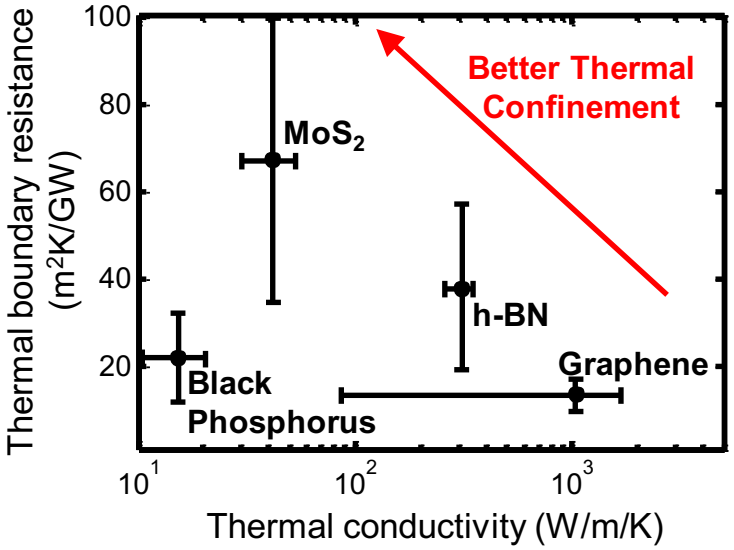


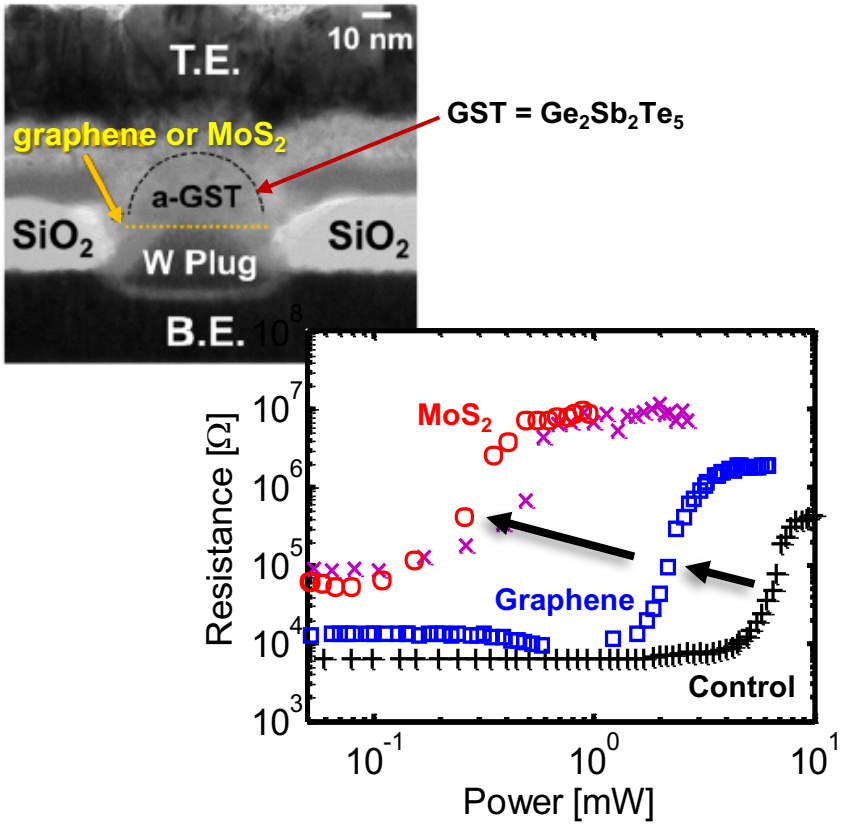
*HRS, LRS = high, low resistance state

Exploiting Graphene, MoS_2 As Thermal Barrier

C. Ahn, S. Fong, Y. Kim, S. Lee, A. Sood, C. Neumann, K. Goodson, E. Pop, H.-S.P. Wong, *Nano Lett.* **15**, 6809 (2015)
C. Neumann, K. Okabe, E. Yalon, R. Grady, H.-S.P. Wong, E. Pop, *Appl. Phys. Lett*. **114**, 082103 (2019)

- Phase-change memory (PCM) needs **good thermal insulation**

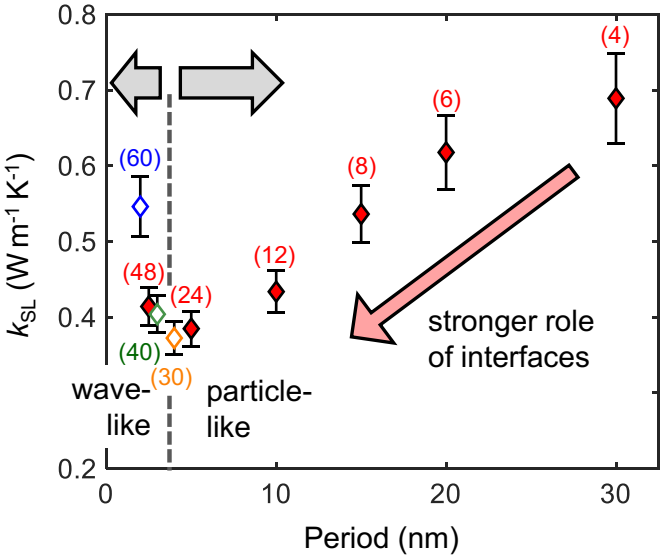


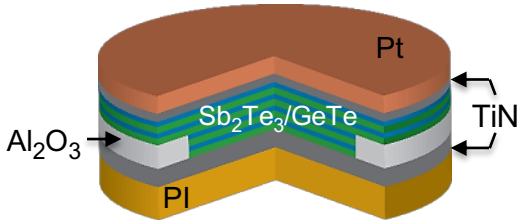


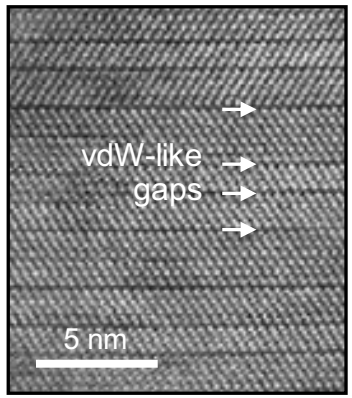
- Exploiting 2D **cross-plane** thermal boundary resistance (TBR)
- Ultrathin **thermal barrier** limits PCM heat loss → lower switching power

Layered Superlattice Phase-Change Memory

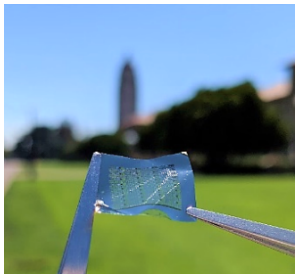
H. Kwon, A.I. Khan, C. Perez, M. Asheghi, E. Pop, K. Goodson, *Nano Letters* **21**, 5984 (2021)
A.I. Khan, A. Daus, R. Islam, K. Neilson, H.-S.P. Wong, E. Pop, *Science* **373**, 1243 (2021)

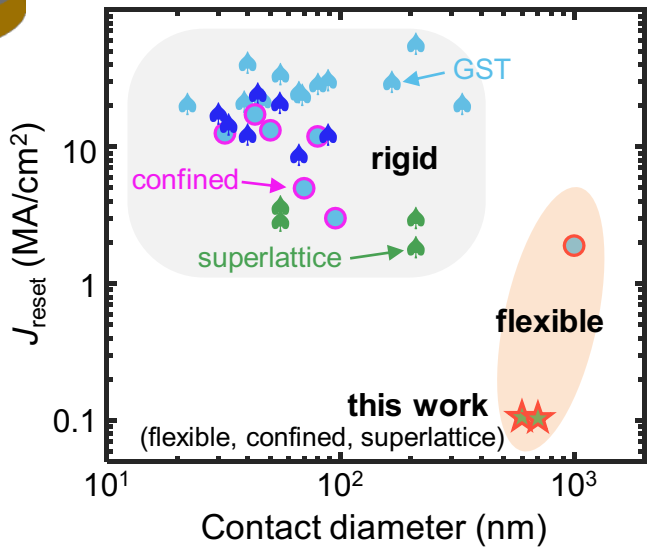






Sb_2Te_3/GeTe



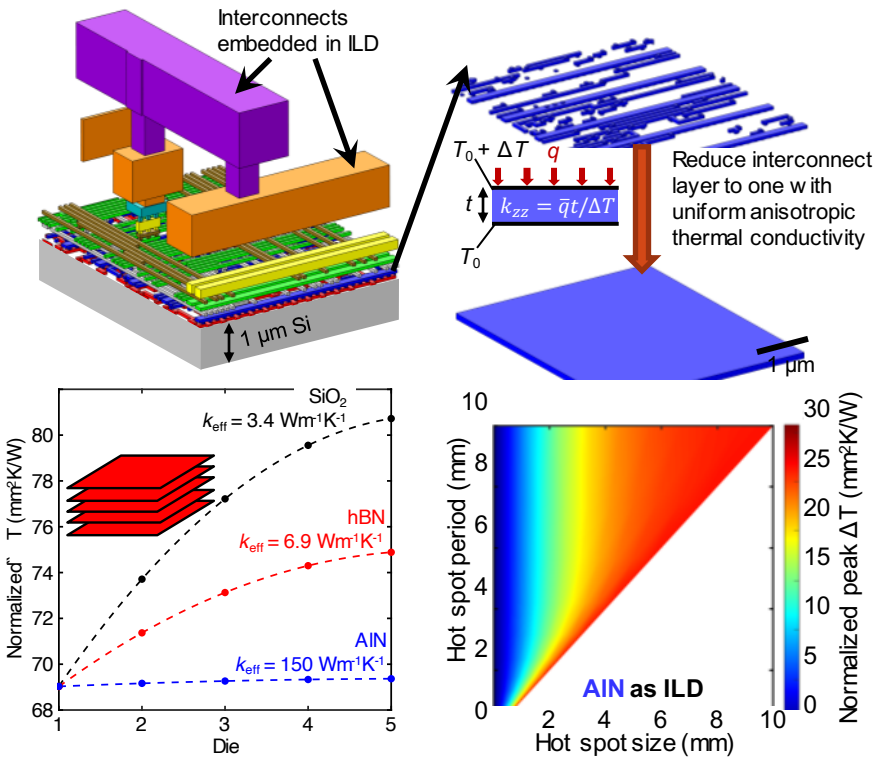


- If one thermal barrier is good, how about a **superlattice** of them?
- Sb_2Te_3/GeTe superlattices → from wave-like to particle-like heat flow
- Superlattice **PCM on flexible plastic** substrates with **ultralow current** → also assisted by low thermal conductivity substrate

Thermal Challenges in 3D Systems

Ç. Köroğlu, E. Pop, *IEEE Electron Device Lett.* **44**, 496 (2023)

https://www.youtube.com/c/MerryNightmare7710

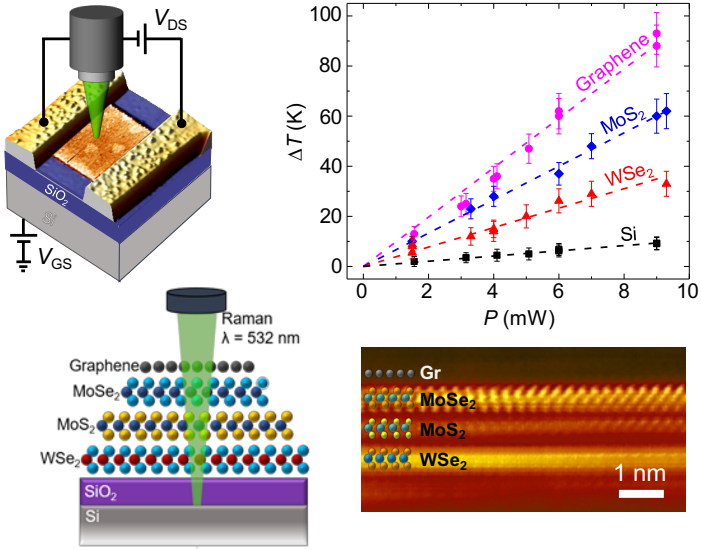


- **High power density in 3D** → different layers are cooking each other
- 3D integration has many **interfaces** and (usually) **low-*K**** dielectrics
- We looked at **AlN** (iso) and **hBN** (anisotropic) as heat spreaders in 3D ICs

* Low-*k* (permittivity) and low-κ (thermal conductivity)

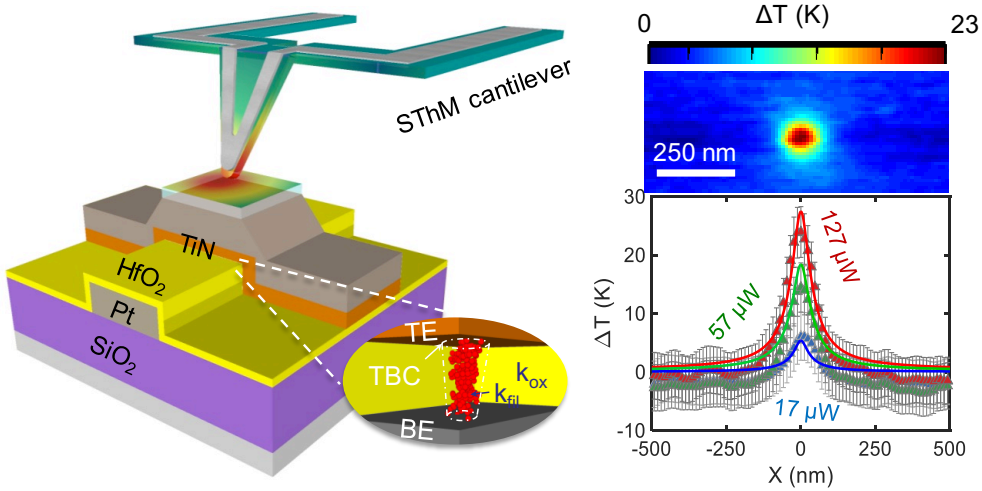
Thermal Measurements in Our Group

Raman thermometry



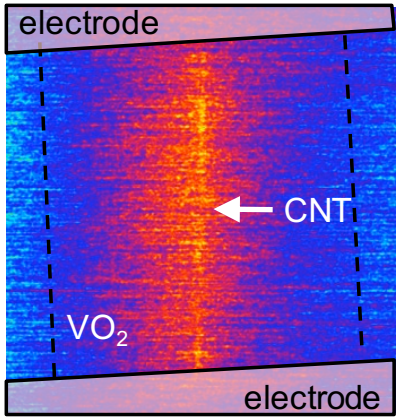
S. Vaziri et al. *Sci. Adv.* **5**, eaax1325 (2019)

Scanning Thermal Microscopy (SThM)



S. Deshmukh et al., *Science Adv.* **8**, eabk1514 (2022)

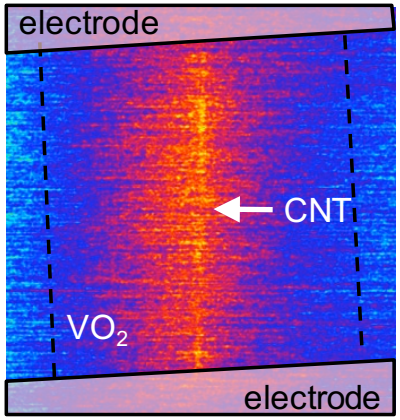
- Raman thermometry → **material-specific**,
  ~0.5 μm spatial resolution, sub-1 nm vertical resolution
- Scanning Thermal Microscopy (SThM) →
  surface temperature, **~50 nm resolution**



S. Bohaichuk, *Nano Lett.* (2019)
neuron-like spiking

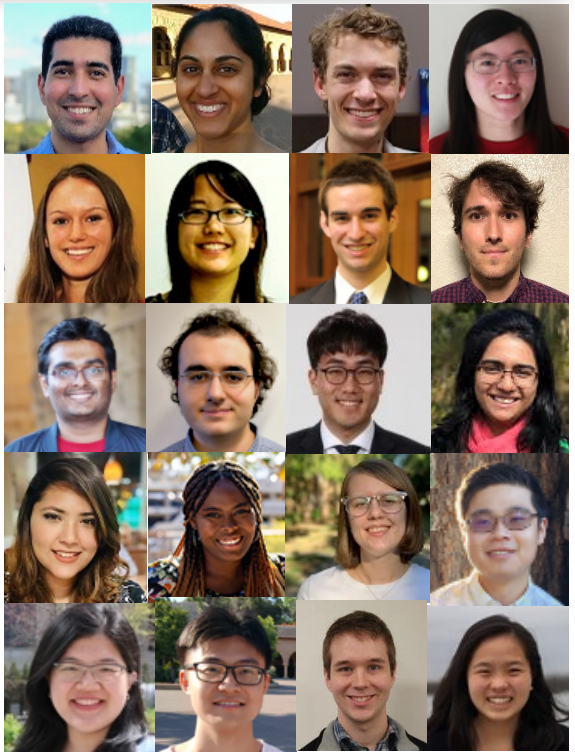
Summary

- **Moore's Law** is not dead, it's going 3D
- **VdW interfaces** → 2D semiconductors are good for 3D integration
- But, also: VdW interfaces → weak thermal coupling
  (sometimes we can leverage these, other times they are headaches)
- **3D integrated systems** have thermal challenges
- Nanoscale **thermal measurements** are key
- Electro-thermal **co-design** is important



Acknowledgements

W: http://poplab.stanford.edu
E: epop@stanford.edu | **T:** @profericpop



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